

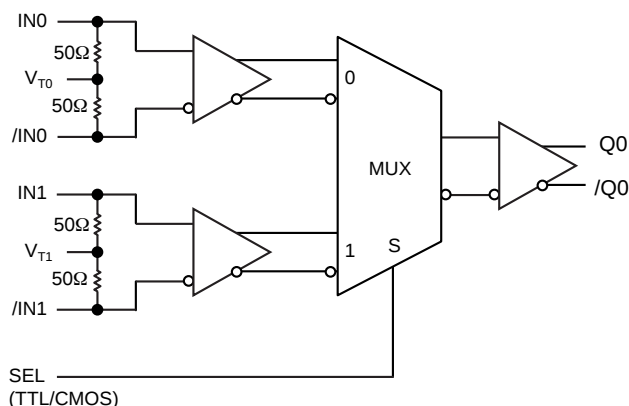
## FEATURES

- **Guaranteed AC performance over temperature and voltage:**
  - DC to 10.7Gbps data throughput
  - DC to > 7GHz  $f_{MAX}$  (clock)
  - < 240ps propagation delay
  - < 70ps  $t_r$  /  $t_f$  times
- **Ultra-low crosstalk-induced jitter: 0.7ps<sub>RMS</sub>**
- **Ultra-low jitter design:**
  - < 1ps<sub>RMS</sub> random jitter
  - < 10ps<sub>PP</sub> deterministic jitter
  - < 10ps<sub>PP</sub> total jitter (clock)
- **Unique input termination and  $V_T$  pin accepts DC-coupled and AC-coupled inputs (CML, PECL, LVDS)**
- **400mV (100k) LVPECL output swing**
- **Power supply 2.5V  $\pm$ 5% or 3.3V  $\pm$ 10%**
- **–40°C to +85°C temperature range**
- **Available in 16-pin (3mm  $\times$  3mm) MLF® package**

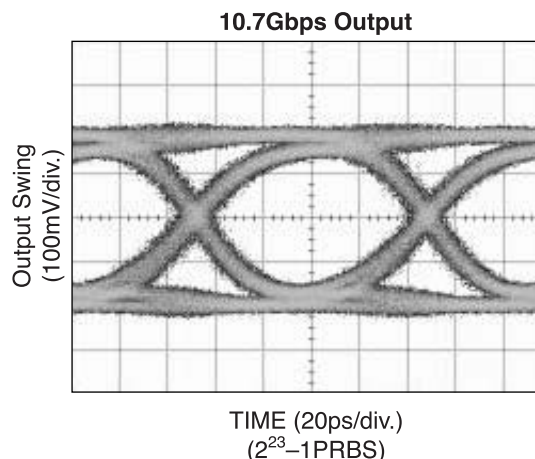
## APPLICATIONS

- **Redundant clock distribution**
- **OC-3 to OC-192 SONET/SDH clock/data distribution**
- **Loopback**
- **Fibre Channel distribution**

## FUNCTIONAL BLOCK DIAGRAM



## TYPICAL PERFORMANCE



Precision Edge®

## DESCRIPTION

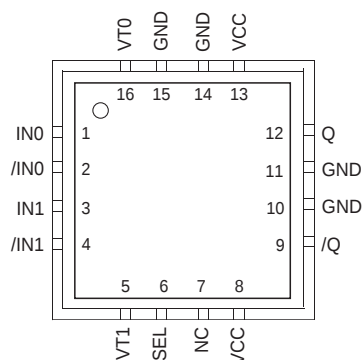
The SY58019U is a 2.5V/3.3V precision, high-speed, 2:1 differential MUX capable of handling clocks up to 7GHz and data up to 10.7Gbps.

The differential input includes Micrel's unique, 3-pin input termination architecture that allows customers to interface to any differential signal (AC- or DC-coupled) as small as 100mV without any level shifting or termination resistor networks in the signal path. The outputs are 400mV, 100k compatible, LVPECL, with extremely fast rise/fall times guaranteed to be less than 70ps.

The SY58019U operates from a 2.5V  $\pm$ 5% supply or a 3.3V  $\pm$ 10% supply and is guaranteed over the full industrial temperature range of –40°C to +85°C. For applications that require CML outputs, consider the SY58017U or for 800mV LVPECL outputs the SY58018U. The SY58019U is part of Micrel's high-speed, Precision Edge® product line.

All support documentation can be found on Micrel's web site at [www.micrel.com](http://www.micrel.com).

## PACKAGE/ORDERING INFORMATION



16-Pin MLF®

Ordering Information<sup>(1)</sup>

| Part Number                    | Package Type | Operating Range | Package Marking                      | Lead Finish    |
|--------------------------------|--------------|-----------------|--------------------------------------|----------------|
| SY58019UMI                     | MLF-16       | Industrial      | 019U                                 | Sn-Pb          |
| SY58019UMITR <sup>(2)</sup>    | MLF-16       | Industrial      | 019U                                 | Sn-Pb          |
| SY58019UMG <sup>(3)</sup>      | MLF-16       | Industrial      | 019U with Pb-Free bar-line indicator | Pb-Free NiPdAu |
| SY58019UMGTR <sup>(2, 3)</sup> | MLF-16       | Industrial      | 019U with Pb-Free bar-line indicator | Pb-Free NiPdAu |

## Notes:

1. Contact factory for die availability. Dice are guaranteed at  $T_A = 25^\circ\text{C}$ , DC electricals only.
2. Tape and Reel.
3. Pb-Free package recommended for new designs.

## PIN DESCRIPTION

| Pin Number     | Pin Name               | Pin Function                                                                                                                                                                                                                                                                                                                                                                                        |
|----------------|------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1, 2<br>3, 4   | IN0, /IN0<br>IN1, /IN1 | Differential Input: These input pairs are the differential signal inputs to the device. They accept differential AC- or DC-coupled signals as small as 100mV. Each pin of a pair internally terminates to a $V_T$ pin through $50\Omega$ . Note that these inputs will default to an indeterminate state if left open. Please refer to the "Input Interface Applications" section for more details. |
| 16, 5          | VT0, VT1               | Input Termination Center-Tap: Each side of the differential input pair terminates to a $V_T$ pin. The $V_{T0}$ and $V_{T1}$ pins provide a center-tap to a termination network for maximum interface flexibility. See "Input Interface Applications" section for more details.                                                                                                                      |
| 6              | SEL                    | This single-ended TTL/CMOS compatible input selects the inputs to the multiplexer. Note that this input is internally connected to a $25k\Omega$ pull-up resistor and will default to a logic HIGH state if left open.                                                                                                                                                                              |
| 7              | NC                     | No connect.                                                                                                                                                                                                                                                                                                                                                                                         |
| 8, 13          | VCC                    | Positive Power Supply: Bypass with $0.1\mu\text{F}$   $0.01\mu\text{F}$ low ESR capacitors. $0.01\mu\text{F}$ capacitor should be as close to $V_{CC}$ pin as possible.                                                                                                                                                                                                                             |
| 12, 9          | Q, /Q                  | Differential Outputs: This 100k compatible LVPECL output pair is the output of the device. Terminate through $50\Omega$ to $V_{CC} - 2V$ . See "Output Interface Applications" section. It is a logic function of the IN0, IN1, and SEL inputs. Please refer to the "Truth Table" for details.                                                                                                      |
| 10, 11, 14, 15 | GND,<br>Exposed Pad    | Ground. Ground pins and exposed pad must be connected to the same ground plane.                                                                                                                                                                                                                                                                                                                     |

## TRUTH TABLE

| SEL | Output             |
|-----|--------------------|
| 0   | CH0 Input Selected |
| 1   | CH1 Input Selected |

**Absolute Maximum Ratings<sup>(1)</sup>**

|                                       |                   |
|---------------------------------------|-------------------|
| Power Supply Voltage ( $V_{CC}$ )     | –0.5V to +4.0V    |
| Input Voltage ( $V_{IN}$ )            | –0.5V to $V_{CC}$ |
| LVPECL Output Current ( $I_{OUT}$ )   |                   |
| Continuous                            | 50mA              |
| Surge                                 | 100mA             |
| Termination Current <sup>(3)</sup>    |                   |
| Source or Sink Current on $V_T$ pin   | ±100mA            |
| Input Current                         |                   |
| Source or Sink Current on IN, /IN pin | ±50mA             |
| Lead Temperature (soldering, 20 sec.) | 260°C             |
| Storage Temperature Range ( $T_S$ )   | –65°C to +150°C   |

**Operating Ratings<sup>(2)</sup>**

|                                           |                    |
|-------------------------------------------|--------------------|
| Power Supply Voltage ( $V_{CC}$ )         | +2.375V to +2.625V |
|                                           | +3.0V to +3.6V     |
| Ambient Temperature Range ( $T_A$ )       | –40°C to +85°C     |
| Package Thermal Resistance <sup>(4)</sup> |                    |
| MLF® ( $\theta_{JA}$ )                    |                    |
| Still-Air                                 | 60°C/W             |
| MLF® ( $\psi_{JB}$ )                      |                    |
| Junction-to-Board                         | 38°C/W             |

**DC ELECTRICAL CHARACTERISTICS<sup>(5)</sup>**

$T_A$  = –40°C to +85°C, unless otherwise stated.

| Symbol         | Parameter                                                                                             | Condition                          | Min            | Typ        | Max            | Units    |
|----------------|-------------------------------------------------------------------------------------------------------|------------------------------------|----------------|------------|----------------|----------|
| $V_{CC}$       | Power Supply Voltage                                                                                  | $V_{CC} = 2.5V$<br>$V_{CC} = 3.3V$ | 2.375<br>3.0   | 2.5<br>3.3 | 2.625<br>3.6   | V        |
| $I_{CC}$       | Power Supply Current                                                                                  | No load, max. $V_{CC}$             |                | 55         | 70             | mA       |
| $R_{DIFF\_IN}$ | Differential Input Resistance<br>(IN0-to-/IN0, IN1-to-/IN1)                                           |                                    | 80             | 100        | 120            | $\Omega$ |
| $R_{IN}$       | Input Resistance<br>(IN0-to- $V_{T0}$ , /IN0-to- $V_{T0}$ ,<br>IN1-to- $V_{T1}$ , /IN1-to- $V_{T1}$ ) |                                    | 40             | 50         | 60             | $\Omega$ |
| $V_{IH}$       | Input HIGH Voltage<br>(IN0, /IN0, IN1, /IN1)                                                          | <b>Note 6</b>                      | $V_{CC} - 1.6$ |            | $V_{CC}$       | V        |
| $V_{IL}$       | Input LOW Voltage<br>(IN0, /IN0, IN1, /IN1)                                                           |                                    | 0              |            | $V_{IH} - 0.1$ | V        |
| $V_{IN}$       | Input Voltage Swing<br>(IN0, /IN0, IN1, /IN1)                                                         | See Figure 1a                      | 0.1            |            | 1.7            | V        |
| $V_{DIFF\_IN}$ | Differential Input Voltage Swing<br> IN0, /IN0 ,  IN1, /IN1                                           | See Figure 1b                      | 0.2            |            |                | V        |
| $V_{T\ IN}$    | IN to $V_T$<br>(IN0, /IN0, IN1, /IN1)                                                                 |                                    |                |            | 1.28           | V        |

**Notes:**

1. Permanent device damage may occur if “*Absolute Maximum Ratings*” are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to “*Absolute Maximum Ratings*” conditions for extended periods may affect device reliability.
2. The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.
3. Due to the limited drive capability, use for input of the same package only.
4. Package thermal resistance assumes exposed pad is soldered (or equivalent) to the device's most negative potential (GND) on the PCB.  $\psi_{JB}$  uses 4-layer  $\theta_{JA}$  in still-air measurement, unless otherwise stated.
5. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.
6.  $V_{IH}$  (min) not lower than 1.2V.

**LVPECL OUTPUT DC ELECTRICAL CHARACTERISTICS<sup>(7)</sup>**

$V_{CC} = 2.5V \pm 5\%$  or  $3.3V \pm 10\%$ ;  $T_A = -40^\circ C$  to  $+85^\circ C$ ;  $R_L = 50\Omega$  to  $V_{CC} - 2V$ , unless otherwise stated.

| Symbol          | Parameter                                  | Condition     | Min              | Typ | Max              | Units |
|-----------------|--------------------------------------------|---------------|------------------|-----|------------------|-------|
| $V_{OH}$        | Output HIGH Voltage<br>Q, /Q               |               | $V_{CC} - 1.145$ |     | $V_{CC} - 0.895$ | V     |
| $V_{OL}$        | Output LOW Voltage<br>Q, /Q                |               | $V_{CC} - 1.545$ |     | $V_{CC} - 1.295$ | V     |
| $V_{OUT}$       | Output Differential Swing<br>Q, /Q         | See Figure 1a | 150              | 400 |                  | mV    |
| $V_{DIFF\_OUT}$ | Differential Output Voltage Swing<br>Q, /Q | See Figure 1b | 300              | 800 |                  | mV    |

**LVTTL/CMOS DC ELECTRICAL CHARACTERISTICS<sup>(7)</sup>**

$V_{CC} = 2.5V \pm 5\%$  or  $3.3V \pm 10\%$ ;  $T_A = -40^\circ C$  to  $+85^\circ C$

| Symbol   | Parameter          | Condition | Min  | Typ | Max | Units   |
|----------|--------------------|-----------|------|-----|-----|---------|
| $V_{IH}$ | Input HIGH Voltage |           | 2.0  |     |     | V       |
| $V_{IL}$ | Input LOW Voltage  |           |      |     | 0.8 | V       |
| $I_{IH}$ | Input HIGH Current |           |      |     | 40  | $\mu A$ |
| $I_{IL}$ | Input LOW Current  |           | -300 |     |     | $\mu A$ |

**Note:**

7. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.

**AC ELECTRICAL CHARACTERISTICS<sup>(8)</sup>**

$V_{CC} = 2.5V \pm 5\%$  or  $3.3V \pm 10\%$ ;  $T_A = -40^\circ C$  to  $+85^\circ C$ ,  $R_L = 50\Omega$  to  $V_{CC} - 2V$ , unless otherwise stated.

| Symbol                  | Parameter                                              | Condition                  | Min  | Typ | Max | Units             |
|-------------------------|--------------------------------------------------------|----------------------------|------|-----|-----|-------------------|
| $f_{MAX}$               | Maximum Operating Frequency                            | NRZ Data                   | 10.7 |     |     | Gbps              |
|                         |                                                        | $V_{OUT} \geq 200mV$ Clock |      | 7   |     | GHz               |
| $t_{pd}$                | Differential Propagation Delay                         | IN-to-Q                    | 90   | 160 | 240 | ps                |
|                         |                                                        | SEL-to-Q                   | 50   | 160 | 350 | ps                |
| $t_{pd} \text{ Tempco}$ | Differential Propagation Delay Temperature Coefficient |                            |      | 75  |     | fs/ $^\circ C$    |
| $t_{SKEW}$              | Input-to-Input Skew                                    | <b>Note 9</b>              |      | 3   | 15  | ps                |
|                         | Part-to-Part Skew                                      | <b>Note 10</b>             |      |     | 100 | ps                |
| $t_{JITTER}$            | Data Random Jitter                                     | <b>Note 11</b>             |      |     | 1   | ps <sub>RMS</sub> |
|                         | Deterministic Jitter                                   | <b>Note 12</b>             |      |     | 10  | ps <sub>PP</sub>  |
|                         | Clock Cycle-to-Cycle Jitter                            | <b>Note 13</b>             |      |     | 1   | ps <sub>RMS</sub> |
|                         | Total Jitter                                           | <b>Note 14</b>             |      |     | 10  | ps <sub>PP</sub>  |
|                         | Crosstalk-Induced Jitter                               | <b>Note 15</b>             |      |     | 0.7 | ps <sub>RMS</sub> |
| $t_r, t_f$              | Output Rise/Fall Time                                  | 20% to 80%, at full swing  | 20   | 40  | 70  | ps                |

**Notes:**

8. High frequency AC parameters are guaranteed by design and characterization.
9. Input-to-input skew is the difference in time from an input-to-output in comparison to any other input-to-output. In addition, the input-to-input skew does not include the output skew.
10. Part-to-part skew is defined for two parts with identical power supply voltages at the same temperature and with no skew of the edges at the respective inputs.
11. RJ is measured with a K28.7 comma detect character pattern, measured at 2.5Gbps/3.2Gbps.
12. DJ is measured at 2.5Gbps/3.2Gbps, with both K28.5 and  $2^{23}-1$  PRBS pattern.
13. Cycle-to-cycle jitter definition: the variation of periods between adjacent cycles,  $T_n - T_{n-1}$  where T is the time between rising edges of the output signal.
14. Total jitter definition: with an ideal clock input of frequency  $\leq f_{MAX}$ , no more than one output edge in  $10^{12}$  output edges will deviate by more than the specified peak-to-peak jitter value.
15. Crosstalk is measured at the output while applying two similar frequencies that are asynchronous with respect to each other at the inputs.

## SINGLE-ENDED AND DIFFERENTIAL SWINGS

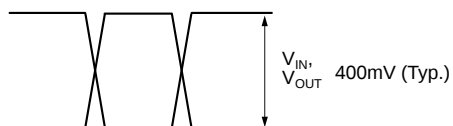


Figure 1a. Single-Ended Voltage Swing

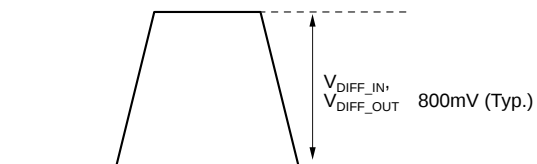
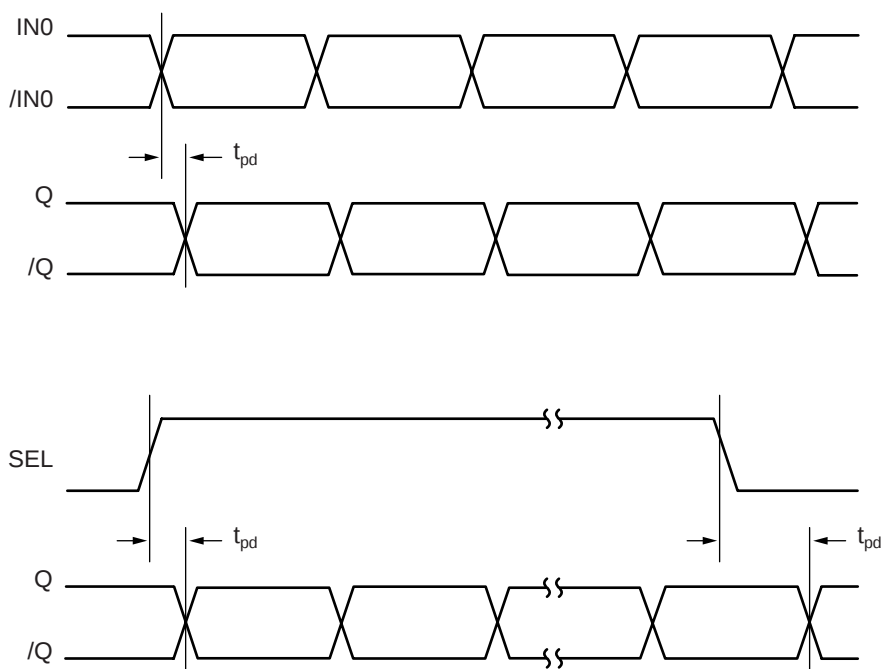


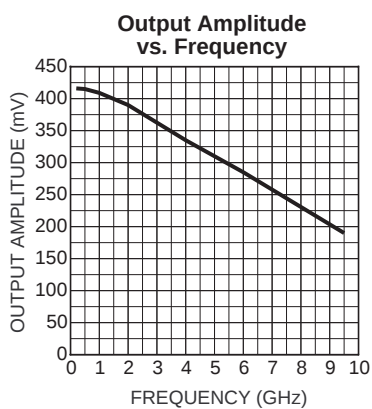
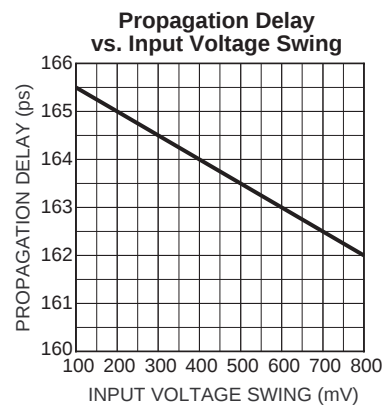
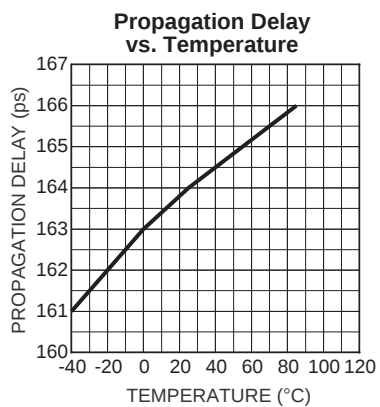
Figure 1b. Differential Voltage Swing

## TIMING DIAGRAMS



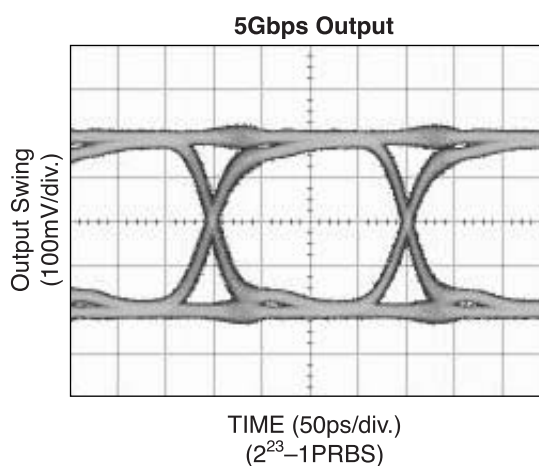
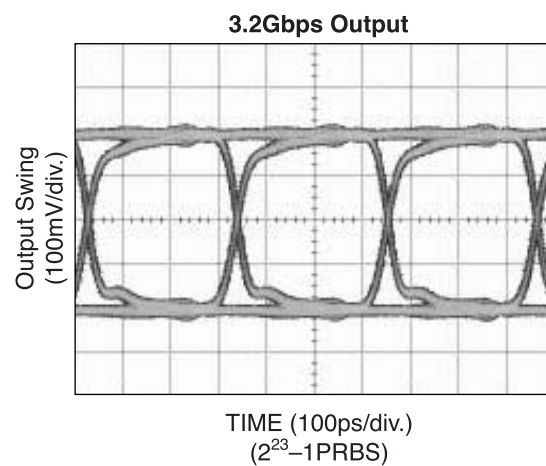
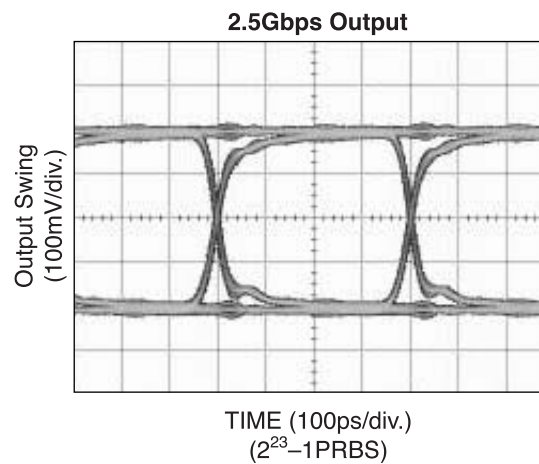
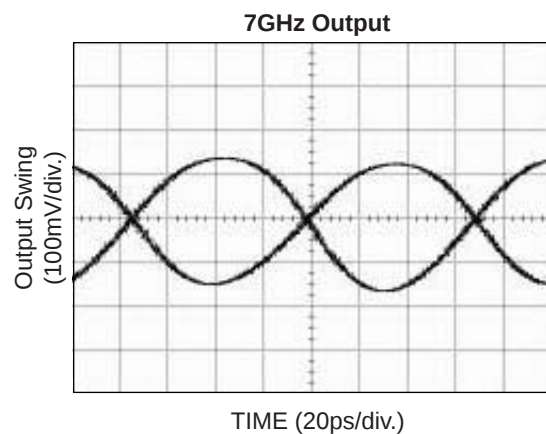
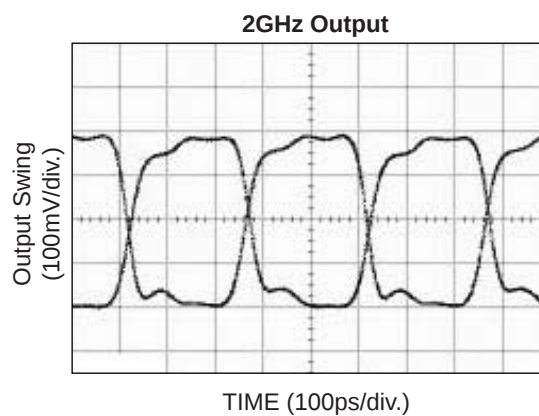
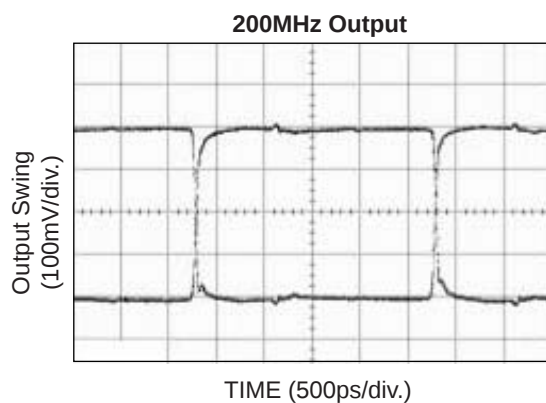
**TYPICAL OPERATING CHARACTERISTICS**

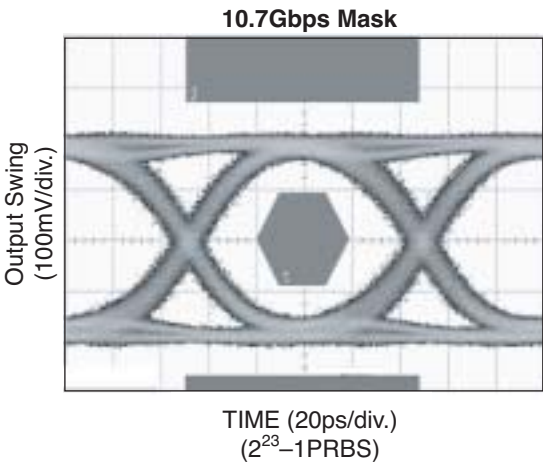
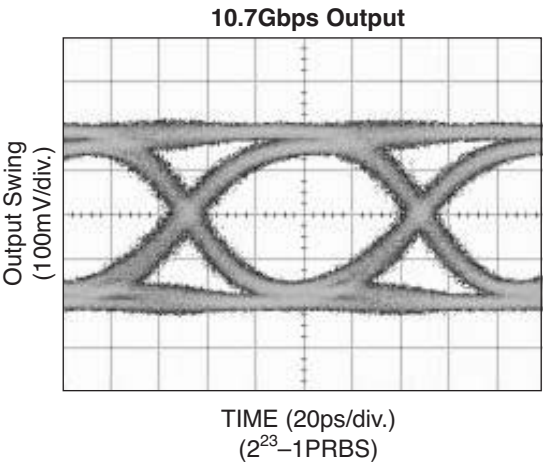
$V_{CC} = 3.3V$ ,  $V_{IN} = 100mV$ ,  $T_A = 25^\circ C$ , unless otherwise stated.



**TYPICAL OPERATING CHARACTERISTICS**

$V_{CC} = 3.3V$ ,  $V_{IN} = 100mV$ ,  $T_A = 25^\circ C$ , unless otherwise stated.





## INPUT AND OUTPUT STAGES

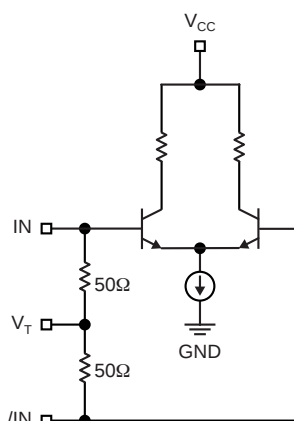


Figure 2a. Simplified Differential Input Stage

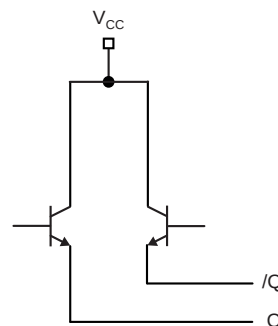


Figure 2b. Simplified LVPECL Output Stage

## INPUT INTERFACE APPLICATIONS

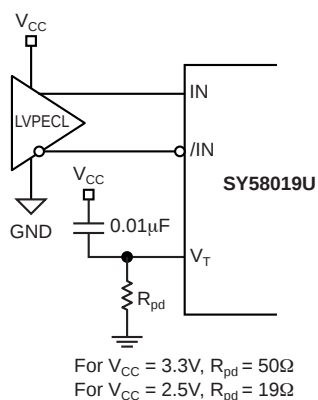
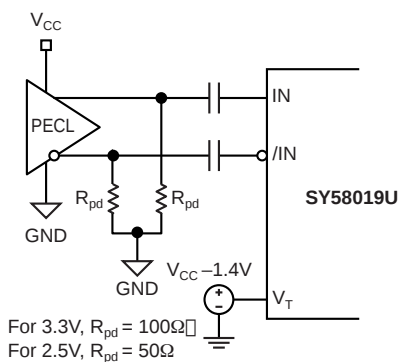
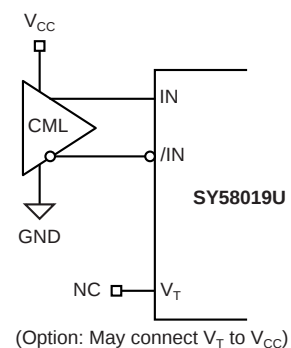
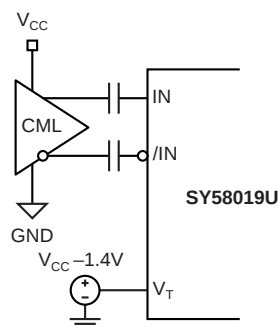
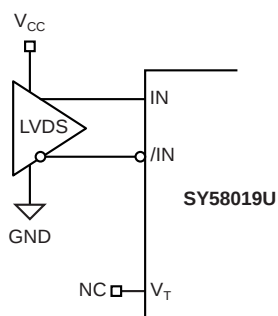
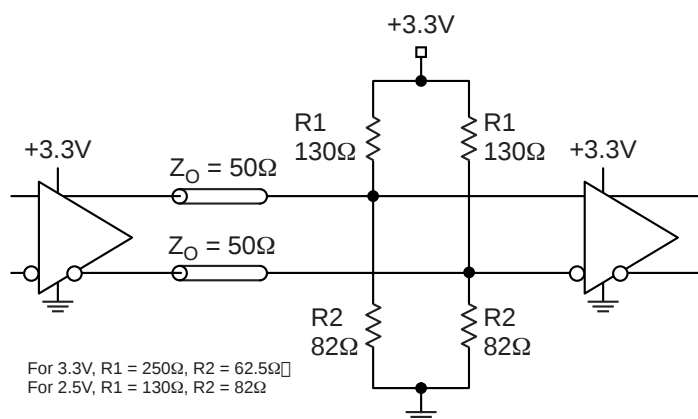
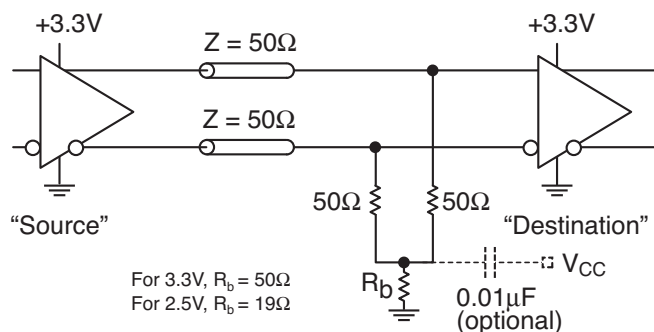
Figure 3a. LVPECL  
Interface (DC-Coupled)Figure 3b. LVPECL  
Interface (AC-Coupled)Figure 3c. CML  
Interface (DC-Coupled)Figure 3d. CML  
Interface (AC-Coupled)

Figure 3e. LVDS Interface

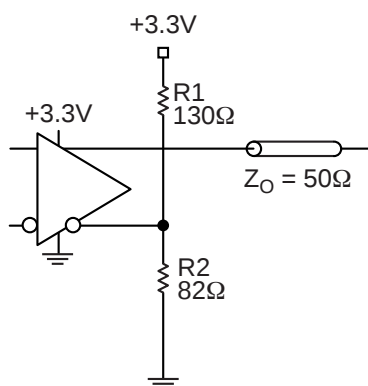
## OUTPUT INTERFACE APPLICATIONS



**Figure 4a. Parallel Thevenin-Equivalent Termination**



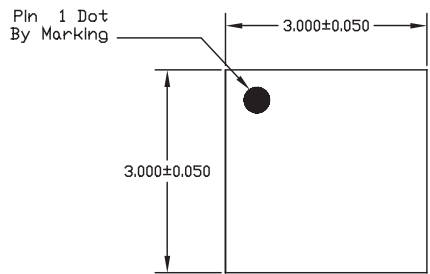
**Figure 4b. Three-Resistor "Y" Termination**



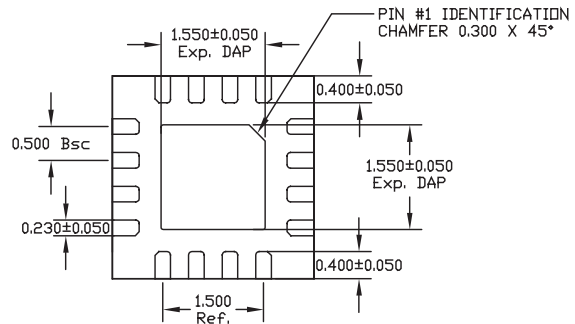
**Figure 4c. Terminating Unused I/O**

## RELATED MICREL PRODUCTS AND SUPPORT DOCUMENTATION

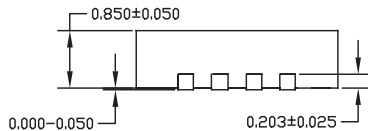
| Part Number   | Function                                                                        | Data Sheet Link                                                                                                                        |
|---------------|---------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------|
| SY58016L      | 3.3V 10Gbps Differential CML Line Driver/Receiver with Internal I/O Termination | <a href="http://www.micrel.com/product-info/products/sy58016l.shtml">http://www.micrel.com/product-info/products/sy58016l.shtml</a>    |
| SY58017U      | Ultra Precision Differential CML 2:1 MUX with Internal I/O Termination          | <a href="http://www.micrel.com/product-info/products/sy58017u.shtml">http://www.micrel.com/product-info/products/sy58017u.shtml</a>    |
| SY58018U      | Ultra Precision Differential LVPECL 2:1 MUX with Internal Termination           | <a href="http://www.micrel.com/product-info/products/sy58018u.shtml">http://www.micrel.com/product-info/products/sy58018u.shtml</a>    |
| SY58025U      | 10.7Gbps Dual 2:1 CML MUX with Internal I/O Termination                         | <a href="http://www.micrel.com/product-info/products/sy58025u.shtml">http://www.micrel.com/product-info/products/sy58025u.shtml</a>    |
| SY58026U      | 5Gbps Dual 2:1 MUX with Internal Termination                                    | <a href="http://www.micrel.com/product-info/products/sy58026u.shtml">http://www.micrel.com/product-info/products/sy58026u.shtml</a>    |
| SY58027U      | 10.7Gbps Dual 2:1 400mV LVPECL MUX with Internal Termination                    | <a href="http://www.micrel.com/product-info/products/sy58027u.shtml">http://www.micrel.com/product-info/products/sy58027u.shtml</a>    |
| SY58051U      | 10.7Gbps AnyGate® with Internal Input and Output Termination                    | <a href="http://www.micrel.com/product-info/products/sy58051u.shtml">http://www.micrel.com/product-info/products/sy58051u.shtml</a>    |
| SY58052U      | 10Gbps Clock/Data Retimer with 50Ω Input Termination                            | <a href="http://www.micrel.com/product-info/products/sy58052u.shtml">http://www.micrel.com/product-info/products/sy58052u.shtml</a>    |
|               | MLF® Application Note                                                           | <a href="http://www.amkor.com/products/notes_papers/MLF_AppNote_0902.pdf">www.amkor.com/products/notes_papers/MLF_AppNote_0902.pdf</a> |
| HBW Solutions | New Products and Applications                                                   | <a href="http://www.micrel.com/product-info/products/solutions.shtml">www.micrel.com/product-info/products/solutions.shtml</a>         |

**16-PIN MicroLeadFrame® (MLF-16)**

TOP VIEW



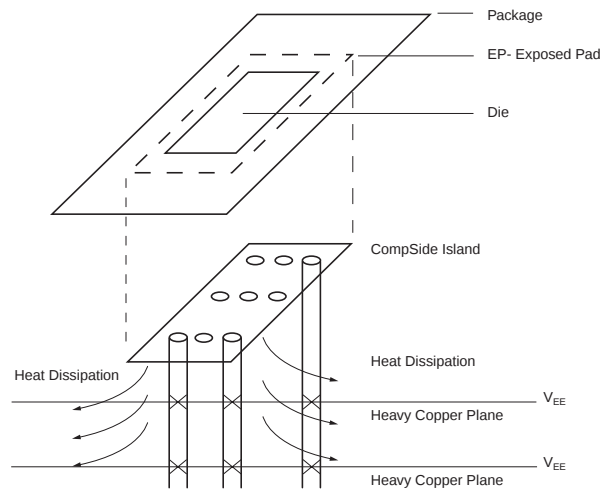
BOTTOM VIEW



SIDE VIEW

## NOTE:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. MAX. PACKAGE WARPAGE IS 0.05 mm.
3. MAXIMUM ALLOWABLE BURRS IS 0.076 mm IN ALL DIRECTIONS.
4. PIN #1 ID ON TOP WILL BE LASER/INK MARKED.



**PCB Thermal Consideration for 16-Pin MLF® Package**  
**(Always solder, or equivalent, the exposed pad to the PCB)**

**Package Notes:**

1. Package meets Level 2 qualification.
2. All parts are dry-packaged before shipment.
3. Exposed pads must be soldered to a ground for proper thermal management.

**MICREL, INC. 2180 FORTUNE DRIVE SAN JOSE, CA 95131 USA**

TEL + 1 (408) 944-0800 FAX + 1 (408) 474-1000 WEB <http://www.micrel.com>

The information furnished by Micrel in this data sheet is believed to be accurate and reliable. However, no responsibility is assumed by Micrel for its use. Micrel reserves the right to change circuitry and specifications at any time without notification to the customer.

Micrel Products are not designed or authorized for use as components in life support appliances, devices or systems where malfunction of a product can reasonably be expected to result in personal injury. Life support devices or systems are devices or systems that (a) are intended for surgical implant into the body or (b) support or sustain life, and whose failure to perform can be reasonably expected to result in a significant injury to the user. A Purchaser's use or sale of Micrel Products for use in life support appliances, devices or systems is at Purchaser's own risk and Purchaser agrees to fully indemnify Micrel for any damages resulting from such use or sale.

© 2005 Micrel, Incorporated.