LM5116WG Wide Range Synchronous Buck Controller

Check for Samples: LM5116WG

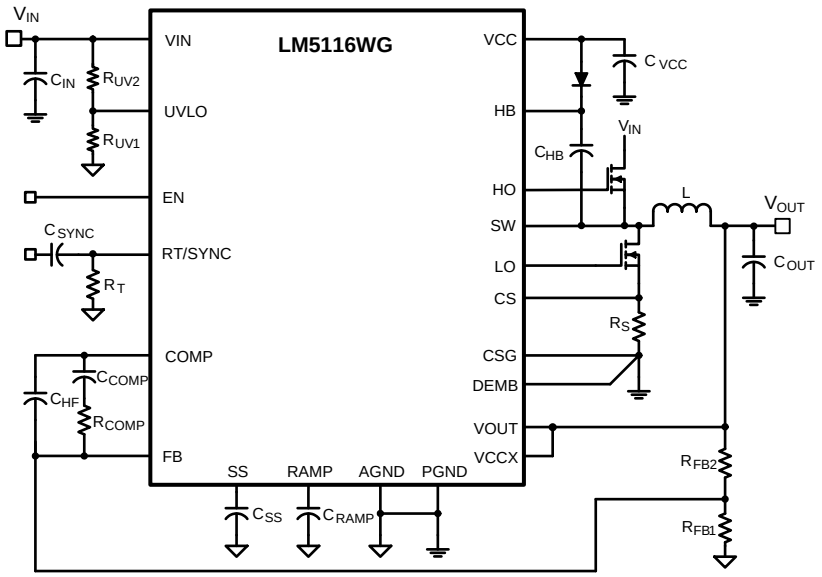
FEATURES

- **Hermetic Package for Harsh Operating Environments**
- **Emulated Peak Current Mode**
- **Wide Operating Range up to 100V**
- **Low I_Q Shutdown (< 10 µA)**
- **Drives Standard or Logic Level MOSFETs**
- **Robust 3.5A Peak Gate Drive**
- **Free-Run or Synchronous Operation to 1 MHz**
- **Optional Diode Emulation Mode**
- **Programmable Output from 1.215V to 80V**
- **Precision 1.5% Voltage Reference**
- **Programmable Current Limit**
- **Programmable Soft-Start**
- **Programmable Line Under-Voltage Lockout**
- **Automatic Switch to External Bias Supply**
- **CPGA-20 with No Thermal Shutdown**

DESCRIPTION

The LM5116WG is a synchronous buck controller intended for step-down regulator applications from a high voltage or widely varying input supply. The control method is based upon current mode control utilizing an emulated current ramp. Current mode control provides inherent line feed-forward, cycle by cycle current limiting and ease of loop compensation. The use of an emulated control ramp reduces noise sensitivity of the pulse-width modulation circuit, allowing reliable control of very small duty cycles necessary in high input voltage applications. The operating frequency is programmable from 50 kHz to 1 MHz. The LM5116WG drives external high-side and low-side NMOS power switches with adaptive dead-time control. A user-selectable diode emulation mode enables discontinuous mode operation for improved efficiency at light load conditions. A low quiescent current shutdown disables the controller and consumes less than 10 µA of total input current. Additional features include a high voltage bias regulator, automatic switch-over to external bias for improved efficiency, frequency synchronization, cycle by cycle current limit and adjustable line under-voltage lockout. The device is available in a CPGA-20 high temperature ceramic package with the thermal shutdown feature disabled.

Typical Application



Connection Diagram

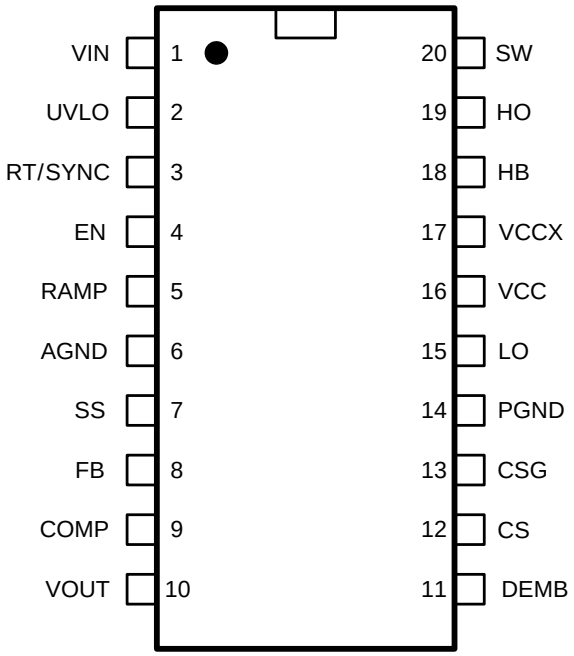


Figure 1. Top View
See Package Number NAR0020A

PIN DESCRIPTIONS

Pin	Name	Description
1	VIN	Chip supply voltage, input voltage monitor and input to the VCC regulator.
2	UVLO	If the UVLO pin is below 1.215V, the regulator will be in standby mode (VCC regulator running, switching regulator disabled). If the UVLO pin voltage is above 1.215V, the regulator is operational. An external voltage divider can be used to set an under-voltage shutdown threshold. There is a fixed 5 µA pull up current on this pin when EN is high. UVLO is pulled to ground in the event a current limit condition exists for 256 clock cycles.
3	RT/SYNC	The internal oscillator is set with a single resistor between this pin and the AGND pin. The recommended frequency range is 50 kHz to 1 MHz. The internal oscillator can be synchronized to an external clock by AC coupling a positive edge onto this node.
4	EN	If the EN pin is below 0.5V, the regulator will be in a low power state drawing less than 10 µA from VIN. EN must be pulled above 3.3V for normal operation.
5	RAMP	Ramp control signal. An external capacitor connected between this pin and the AGND pin sets the ramp slope used for current mode control.
6	AGND	Analog ground. Connect directly to PGND under the LM5116WG.
7	SS	An external capacitor and an internal 10 µA current source set the soft start time constant for the rise of the error amp reference. The SS pin is held low during VCC < 4.5V, UVLO < 1.215V, or EN input low.
8	FB	Feedback signal from the regulated output. This pin is connected to the inverting input of the internal error amplifier. The regulation threshold is 1.215V.
9	COMP	Output of the internal error amplifier. The loop compensation network should be connected between this pin and the FB pin.
10	VOUT	Output monitor. Connect directly to the output voltage.
11	DEMB	Low-side MOSFET source voltage monitor for diode emulation. For start-up into a pre-biased load, tie this pin to ground at the CSG connection. For fully synchronous operation, use an external series resistor between DEMB and ground to raise the diode emulation threshold above the low-side SW on-voltage.
12	CS	Current sense amplifier input. Connect to the top of the current sense resistor or the drain of the low-sided MOSFET if $R_{DS(ON)}$ current sensing is used.
13	CSG	Current sense amplifier input. Connect to the bottom of the sense resistor or the source of the low-side MOSFET if $R_{DS(ON)}$ current sensing is used.
14	PGND	Power ground. Connect directly to AGND under the LM5116WG.
15	LO	Connect to the gate of the low-side synchronous MOSFET through a short, low inductance path.
16	VCC	Locally decouple to PGND using a low ESR/ESL capacitor located as close to the controller as possible.
17	VCCX	Optional input for an externally supplied VCC. If VCCX > 4.5V, VCCX is internally connected to VCC and the internal VCC regulator is disabled. If VCCX is unused, it should be connected to ground.
18	HB	High-side driver supply for bootstrap gate drive. Connect to the cathode of the bootstrap diode and the positive terminal of the bootstrap capacitor. The bootstrap capacitor supplies current to charge the high-side MOSFET gate and should be placed as close to the controller as possible.
19	HO	Connect to the gate of the high-side synchronous MOSFET through a short, low inductance path.
20	SW	Switch node. Connect to the negative terminal of the bootstrap capacitor and the source terminal of the high-side MOSFET.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings(1)(2)

VIN to GND	-0.3V to 100V
VCC, VCCX, UVLO to GND (3)	-0.3 to 16V
SW, CS to GND	-3.0 to 100V
HB to SW	-0.3 to 16V
HO to SW	-0.3 to HB+0.3V
VOUT to GND	-0.3 to 100V
CSG to GND	-1V to 1V
LO to GND	-0.3 to VCC+0.3V
SS to GND	-0.3 to 7V
FB to GND	-0.3 to 7V
DEMB to GND	-0.3 to VCC
RT to GND	-0.3 to 7V
EN to GND	-0.3 to 100V
ESD Rating HBM (4)	2 kV
Storage Temperature Range	-55°C to +150°C
Junction Temperature	+150°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the component may occur.
(2) If Military/Aerospace specified devices are required, please contact the TI Sales Office/Distributors for availability and specifications.
(3) These pins must not exceed VIN.
(4) The human body model is a 100 pF capacitor discharged through a 1.5 kΩ resistor into each pin. LO, HO and HB are rated at 1 kV. 2 kV rating for all pins except V_{IN} which is rated for 1.5 kV.

Operating Ratings(1)(2)

VIN	6V to 100V
VCC, VCCX	4.75V to 15V
HB to SW	4.75V to 15V
DEMB to GND	-0.3V to 2V
Junction Temperature	-40°C to +125°C

(1) Operating Ratings are conditions under which operation of the device is intended to be functional. Operating Ratings do not imply guaranteed performance limits.
(2) Note: RAMP, COMP are output pins. As such they are not specified to have an external voltage applied.

Electrical Characteristics

Limits in standard type are for T_J = 25°C only; limits in boldface type apply over the junction temperature range of -40°C to +125°C and are provided for reference only. Unless otherwise specified, the following conditions apply: VIN = 48V, VCC = 7.4V, VCCX = 0V, EN = 5V, R_T = 16 kΩ, no load on LO and HO.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
VIN Supply						
I_{BIAS}	VIN Operating Current	VCCX = 0V, VIN = 48V		5	**7**	mA
		VCCX = 0V, VIN = 100V		5.9	**8**	mA
I_{BIASX}	VIN Operating Current	VCCX = 5V, VIN = 48V		1.2	**1.7**	mA
		VCCX = 5V, VIN = 100V		1.6	**2.3**	mA
I_{STDBY}	VIN Shutdown Current	EN = 0V, VIN = 48V		1	**10**	µA
		EN = 0V, VIN = 100V		1		µA

Electrical Characteristics (continued)

Limits in standard type are for T_J = 25°C only; limits in boldface type apply over the junction temperature range of -40°C to +125°C and are provided for reference only. Unless otherwise specified, the following conditions apply: VIN = 48V, VCC = 7.4V, VCCX = 0V, EN = 5V, R_T = 16 kΩ, no load on LO and HO.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
VCC Regulator						
$V_{CC(REG)}$	VCC Regulation		**7.1**	7.4	**7.7**	V
	VCC LDO Mode Turn-off			10.6		V
	VCC Regulation	VIN = 6V	**5.0**	5.9	**6.0**	V
	VCC Sourcing Current Limit	VCC = 0V	**15**	26		mA
	VCCX Switch Threshold	VCCX Rising	**4.3**	4.5	**4.7**	V
	VCCX Switch Hysteresis			0.25		V
	VCCX Switch $R_{DS(ON)}$	ICCX = 10 mA		3.8	**6.2**	Ω
	VCCX Leakage	VCCX = 0V		-200		nA
	VCCX Pull- down Resistance	VCCX = 3V		100		kΩ
	VCC Under-voltage Threshold	VCC Rising	**4.3**	4.5	**4.7**	V
	VCC Under-voltage Hysteresis			0.2		V
	HB DC Bias Current	HB - SW = 15V		125	**200**	µA
EN Input						
VIL max	EN Input Low Threshold				**0.5**	V
VIH min	EN Input High Threshold		**3.3**			V
	EN Input Bias Current	VEN = 3V	**-7.5**	-3	**1**	µA
	EN Input Bias Current	VEN = 0.5V	**-1**	0	**1**	µA
	EN Input Bias Current	VEN = 100V		20	**90**	µA
UVLO Thresholds						
	UVLO Standby Threshold	UVLO Rising	**1.170**	1.215	**1.262**	V
	UVLO Threshold Hysteresis			0.1		V
	UVLO Pull-up Current Source	UVLO = 0V		5.4		µA
	UVLO Pull-down $R_{DS(ON)}$			80	**210**	Ω
Soft Start						
	SS Current Source	SS = 0V	**8**	11	**14**	µA
	SS Diode Emulation Ramp Disable Threshold	SS Rising		3		V
	SS to FB Offset	FB = 1.25V		160		mV
	SS Output Low Voltage	Sinking 100 µA, UVLO = 0V		45		mV
Error Amplifier						
V_{REF}	FB Reference Voltage	Measured at FB pin, FB = COMP	**1.195**	1.215	**1.231**	V
	FB Input Bias Current	FB = 2V		15	**500**	nA
	COMP Sink/Source Current		**3**			mA
A_{OL}	DC Gain			80		dB
f_{BW}	Unity Gain Bandwidth			3		MHz
PWM Comparators						
$t_{HO(OFF)}$	Forced HO Off-time		**320**	450	**580**	ns
$t_{ON(min)}$	Minimum HO On-time	VIN = 80V, C_{RAMP} = 50 pF		100		ns
Oscillator						
f_{SW1}	Frequency 1	RT = 16 kΩ	**180**	200	**220**	kHz
f_{SW2}	Frequency 2	RT = 5 kΩ	**480**	535	**590**	kHz
	RT output voltage		**1.191**	1.215	**1.239**	V
	RT sync positive threshold		**3.0**	3.5	**4.0**	V

Electrical Characteristics (continued)

Limits in standard type are for T_J = 25°C only; limits in boldface type apply over the junction temperature range of -40°C to +125°C and are provided for reference only. Unless otherwise specified, the following conditions apply: VIN = 48V, VCC = 7.4V, VCCX = 0V, EN = 5V, R_T = 16 kΩ, no load on LO and HO.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Current Limit						
$V_{CS(TH)}$	Cycle-by-cycle Sense Voltage Threshold (CSG - CS)	VCCX = 0V, RAMP = 0V	**94**	110	**126**	mV
$V_{CS(THX)}$	Cycle-by-cycle Sense Voltage Threshold (CSG - CS)	VCCX = 5V, RAMP = 0V	**105**	122	**139**	mV
	CS Bias Current	CS = 100V	**-1**		1	µA
	CS Bias Current	CS = 0V		90	**125**	µA
	CSG Bias Current	CSG = 0V		90	**125**	µA
	Current Limit Fault Timer	R_T = 16 kΩ, (200 kHz), (256 clock cycles)		1.28		ms
RAMP Generator						
I_{R1}	RAMP Current 1	VIN = 60V, VOUT=10V	**235**	285	**335**	µA
I_{R2}	RAMP Current 2	VIN = 10V, VOUT = 10V	**21**	28	**35**	µA
	VOUT Bias Current	VOUT = 36V		200		µA
	RAMP Output Low Voltage	VIN = 60V, VOUT = 10V		265		mV
Diode Emulation						
	SW Zero Cross Threshold			-6		mV
	DEMB Output Current	DEMB = 0V, SS = 1.25V	**1.6**	2.7	**3.8**	µA
	DEMB Output Current	DEMB =0V, SS = 2.8V	**28**	38	**48**	µA
	DEMB Output Current	DEMB = 0V, SS = Regulated by FB	**45**	65	**85**	µA
LO Gate Driver						
V_{OLL}	LO Low-state Output Voltage	I_{LO} = 100 mA		0.08	**0.17**	V
V_{OHL}	LO High-state Output Voltage	I_{LO} = -100 mA, V_{OHL} = V_{CC} - V_{LO}		0.25		V
	LO Rise Time	C-load = 1000 pF		18		ns
	LO Fall Time	C-load = 1000 pF		12		ns
I_{OHL}	Peak LO Source Current	V_{LO} = 0V		1.8		A
I_{OLL}	Peak LO Sink Current	V_{LO} = VCC		3.5		A
HO Gate Driver						
V_{OLH}	HO Low-state Output Voltage	I_{HO} = 100 mA		0.17	**0.27**	V
V_{OHH}	HO High-state Output Voltage	I_{HO} = -100 mA, V_{OHH} = V_{HB} - V_{HO}		0.45		V
	HO Rise Time	C-load = 1000 pF		19		ns
	HO High-side Fall Time	C-load = 1000 pF		13		ns
I_{OHH}	Peak HO Source Current	V_{HO} = 0V		1		A
I_{OLH}	Peak HO Sink Current	V_{HO} = VCC		2.2		A
	HB to SW under-voltage			3		V
Switching Characteristics						
	LO Fall to HO Rise Delay	C-load = 0		75		ns
	HO Fall to LO Rise Delay	C-load = 0		70		ns
Thermal						
θ_{JA}	Junction to Ambient			115		°C/W
θ_{JC}	Junction to Case			13		°C/W

Typical Performance Characteristics

FB Reference Voltage vs Temperature

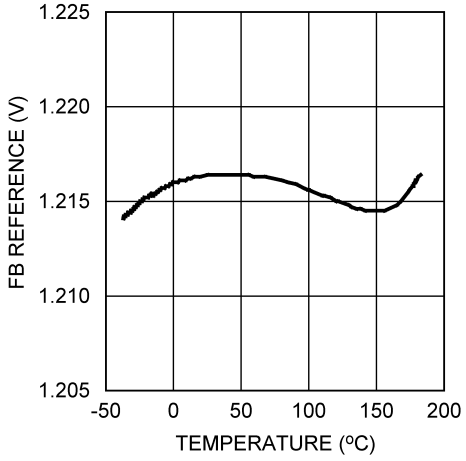


Figure 2.

FB Input Bias Current vs Temperature

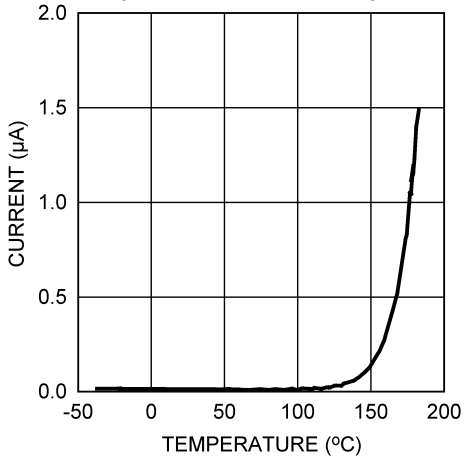


Figure 3.

EN Input Threshold vs Temperature

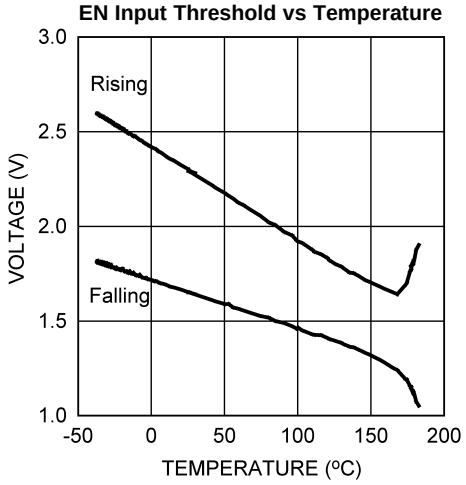


Figure 4.

VIN Operating Current vs Temperature

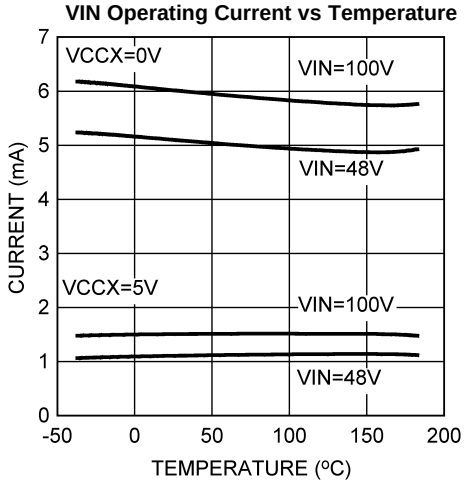


Figure 5.

SS Current vs Temperature

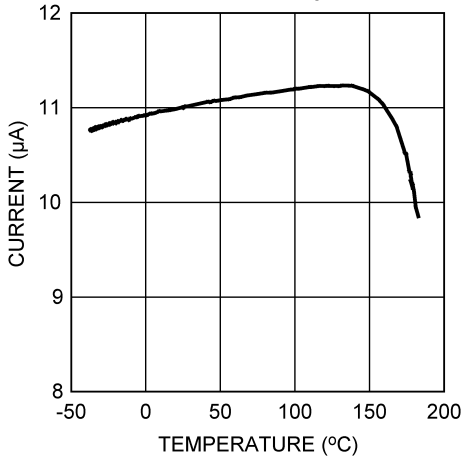


Figure 6.

RAMP Current vs Temperature

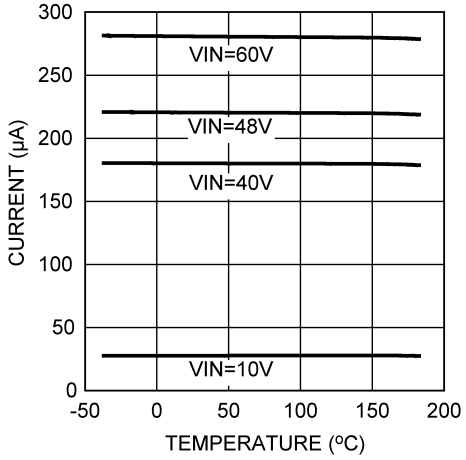


Figure 7.

Typical Performance Characteristics (continued)

VCC UVLO vs Temperature

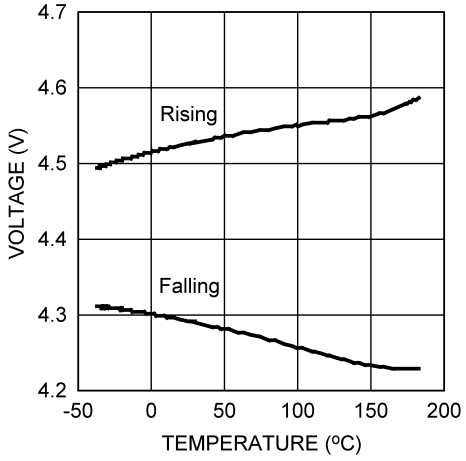


Figure 8.

VCC LDO Switch vs Temperature

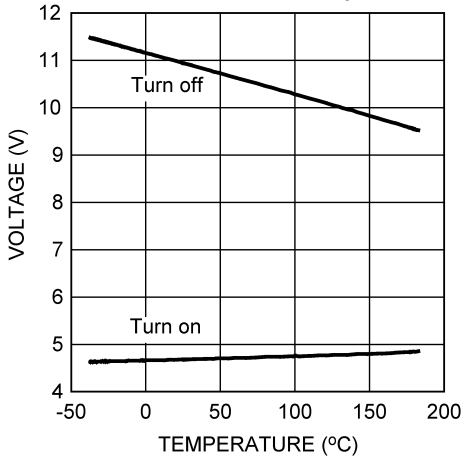


Figure 9.

VCC Regulation vs Temperature

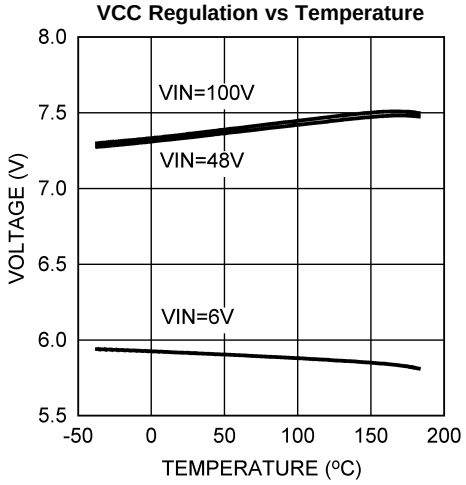


Figure 10.

VCC Current Limit vs Temperature

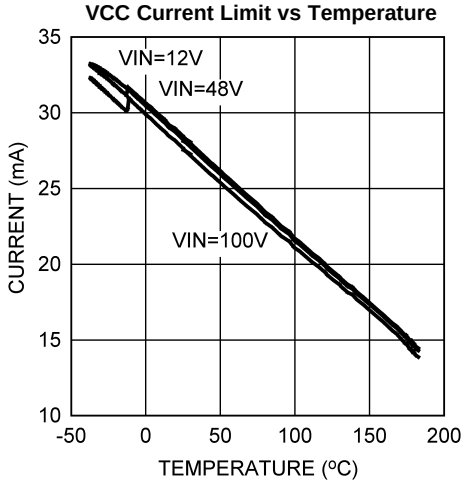


Figure 11.

VCCX Switch Threshold vs Temperature

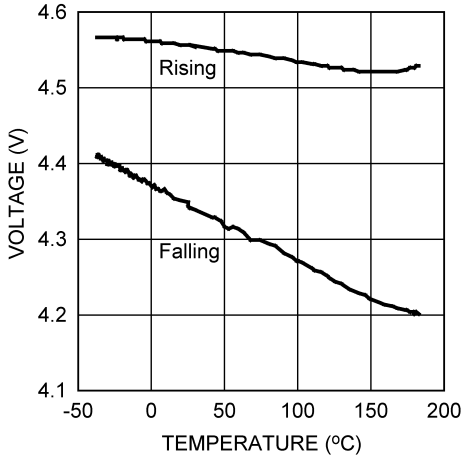


Figure 12.

VCCX Switch $R_{DS(ON)}$ vs Temperature

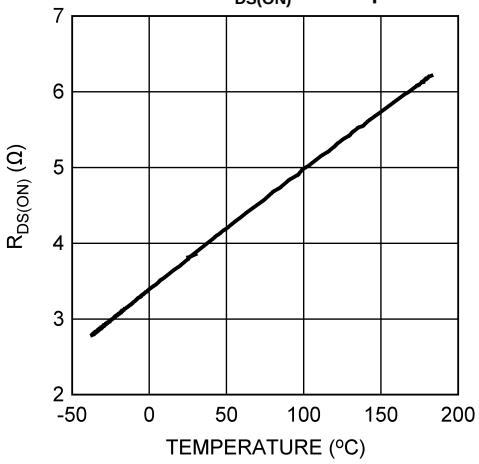


Figure 13.

Typical Performance Characteristics (continued)

Frequency vs Temperature

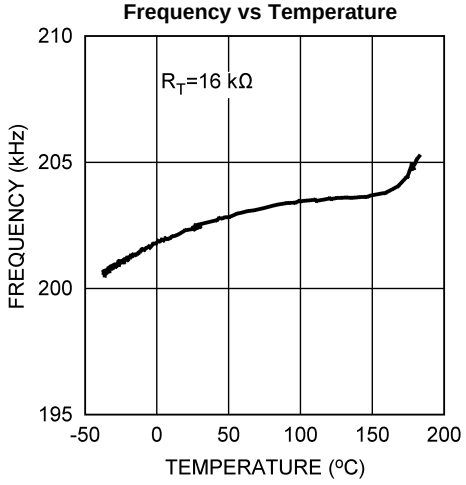


Figure 14.

Frequency vs Temperature

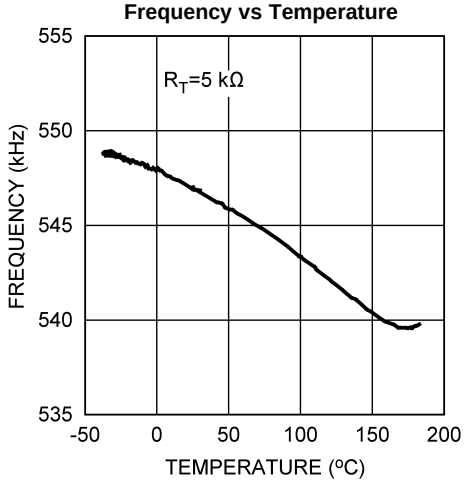


Figure 15.

RT/SYNC Threshold vs Temperature

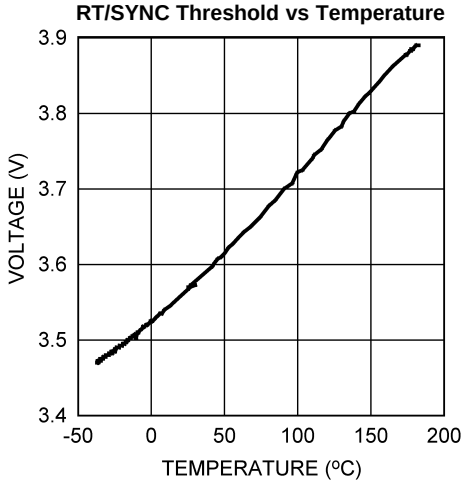


Figure 16.

RT/SYNC Hysteresis vs Temperature

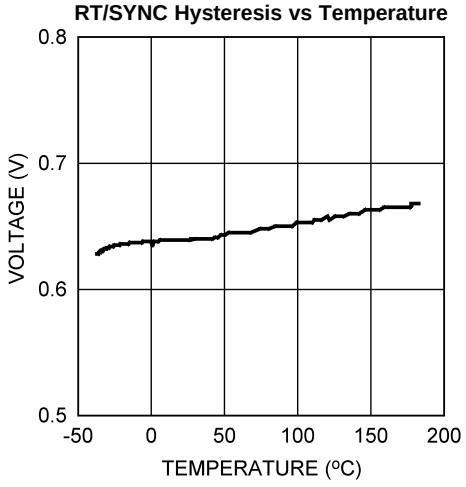


Figure 17.

Forced HO Off-Time vs Temperature

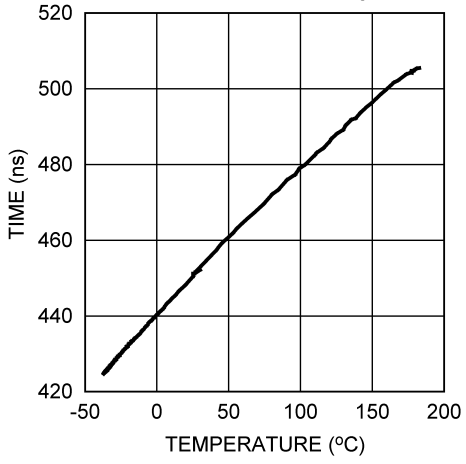


Figure 18.

DEMB Output Current vs Temperature

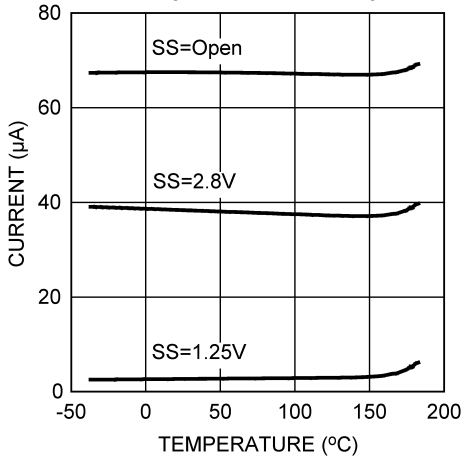


Figure 19.

Typical Performance Characteristics (continued)

Current Limit Threshold vs Temperature

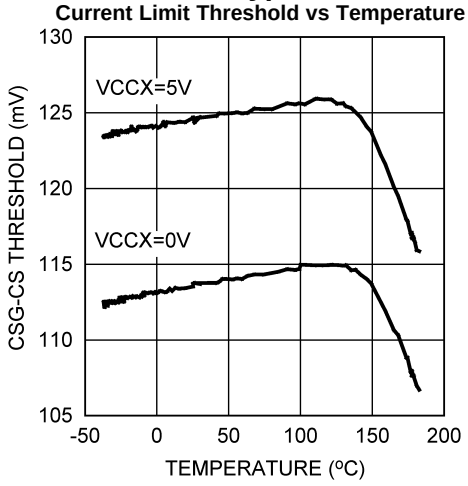


Figure 20.

HO UVLO vs Temperature

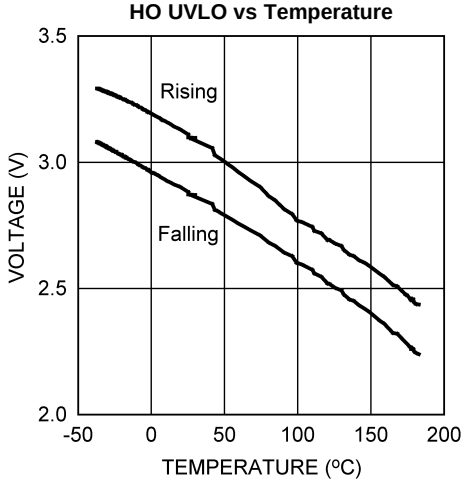


Figure 21.

CS & CSG Input Bias Current vs Temperature

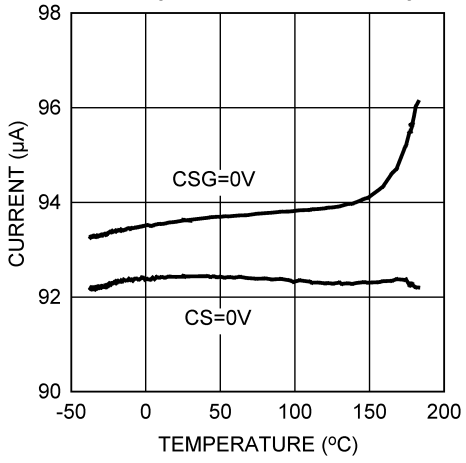


Figure 22.

HO & LO Delay vs Temperature

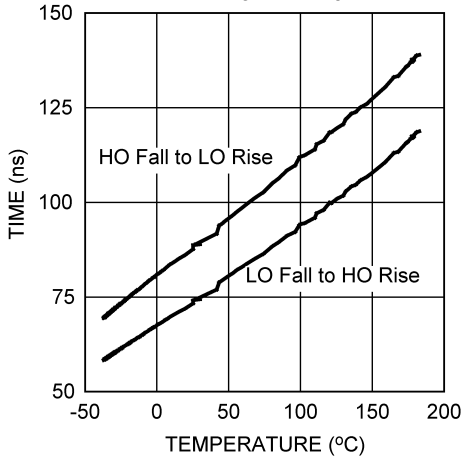


Figure 23.

CS Input Bias Current vs Temperature

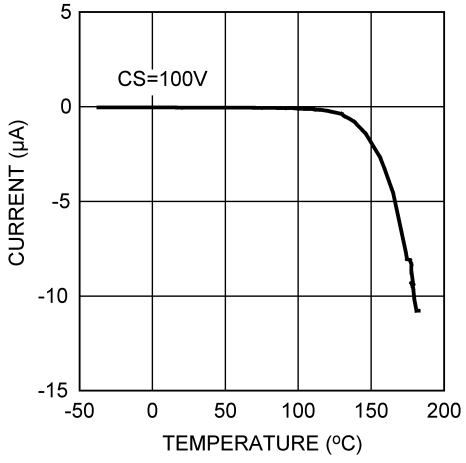


Figure 24.

HB Input Bias Current vs Temperature

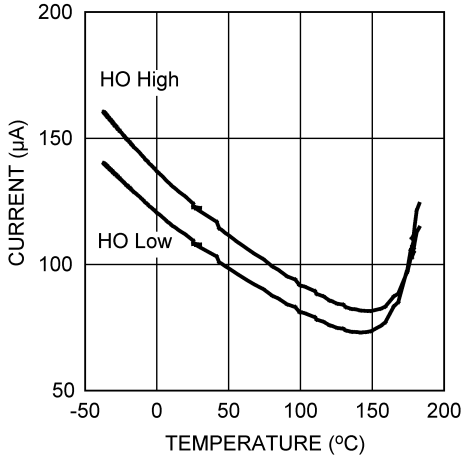


Figure 25.

Block Diagram and Typical Application Circuit

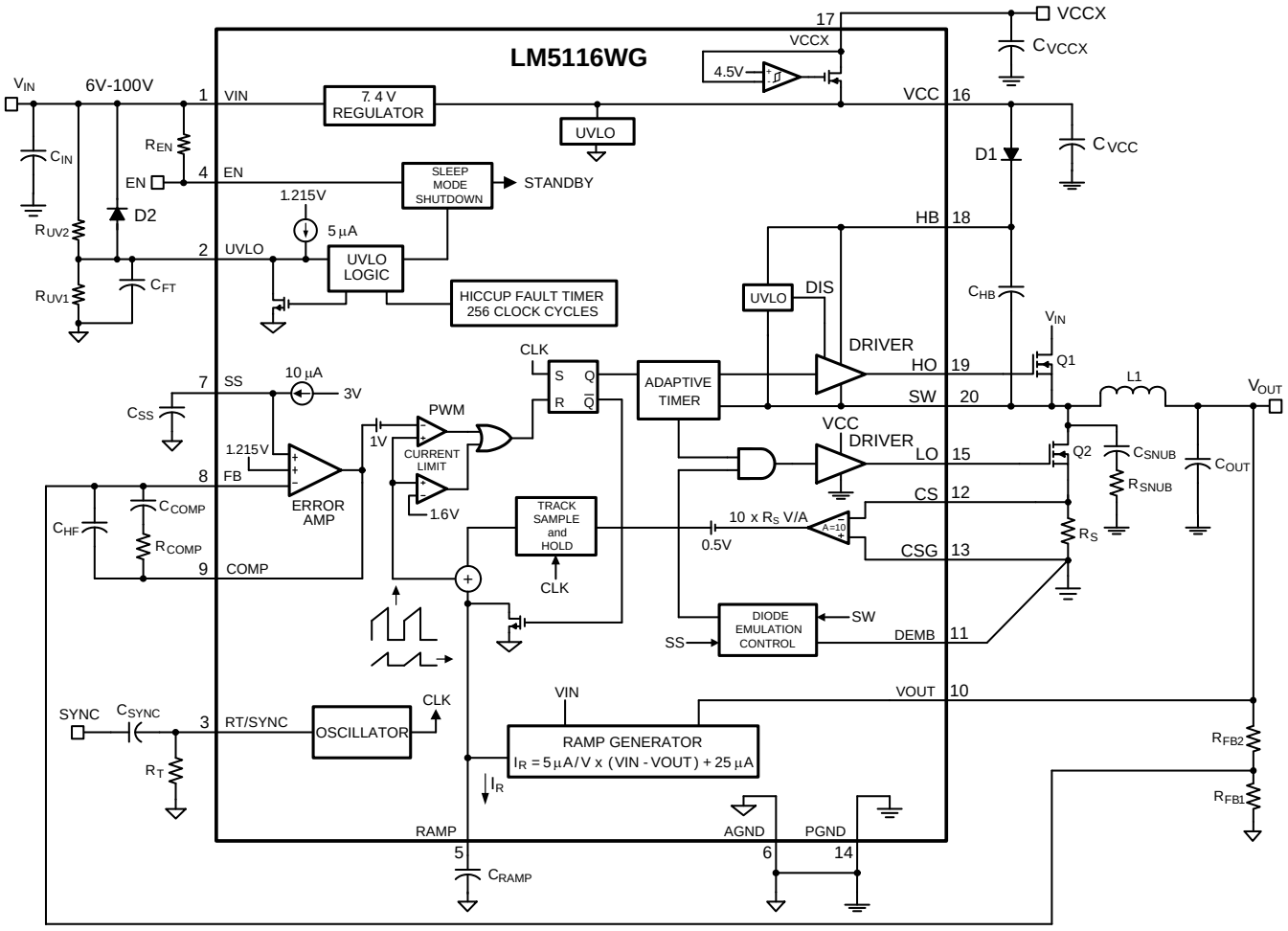


Figure 26.

DETAILED OPERATING DESCRIPTION

The LM5116WG high voltage switching regulator features all of the functions necessary to implement an efficient high voltage buck regulator using a minimum of external components. This easy to use regulator integrates high-side and low-side MOSFET drivers capable of supplying peak currents of 2 Amps. The regulator control method is based on current mode control utilizing an emulated current ramp. Emulated peak current mode control provides inherent line feed-forward, cycle by cycle current limiting and ease of loop compensation. The use of an emulated control ramp reduces noise sensitivity of the pulse-width modulation circuit, allowing reliable processing of the very small duty cycles necessary in high input voltage applications. The operating frequency is user programmable from 50 kHz to 1 MHz. An oscillator/synchronization pin allows the operating frequency to be set by a single resistor or synchronized to an external clock. Fault protection features include current limiting and remote shutdown capability. An under-voltage lockout input allows regulator shutdown when the input voltage is below a user selected threshold, and an enable function will put the regulator into an extremely low current shutdown via the enable input.

High Voltage Start-Up Regulator

The LM5116WG contains a dual mode internal high voltage startup regulator that provides the VCC bias supply for the PWM controller and a boot-strap gate drive for the high-side buck MOSFET. The input pin (VIN) can be connected directly to an input voltage source as high as 100 volts. For input voltages below 10.6V, a low dropout switch connects VCC directly to VIN. In this supply range, VCC is approximately equal to VIN. For VIN voltages greater than 10.6V, the low dropout switch is disabled and the VCC regulator is enabled to maintain VCC at approximately 7.4V. The wide operating range of 6V to 100V is achieved through the use of this dual mode regulator.

Upon power-up, the regulator sources current into the capacitor connected to the VCC pin. When the voltage at the VCC pin exceeds 4.5V and the UVLO pin is greater than 1.215V, the output switch is enabled and a soft-start sequence begins. The output switch remains enabled until VCC falls below 4.5V, EN is pulled low or the UVLO pin falls below 1.215V.

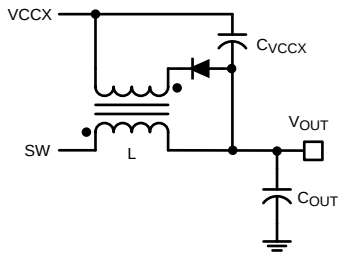


Figure 27. VCCX Bias Supply with Additional Inductor Winding

An output voltage derived bias supply can be applied to the VCCX pin to reduce the IC power dissipation. If the bias supply voltage is greater than 4.5V, the internal regulator will essentially shut off, reducing the IC power dissipation. The VCC regulator series pass transistor includes a diode between VCC and VIN that should not be forward biased in normal operation. For an output voltage between 5V and 15V, VOUT can be connected directly to VCCX. For VOUT < 5V, a bias winding on the output inductor can be added to VOUT. If the bias winding can supply VCCX greater than VIN, an external blocking diode is required from the input power supply to the VIN pin to prevent VCC from discharging into the input supply.

The output of the VCC regulator is current limited to 15 mA minimum. The VCC current is determined by the MOSFET gate charge, switching frequency and quiescent current (see MOSFETs section in the Application Information). If VCCX is powered by the output voltage or an inductor winding, the VCC current should be evaluated during startup to ensure that it is less than the 15 mA minimum current limit specification. IF VCCX is powered by an external regulator derived from VIN, there is no restriction on the VCC current.

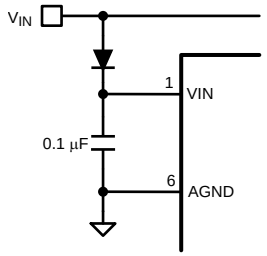


Figure 28. Input Blocking Diode for VCCX > VIN

In high voltage applications extra care should be taken to ensure the VIN pin does not exceed the absolute maximum voltage rating of 100V. During line or load transients, voltage ringing on the VIN line that exceeds the Absolute Maximum Ratings can damage the IC. Both careful PC board layout and the use of quality bypass capacitors located close to the VIN and GND pins are essential.

Enable

The LM5116WG contains an enable function allowing a very low input current shutdown. If the enable pin is pulled below 0.5V, the regulator enters shutdown, drawing less than 10 µA from the VIN pin. Raising the EN input above 3.3V returns the regulator to normal operation. The maximum EN transition time for proper operation is one switching period. For example, the enable rise time must be less than 4 µs for 250 kHz operation.

A 1 MΩ pull-up resistor to VIN can be used to interface with an open collector control signal. At low input voltage the pull-up resistor may be reduced to 100 kΩ to speed up the EN transition time. The EN pin can be tied directly to VIN if this function is not needed. It must not be left floating. If low-power shutdown is not needed, the UVLO pin should be used as an on/off control.

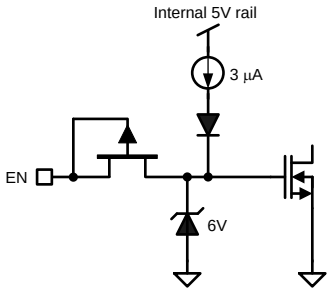


Figure 29. Enable Circuit

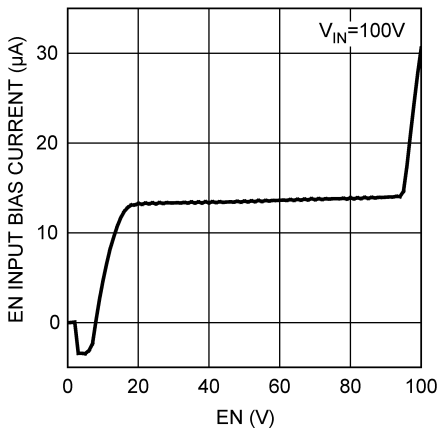


Figure 30. EN Bias Current vs Voltage

UVLO

An under-voltage lockout pin is provided to disable the regulator without entering shutdown. If the UVLO pin is pulled below 1.215V, the regulator enters a standby mode of operation with the soft-start capacitor discharged and outputs disabled, but with the VCC regulator running. If the UVLO input is pulled above 1.215V, the controller will resume normal operation. A voltage divider from input to ground can be used to set a VIN threshold to disable the supply in brown-out conditions or for low input faults. The UVLO pin has a 5 µA internal pull up current that allows this pin to left open if the input under-voltage lockout function is not needed. For applications which require fast on/off cycling, the UVLO pin with an open collector control signal may be used to ensure proper start-up sequencing.

The UVLO pin is also used to implement a “hiccup” current limit. If a current limit fault exists for more than 256 consecutive clock cycles, the UVLO pin will be internally pulled down to 200 mV and then released. A capacitor to ground connected to the UVLO pin will set the timing for hiccup mode current limit. When this feature is used in conjunction with the voltage divider, a diode across the top resistor may be used to discharge the capacitor in the event of an input under-voltage condition. There is a 5 µs filter at the input to the fault comparator. At higher switching frequency (greater than approximately 250 kHz) the hiccup timer may be disabled if the fault capacitor is not used.

Oscillator and Sync Capability

The LM5116WG oscillator frequency is set by a single external resistor connected between the RT/SYNC pin and the AGND pin. The resistor should be located very close to the device and connected directly to the pins of the IC (RT/SYNC and AGND). To set a desired oscillator frequency (f_{SW}), the necessary value for the resistor can be calculated from the following equation:

$$R_T = \frac{T - 450\ ns}{284\ pF} \quad (1)$$

Where $T = 1 / f_{SW}$ and R_T is in ohms. 450 ns represents the fixed minimum off time.

The LM5116WG oscillator has a maximum programmable frequency that is dependent on the VCC voltage. If VCC is above 6V, the frequency can be programmed up to 1 MHz. If VCCX is used to bias VCC and VCCX < 6V, the maximum programmable oscillator frequency is 750 kHz.

The RT/SYNC pin can be used to synchronize the internal oscillator to an external clock. The external clock must be a higher frequency than the free-running frequency set by the RT resistor. The internal oscillator can be synchronized to an external clock by AC coupling a positive edge into the RT/SYNC pin. The voltage at the RT/SYNC pin is nominally 1.215V and must exceed 4V to trip the internal synchronization pulse detection. A 5V amplitude signal and 100 pF coupling capacitor are recommended. The free-running frequency should be set nominally 15% below the external clock. Synchronizing above twice the free-running frequency may result in abnormal behavior of the pulse width modulator.

Error Amplifier and PWM Comparator

The internal high-gain error amplifier generates an error signal proportional to the difference between the regulated output voltage and an internal precision reference (1.215V). The output of the error amplifier is connected to the COMP pin allowing the user to provide loop compensation components, generally a type II network. This network creates a pole at very low frequency, a mid-band zero, and a noise reducing high frequency pole. The PWM comparator compares the emulated current sense signal from the RAMP generator to the error amplifier output voltage at the COMP pin.

Ramp Generator

The ramp signal used in the pulse width modulator for current mode control is typically derived directly from the buck switch current. This switch current corresponds to the positive slope portion of the inductor current. Using this signal for the PWM ramp simplifies the control loop transfer function to a single pole response and provides inherent input voltage feed-forward compensation. The disadvantage of using the buck switch current signal for PWM control is the large leading edge spike due to circuit parasitics that must be filtered or blanked. Also, the current measurement may introduce significant propagation delays. The filtering, blanking time and propagation delay limit the minimal achievable pulse width. In applications where the input voltage may be relatively large in

comparison to the output voltage, controlling small pulse widths and duty cycles is necessary for regulation. The LM5116WG utilizes a unique ramp generator which does not actually measure the buck switch current but rather reconstructs the signal. Representing or emulating the inductor current provides a ramp signal to the PWM comparator that is free of leading edge spikes and measurement or filtering delays. The current reconstruction is comprised of two elements, a sample-and-hold DC level and an emulated current ramp.

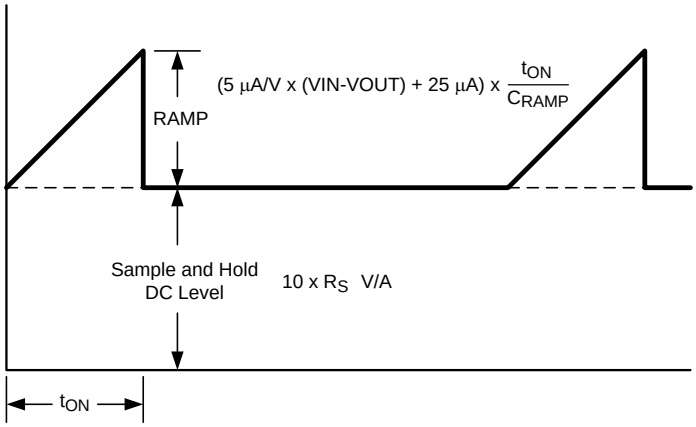


Figure 31. Composition of Current Sense Signal

The sample-and-hold DC level is derived from a measurement of the recirculating current through either the low-side MOSFET or current sense resistor. The voltage level across the MOSFET or sense resistor is sampled and held just prior to the onset of the next conduction interval of the buck switch. The current sensing and sample-and-hold provide the DC level of the reconstructed current signal. The positive slope inductor current ramp is emulated by an external capacitor connected from the RAMP pin to the AGND and an internal voltage controlled current source. The ramp current source that emulates the inductor current is a function of the VIN and VOUT voltages per the following equation:

$$I_R = 5\ \mu A/V \times (VIN - VOUT) + 25\ \mu A \quad (2)$$

Proper selection of the RAMP capacitor (C_{RAMP}) depends upon the value of the output inductor (L) and the current sense resistor (R_S). For proper current emulation, the DC sample and hold value and the ramp amplitude must have the same dependence on the load current. That is:

$$R_S \times A = \frac{g_m \times L}{C_{RAMP}}, \text{ so}$$

$$C_{RAMP} = \frac{g_m \times L}{A \times R_S} \quad (3)$$

Where g_m is the ramp generator transconductance (5 µA/V) and A is the current sense amplifier gain (10 V/V). The ramp capacitor should be located very close to the device and connected directly to the pins of the IC (RAMP and AGND).

The difference between the average inductor current and the DC value of the sampled inductor current can cause instability for certain operating conditions. This instability is known as sub-harmonic oscillation, which occurs when the inductor ripple current does not return to its initial value by the start of next switching cycle. Sub-harmonic oscillation is normally characterized by observing alternating wide and narrow pulses at the switch node. Adding a fixed slope voltage ramp (slope compensation) to the current sense signal prevents this oscillation. The 25 µA of offset current provided from the emulated current source adds the optimal slope compensation to the ramp signal for a 5V output. For higher output voltages, additional slope compensation may be required. In these applications, a resistor is added between RAMP and VCC to increase the ramp slope compensation.

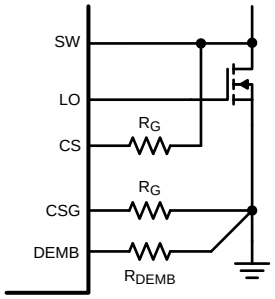


Figure 32. $R_{DS(ON)}$ Current Sensing without Diode Emulation

The DC current sample is obtained using the CS and CSG pins connected to either a source sense resistor (R_S) or the $R_{DS(ON)}$ of the low-side MOSFET. For $R_{DS(ON)}$ sensing, $R_S = R_{DS(ON)}$ of the low-side MOSFET. In this case it is sometimes helpful to adjust the current sense amplifier gain (A) to a lower value in order to obtain the desired current limit. Adding external resistors R_G in series with CS and CSG, the current sense amplifier gain A becomes:

$$A \approx \frac{10k}{1k + R_G} \tag{4}$$

Current Limit

The LM5116WG contains a current limit monitoring scheme to protect the circuit from possible over-current conditions. When set correctly, the emulated current sense signal is proportional to the buck switch current with a scale factor determined by the current limit sense resistor. The emulated ramp signal is applied to the current limit comparator. If the emulated ramp signal exceeds 1.6V, the current cycle is terminated (cycle-by-cycle current limiting). Since the ramp amplitude is proportional to V_{IN} - V_{OUT}, if V_{OUT} is shorted, there is an immediate reduction in duty cycle. To further protect the external switches during prolonged current limit conditions, an internal counter counts clock pulses when in current limit. When the counter detects 256 consecutive clock cycles, the regulator enters a low power dissipation hiccup mode of current limit. The regulator is shut down by momentarily pulling UVLO low, and the soft-start capacitor discharged. The regulator is restarted with a full soft-start cycle once UVLO charges back to 1.215V. This process is repeated until the fault is removed. The hiccup off-time can be controlled by a capacitor to ground on the UVLO pin. In applications with low output inductance and high input voltage, the switch current may overshoot due to the propagation delay of the current limit comparator. If an overshoot should occur, the sample-and-hold circuit will detect the excess recirculating current. If the sample-and-hold DC level exceeds the internal current limit threshold, the buck switch will be disabled and skip pulses until the current has decayed below the current limit threshold. This approach prevents current runaway conditions due to propagation delays or inductor saturation since the inductor current is forced to decay following any current overshoot.

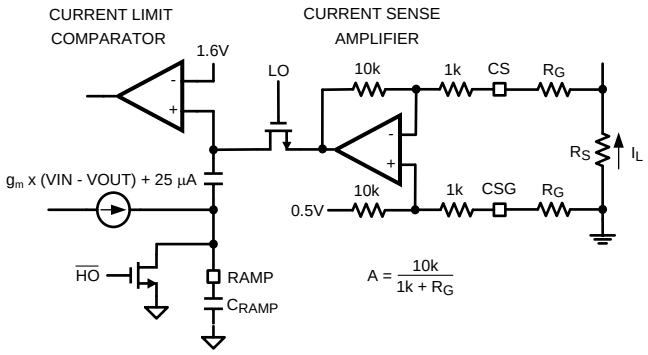


Figure 33. Current Limit and Ramp Circuit

Using a current sense resistor in the source of the low-side MOSFET provides superior current limit accuracy compared to $R_{DS(ON)}$ sensing. $R_{DS(ON)}$ sensing is far less accurate due to the large variation of MOSFET $R_{DS(ON)}$ with temperature and part-to-part variation. The CS and CSG pins should be Kelvin connected to the current sense resistor or MOSFET drain and source.

The peak current which triggers the current limit comparator is:

$$I_{PEAK} = \frac{1.1V - \frac{25\ \mu A \times t_{ON}}{C_{RAMP}}}{A \times R_S} \approx \frac{1.1V}{A \times R_S} \quad (5)$$

Where t_{ON} is the on-time of the high-side MOSFET. The 1.1V threshold is the difference between the 1.6V reference at the current limit comparator and the 0.5V offset at the current sense amplifier. This offset at the current sense amplifier allows the inductor ripple current to go negative by 0.5V / (A x R_S) when running full synchronous operation.

Current limit hysteresis prevents chatter around the threshold when VCCX is powered from VOUT. When 4.5V < VCC < 5.8V, the 1.6V reference is increased to 1.72V. The peak current which triggers the current limit comparator becomes:

$$I_{PEAK} = \frac{1.22V - \frac{25\ \mu A \times t_{ON}}{C_{RAMP}}}{A \times R_S} \approx \frac{1.22V}{A \times R_S} \quad (6)$$

This has the effect of a 10% fold-back of the peak current during a short circuit when VCCX is powered from a 5V output.

Soft-Start and Diode Emulation

The soft-start feature allows the regulator to gradually reach the initial steady state operating point, thus reducing start-up stresses and surges. The LM5116WG will regulate the FB pin to the SS pin voltage or the internal 1.215V reference, whichever is lower. At the beginning of the soft-start sequence when SS = 0V, the internal 10 µA soft-start current source gradually increases the voltage of an external soft-start capacitor (C_{SS}) connected to the SS pin resulting in a gradual rise of FB and the output voltage.

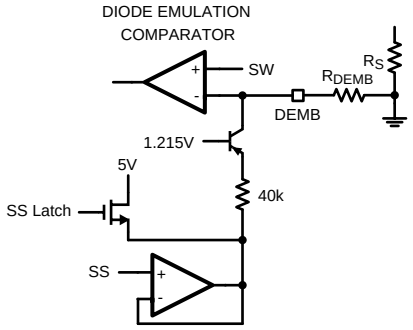


Figure 34. Diode Emulation Control

During this initial charging of C_{SS} to the internal reference voltage, the LM5116WG will force diode emulation. That is, the low-side MOSFET will turn off for the remainder of a cycle if the sensed inductor current becomes negative. The inductor current is sensed by monitoring the voltage between SW and DEMB. As the SS capacitor continues to charge beyond 1.215V to 3V, the DEMB bias current will increase from 0 µA up to 40 µA. With the use of an external DEMB resistor (R_{DEMB}), the current sense threshold for diode emulation will increase resulting in the gradual transition to synchronous operation. Forcing diode emulation during soft-start allows the LM5116WG to start up into a pre-biased output without unnecessarily discharging the output capacitor. Full synchronous operation is obtained if the DEMB pin is always biased to a higher potential than the SW pin when LO is high. R_{DEMB} = 10 kΩ will bias the DEMB pin to 0.45V minimum, which is adequate for most applications. The DEMB bias potential should always be kept below 2V. At very light loads with larger values of output inductance and MOSFET capacitance, the switch voltage may fall slowly. If the SW voltage does not fall below the DEMB threshold before the end of the HO fall to LO rise dead-time, switching will default to diode emulation mode. When R_{DEMB} = 0Ω, the LM5116WG will always run in diode emulation.

Once SS charges to 3V the SS latch is set, increasing the DEMB bias current to 65 µA. An amplifier is enabled that regulates SS to 160 mV above the FB voltage. This feature can prevent overshoot of the output voltage in the event the output voltage momentarily dips out of regulation. When a fault is detected (VCC under-voltage, UVLO pin < 1.215, or EN = 0V) the soft-start capacitor is discharged. Once the fault condition is no longer present, a new soft-start sequence begins.

HO Ouput

The LM5116WG contains a high current, high-side driver and associated high voltage level shift. This gate driver circuit works in conjunction with an external diode and bootstrap capacitor. A 1 µF ceramic capacitor, connected with short traces between the HB pin and SW pin, is recommended. During the off-time of the high-side MOSFET, the SW pin voltage is approximately -0.5V and the bootstrap capacitor charges from VCC through the external bootstrap diode. When operating with a high PWM duty cycle, the buck switch will be forced off each cycle for 450 ns to ensure that the bootstrap capacitor is recharged.

The LO and HO outputs are controlled with an adaptive deadtime methodology which insures that both outputs are never enabled at the same time. When the controller commands HO to be enabled, the adaptive block first disables LO and waits for the LO voltage to drop below approximately 25% of VCC. HO is then enabled after a small delay. Similarly, when HO turns off, LO waits until the SW voltage has fallen to ½ of VCC. LO is then enabled after a small delay. In the event that SW does not fall within approximately 150 ns, LO is asserted high. This methodology insures adequate dead-time for appropriately sized MOSFETs.

In some applications it may be desirable to slow down the high-side MOSFET turn-on time in order to control switching spikes. This may be accomplished by adding a resistor is series with the HO output to the high-side gate. Values greater than 10Ω should be avoided so as not to interfere with the adaptive gate drive. Use of an HB resistor for this function should be carefully evaluated so as not cause potentially harmful negative voltage to the high-side driver, and is generally limited to 2.2Ω maximum.

Thermal Protection

For high temperature applications in the CPGA-20, the internal thermal shutdown circuitry is disabled.

Application Information

EXTERNAL COMPONENTS

The procedure for calculating the external components is illustrated with the following design example. The Bill of Materials for this design is listed in Table 1. The circuit shown in Figure 41 is configured for the following specifications:

- Output voltage = 5V
- Input voltage = 7V to 60V
- Maximum load current = 7A
- Switching frequency = 250 kHz

Simplified equations are used as a general guideline for the design method. Comprehensive equations are provided at the end of this section.

TIMING RESISTOR

R_T sets the oscillator switching frequency. Generally, higher frequency applications are smaller but have higher losses. Operation at 250 kHz was selected for this example as a reasonable compromise for both small size and high efficiency. The value of R_T for 250 kHz switching frequency can be calculated as follows:

$$R_T = \frac{\frac{1}{250\ \text{kHz}} - 450\ \text{ns}}{284\ \text{pF}} = 12.5\ \text{k}\Omega \quad (7)$$

The nearest standard value of 12.4 kΩ was chosen for R_T.

OUTPUT INDUCTOR

The inductor value is determined based on the operating frequency, load current, ripple current and the input and output voltages.

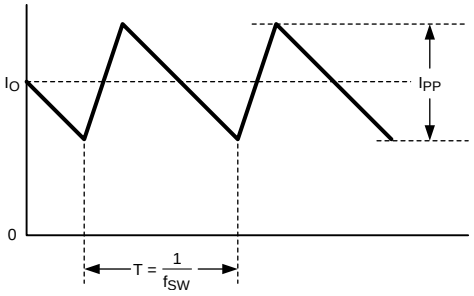


Figure 35. Inductor Current

Knowing the switching frequency (f_{SW}), maximum ripple current (I_{PP}), maximum input voltage ($V_{IN(MAX)}$) and the nominal output voltage (V_{OUT}), the inductor value can be calculated:

$$L = \frac{V_{OUT}}{I_{PP} \times f_{SW}} \times \left(1 - \frac{V_{OUT}}{V_{IN(MAX)}}\right) \quad (8)$$

The maximum ripple current occurs at the maximum input voltage. Typically, I_{PP} is 20% to 40% of the full load current. When running diode emulation mode, the maximum ripple current should be less than twice the minimum load current. For full synchronous operation, higher ripple current is acceptable. Higher ripple current allows for a smaller inductor size, but places more of a burden on the output capacitor to smooth the ripple current for low output ripple voltage. For this example, 40% ripple current was chosen for a smaller sized inductor.

$$L = \frac{5V}{0.4 \times 7A \times 250kHz} \times \left(1 - \frac{5V}{60V}\right) = 6.5\,\mu H \quad (9)$$

The nearest standard value of 6 µH will be used. The inductor must be rated for the peak current to prevent saturation. During normal operation, the peak current occurs at maximum load current plus maximum ripple. During overload conditions with properly scaled component values, the peak current is limited to $V_{CS(TH)}$ / R_S (See next section). At the maximum input voltage with a shorted output, the valley current must fall below $V_{CS(TH)}$ / R_S before the high-side MOSFET is allowed to turn on. The peak current in steady state will increase to $V_{IN(MAX)}$ x $t_{ON(min)}$ / L above this level. The chosen inductor must be evaluated for this condition, especially at elevated temperature where the saturation current rating may drop significantly.

CURRENT SENSE RESISTOR

The current limit is set by the current sense resistor value (R_S).

$$I_{LIM} = \frac{V_{CS(TH)}}{R_S} \quad (10)$$

For a 5V output, the maximum current sense signal occurs at the minimum input voltage, so R_S is calculated from:

$$R_S \le \frac{V_{CS(TH)}}{I_O + \frac{V_{OUT}}{2 \times L \times f_{SW}} \times \left(1 + \frac{V_{OUT}}{V_{IN(MIN)}}\right)} \quad (11)$$

For this example VCCX = 0V, so $V_{CS(TH)}$ = 0.11V. The current sense resistor is calculated as:

$$R_S \le \frac{0.11V}{7A + \frac{5V}{2 \times 6\,\mu H \times 250\,kHz} \times \left(1 + \frac{5V}{7V}\right)} \le 0.011\Omega \quad (12)$$

The next lowest standard value of 10 mΩ was chosen for R_S.

RAMP CAPACITOR

With the inductor and sense resistor value selected, the value of the ramp capacitor (C_{RAMP}) necessary for the emulation ramp circuit is:

$$C_{RAMP} \approx \frac{g_m \times L}{A \times R_S} \tag{13}$$

Where L is the value of the output inductor in Henrys, g_m is the ramp generator transconductance (5 µA/V), and A is the current sense amplifier gain (10 V/V). For the 5V output design example, the ramp capacitor is calculated as:

$$C_{RAMP} = \frac{5\ \mu A/V \times 6\ \mu H}{10 V/V \times 10\ m\Omega} = 300\ pF \tag{14}$$

The next lowest standard value of 270 pF was selected for C_{RAMP}. A COG type capacitor with 5% or better tolerance is recommended.

OUTPUT CAPACITORS

The output capacitors smooth the inductor ripple current and provide a source of charge for transient loading conditions. For this design example, five 100 µF ceramic capacitors where selected. Ceramic capacitors provide very low equivalent series resistance (ESR), but can exhibit a significant reduction in capacitance with DC bias. From the manufacturer's data, the ESR at 250 kHz is 2 mΩ / 5 = 0.4 mΩ, with a 36% reduction in capacitance at 5V. This is verified by measuring the output ripple voltage and frequency response of the circuit. The fundamental component of the output ripple voltage is calculated as:

$$\Delta V_{OUT} = I_{PP} \times \sqrt{ESR^2 + \left(\frac{1}{8 \times f_{SW} \times C_{OUT}}\right)^2} \tag{15}$$

With typical values for the 5V design example:

$$\Delta V_{OUT} = 3A \times \sqrt{0.4\ m\Omega^2 + \left(\frac{1}{8 \times 250\ kHz \times 320\ \mu F}\right)^2}$$

$$\Delta V_{OUT} = 4.8\ mV \tag{16}$$

INPUT CAPACITORS

The regulator supply voltage has a large source impedance at the switching frequency. Good quality input capacitors are necessary to limit the ripple voltage at the VIN pin while supplying most of the switch current during the on-time. When the buck switch turns on, the current into the switch steps to the valley of the inductor current waveform, ramps up to the peak value, and then drops to zero at turn-off. The input capacitors should be selected for RMS current rating and minimum ripple voltage. A good approximation for the required ripple current rating is $I_{RMS} > I_{OUT} / 2$.

Quality ceramic capacitors with a low ESR were selected for the input filter. To allow for capacitor tolerances and voltage rating, four 2.2 µF, 100V ceramic capacitors were used for the typical application circuit. With ceramic capacitors, the input ripple voltage will be triangular and peak at 50% duty cycle. Taking into account the capacitance change with DC bias, the input ripple voltage is approximated as:

$$\Delta V_{IN} = \frac{I_{OUT}}{4 \times f_{SW} \times C_{IN}} = \frac{7A}{4 \times 250\ kHz \times 7\ \mu F} = 1V \tag{17}$$

When the converter is connected to an input power source, a resonant circuit is formed by the line impedance and the input capacitors. If step input voltage transients are expected near the maximum rating of the LM5116WG, a careful evaluation of the ringing and possible overshoot at the device VIN pin should be completed. To minimize overshoot make $C_{IN} > 10 \times L_{IN}$. The characteristic source impedance and resonant frequency are:

$$Z_S = \sqrt{\frac{L_{IN}}{C_{IN}}} \qquad f_S = \frac{1}{2\pi\sqrt{L_{IN} \times C_{IN}}} \tag{18}$$

The converter exhibits a negative input impedance which is lowest at the minimum input voltage:

$$Z_{IN} = -\frac{V_{IN}^2}{P_{OUT}} \tag{19}$$

The damping factor for the input filter is given by:

$$\delta = \frac{1}{2}\left(\frac{R_{IN} + ESR}{Z_S} + \frac{Z_S}{Z_{IN}}\right) \tag{20}$$

where R_{IN} is the input wiring resistance and ESR is the series resistance of the input capacitors. The term Z_S/Z_{IN} will always be negative due to Z_{IN}.

When δ = 1, the input filter is critically damped. This may be difficult to achieve with practical component values. With δ < 0.2, the input filter will exhibit significant ringing. If δ is zero or negative, there is not enough resistance in the circuit and the input filter will sustain an oscillation. When operating near the minimum input voltage, an aluminum electrolytic capacitor across C_{IN} may be needed to damp the input for a typical bench test setup. Any parallel capacitor should be evaluated for its RMS current rating. The current will split between the ceramic and aluminum capacitors based on the relative impedance at the switching frequency.

VCC CAPACITOR

The primary purpose of the VCC capacitor (C_{VCC}) is to supply the peak transient currents of the LO driver and bootstrap diode (D1) as well as provide stability for the VCC regulator. These current peaks can be several amperes. The recommended value of C_{VCC} should be no smaller than 0.47 µF, and should be a good quality, low ESR, ceramic capacitor located at the pins of the IC to minimize potentially damaging voltage transients caused by trace inductance. A value of 1 µF was selected for this design.

BOOTSTRAP CAPACITOR

The bootstrap capacitor (C_{HB}) between the HB and SW pins supplies the gate current to charge the high-side MOSFET gate at each cycle's turn-on as well as supplying the recovery charge for the bootstrap diode (D1). These current peaks can be several amperes. The recommended value of the bootstrap capacitor is at least 0.1 µF, and should be a good quality, low ESR, ceramic capacitor located at the pins of the IC to minimize potentially damaging voltage transients caused by trace inductance. The absolute minimum value for the bootstrap capacitor is calculated as:

$$C_{HB} \geq \frac{Q_g}{\Delta V_{HB}} \tag{21}$$

Where Q_g is the high-side MOSFET gate charge and ΔV_{HB} is the tolerable voltage droop on C_{HB}, which is typically less than 5% of VCC. A value of 1 µF was selected for this design.

SOFT-START CAPACITOR

The capacitor at the SS pin (C_{SS}) determines the soft-start time, which is the time for the reference voltage and the output voltage to reach the final regulated value. The soft-start time t_{SS} should be substantially longer than the time required to charge C_{OUT} to V_{OUT} at the maximum output current. To meet this requirement:

$$t_{SS} > V_{OUT} \times C_{OUT} / (I_{CURRENT\ LIMIT} - I_{OUT}) \tag{22}$$

The value of C_{SS} for a given time is determined from:

$$C_{SS} = \frac{t_{SS} \times 10\ \mu A}{1.215V} \tag{23}$$

For this application, a value of 0.01 µF was chosen for a soft-start time of 1.2 ms.

OUTPUT VOLTAGE DIVIDER

R_{FB1} and R_{FB2} set the output voltage level, the ratio of these resistors is calculated from:

$$\frac{R_{FB2}}{R_{FB1}} = \frac{V_{OUT}}{1.215V} - 1 \tag{24}$$

R_{FB1} is typically 1.21 kΩ for a divider current of 1 mA. The divider current can be reduced to 100 µA with R_{FB1}=12.1 kΩ. For the 5V output design example used here, R_{FB1} = 1.21 kΩ and R_{FB2} = 3.74 kΩ.

UVLO DIVIDER

A voltage divider and filter can be connected to the UVLO pin to set a minimum operating voltage $V_{IN(MIN)}$ for the regulator. If this feature is required, the following procedure can be used to determine appropriate resistor values for R_{UV2}, R_{UV1} and C_{FT}.

1. R_{UV2} must be large enough such that in the event of a current limit, the internal UVLO switch can pull UVLO < 200mV. This can be guaranteed if:

   $R_{UV2} > 500 \times V_{IN(MAX)}$

   where

   - $V_{IN(MAX)}$ is the maximum input voltage and R_{UV2} is in ohms.
2. With an appropriate value for R_{UV2}, R_{UV1} can be selected using the following equation:

   $$R_{UV1} = 1.215 \times \left(\frac{R_{UV2}}{V_{IN(MIN)} + (5\ \mu A \times R_{UV2}) - 1.215} \right)$$

   where

   - $V_{IN(MIN)}$ is the desired shutdown voltage.
3. Capacitor C_{FT} provides filtering for the divider and determines the off-time of the “hiccup” duty cycle during current limit. When C_{FT} is used in conjunction with the voltage divider, a diode across the top resistor should be used to discharge C_{FT} in the event of an input under-voltage condition.

   $$t_{OFF} = - \left(\frac{R_{UV1} \times R_{UV2}}{R_{UV1} + R_{UV2}} \right) \times C_{FT} \times \ln \left(1 - \frac{1.215 \times (R_{UV1} + R_{UV2})}{V_{IN} \times R_{UV1}} \right)$$

If under-voltage shutdown is not required, R_{UV1} and R_{UV2} can be eliminated and the off-time becomes:

$$t_{OFF} = C_{FT} \times \frac{1.215V}{5\ \mu A} \tag{25}$$

The voltage at the UVLO pin should never exceed 16V when using an external set-point divider. It may be necessary to clamp the UVLO pin at high input voltages. For the design example, R_{UV2} = 102 kΩ and R_{UV1} = 21 kΩ for a shut-down voltage of 6.6V. If sustained short circuit protection is required, $C_{FT} \geq 1\ \mu F$ will limit the short circuit power dissipation. D2 may be installed when using C_{FT} with R_{UV1} and R_{UV2}.

MOSFETs

Selection of the power MOSFETs is governed by the same tradeoffs as switching frequency. Breaking down the losses in the high-side and low-side MOSFETs is one way to determine relative efficiencies between different devices. When using discrete SO-8 MOSFETs the LM5116WG is most efficient for output currents of 2A to 10A. Losses in the power MOSFETs can be broken down into conduction loss, gate charging loss, and switching loss. Conduction, or I^2R loss P_{DC}, is approximately:

$$P_{DC(HO\text{-}MOSFET)} = D \times (I_O^2 \times R_{DS(ON)} \times 1.3) \tag{26}$$

$$P_{DC(LO\text{-}MOSFET)} = (1 - D) \times (I_O^2 \times R_{DS(ON)} \times 1.3) \tag{27}$$

Where D is the duty cycle. The factor 1.3 accounts for the increase in MOSFET on-resistance due to heating. Alternatively, the factor of 1.3 can be ignored and the on-resistance of the MOSFET can be estimated using the $R_{DS(ON)}$ vs Temperature curves in the MOSFET datasheet. Gate charging loss, P_{GC}, results from the current driving the gate capacitance of the power MOSFETs and is approximated as:

$$P_{GC} = n \times VCC \times Q_g \times f_{SW} \tag{28}$$

Q_g refer to the total gate charge of an individual MOSFET, and ‘n’ is the number of MOSFETs. If different types of MOSFETs are used, the ‘n’ term can be ignored and their gate charges summed to form a cumulative Q_g. Gate charge loss differs from conduction and switching losses in that the actual dissipation occurs in the LM5116WG and not in the MOSFET itself. Further loss in the LM5116WG is incurred as the gate driving current is supplied by the internal linear regulator. The gate drive current supplied by the VCC regulator is calculated as:

$$I_{GC} = (Q_{gh} + Q_{gl}) \times f_{SW} \tag{29}$$

Where $Q_{gh} + Q_{gl}$ represent the gate charge of the HO and LO MOSFETs at VGS = VCC. To ensure start-up, I_{GC} should be less than the VCC current limit rating of 15 mA minimum when powered by the internal 7.4V regulator. Failure to observe this rating may result in excessive MOSFET heating and potential damage. The I_{GC} run current may exceed 15 mA when VCC is powered by VCCX.

Switching loss occurs during the brief transition period as the MOSFET turns on and off. During the transition period both current and voltage are present in the channel of the MOSFET. The switching loss can be approximated as:

$$P_{SW} = 0.5 \times V_{IN} \times I_O \times (t_R + t_F) \times f_{SW} \quad (30)$$

Where t_R and t_F are the rise and fall times of the MOSFET. Switching loss is calculated for the high-side MOSFET only. Switching loss in the low-side MOSFET is negligible because the body diode of the low-side MOSFET turns on before the MOSFET itself, minimizing the voltage from drain to source before turn-on. For this example, the maximum drain-to-source voltage applied to either MOSFET is 60V. VCC provides the drive voltage at the gate of the MOSFETs. The selected MOSFETs must be able to withstand 60V plus any ringing from drain to source, and be able to handle at least VCC plus ringing from gate to source. A good choice of MOSFET for the 60V input design example is the Si7850DP. It has an $R_{DS(ON)}$ of 20 mΩ, total gate charge of 14 nC, and rise and fall times of 10 ns and 12 ns respectively. In applications where a high step-down ratio is maintained for normal operation, efficiency may be optimized by choosing a high-side MOSFET with lower Q_g, and low-side MOSFET with lower $R_{DS(ON)}$.

For higher voltage MOSFETs which are not true logic level, it is important to use the UVLO feature. Choose a minimum operating voltage which is high enough for VCC and the bootstrap (HB) supply to fully enhance the MOSFET gates. This will prevent operation in the linear region during power-on or power-off which can result in MOSFET failure. Similar consideration must be made when powering VCCX from the output voltage. For the high-side MOSFET, the gate threshold should be considered and careful evaluation made if the gate threshold voltage exceeds the HO driver UVLO.

MOSFET SNUBBER

A resistor-capacitor snubber network across the low-side MOSFET reduces ringing and spikes at the switching node. Excessive ringing and spikes can cause erratic operation and couple spikes and noise to the output. Selecting the values for the snubber is best accomplished through empirical methods. First, make sure the lead lengths for the snubber connections are very short. Start with a resistor value between 5Ω and 50Ω. Increasing the value of the snubber capacitor results in more damping, but higher snubber losses. Select a minimum value for the snubber capacitor that provides adequate damping of the spikes on the switch waveform at high load.

ERROR AMPLIFIER COMPENSATION

R_{COMP}, C_{COMP} and C_{HF} configure the error amplifier gain characteristics to accomplish a stable voltage loop gain. One advantage of current mode control is the ability to close the loop with only two feedback components, R_{COMP} and C_{COMP}. The voltage loop gain is the product of the modulator gain and the error amplifier gain. For the 5V output design example, the modulator is treated as an ideal voltage-to-current converter. The DC modulator gain of the LM5116WG can be modeled as:

$$\text{DC Gain}_{(MOD)} = R_{LOAD} / (A \times R_S) \quad (31)$$

The dominant low frequency pole of the modulator is determined by the load resistance (R_{LOAD}) and output capacitance (C_{OUT}). The corner frequency of this pole is:

$$f_{P(MOD)} = 1 / (2\pi \times R_{LOAD} \times C_{OUT}) \quad (32)$$

For R_{LOAD} = 5V / 7A = 0.714Ω and C_{OUT} = 320 µF (effective) then $f_{P(MOD)}$ = 700 Hz

$\text{DC Gain}_{(MOD)}$ = 0.714Ω / (10 x 10 mΩ) = 7.14 = 17 dB

For the 5V design example the modulator gain vs. frequency characteristic was measured as shown in Figure 36.

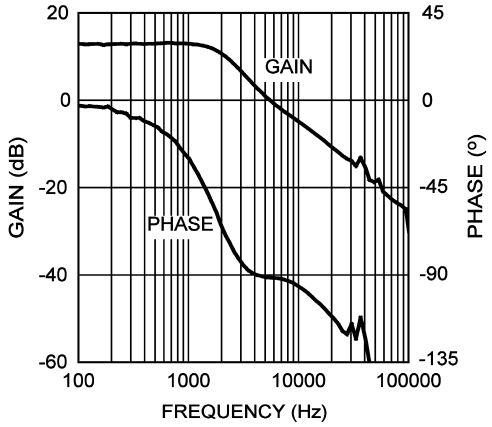


Figure 36. Modulator Gain and Phase

Components R_{COMP} and C_{COMP} configure the error amplifier as a type II configuration. The DC gain of the amplifier is 80 dB which has a pole at low frequency and a zero at $f_{ZEA} = 1 / (2\pi \times R_{COMP} \times C_{COMP})$. The error amplifier zero cancels the modulator pole leaving a single pole response at the crossover frequency of the voltage loop. A single pole response at the crossover frequency yields a very stable loop with 90° of phase margin. For the design example, a target loop bandwidth (crossover frequency) of one-tenth the switching frequency or 25 kHz was selected. The compensation network zero (f_{ZEA}) should be selected at least an order of magnitude less than the target crossover frequency. This constrains the product of R_{COMP} and C_{COMP} for a desired compensation network zero $1 / (2\pi \times R_{COMP} \times C_{COMP})$ to be 2.5 kHz. Increasing R_{COMP}, while proportionally decreasing C_{COMP}, increases the error amp gain. Conversely, decreasing R_{COMP} while proportionally increasing C_{COMP}, decreases the error amp gain. For the design example C_{COMP} was selected as 3300 pF and R_{COMP} was selected as 18 kΩ. These values configure the compensation network zero at 2.7 kHz. The error amp gain at frequencies greater than f_{ZEA} is: R_{COMP} / R_{FB2}, which is approximately 4.8 (13.6 dB).

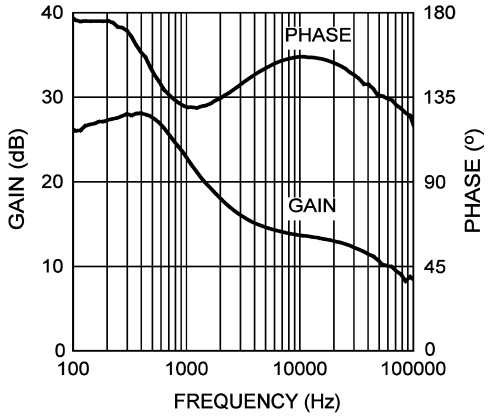


Figure 37. Error Amplifier Gain and Phase

The overall voltage loop gain can be predicted as the sum (in dB) of the modulator gain and the error amp gain.

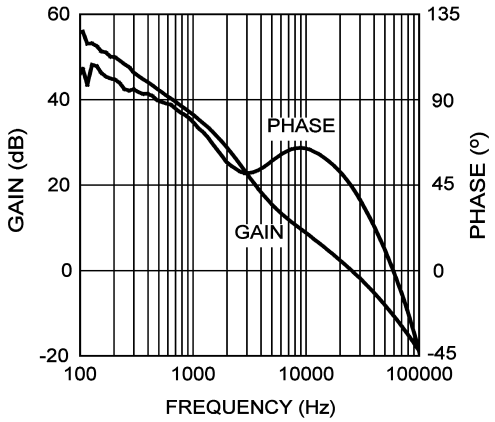


Figure 38. Overall Voltage Loop Gain and Phase

If a network analyzer is available, the modulator gain can be measured and the error amplifier gain can be configured for the desired loop transfer function. If a network analyzer is not available, the error amplifier compensation components can be designed with the guidelines given. Step load transient tests can be performed to verify acceptable performance. The step load goal is minimum overshoot with a damped response. C_{HF} can be added to the compensation network to decrease noise susceptibility of the error amplifier. The value of C_{HF} must be sufficiently small since the addition of this capacitor adds a pole in the error amplifier transfer function. This pole must be well beyond the loop crossover frequency. A good approximation of the location of the pole added by C_{HF} is: $f_{P2} = f_{ZEA} \times C_{COMP} / C_{HF}$. The value of C_{HF} was selected as 100 pF for the design example.

PCB BOARD LAYOUT and THERMAL CONSIDERATIONS

In a buck regulator the primary switching loop consists of the input capacitor, MOSFETs and current sense resistor. Minimizing the area of this loop reduces the stray inductance and minimizes noise and possible erratic operation. The input capacitor should be placed as close as possible to the MOSFETs, with the VIN side of the capacitor connected directly to the high-side MOSFET drain, and the GND side of the capacitor connected as close as possible to the low-side source or current sense resistor ground connection. A ground plane in the PC board is recommended as a means to connect the quiet end (input voltage ground side) of the input filter capacitors to the output filter capacitors and the PGND pin of the regulator. Connect all of the low power ground connections (C_{SS}, R_T, C_{RAMP}) directly to the regulator AGND pin. Connect the AGND and PGND pins together through to a topside copper area covering the entire underside of the device. Place several vias in this underside copper area to the ground plane.

The highest power dissipating components are the two power MOSFETs. The easiest way to determine the power dissipated in the MOSFETs is to measure the total conversion losses (P_{IN} - P_{OUT}), then subtract the power losses in the output inductor and any snubber resistors. The resulting power losses are primarily in the switching MOSFETs.

If a snubber is used, the power loss can be estimated with an oscilloscope by observation of the resistor voltage drop at both turn-on and turn-off transitions. Assuming that the RC time constant is << 1 / f_{SW}.

$$P = C \times V^2 \times f_{SW} \quad (33)$$

Selecting MOSFETs with exposed pads will aid the power dissipation of these devices. Careful attention to $R_{DS(ON)}$ at high temperature should be observed. Also, at 250 kHz, a MOSFET with low gate capacitance will result in lower switching losses.

Comprehensive Equations

CURRENT SENSE RESISTOR AND RAMP CAPACITOR

$T = 1 / f_{SW}$, g_m = 5 µA/V, A = 10 V/V. I_{OUT} is the maximum output current at current limit.

General Method for V_{OUT} < 5V:

$$R_S = \frac{V_{CS(TH)}}{I_{OUT} - \frac{V_{OUT} \times T}{2 \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN(MIN)}}\right) + \frac{V_{OUT} \times T}{L} \times \frac{\left(1 + \frac{5 - V_{OUT}}{V_{IN(MIN)}}\right)}{\left(1 + \frac{5 - V_{OUT}}{V_{IN(MAX)}}\right)}} \quad (34)$$

$$C_{RAMP} = \frac{g_m \times L}{A \times R_S} \times \left(1 + \frac{5 - V_{OUT}}{V_{IN(MAX)}}\right) \quad (35)$$

General Method for 5V < V_{OUT} < 7.5V:

$$R_S = \frac{V_{CS(TH)}}{I_{OUT} - \frac{V_{OUT} \times T}{2 \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN(MIN)}}\right) + \frac{V_{OUT} \times T}{L}} \quad (36)$$

$$C_{RAMP} = \frac{g_m \times L}{A \times R_S} \times \left(1 + \frac{5 - V_{OUT}}{V_{IN(MIN)}}\right) \quad (37)$$

Best Performance Method:

This minimizes the current limit deviation due to changes in line voltage, while maintaining near optimal slope compensation.

Calculate optimal slope current, I_{OS} = (V_{OUT} / 3) x 10 µA/V. For example, at V_{OUT} = 7.5V, I_{OS} = 25 µA.

$$R_S = \frac{V_{CS(TH)}}{I_{OUT} + \frac{V_{OUT} \times T}{L}} \quad C_{RAMP} = \frac{I_{OS} \times L}{V_{OUT} \times A \times R_S} \quad (38)$$

Calculate V_{RAMP} at the nominal input voltage.

$$V_{RAMP} = \frac{V_{OUT}}{V_{IN}} \times \frac{((V_{IN} - V_{OUT}) \times g_m + I_{OS}) \times T}{C_{RAMP}} \quad (39)$$

For V_{OUT} > 7.5V, install a resistor from the RAMP pin to VCC.

$$R_{RAMP} = \frac{VCC - V_{RAMP}}{I_{OS} - 25\ \mu A} \quad (40)$$

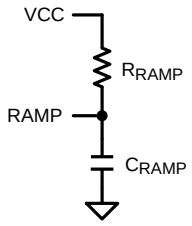


Figure 39. R_{RAMP} to VCC for V_{OUT} > 7.5V

For V_{OUT} < 7.5V, a negative VCC is required. This can be made with a simple charge pump from the LO gate output. Install a resistor from the RAMP pin to the negative VCC.

$$R_{RAMP} = \frac{VCC - 0.5V + V_{RAMP}}{25\ \mu A - I_{OS}} \quad (41)$$

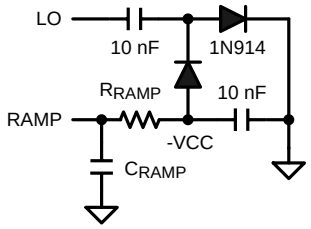


Figure 40. R_{RAMP} to -VCC for V_{OUT} < 7.5V

If a large variation is expected in VCC, say for V_{IN} < 11V, a Zener regulator may be added to supply a constant voltage for R_{RAMP}.

MODULATOR TRANSFER FUNCTION

The following equations can be used to calculate the control-to-output transfer function:

$$\frac{\hat{V}_{OUT}}{\hat{V}_{COMP}} = \frac{R_{LOAD}}{A \times R_S} \times \frac{1}{1 + \frac{R_{LOAD}}{K_m \times A \times R_S}} \times \frac{1 + \frac{s}{\omega_Z}}{\left(1 + \frac{s}{\omega_P}\right) \times \left(1 + \frac{s}{\omega_n \times Q} + \frac{s^2}{\omega_n^2}\right)} \tag{42}$$

$$K_m = \frac{1}{\frac{(D - 0.5) \times A \times R_S \times T}{L} + (1 - 2 \times D) \times K_{SL} + \frac{V_{SL}}{V_{IN}}} \tag{43}$$

$$K_{SL} = \frac{g_m \times T}{C_{RAMP}} \qquad V_{SL} = \frac{I_{OS} \times T}{C_{RAMP}} \tag{44}$$

$$\omega_Z = \frac{1}{C_{OUT} \times ESR} \quad \omega_P = \frac{1}{C_{OUT}} \times \left(\frac{1}{R_{LOAD}} + \frac{1}{K_m \times A \times R_S}\right) \quad \omega_n = \frac{\pi}{T} \tag{45}$$

$$S_e = \frac{(V_{IN} - V_{OUT}) \times K_{SL} + V_{SL}}{T} \qquad S_n = \frac{V_{IN} \times A \times R_S}{L}$$

$$m_C = \frac{S_e}{S_n} \qquad Q = \frac{1}{\pi \times (m_C - 0.5)} \tag{46}$$

K_m is the effective DC gain of the modulating comparator. The duty cycle D = V_{OUT} / V_{IN}. K_{SL} is the proportional slope compensation term. V_{SL} is the fixed slope compensation term. Slope compensation is set by m_c, which is the ratio of the external ramp to the natural ramp. The switching frequency sampling gain is characterized by ω_n and Q, which accounts for the high frequency inductor pole.

For V_{SL} without R_{RAMP}, use I_{OS} = 25 µA

For V_{SL} with R_{RAMP} to V_{CC}, use I_{OS} = 25 µA + V_{CC}/R_{RAMP}

For V_{SL} with R_{RAMP} to -V_{CC}, use I_{OS} = 25 µA - V_{CC}/R_{RAMP}

ERROR AMPLIFIER TRANSFER FUNCTION

The following equations are used to calculate the error amplifier transfer function:

$$\frac{\hat{V}_{COMP}}{\hat{V}_{OUT(FB)}} = -G_{EA(S)} \times \frac{1}{1 + \left(\frac{1}{A_{OL}} + \frac{s}{\omega_{BW}}\right) \times \left(1 + \frac{G_{EA(S)}}{K_{FB}}\right)} \tag{47}$$

$$G_{EA(S)} = \frac{1 + \frac{s}{\omega_{ZEA}}}{\frac{s}{\omega_O} \times \left(1 + \frac{s}{\omega_{HF}}\right)} \quad K_{FB} = \frac{R_{FB1}}{R_{FB1} + R_{FB2}} \tag{48}$$

$$\omega_{ZEA} = \frac{1}{C_{COMP} \times R_{COMP}} \quad \omega_O = \frac{1}{(C_{HF} + C_{COMP}) \times R_{FB2}}$$

$$\omega_{HF} = \frac{(C_{HF} + C_{COMP})}{C_{HF} \times C_{COMP} \times R_{COMP}} \tag{49}$$

Where A_{OL} = 10,000 (80 dB) and $\omega_{BW} = 2\pi \times f_{BW}$. $G_{EA(S)}$ is the ideal error amplifier gain, which is modified at DC and high frequency by the open loop gain of the amplifier and the feedback divider ratio.

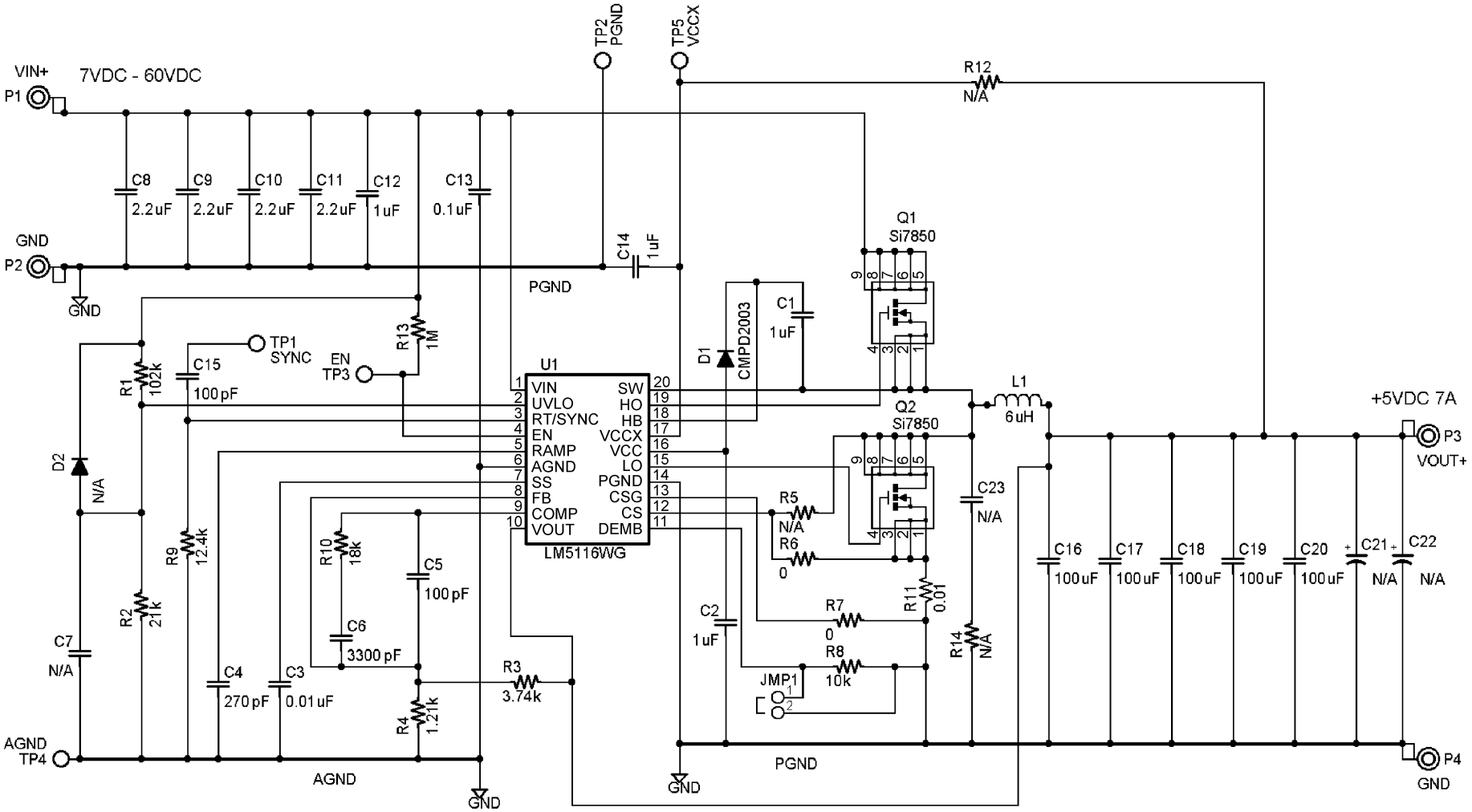


Figure 41. 5V 7A Typical Application Schematic

Table 1. Bill of Materials for 7V-60V Input, 5V 7A Output, 250kHz

ID	Part Number	Type	Size	Parameters	Qty	Vendor
C1, C2, C14	C2012X7R1E105K	Capacitor, Ceramic	0805	1µF, 25V, X7R	3	TDK
C3	VJ0603Y103KXAAT	Capacitor, Ceramic	0603	0.01µF, 50V, X7R	1	Vishay
C4	VJ0603A271JXAAT	Capacitor, Ceramic	0603	270pF, 50V, COG, 5%	1	Vishay
C5, C15	VJ0603Y101KXAT W1BC	Capacitor, Ceramic	0603	100pF, 50V, X7R	2	Vishay
C6	VJ0603Y332KXXAT	Capacitor, Ceramic	0603	3300pF, 25V, X7R	1	Vishay
C7		Capacitor, Ceramic	0603	Not Used	0	
C8, C9, C10, C11	C4532X7R2A225M	Capacitor, Ceramic	1812	2.2µF, 100V X7R	4	TDK
C12	C3225X7R2A105M	Capacitor, Ceramic	1210	1µF, 100V X7R	1	TDK
C13	C2012X7R2A104M	Capacitor, Ceramic	0805	0.1µF, 100V X7R	1	TDK
C16, C17, C18, C19, C20	C4532X6S0J107M	Capacitor, Ceramic	1812	100µF, 6.3V, X6S, 105°C	5	TDK
C21, C22		Capacitor, Tantalum	D Case	Not Used	0	
C23		Capacitor, Ceramic	0805	Not Used	0	
D1	CMPD2003	Diode, Switching	SOT-23	200mA, 200V	1	Central Semi
D2	CMPD2003	Diode, Switching	SOT-23	Not Used	0	Central Semi
JMP1		Connector, Jumper		2 pin sq. post	1	
L1	HC2LP-6R0	Inductor		6µH, 16.5A	1	Cooper
P1-P4	1514-2	Turret Terminal	.090” dia.		4	Keystone
TP1-TP5	5012	Test Point	.040” dia.		5	Keystone
Q1, Q2	Si7850DP	N-CH MOSFET	SO-8 Power PAK	10.3A, 60V	2	Vishay Siliconix
R1	CRCW06031023F	Resistor	0603	102kΩ, 1%	1	Vishay
R2	CRCW06032102F	Resistor	0603	21.0kΩ, 1%	1	Vishay
R3	CRCW06033741F	Resistor	0603	3.74kΩ, 1%	1	Vishay
R4	CRCW06031211F	Resistor	0603	1.21kΩ, 1%	1	Vishay
R5		Resistor	0603	Not Used	0	
R6, R7	CRCW06030R0J	Resistor	0603	0Ω	2	Vishay
R8	CRCW0603103J	Resistor	0603	10kΩ, 5%	1	Vishay
R9	CRCW06031242F	Resistor	0603	12.4kΩ, 1%	1	Vishay
R10	CRCW0603183J	Resistor	0603	18kΩ, 5%	1	Vishay
R11	LRC-LRF2010-01-R010-F	Resistor	2010	0.010Ω, 1%	1	IRC
R12		Resistor	0603	Not Used	0	
R13	CRCW0603105J	Resistor	0603	1MΩ, 5%	1	Vishay
R14		Resistor	1206	Not Used	0	
U1	LM5116WG	Synchronous Buck Controller	CPGA-20		1	TI

Changes from Revision B (February 2013) to Revision C **Page**

- Changed layout of National Data Sheet to TI format 30

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM5116WG/NOPB	ACTIVE	CFP	NAR	20	30	Green (RoHS & no Sb/Br)	Call TI	Level-1-NA-UNLIM	-40 to 125	LM5116WG	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

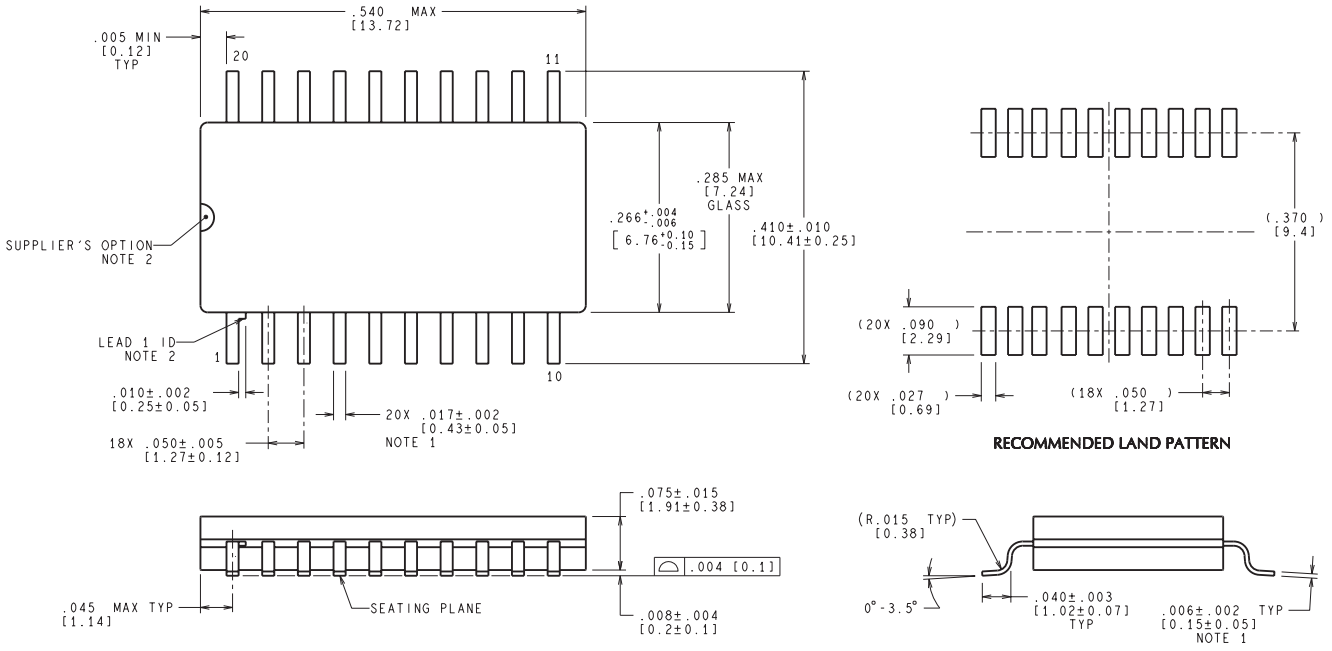
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

NAR0020A



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