



DS160PR410 Quad Channel PCI Express 4.0 Linear Redriver

1 Features

- Quad-channel linear equalizer supporting PCIe 1.0/2.0/3.0/4.0 up to 16 Gbps interfaces
- CTLE boosts up to 18 dB at 8 GHz helps to extend channel reach
- Automatic receiver detection for PCIe use cases
- Protocol agnostic linear redriver allows seamless support for PCIe link training
- Supports data rates up to 25 Gbps including Ultra Path Interconnect (UPI)
- Ultra-low latency of 70 ps (typical)
- Low additive random jitter of 60 fs (typical) with PRBS data
- Single 3.3 V supply
- Low active power of 124 mW/channel (typical) - no heat sink required
- Pin-strap, SMBus or EEPROM programming
- Support for x2, x4, x8, x16 PCIe bus width with one or multiple DS160PR410
- Industrial temperature range of -40°C to 85°C
- 4.0 mm × 6.0 mm, 40 pin WQFN package

2 Applications

- [Rack server](#)
- [Microserver & tower server](#)
- [High performance computing](#)
- [Network attached storage](#)
- [Storage area network \(SAN\) & host bus adapter \(HBA\) card](#)
- [Hardware accelerator](#)
- [Network interface card \(NIC\)](#)
- [Desktop PC/motherboard](#)

3 Description

The DS160PR410 is a four channel low-power high-performance linear repeater/redriver designed to support PCI Express (PCIe) Generation 1.0, 2.0, 3.0 and 4.0. The device is a protocol agnostic linear redriver that can operate for interfaces up to 25 Gbps including Ultra Path Interface (UPI) 2.0.

The DS160PR410 receivers deploy continuous time linear equalizers (CTLE) to provide a programmable high-frequency boost. The equalizer can open an input eye that is completely closed due to inter-symbol interference (ISI) induced by an interconnect medium, such as PCB traces. The CTLE receiver is followed by a linear output driver. The linear datapaths of DS160PR410 preserve transmit preset signal characteristics. The linear redriver becomes part of the passive channel that as a whole get link trained for best transmit and receive equalization settings. This transparency in the link training protocol result in best electrical link and lowest possible latency. The programmable equalization of the device along with its linear datapaths maximizes the flexibility of physical placement within the interconnect channel and improves overall channel performance.

The programmable settings can be applied easily through software (SMBus or I²C), direct loading from an external EEPROM, or by using pin control. In EEPROM mode, the configurations are automatically loaded on power up, eliminating the need for an external microprocessor or software driver.

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
DS160PR410	WQFN (40)	4.00 mm × 6.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application

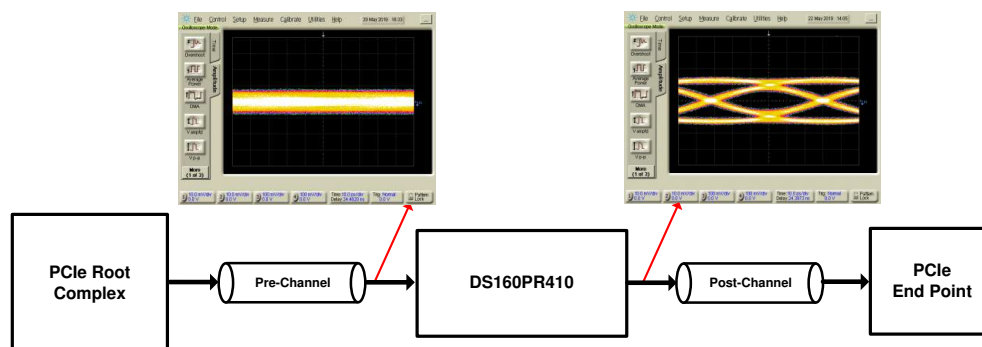


Table of Contents

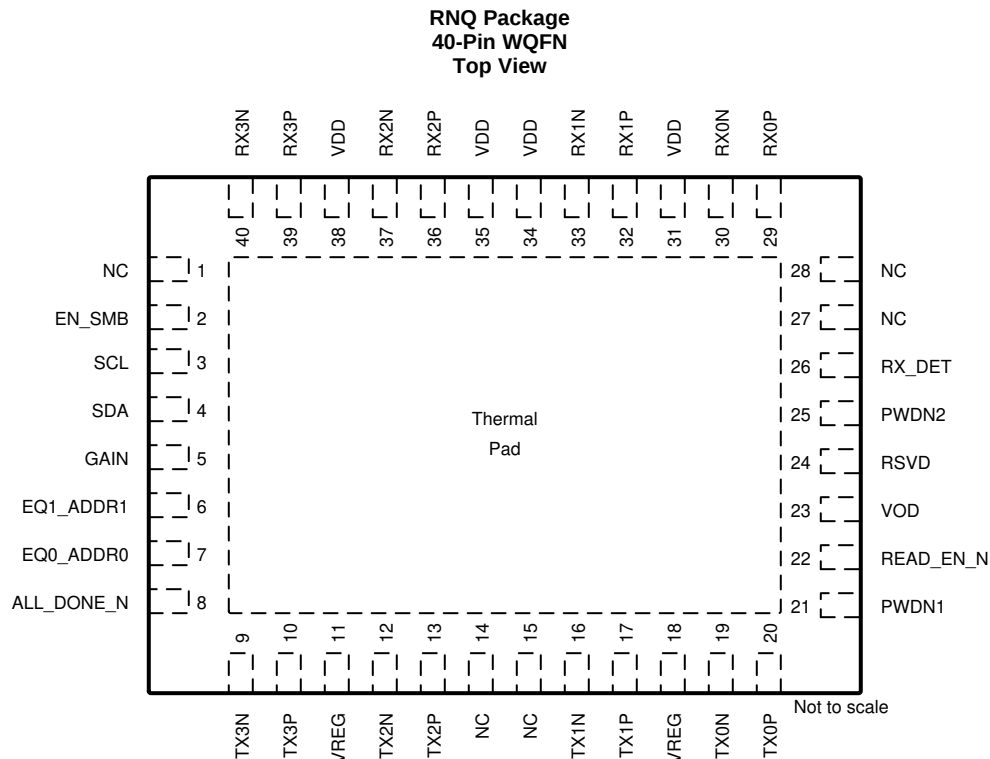
1 Features	1	7.4 Device Functional Modes.....	14
2 Applications	1	7.5 Programming.....	14
3 Description	1	8 Application and Implementation	17
4 Revision History	2	8.1 Application Information.....	17
5 Pin Configuration and Functions	3	8.2 Typical Applications	17
6 Specifications	5	9 Power Supply Recommendations	24
6.1 Absolute Maximum Ratings	5	10 Layout	24
6.2 ESD Ratings.....	5	10.1 Layout Guidelines	24
6.3 Recommended Operating Conditions.....	5	10.2 Layout Example	25
6.4 Thermal Information	6	11 Device and Documentation Support	26
6.5 DC Electrical Characteristics	6	11.1 Documentation Support	26
6.6 High Speed Electrical Characteristics.....	7	11.2 Receiving Notification of Documentation Updates	26
6.7 SMBUS/I ² C Timing Characteristics	9	11.3 Support Resources	26
6.8 Typical Characteristics.....	10	11.4 Trademarks	26
7 Detailed Description	12	11.5 Electrostatic Discharge Caution.....	26
7.1 Overview	12	11.6 Glossary	26
7.2 Functional Block Diagram	12	12 Mechanical, Packaging, and Orderable Information	26
7.3 Feature Description.....	12		

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (August 2019) to Revision A	Page
• Advance Information to Production Data Release	1

5 Pin Configuration and Functions



Pin Functions

PIN		I/O, TYPE	DESCRIPTION
NAME	NO.		
ALL_DONE_N	8	O, 3.3 V open drain	In SMBus/I²C Master Mode (EN_SMB = L1): Indicates the completion of a valid EEPROM register load operation. External pullup resistor such as 4.7 kΩ required for operation. High: External EEPROM load failed or incomplete Low: External EEPROM load successful and complete In SMBus/I²C slave/Pin Mode (EN_SMB = L3/L0): Leave the pin floating.
EN_SMB	2	I, 4-level	Four-level control input used to select SMBus/I ² C or Pin control. L0: Pin mode L1: I²C or SMBus Master Mode L2: RESERVED L3: I²C or SMBus Slave Mode
EQ0_ADDR0	7	I, 4-level	The 4-Level Control Input pins of DS160PR410 is defined according to Table 4 . In I²C or SMBus Mode (EN_SMB = L1 or L3), the pins are used to set the I ² C or SMBus address of the device. The pin state is read on power up and decoded according to Table 5 . In Pin mode (EN_SMB = L0), the pins are decoded at power up to control the CTLE boost setting according to Table 1 .
EQ1_ADDR1	6	I, 4-level	
GAIN	5	I, 4-level	Sets DC gain of CTLE at power up. L0: Reserved L1: Reserved L2: 0 dB (recommended) L3: 3.5 dB
GND	EP	P	EP is the Exposed Pad at the bottom of the WQFN package. It is used as the GND return for the device. The EP should be connected to ground plane(s) through low resistance path. A via array provides a low impedance path to GND, and also improves thermal dissipation.

Pin Functions (continued)

PIN		I/O, TYPE	DESCRIPTION
NAME	NO.		
NC	1, 14, 15, 27, 28	—	No connect
PWDN1	21	I, 3.3 V LVC MOS	Two-level logic controlling the operating state of the redriver. High: Power down for channels 0 and 1 Low: Power up, normal operation for channels 0 and 1.
PWDN2	25	I, 3.3 V LVC MOS	Two-level logic controlling the operating state of the redriver. High: Power down for channels 2 and 3 Low: Power up, normal operation for channels 2 and 3.
READ_EN_N	22	I, 3.3 V LVC MOS	SMBus / I²C Master Mode (EN_SMB = L1): When asserted low, initiates the SMBus / I ² C master mode EEPROM read function. When the EEPROM read is complete (indicated by assertion of ALL_DONE_N low), this pin can be held low for normal device operation. SMBus / I²C Slave Mode (EN_SMB = L3): When asserted low, this causes the device to be held in reset (I ² C state machine reset and register reset). This pin should be pulled high to 3.3 V with a external 4.7-kΩ pullup for normal operation in SMBus / I²C Slave Mode or in Pin Mode .
RSVD	24	—	Reserved use for TI. The pin must be left floating (NC).
RX_DET	26	I, 4-level	The RX_DET pin controls the receiver detect function. Depending on the input level, a 50 Ω or >50 kΩ termination to the power rail is enabled. See Table 3 for details.
RX0N	30	I	Inverting differential inputs to the equalizer. An on-chip, 100 Ω termination resistor connects RXP to RXN. Channel 0.
RX0P	29	I	Non-inverting differential inputs to the equalizer. An on-chip, 100 Ω termination resistor connects RXP to RXN. Channel 0.
RX1N	33	I	Inverting differential inputs to the equalizer. An on-chip, 100 Ω termination resistor connects RXP to RXN. Channel 1.
RX1P	32	I	Non-inverting differential inputs to the equalizer. An on-chip, 100 Ω termination resistor connects RXP to RXN. Channel 1.
RX2N	37	I	Inverting differential inputs to the equalizer. An on-chip, 100 Ω termination resistor connects RXP to RXN. Channel 2.
RX2P	36	I	Non-inverting differential inputs to the equalizer. An on-chip, 100 Ω termination resistor connects RXP to RXN. Channel 2.
RX3N	40	I	Inverting differential inputs to the equalizer. An on-chip, 100 Ω termination resistor connects RXP to RXN. Channel 3.
RX3P	39	I	Non-inverting differential inputs to the equalizer. An on-chip, 100 Ω termination resistor connects RXP to RXN. Channel 3.
SCL	3	I/O, 3.3 V LVC MOS, open drain	SMBus / I ² C clock input / open-drain output. External 1 kΩ to 5 kΩ pullup resistor is required as per SMBus / I ² C interface standard. This pin is 3.3 V tolerant.
SDA	4	I/O, 3.3 V LVC MOS, open drain	SMBus / I ² C data input / open-drain clock output. External 1 kΩ to 5 kΩ pullup resistor is required as per SMBus interface standard. This pin is 3.3 V tolerant.
TX0N	19	O	Inverting 50 Ω driver outputs. Compatible with AC-coupled differential inputs. Also used for RX detection at power up. Channel 0.
TX0P	20	O	Non-inverting 50 Ω driver outputs. Compatible with AC-coupled differential inputs. Also used for RX detection at power up. Channel 0.
TX1N	16	O	Inverting 50 Ω driver outputs. Compatible with AC-coupled differential inputs. Also used for RX detection at power up. Channel 1.
TX1P	17	O	Non-inverting 50 Ω driver outputs. Compatible with AC-coupled differential inputs. Also used for RX detection at power up. Channel 1.
TX2N	12	O	Inverting 50 Ω driver outputs. Compatible with AC-coupled differential inputs. Also used for RX detection at power up. Channel 2.
TX2P	13	O	Non-inverting 50 Ω driver outputs. Compatible with AC-coupled differential inputs. Also used for RX detection at power up. Channel 2.
TX3N	9	O	Inverting 50 Ω driver outputs. Compatible with AC-coupled differential inputs. Also used for RX detection at power up. Channel 3.
TX3P	10	O	Non-inverting 50 Ω driver outputs. Compatible with AC-coupled differential inputs. Also used for RX detection at power up. Channel 3.

Pin Functions (continued)

PIN		I/O, TYPE	DESCRIPTION
NAME	NO.		
VDD	31, 34, 35, 38	P	Power supply pins. VDD = 3.3 V $\pm$ 10%. The VDD pins on this device should be connected through a low-resistance path to the board VDD plane. Typical supply decoupling consists of a 0.1 μ F capacitor per VDD pin and one 1.0 μ F bulk capacitor per device.
VOD	23	I, 4-level	Sets TX VOD setting at power up. L0: –6 dB L1: –3.5 dB L2: 0 dB (recommended) L3: –1.5 dB
VREG	11, 18	P	Internal voltage regulator output. Must add decoupling caps of 0.1 μ F near each pin. The regulator is only for internal use. Do not use to power any external components. Do not route the signal beyond the decoupling capacitors on board.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
VDD _{ABSMAX}	Supply Voltage (VDD)	–0.5	4.0	V
VIO _{CMOS,ABSMAX}	3.3 V LVCMOS and Open Drain I/O voltage	–0.5	4.0	V
VIO _{4LVL,ABSMAX}	4-level Input I/O voltage	–0.5	2.75	V
VIO _{HS-RX,ABSMAX}	High-speed I/O voltage (RXnP, RXnN)	–0.5	3.2	V
VIO _{HS-TX,ABSMAX}	High-speed I/O voltage (TXnP, TXnN)	–0.5	2.75	V
T _{J,ABSMAX}	Junction temperature		150	°C
T _{stg}	Storage temperature range	–65	150	°C

- (1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	$\pm$ 2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	$\pm$ 500	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Pins listed as $\pm$ 2 kV may actually have higher performance.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
VDD	Supply voltage, VDD to GND	DC plus AC power should not exceed these limits	3.0	3.3	3.6	V
N _{VDD}	Supply noise tolerance	Supply noise, DC to <50 Hz, sinusoidal ¹			250	mVpp
		Supply noise, 50 Hz to 10 MHz, sinusoidal ¹			20	mVpp
		Supply noise, >10 MHz, sinusoidal ¹			10	mVpp
T _{RampVDD}	VDD supply ramp time	From 0 V to 3.0 V	0.150		100	ms
T _J	Operating junction temperature		–40		125	°C
T _A	Operating ambient temperature		–40		85	°C

Recommended Operating Conditions (continued)

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
PW _{LVC MOS}	Minimum pulse width required for the device to detect a valid signal on LVC MOS inputs	PWDN1/2, READ_EN_N	200			μs
VDD _{SMBUS}	SMBus SDA and SCL Open Drain Termination Voltage	Supply voltage for open drain pull-up resistor			3.6	V
F _{SMBus}	SMBus clock (SCL) frequency in SMBus slave mode		10		400	kHz
VID _{LAUNCH}	Source differential launch amplitude		800		1200	mVpp
DR	Data rate	DS160PR410	1		25	Gbps

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾			DS160PR410 RNQ, 40 Pins	UNIT
R _{θJA} -High K	Junction-to-ambient thermal resistance		31.1	°C/W
R _{θJC} (top)	Junction-to-case (top) thermal resistance		21.4	°C/W
R _{θJB}	Junction-to-board thermal resistance		12.1	°C/W
ψ _{JT}	Junction-to-top characterization parameter		0.3	°C/W
ψ _{JB}	Junction-to-board characterization parameter		12.1	°C/W
R _{θJC} (bot)	Junction-to-case (bottom) thermal resistance		4.1	°C/W

(1) For more information about traditional and new thermal metrics, see the [IC Package Thermal Metrics](#) application report.

6.5 DC Electrical Characteristics

over operating free-air temperature and voltage range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power						
I _{ACTIVE}	Device current consumption when all four channels are active	All four channels enabled with VOD = L2, PWDN1,2 = L		150	200	mA
I _{ACTIVE-HALF}	Device current consumption when two channels are active	Two channels enabled with VOD = L2, PWDN1 or PWDN2 = L		85	112	mA
I _{STBY}	Device current consumption in standby power mode	All four channels disabled, PWDN1,2 = H		22	33	mA
V _{REG}	Internal regulator output			2.5		V
Control IO						
V _{IH}	High level input voltage	SDA, SCL, PWDN1, PWDN2, READ_EN_N pins	2.1			V
V _{IL}	Low level input voltage	SDA, SCL, PWDN1, PWDN2, READ_EN_N pins			1.08	V
V _{OH}	High level output voltage	R _{pull-up} = 100 kΩ (SDA, SCL, ALL_DONE_N pins)	2			V
V _{OL}	Low level output voltage	I _{OL} = -4 mA (SDA, SCL, ALL_DONE_N pins)			0.4	V
I _{IH}	Input high leakage current	V _{Input} = VDD, (SCL, SDA, PWDN1, PWDN2, READ_EN_N pins)			10	μA
I _{IL}	Input low leakage current	V _{Input} = 0 V, (SCL, SDA, PWDN1, PWDN2, READ_EN_N pins)	-10			μA
C _{IN-CTRL}	Input capacitance			1.5		pF
4 Level IOs (EQ0_ADDR0, EQ1_ADDR1, EN_SMB, RX_DET, VOD, GAIN pins)						
I _{IH_4L}	Input high leakage current, 4 level IOs	VIN = 2.5V			10	μA
I _{IL_4L}	Input low leakage current, , 4 level IOs	VIN = GND	-150			μA

DC Electrical Characteristics (continued)

over operating free-air temperature and voltage range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Receiver						
Z_{RX-DC}	Rx DC Single-Ended Impedance			50		Ω
$Z_{RX-DIFF-DC}$	Rx DC Differential Impedance			100		Ω
Transmitter						
$Z_{TX-DIFF-DC}$	DC Differential Tx Impedance	Impedance of Tx during active signaling, VID,diff = 1Vpp			120	Ω
$V_{TX-DC-CM}$	Tx DC common mode Voltage			0.75		V
$I_{TX-SHORT}$	Tx Short Circuit Current	Total current the Tx can supply when shorted to GND			90	mA

6.6 High Speed Electrical Characteristics

over operating free-air temperature and voltage range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Receiver						
$RL_{RX-DIFF}$	Input differential return loss with minimal channel in TI evaluation board	50 MHz to 1.25 GHz		-22		dB
		1.25 GHz to 2.5 GHz		-19		dB
		2.5 GHz to 4.0 GHz		-17		dB
		4.0 GHz to 8.0 GHz		-14		dB
$RL_{RX-DIFF}$	Input differential return loss with minimal channel in TI evaluation board	8.0 GHz to 12.5 GHz		-13		dB
RL_{RX-CM}	Input common-mode return loss with minimal channel in TI evaluation board	50 MHz to 2.5 GHz		-18		dB
		2.5 GHz to 8.0 GHz		-13		dB
RL_{RX-CM}	Input common-mode return loss with minimal channel in TI evaluation board	8.0 GHz to 12.5 GHz		-10		dB
XT_{RX}	Receive-side pair-to-pair isolation	Minimum pair-to-pair isolation (SDD21) between two adjacent receiver pairs from 10 MHz to 8 GHz.		-45		dB
GAIN	CTLE block DC gain	Ratio at GAIN = L3 and GAIN = L2, with low freq CK		3.0		dB
Transmitter						
VOD_{L0-L2}	Ratio of VOD gain L0 to L2	GAIN = L2, with low freq CK		-6		dB
VOD_{L1-L2}	Ratio of VOD gain L1 to L2	GAIN = L2, with low freq CK		-3.5		dB
VOD_{L3-L2}	Ration of VOD gain L3 to L2	GAIN = L2, with low freq CK		-1.5		dB
$V_{TX-AC-CM-PP}$	Tx AC Peak-to-Peak Common Mode Voltage	Measured with lowest EQ, VOD = L2; PRBS-7, 16 Gbps, over at least 10^6 bits using a bandpass-Pass Filter from 30 KHz - 500 Mhz			50	mVpp
$V_{TX-CM-DC-ACTIVE-IDLE-DELTA}$	Absolute Delta of DC Common Mode Voltage during L0 and Electrical Idle	$V_{TX-CM-DC} = V_{OUTn+} + V_{OUTn-} /2$, Measured by taking the absolute difference of $V_{TX-CM-DC}$ during PCIe state L0 and Electrical Idle	0		100	mV
$V_{TX-IDLE-DIFF-AC-p}$	AC Electrical Idle Differential Output Voltage	Measured by taking the absolute difference of V_{OUTn+} and V_{OUTn-} during Electrical Idle, Measured with a band-pass filter consisting of two first-order filters. The High-Pass and Low-Pass -3 dB bandwidths are 10 kHz and 1.25 GHz, respectively - zero at input	0		10	mV
$V_{TX-RCV-DETECT}$	Amount of Voltage change allowed during Receiver Detection	Measured while Tx is sensing whether a low-impedance Receiver is present. No load is connected to the driver output	0		600	mV

High Speed Electrical Characteristics (continued)

over operating free-air temperature and voltage range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
RL _{TX-DIFF}	Output differential return loss with minimal channel in TI evaluation board	50 MHz to 1.25 GHz		-22		dB
		1.25 GHz to 2.5 GHz		-20		dB
		2.5 GHz to 4.0 GHz		-18		dB
		4.0 GHz to 8.0 GHz		-15		dB
RL _{TX-CM}	Output Common-mode return loss with minimal channel in TI evaluation board	50 MHz to 2.5 GHz		-13		dB
		2.5 GHz to 8.0 GHz		-11		dB
XT _{TX}	Transmit-side pair-to-pair isolation	Minimum pair-to-pair isolation (SDD21) between two adjacent transmitter pairs from 10 MHz to 8 GHz.		-45		dB
Device Datapath						
T _{PLHD/PHLD}	Input-to-output latency (propagation delay) through a channel	Measured by observing propagation delay during either Low-to-High or High-to-Low transition		70	90	ps
L _{TX-SKEW}	Lane-to-Lane Output Skew	Measured between any two lanes within a single transmitter			20	ps
T _{RJ-DATA}	Additive Random Jitter with data (RMS)	Difference between through redriver and baseline setup. 16 Gbps PRBS15. Minimal input/output channels. Minimum EQ. 800 mV input.		60	110	fs
T _{RJ-INTRINSIC}	Intrinsic additive Random Jitter with clock (RMS)	Difference between through redriver and baseline setup. 8Ghz clock. Minimal input/output channels. Minimum EQ. 400mV input.		150	190	fs
T _{DJ-DATA}	Added Deterministic Jitter with data	Difference between through redriver and baseline setup. 16 Gbps PRBS15. Minimal input/output channels. Minimum EQ..		3	5	ps
JITTER _{INTRIN SIC-DJ}	Intrinsic additive Deterministic Jitter with clock	Difference between through redriver and baseline setup. 8 Ghz CK. Minimal input/output channels. Minimum EQ.		0.4	1.2	ps
JITTER _{INTRIN SIC-TOTAL}	Redriver intrinsic additive Total Jitter	Difference between measurement through redriver and baseline setup with 8 Ghz clock signals, lowest EQ		2.5	3.0	ps
EQGAIN _{8G}	High-frequency EQ boost @ 8 GHz	Measured with maximum CTLE setting and maximum BW setting (EQ1 = L3, EQ0 = L3). Boost is defined as the gain at 8 GHz relative to 100 MHz.		18		dB
DCGAIN _{VAR, max}	Maximum DC gain variation	VOD=L2, GAIN=L2, min EQ setting	-2.1		1.1	dB
EQGAIN _{VAR, max}	Maximum EQ boost variation	VOD=L2, GAIN=L2, max EQ setting, at 8 Ghz	-2.9		3.5	dB
LINEARITY _{D C}	The maximum DC input amplitude for which the repeater remains linear, defined as ≤1 dB compression of Vout/Vin.	VOD = L2. Minimal input channel and minimum EQ using 128T pattern at 2.5 Gbps.		800		mVpp
LINEARITY _{A C}	The maximum DC input amplitude for which the repeater remains linear, defined as ≤1 dB compression of Vout/Vin.	VOD = L2. Minimal input channel and minimum EQ using 1T pattern at 16 Gbps.		750		mVpp

6.7 SMBUS/I²C Timing Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Slave Mode						
T _{SDA-HD}	Data hold time		0			ns
T _{SDA-SU}	Data setup time		100			ns
T _{SDA-R}	SDA rise time, read operation	Pull-up resistor = 1 kΩ, C _b = 50 pF		120		ns
T _{SDA-F}	SDA fall time, read operation	Pull-up resistor = 1 kΩ, C _b = 50 pF		10		ns
Master Mode						
f _{SCL-M}	SCL clock frequency	EN_SMB = L3 (Master Mode)	220	300	365	kHz
T _{SCL-LOW-M}	SCL low period		1.58	2.0	2.62	μs
T _{SCL-HIGH-M}	SCL high period		1.15	1.40	1.8	μs
T _{HD-START-M}	Hold time start operation			1.5		μs
T _{SU-START-M}	Setup time start operation			1.5		μs
T _{SDA-HD-M}	Data hold time			0.9		μs
T _{SDA-SU-M}	Data setup time			1.3		μs
T _{SU-STOP-M}	Stop condition setup time			1.5		μs
T _{BUF-M}	Bus free time between Stop-Start			2.6		μs
T _{SDC-R-M}	SCL rise time	Pull-up resistor = 1 kΩ		120		ns
T _{SDC-F-M}	SCL fall time	Pull-up resistor = 1 kΩ		10		ns
EEPROM Timing						
T _{EEPROM}	EEPROM configuration load time	Time to assert ALL_DONE_N after READ_EN_N has been asserted. Single device reading its configuration from an EEPROM with common channel configuration . This time scales with the number of devices reading from the same EEPROM. Does not include power-on reset time.		1		ms
T _{POR}	Time to first SMBus access	Power supply stable after initial ramp. Includes initial power-on reset time.		26		ms

6.8 Typical Characteristics

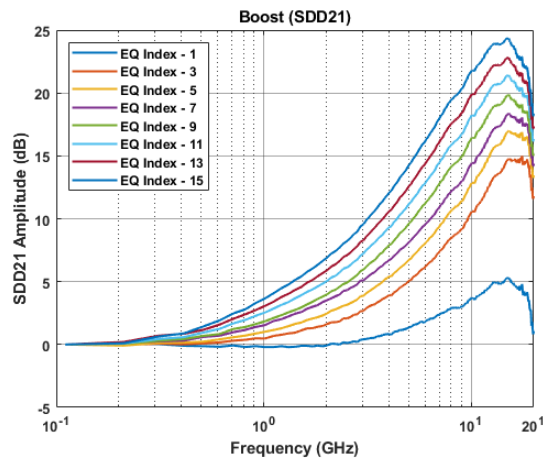


Figure 1. Typical EQ Boost vs Frequency for 8 (Out of Available 16) EQ Indices

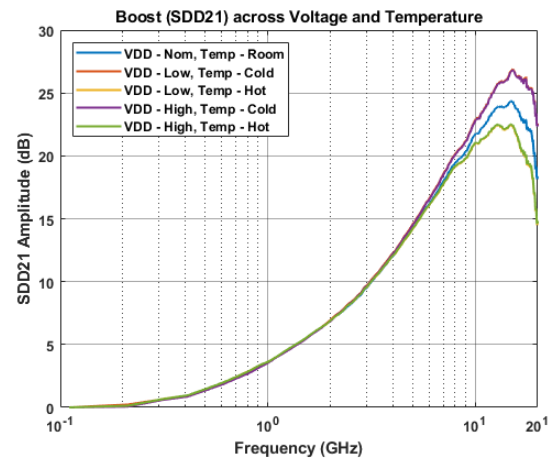


Figure 2. EQ Boost vs Frequency with EQ Index 15 (Maximum Setting) for Different Supply Voltage and Temperature Settings

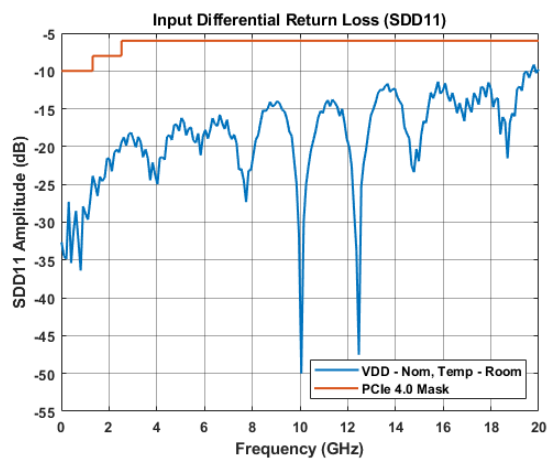


Figure 3. Typical Input (RX) Differential Return Loss vs Frequency in TI Evaluation Board with -2 dB input and -2 dB output loss

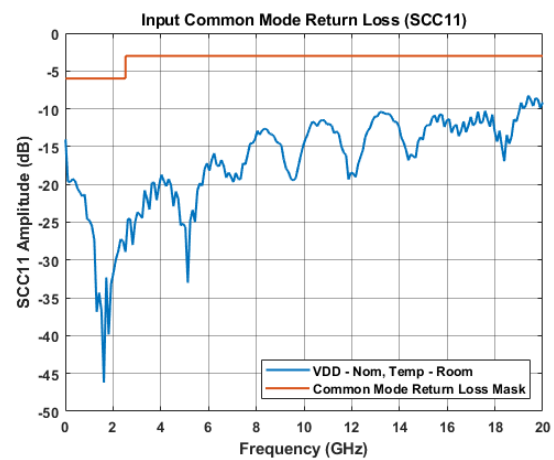


Figure 4. Typical Input (RX) Common Mode Return Loss vs Frequency in TI Evaluation Board with -2 dB Input and -2 dB Output Loss

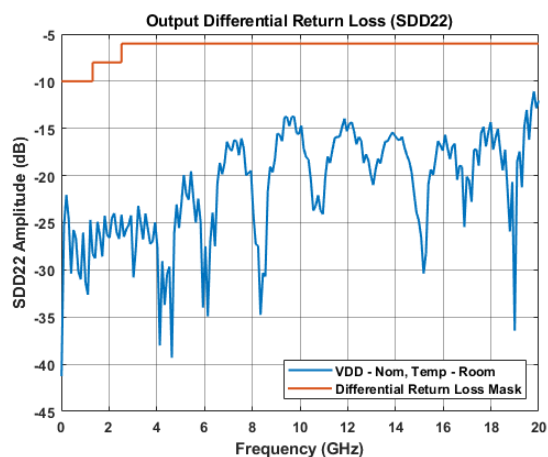


Figure 5. Typical Output (TX) Differential Return Loss vs Frequency in TI Evaluation Board with -2 dB Input and -2 dB Output Loss

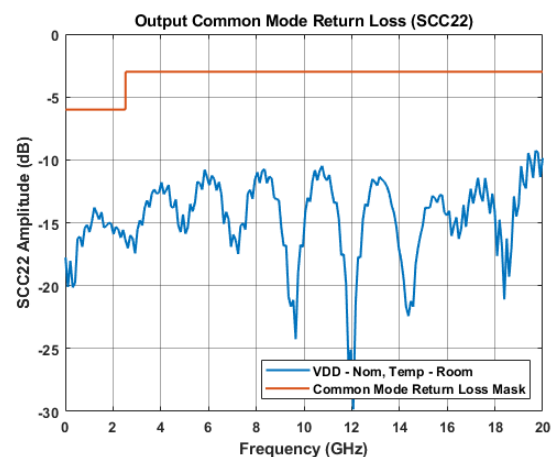


Figure 6. Typical Output (TX) Common Mode Return Loss vs Frequency in TI Evaluation Board with -2 dB Input and -2 dB Output Loss

Typical Characteristics (continued)

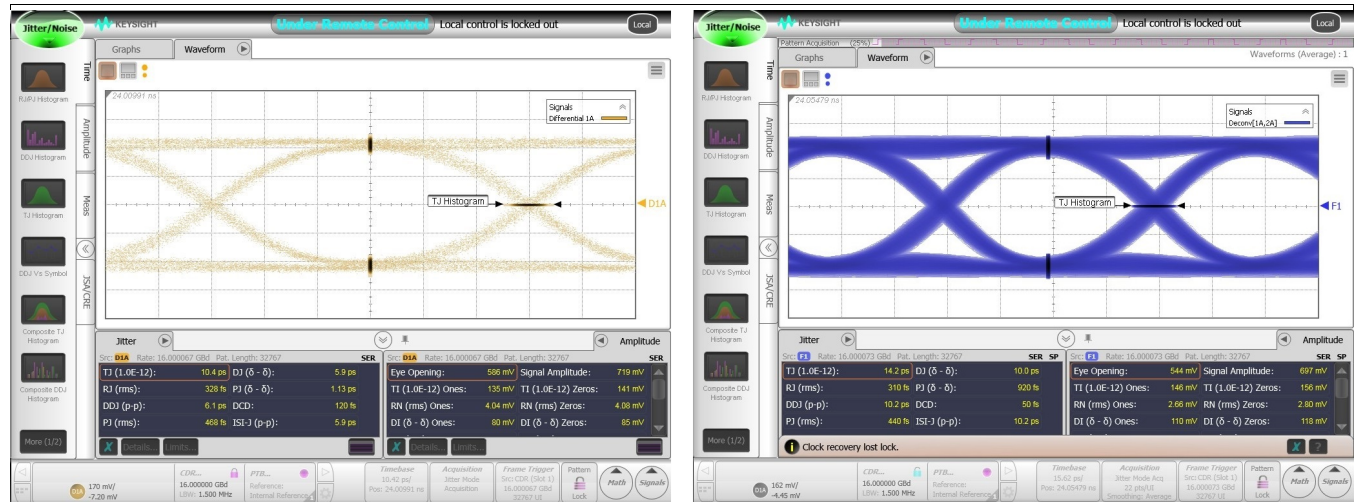


Figure 7. DS160PR410 Typical Jitter Characteristics in TI Evaluation Board. Left - Input to the Device, Right - Output of the Device with Jitter Decomposition Shown.

7 Detailed Description

7.1 Overview

The DS160PR410 is a four-channel multi-rate linear repeater with integrated signal conditioning. The four channels operate independently from one another. Each channel includes a continuous-time linear equalizer (CTLE) and a linear output driver, which together compensate for a lossy transmission channel between the source transmitter and the final receiver. The linearity of the data path is specifically designed to preserve any transmit equalization while keeping receiver equalization effective.

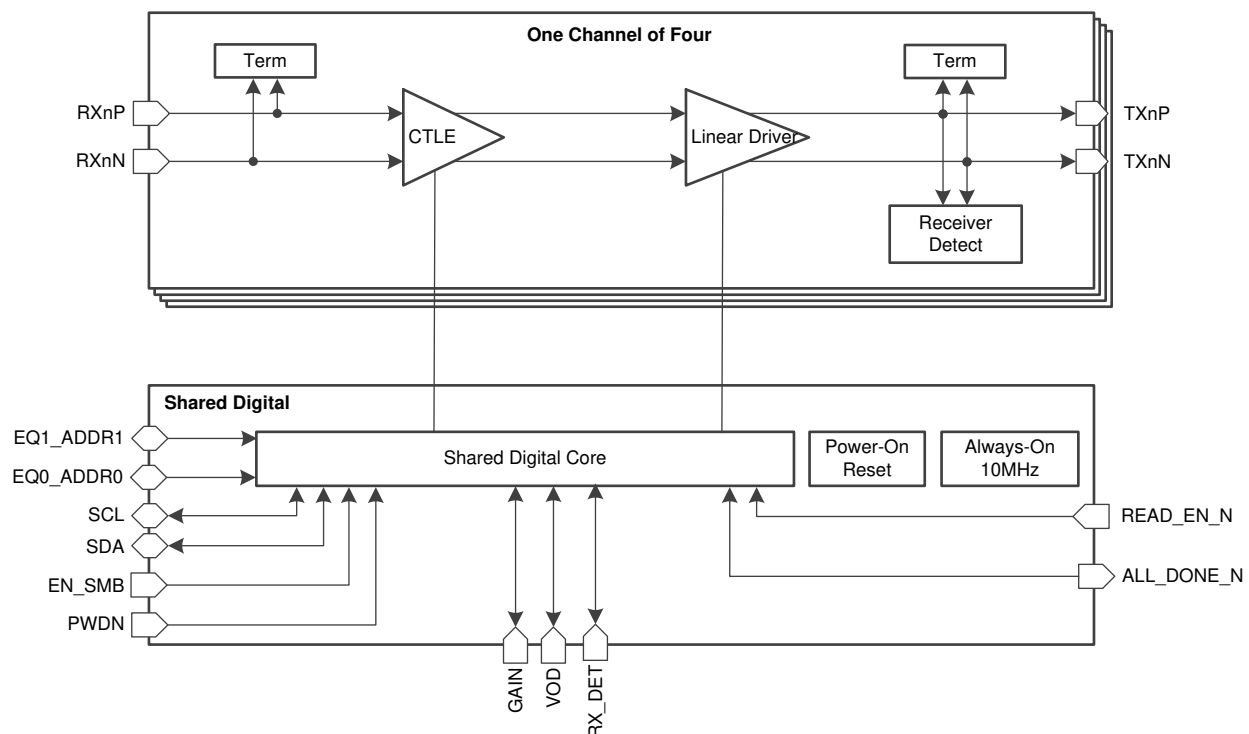
The DS160PR410 can be configured three different ways:

Pin Mode – device control configuration is done solely by strap pins. Pin mode is expected to be good enough for many system implementation needs.

SMBus/I²C Master Mode - device control configuration is read from external EEPROM. When the DS160PR410 has finished reading from the EEPROM successfully, it will drive the ALL_DONE_N pin LOW. SMBus/I²C slave operation is available in this mode before, during or after EEPROM reading. Note during EEPROM reading if the external SMBus/I²C master wants to access DS160PR410 registers it must support arbitration. The mode is preferred when software implementation is not desired.

SMBus/I²C Slave Mode - provides most flexibility. Requires a SMBus/I²C master device to configure DS160PR410 through writing to its slave address.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Linear Equalization

The DS160PR410 receivers feature a continuous-time linear equalizer (CTLE) that applies high-frequency boost and low-frequency attenuation to help equalize the frequency-dependent insertion loss effects of the passive channel. [Table 1](#) shows available equalization boost through EQ0_ADDR0 and EQ1_ADDR1 control pins, when in Pin Control mode (EN_SMB = L0).

Feature Description (continued)

Table 1. Equalization Control Settings

EQUALIZATION SETTING			TYPICAL EQ BOOST	
INDEX	EQ1_ADDR1	EQ0_ADDR0	@ 4 GHz	@ 8 GHz
0	L0	L0	–0.3	–0.8
1	L0	L1	0.4	1.3
2	L0	L2	3.3	5.7
3	L0	L3	3.8	7.1
4	L1	L0	4.9	8.4
5	L1	L1	5.2	9.1
6	L1	L2	5.4	9.8
7	L1	L3	6.5	10.7
8	L2	L0	6.7	11.3
9	L2	L1	7.7	12.6
10	L2	L2	8.7	13.6
11	L2	L3	9.1	14.4
12	L3	L0	9.4	15.0
13	L3	L1	10.3	15.9
14	L3	L2	10.6	16.5
15	L3	L3	11.8	17.8

The equalization of the device can also be set by writing to SMBus/I²C registers in slave or master mode. Refer to the [DS160PR410 Programming Guide](#) (SNLU255) for details.

7.3.2 DC Gain

The VOD or GAIN pins can be used to set the overall data-path DC (low frequency) gain of the DS160PR410 as outlined in the [Pin Configuration and Functions](#) section.

[Table 2](#) shows how DC gain of the overall data-paths can be set using GAIN and VOD pins, when in Pin Control mode (EN_SMB = L0).

Table 2. DC Gain Settings

Desired DC Gain (dB)	GAIN	VOD
+3.5	L3	L2
0	L2	L2
–1.5	L2	L3
–3.5	L2	L1
–6	L2	L0

It is advised that the DC gain and equalization of the DS160PR410 are set such that the signal swing at DC and high frequency does not exceed the DC and AC linearity ranges of the devices, respectively. For most PCIe systems the default DC gain setting 0 dB (GAIN and VOD pins floating) would be sufficient. However a DC attenuation can be utilized to be able to apply extra equalization when needed and keeping the data-path linear.

7.3.3 Receiver Detect State Machine

The DS160PR410 deploys an RX detect state machine that governs the RX detection cycle as defined in the PCI express specifications. At power up, after a manually triggered event through PWDN1 and PWDN2 pins (in pin mode), or writing to the relevant I²C / SMBus register, the redriver determines whether or not a valid PCI express termination is present at the far end of the link. The RX_DET pin of DS160PR410 provides additional flexibility for system designers to appropriately set the device in desired mode according to [Table 3](#).

If all four channels of DS160PR410 are used for same PCI express link, the PRWDN1 and PWDN2 pin can be shorted and driven together.

Table 3. Receiver Detect State Machine Settings

PWDN1 and PWDN2	RXDET	COMMENTS
L	L0	PCI Express RX detection state machine is enabled. RX detection is asserted after 2x valid detections. Pre Detect: Hi-Z, Post Detect: 50 Ω .
L	L1	PCI Express RX detection state machine is enabled. RX detection is asserted after 3x valid detections. Pre Detect: Hi-Z, Post Detect: 50 Ω .
L	L2 (Float)	PCI Express RX detection state machine is enabled. RX detection is asserted after 1x valid detection. Pre Detect: Hi-Z, Post Detect: 50 Ω .
L	L3	PCI Express RX detection state machine is disabled. Recommended for non PCI Express interface use case where the DS160PR410 is used as buffer with equalization. Always 50 Ω .
H	X	Manual reset, input is high impedance.

7.4 Device Functional Modes

7.4.1 Active PCIe Mode

The device is in normal operation with PCIe state machine enabled by RX_DET = L0/L1/L2. In this mode PWDN1/PWDN2 pins are driven low in a system (for example by PCIe connector "PRSNT" signal). In this mode, the DS160PR410 redrivers and equalizes PCIe RX or TX signals to provide better signal integrity.

7.4.2 Active Buffer Mode

The device is in normal operation with PCIe state machine disabled by RX_DET = L3. This mode is recommended for non-PCIe use cases. In this mode the device is working as a buffer to provide linear equalization to improve signal integrity.

7.4.3 Standby Mode

The device is in standby mode invoked by PWDN1/PWDN2 = H. In this mode, the device is in standby mode conserving power.

7.5 Programming

7.5.1 Control and Configuration Interface

7.5.1.1 Pin Mode

The DS160PR410 can be fully configured through GPIO/Pin-strap pins. In this mode the device uses 2-level and 4-level pins for device control and signal integrity optimum settings. The [Pin Configuration and Functions](#) section defines the control pins.

7.5.1.1.1 Four-Level Control Inputs

The DS160PR410 has six (GAIN, VOD, EQ1_ADDR1, EQ0_ADDR0, EN_SMB, and RX_DET) 4-level inputs pins that are used to control the configuration of the device. These 4-level inputs use a resistor divider to help set the four valid levels and provide a wider range of control settings. External resistors must be of 10% tolerance or better.

Table 4. 4-Level Control Pin Settings

LEVEL	SETTING
L0	1 k Ω to GND

Programming (continued)

Table 4. 4-Level Control Pin Settings (continued)

LEVEL	SETTING
L1	13 kΩ to GND
L2	F (Float)
L3	59 kΩ to GND

7.5.1.2 SMBUS/I²C Register Control Interface

If EN_SMB = L3 (SMBus / I²C control mode), the DS160PR410 is configured through a standard I²C or SMBus interface that may operate up to 400 kHz. The slave address of the DS160PR410 is determined by the pin strap settings on the EQ1_ADDR1 and EQ0_ADDR0 pins. The device can be configured for best signal integrity and power settings in the system using the I²C or SMBus interface. The sixteen possible slave addresses (8-bit) for the DS160PR410 are shown in [Table 5](#).

Table 5. SMBUS/I²C Slave Address Settings

EQ1_ADDR1 PIN LEVEL	EQ0_ADDR0 PIN LEVEL	8-BIT WRITE ADDRESS (HEX)	7-BIT ADDRESS (HEX)
L0	L0	0x30	0x18
L0	L1	0x32	0x19
L0	L2	0x34	0x1A
L0	L3	0x36	0x1B
L1	L0	0x38	0x1C
L1	L1	0x3A	0x1D
L1	L2	0x3C	0x1E
L1	L3	0x3E	0x1F
L2	L0	0x40	0x20
L2	L1	0x42	0x21
L2	L2	0x44	0x22
L2	L3	0x46	0x23
L3	L0	0x48	0x24
L3	L1	0x4A	0x25
L3	L2	0x4C	0x26
L3	L3	0x4E	0x27

The DS160PR410 can also be configured by reading from EEPROM. To enter into this mode SMB_EN must be set to L1. Refer to the [Understanding EEPROM Programming for DS160PR410 PCI Express Gen-4 Redriver](#) application report (SNLA320) for details.

7.5.1.3 SMBus/I²C Master Mode Configuration (EEPROM Self Load)

To configure the DS160PR410 for SMBus master mode, set the EN_SMB pin to L1. If the DS160PR410 is configured for SMBus master mode, it will remain in the SMBus IDLE state until the READ_EN_N pin is asserted to LOW. After the READ_EN_N pin is driven LOW, the DS160PR410 becomes an SMBus master and attempts to self-configure by reading device settings stored in an external EEPROM (SMBus 8-bit address 0xA0). When the DS160PR410 has finished reading from the EEPROM successfully, it will drive the ALL_DONE_N pin LOW and then change from a SMBus master to a SMBus slave. Not all bits in the register map can be configured through an EEPROM load. Refer to the [Understanding EEPROM Programming for DS160PR410 PCI Express Gen-4 Redriver](#) application report (SNLA320) for more information.

When designing a system for using the external EEPROM, the user must follow these specific guidelines:

- EEPROM size of 2 kb (256 × 8-bit) is recommended.
- Set EN_SMB = L1, configure for SMBus master mode
- The external EEPROM device address byte must be 0xA0 and capable of 400-kHz operation at 3.3-V supply

DS160PR410

SNLS645A – AUGUST 2019 – REVISED DECEMBER 2019

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Figure 8 outlines how multiple devices can be configured through single external EEPROM device. Figure 8 shows a use case with four DS160PR410, but the user can cascade and number of DS160PR410 devices in a similar way, for brevity pullup resistors (for open-drain outputs) are not shown in the block diagram. Tie first device's READ_EN_N pin low to automatically initiate EEPROM read at power up. Alternately the READ_EN_N pin of the first device can also be controlled by a micro-controller to initiate the EEPROM read manually. Leave the final device's ALL_DONE_N pin floating, or connect the pin to a micro-controller input to monitor the completion of the final EEPROM read.

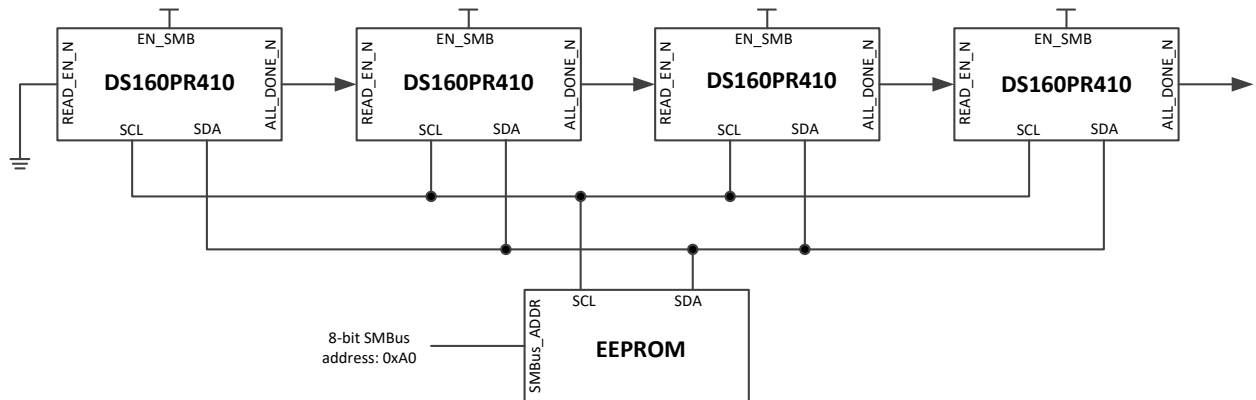


Figure 8. Example Daisy Chain for Multiple Device Single EEPROM Configuration

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The DS160PR410 is a high-speed linear repeater which extends the reach of differential channels impaired by loss from transmission media like PCBs and cables. It can be deployed in a variety of different systems. The following sections outline typical applications and their associated design considerations.

8.2 Typical Applications

The DS160PR410 is a PCI Express linear redriver that can also be configured as interface agnostic redriver by disabling its RX detect feature. The device can be used in wide range of interfaces including:

- PCI Express
- Ultra Path Interconnect (UPI)
- SATA
- SAS
- Display Port

Typical Applications (continued)

The DS160PR410 is a protocol agnostic 4-channel linear redriver with PCI Express receiver-detect capability. Its protocol agnostic nature allows it to be used in PCI Express x2, x4, x8, and x16 applications. [Figure 9](#) shows how a number of DS160PR410 devices can be used to obtain signal conditioning for PCI Express buses of varying widths. Note all four channels of the DS160PR410 flow in same direction. Therefore, if the device is used for x2 configuration, careful layout consideration is needed. In x2 configuration, the two-channel grouping can be used for PCIe receiver detect. PWDN1 pin puts channels 1 and 2, and PWDN2 pin puts channels 3 and 4 into standby.

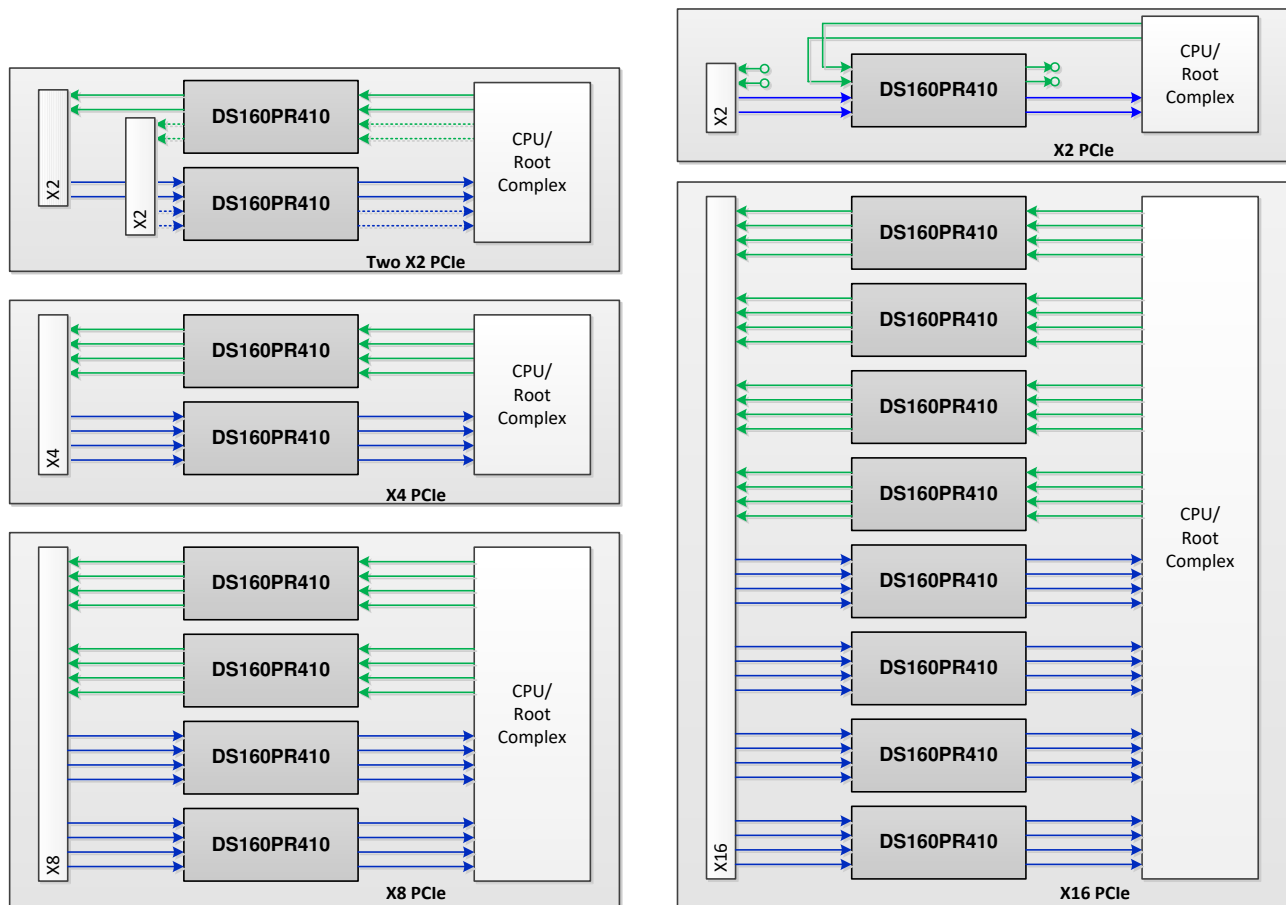


Figure 9. PCI Express x2, x4, x8, and x16 Use Cases Using DS160PR410

Typical Applications (continued)

8.2.1 PCIe x4 Lane Configuration

The DS160PR410 can be used in server or motherboard applications to boost transmit and receive signals to increase the reach of the host or root complex processor to PCI Express slots/connectors. The following design recommendations can be used in any lane configuration. Figure 10 shows a simplified schematic for x4 configuration.

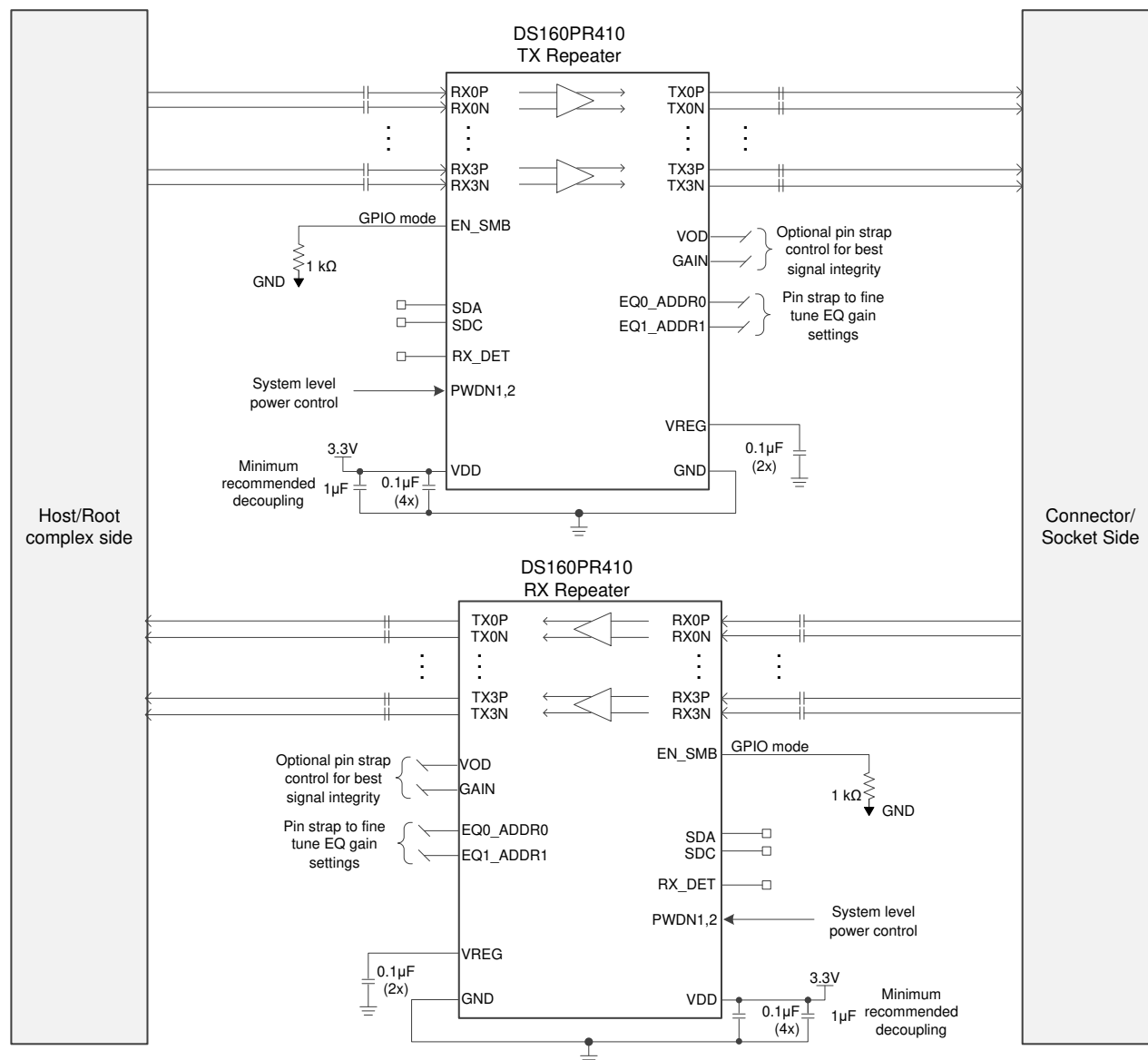


Figure 10. Simplified Schematic for PCIe x4 Lane Configuration

Typical Applications (continued)

8.2.1.1 Design Requirements

As with any high-speed design, there are many factors which influence the overall performance. The following list indicates critical areas for consideration during design.

- Use 85 Ω impedance traces when interfacing with PCIe CEM connectors. Length matching on the P and N traces should be done on the single-ended segments of the differential pair.
- Use a uniform trace width and trace spacing for differential pairs.
- Place AC-coupling capacitors near to the receiver end of each channel segment to minimize reflections.
- For Gen 3.0 and Gen 4.0, AC-coupling capacitors of 220 nF are recommended, set the maximum body size to 0402, and add a cutout void on the GND plane below the landing pad of the capacitor to reduce parasitic capacitance to GND.
- Back-drill connector vias and signal vias to minimize stub length.
- Use reference plane vias to ensure a low inductance path for the return current.

8.2.1.2 Detailed Design Procedure

In PCIe Gen 4.0 and Gen 3.0 applications, the specification requires Rx-Tx link training to establish and optimize signal conditioning settings at 16 Gbps and 8 Gbps, respectively. In link training, the Rx partner requests a series of FIR – pre-shoot and de-emphasis coefficients (10 Presets) from the Tx partner. The Rx partner includes 7-levels (6 dB to 12 dB) of CTLE followed by a single tap DFE. The link training would pre-condition the signal, with an equalized link between the root-complex and endpoint.

Note that there is no link training in PCIe Gen 1.0 (2.5 Gbps) or PCIe Gen 2.0 (5.0 Gbps) applications. The DS160PR410 is placed in between the Tx and Rx. It helps extend the PCB trace reach distance by boosting the attenuated signals with its equalization, which allows the user to recover the signal by the downstream Rx more easily.

For operation in Gen 4.0 and Gen 3.0 links, the DS160PR410 transmit outputs are designed to pass the Tx Preset signaling onto the Rx for the PCIe Gen 4.0 or Gen 3.0 link to train and optimize the equalization settings. The suggested setting for the DS160PR410 are VOD = 0 dB and DC GAIN = 0 dB. Adjustments to the EQ setting should be performed based on the channel loss to optimize the eye opening in the Rx partner. The available EQ gain settings are provided in [Table 1](#).

The Tx equalization presets or CTLE and DFE coefficients in the Rx can also be adjusted to further improve the eye opening.

Typical Applications (continued)

Figure 11 shows as an example for DS160PR410 Typical Connection Schematic.

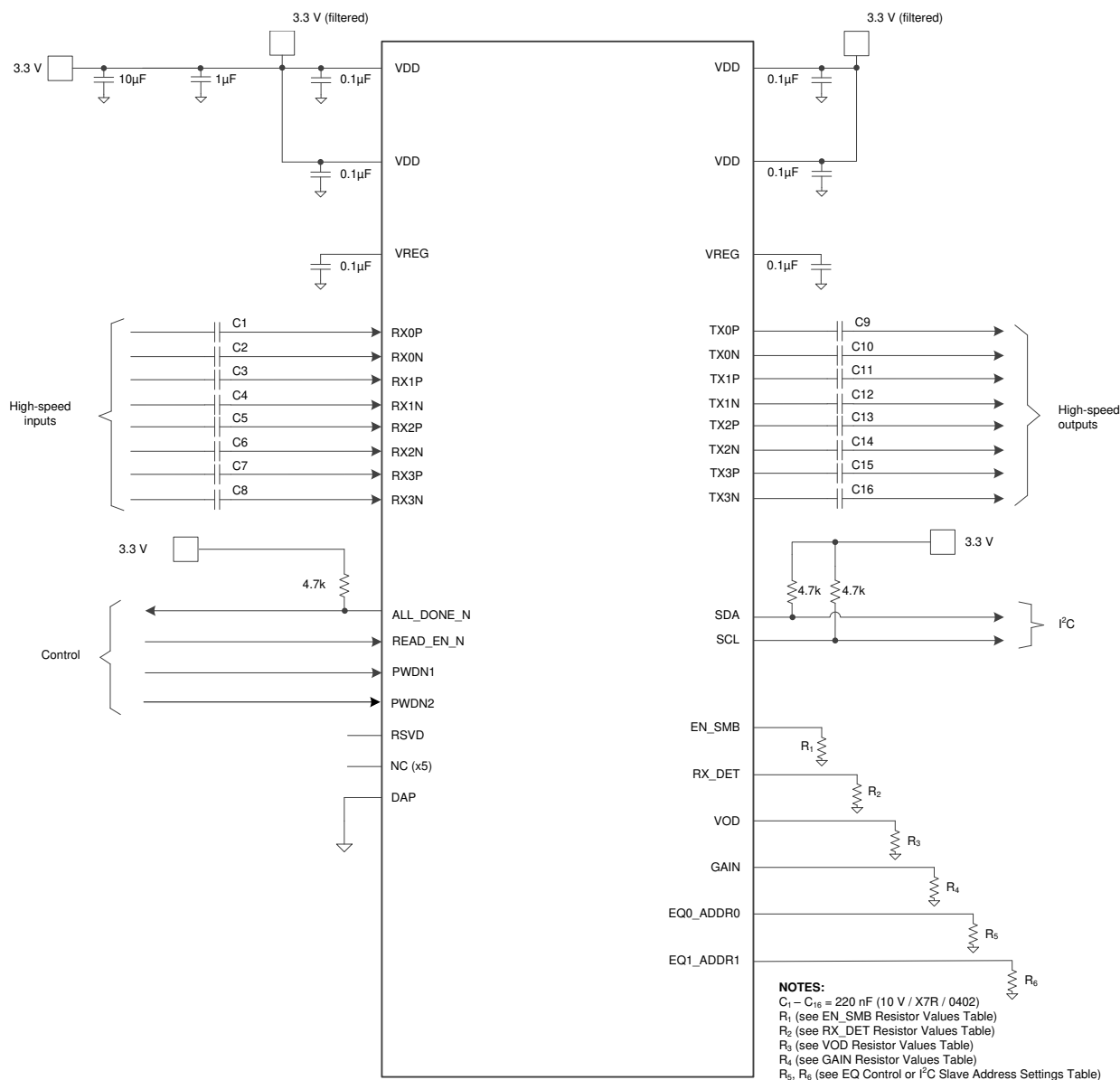


Figure 11. DS160PR410 Typical Connection Schematic

Typical Applications (continued)

8.2.1.3 Application Curves

The DS160PR410 is a linear redriver that can be used to extend channel reach of a PCIe link. Normally, PCIe-compliant TX and RX are equipped with signal-conditioning functions and can handle channel losses of up to 28 dB at 8 GHz. With the DS160PR410, the total channel loss between a PCIe root complex and an end point can be up to 45 dB at 8 GHz.

Figure 12 shows an electric link that models a single channel of a PCIe link and eye diagrams measured at different locations along the link. The source that models a PCIe TX sends a 16 Gbps PRBS-15 signal with P7 presets. After a transmission channel with -30 dB at 8-GHz insertion loss, the eye diagram is fully closed. The DS160PR410 with its CTLE set to the maximum (18 dB boost) together with the source TX equalization compensates for the losses of the pre-channel (TL1) and opens the eye at the output of the DS160PR410.

The post-channel (TL2) losses mandate the use of PCIe RX equalization functions such as CTLE and DFE that are normally available in PCIe compliant receivers.

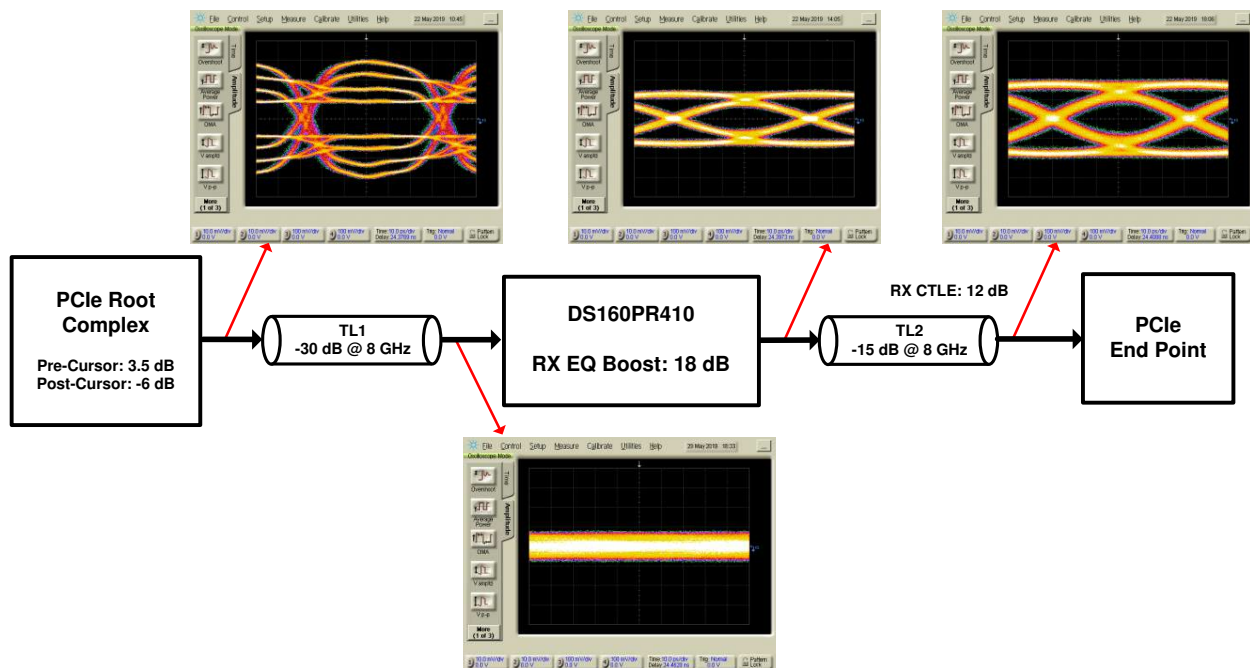


Figure 12. PCIe Gen 4.0 Link Reach Extension Using DS160PR410

Typical Applications (continued)

8.2.2 DisplayPort Application

The DS160PR410 can be used as a four channel DisplayPort (DP) redriver for data rates up to 20 Gbps. To use the device in a non-PCIe application, the RX_DET pin must be pin-strapped to GND with 59 kΩ resistor (L3).

The DS160PR410 is a linear redriver which is agnostic to DP link training. The DP link training negotiation between a display source and sink stays effective through the DS160PR410. The redriver becomes part of the electrical channel along with passive traces, cables, and so forth, resulting into optimum source and sink parameters for best electrical link.

Figure 13 shows a simplified schematic for DisplayPort application. Auxiliary and Hot plug detect (HPD) are bypassed outside of DS160PR410. If system use case requires implementing DP power states, the device must be controlled by the I²C or the pin-strap pins.

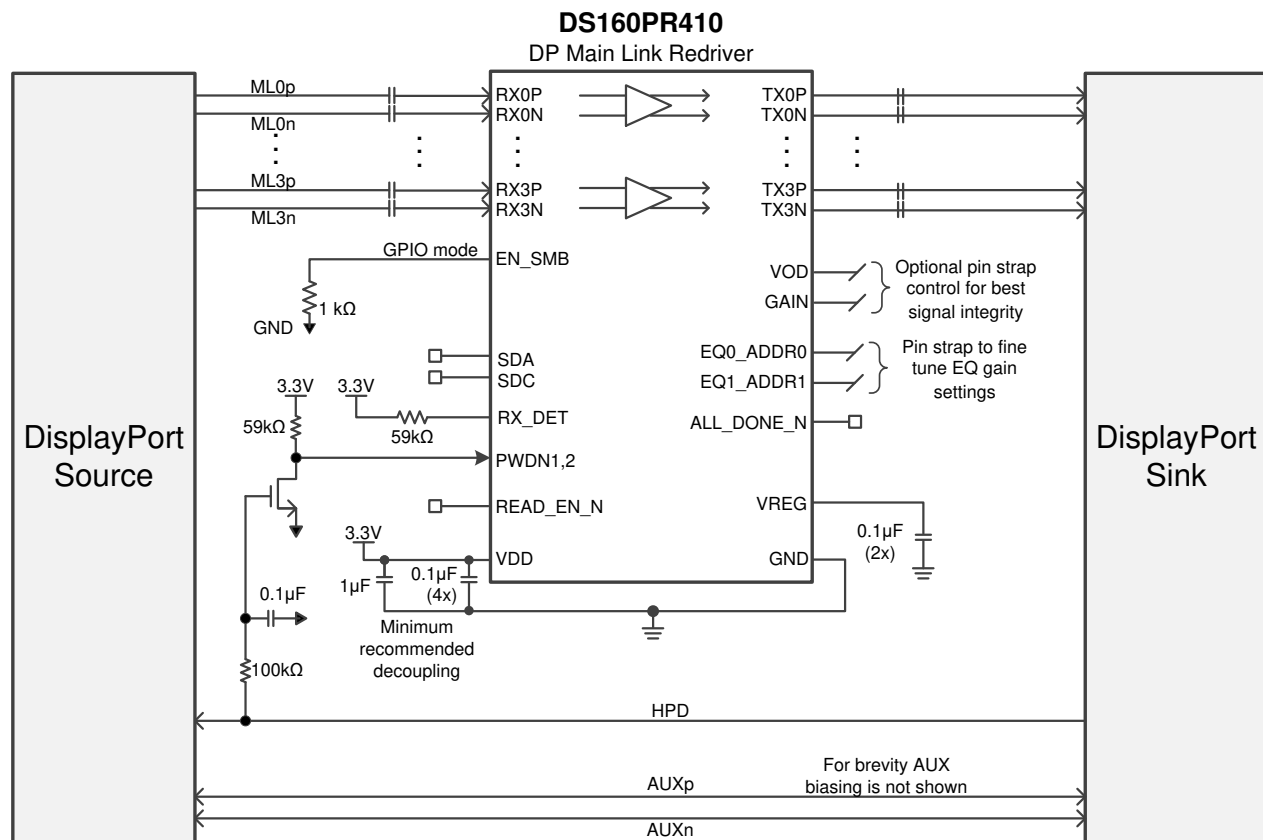


Figure 13. Simplified Schematic for DisplayPort Application

9 Power Supply Recommendations

Follow these general guidelines when designing the power supply:

1. The power supply should be designed to provide the operating conditions outlined in the Recommended Operating Conditions for DC voltage, AC noise, and start-up ramp time.
2. The DS160PR410 does not require any special power supply filtering, such as ferrite beads, provided that the recommended operating conditions are met. Only standard supply decoupling is required. Typical supply decoupling consists of a 0.1 μF capacitor per VDD pin, one 1.0 μF bulk capacitor per device, and one 10 μF bulk capacitor per power bus that delivers power to one or more DS160PR410 devices. The local decoupling (0.1 μF) capacitors must be connected as close to the VDD pins as possible and with minimal path to the DS160PR410 ground pad.

10 Layout

10.1 Layout Guidelines

The following guidelines should be followed when designing the layout:

1. Decoupling capacitors should be placed as close to the VDD pins as possible. Placing the decoupling capacitors directly underneath the device is recommended if the board design permits.
2. High-speed differential signals TXnP/TXnN and RXnP/RXnN should be tightly coupled, skew matched, and impedance controlled.
3. Vias should be avoided when possible on the high-speed differential signals. When vias must be used, take care to minimize the via stub, either by transitioning through most/all layers or by back drilling.
4. GND relief can be used (but is not required) beneath the high-speed differential signal pads to improve signal integrity by counteracting the pad capacitance.
5. GND vias should be placed directly beneath the device connecting the GND plane attached to the device to the GND planes on other layers. This has the added benefit of improving thermal conductivity from the device to the board.

10.2 Layout Example

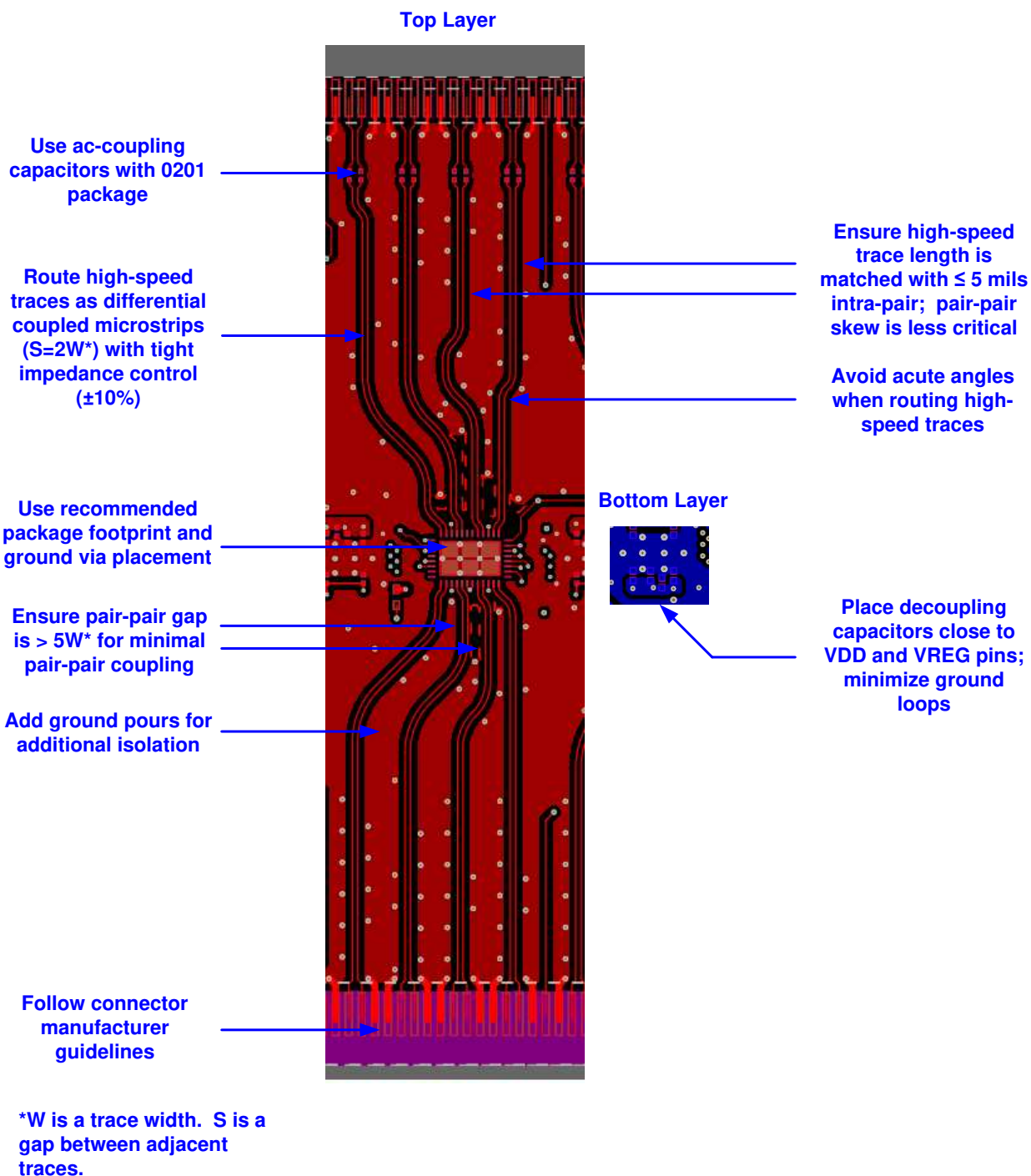


Figure 14. DS160PR410 Layout Example - Sub-Section of a PCIe Riser Card With CEM Connectors

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, [DS160PR410 Programming Guide](#) (SNLU255)
- Texas Instruments, [Understanding EEPROM Programming for DS160PR410 PCI-Express Gen-4 Redriver](#) (SNLA320)

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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11.4 Trademarks

E2E is a trademark of Texas Instruments.

11.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DS160PR410RNQR	ACTIVE	WQFN	RNQ	40	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PX410	Samples
DS160PR410RNQT	ACTIVE	WQFN	RNQ	40	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PX410	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

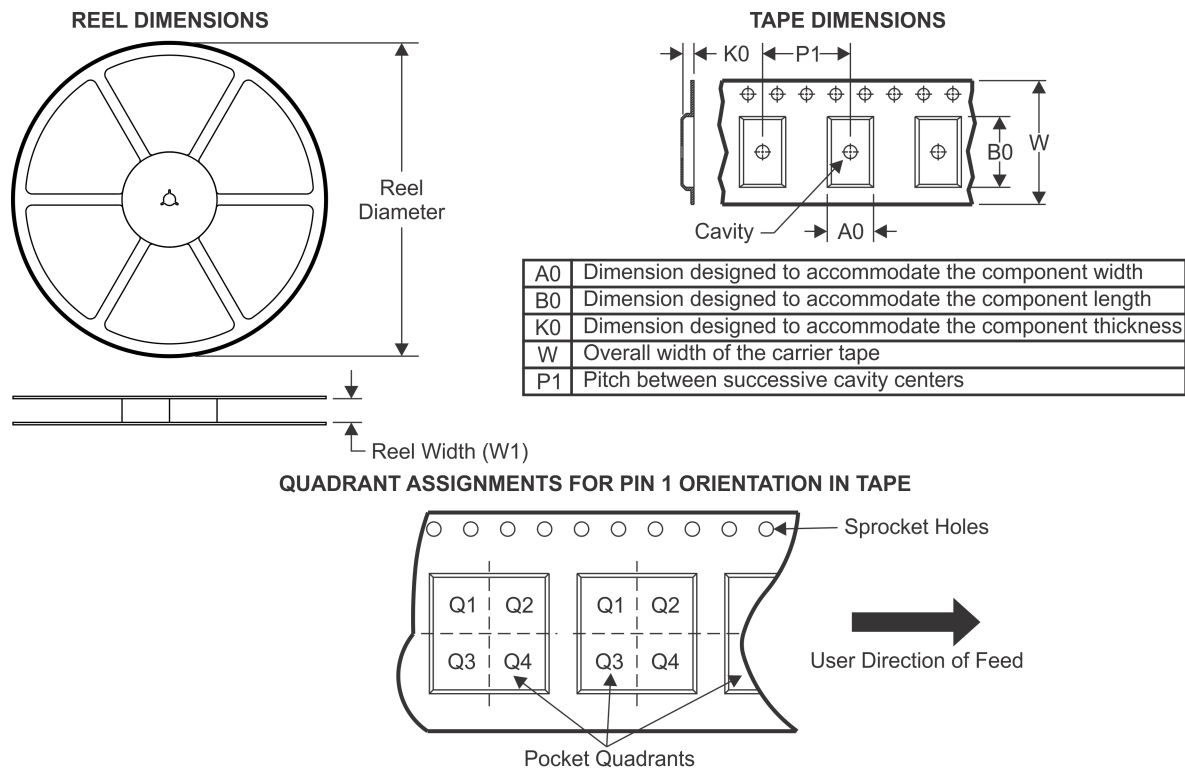
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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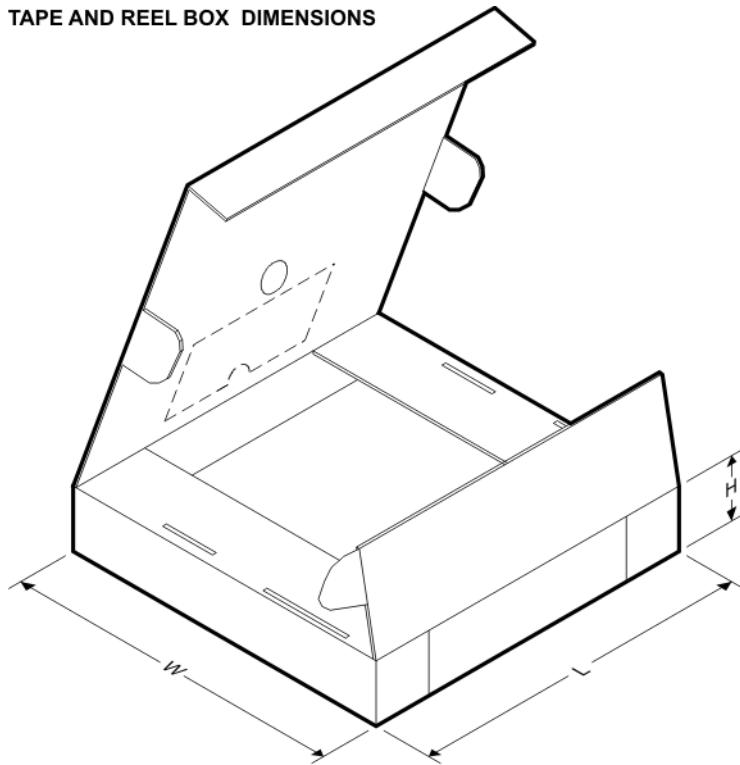
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DS160PR410RNQR	WQFN	RNQ	40	3000	330.0	12.4	4.3	6.3	1.1	8.0	12.0	Q2
DS160PR410RNQT	WQFN	RNQ	40	250	180.0	12.4	4.3	6.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DS160PR410RNQR	WQFN	RNQ	40	3000	367.0	367.0	35.0
DS160PR410RNQT	WQFN	RNQ	40	250	210.0	185.0	35.0

WQFN - 0.8 mm max height

The drawing consists of three views: a top view, a side view, and a detail view of the pin index area.

- Top View:** Shows the overall footprint of the connector. The total width is 6.1 (5.9). The total height is 4.1 (3.9). The pin index area is defined by a 4.7±0.1 width and a 2.7±0.1 height. The pin index area contains 20 pins, with 10 pins on each side. The pin index area is defined by a 4.7±0.1 width and a 2.7±0.1 height. The pin index area contains 20 pins, with 10 pins on each side. The pin index area is defined by a 4.7±0.1 width and a 2.7±0.1 height. The pin index area contains 20 pins, with 10 pins on each side.
- Side View:** Shows the profile of the connector. The total height is 0.8 MAX. The pin index area is defined by a 0.05 height and a 0.00 offset. The pin index area is defined by a 0.05 height and a 0.00 offset. The pin index area is defined by a 0.05 height and a 0.00 offset. The pin index area is defined by a 0.05 height and a 0.00 offset.
- Detail View:** Shows the pin index area in more detail. The pin index area is defined by a 4.7±0.1 width and a 2.7±0.1 height. The pin index area contains 20 pins, with 10 pins on each side. The pin index area is defined by a 4.7±0.1 width and a 2.7±0.1 height. The pin index area contains 20 pins, with 10 pins on each side.

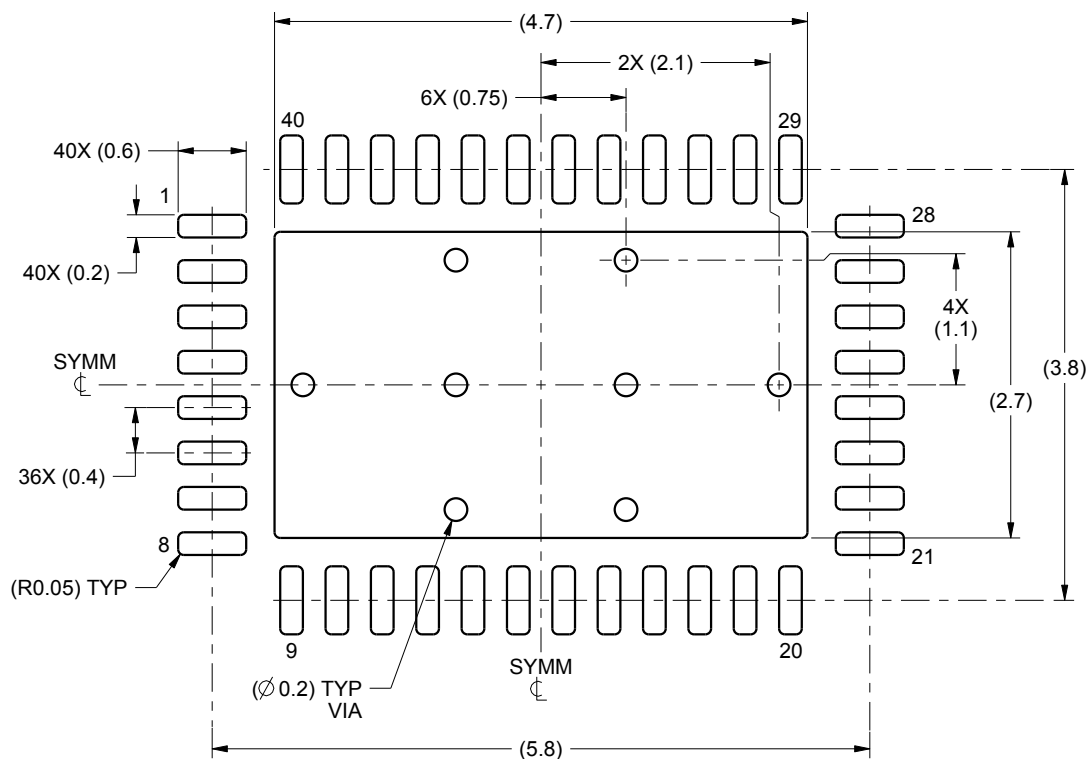
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

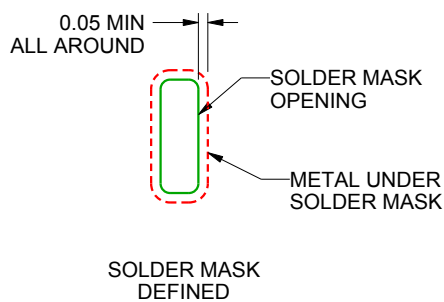
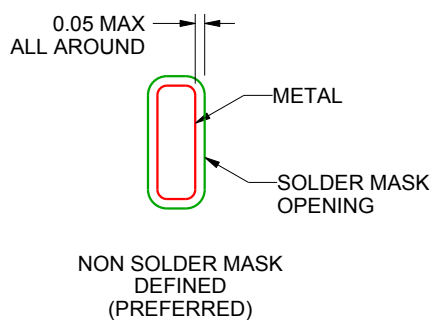
RNQ0040A

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
SCALE:15X



SOLDER MASK DETAILS

4222125/B 01/2016

NOTES: (continued)

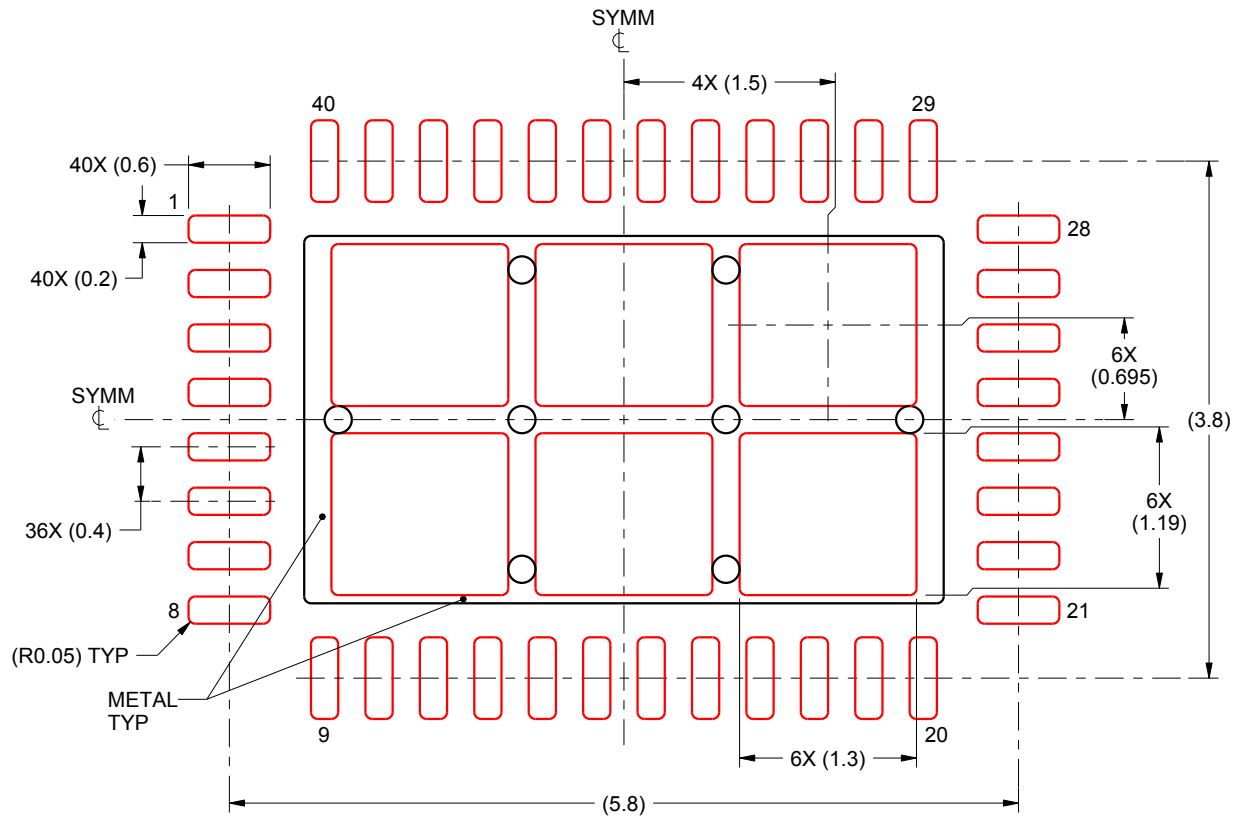
- This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).

EXAMPLE STENCIL DESIGN

RNQ0040A

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD
73% PRINTED SOLDER COVERAGE BY AREA
SCALE:18X

4222125/B 01/2016

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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