TPS4335xEVM Evaluation Module

1 Introduction

The Texas Instruments TPS4335xEVM evaluation module (EVM) helps designers evaluate the operation and performance of the TPS4335x family of Switch Mode Power Supplies – Multiple-output voltage regulator.

The EVM contains one DC / DC converter / controller (see Table 1).

Table 1. Device and Package Configurations

CONVERTER	IC	PACKAGE
U1	TPS43350QDAPQ1	DAP-38
	TPS43351QDAPQ1	

2 Setup

This section describes the jumpers and connectors on the EVM as well and how to properly connect, set up and use the TPS4335xEVM.

2.1 Input/Output Connector Description

J1 – **Input** is the protected power input terminal for the converter with a voltage range from 4V-40V. The terminal block provides a power (Vbat) and ground (GND) connection to allow the user to attach the EVM to a cable harness. The power path provides a series Schottky diode for reverse battery protection.

J2 – **VOUTA** is the output terminal for the TPS4335x buck controller A. The terminal block provides a power (VOUTA) and ground (GND) connection.

J3 – **VOUTB** is the output terminal for the TPS4335x buck controller B. The terminal block provides a power (VOUTB) and ground (GND) connection.

JP5 – **ENA** is the jumper used to enable buck controller A. The controller will be enabled when the ENA is high and disabled when low.

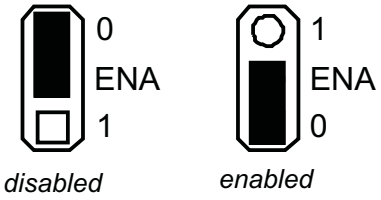


Figure 1. ENA Jumper Settings

JP6 – **ENB** is the jumper used to enable buck controller B. The controller will be enabled when the ENB is high and disabled when low.

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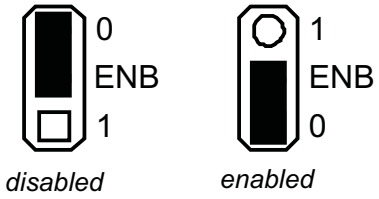


Figure 2. ENB Jumper Settings

JP2 – **SYNC** is the external clock input for switching frequency synchronization of the buck converters and to enable Low Power Mode (LPM). The external clock source can be attached to the center pin of JP4. A high logic level on this pin ensures forced continuous mode operation of the buck controllers and inhibits transition to low power mode. An open or low allows discontinuous mode operation and entry into low power mode at light loads. On the TPS43351, a high level enables frequency-hopping spread spectrum while an open or a low level disables it.

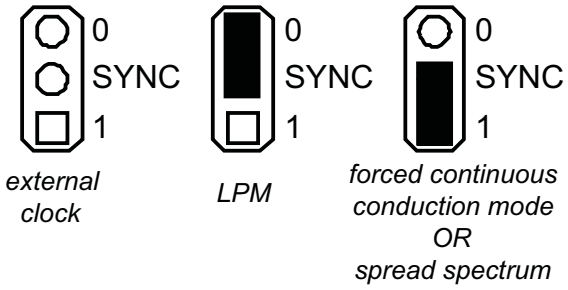


Figure 3. SYNC Jumper Setting

JP5 – **RT** is the jumper used to choose the switching frequency of the Buck controllers. The operating frequency can be set to 240 KHz, 400 KHz or 600 KHz.

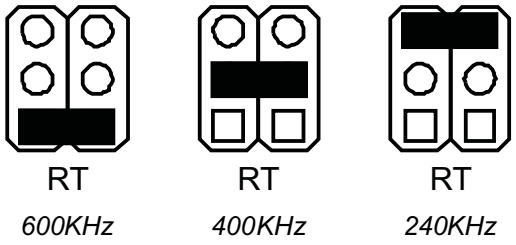


Figure 4. RT Jumper Setting

JP4 – **EXTSUP** is the jumper used to choose one of the Buck output voltages (VOUTA or VOUTB) to provide the internal voltage VREG. If no jumper is plugged, VREG is generated from the input voltage.

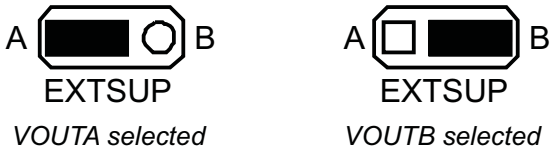


Figure 5. EXTSUP Jumper Setting

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Test Points

DLYAB	Power Good Delay for Buck Controller A and B
GND (x4)	Ground
PGA	Power Good for Buck Controller A
PGB	Power Good for Buck Controller B
PHA	Buck Controller A phase pin
PHB	Buck Controller B phase pin
SSA	Soft Start for Buck Controller A
SSB	Soft Start for Buck Controller B
VBAT	Power Input
VIN	Power Input after the reverse-polarity protection stage
VOUTA	Buck Controller A output
VOUTB	Buck Controller B output

2.2 Setup

The input voltage range for the device is from 4V-40V. At start-up, minimum input voltage is 6.5V. With the settings of the EVM, for Buck B (set to 3.3V output) an input voltage of 4V is sufficient (after meeting the start-up condition). Buck A, set to 5V output, naturally requires a higher supply voltage for proper operation.

2.3 Operation

For proper operation of the TPS4335x, ENA, ENB, EXTSUP, RT and SYNC jumpers should be properly configured. The recommended setting, using the switch and shorting blocks.

ENA	enabled
ENB	enabled
EXTSUP	A
RT	400KHz
SYNC	LPM

In this configuration, the regulators will turn on when power is applied. Delay sets the power-on reset delay, slow, medium or fast. ENA and ENB turn the regulators on or off, disabled or enabled. EXTSUP selects the power supply source for the gate drive. RT sets the switching frequency for the regulators to approximately 240KHz, 400KHz or 600KHz. SYNC enabled LPM or forced continuous conduction mode and is the external clock input for switching frequency synchronization of the buck converters. SYNC will disable spread spectrum operation on the TPS43351-Q1 when set low or left open. The device can be setup to run in low power mode, to reduce the quiescent operating current, by connecting the Sync test point to ground. Low power mode will allow the device to switch into a PFM mode of operation if the load current demand is low. It will automatically switch back to PWM mode as the load current increases.

Table 2. Regulator Configuration

REGULATOR	OUTPUT VOLTAGE	MAXIMUM OUTPUT CURRENT
Buck Controller A	5.0 V	2A
Buck Controller B	3.3 V	4A

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If jitter is observed on the phase signal of the regulator, then noise may be entering the feedback interface and a capacitive filter may be required. The EVM provides a 47pF-capacitor across the low-side feedback resistors. Typically 47pF to 100pF is sufficient to filter any noise issues.

3 Board Layout

Figure 6, Figure 7, Figure 8, and Figure 9 show the board layout for the TPS4335xEVM PWB. Figure 10 displays the schematic.

The TPS4335x controller offers high efficiency, but does dissipate power. The PowerPAD package offers an exposed thermal pad to enhance thermal performance. This must be soldered to the copper landing on the PCB for optimal performance. The PCB provides 1 oz copper planes on the top and bottom to dissipate heat.

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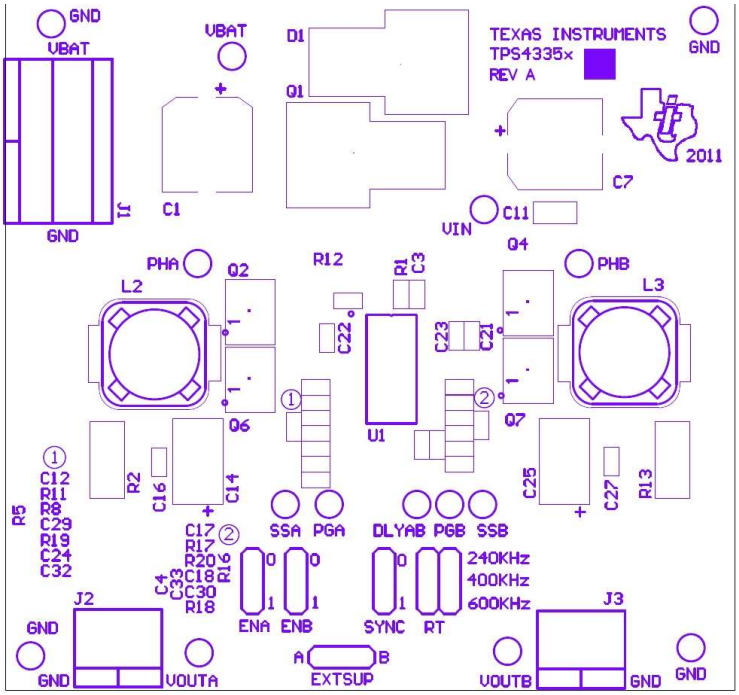


Figure 6. Top Assembly Layer

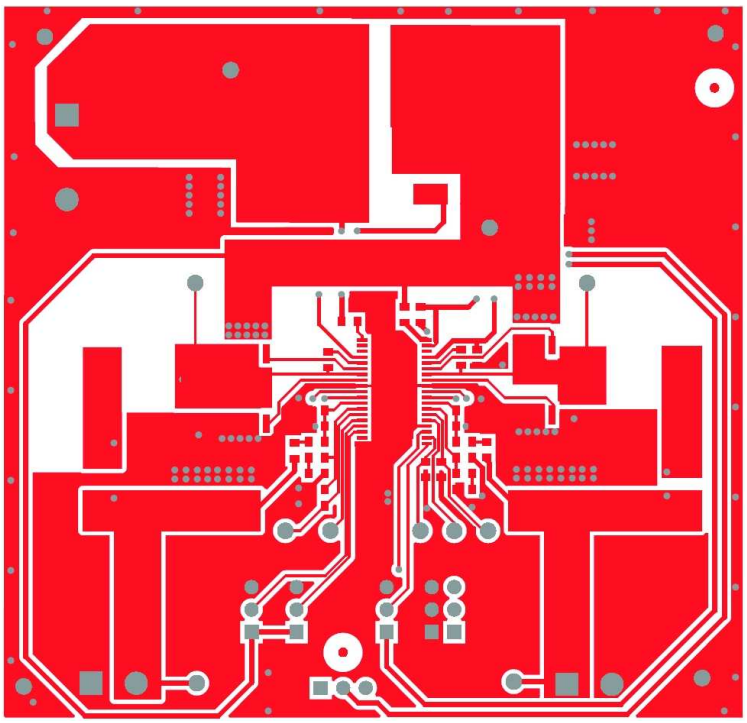


Figure 7. Top Layer Routing

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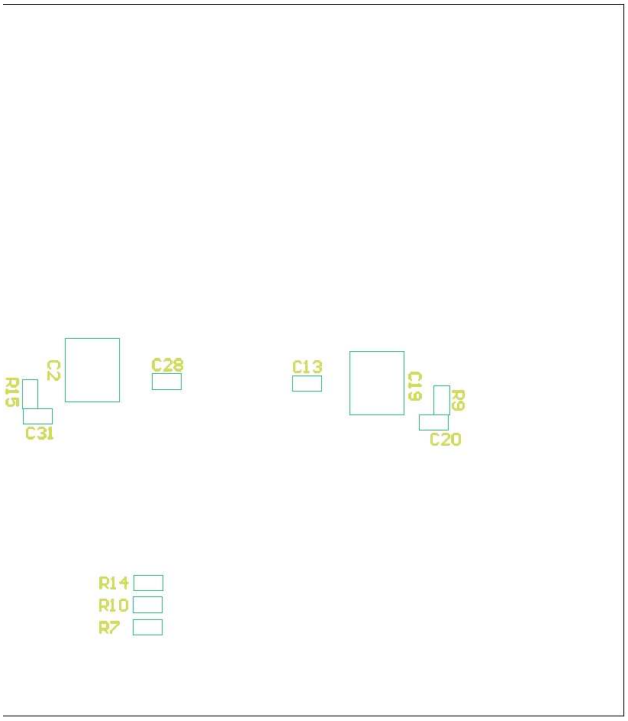


Figure 8. Bottom Assembly Layer

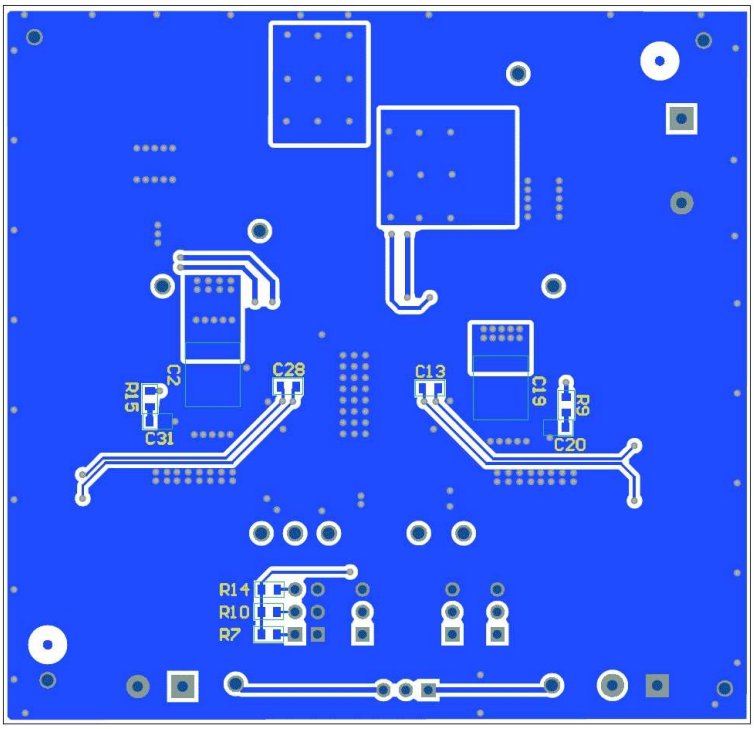


Figure 9. Bottom Layer Routing

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4 Schematic and Bill of Materials

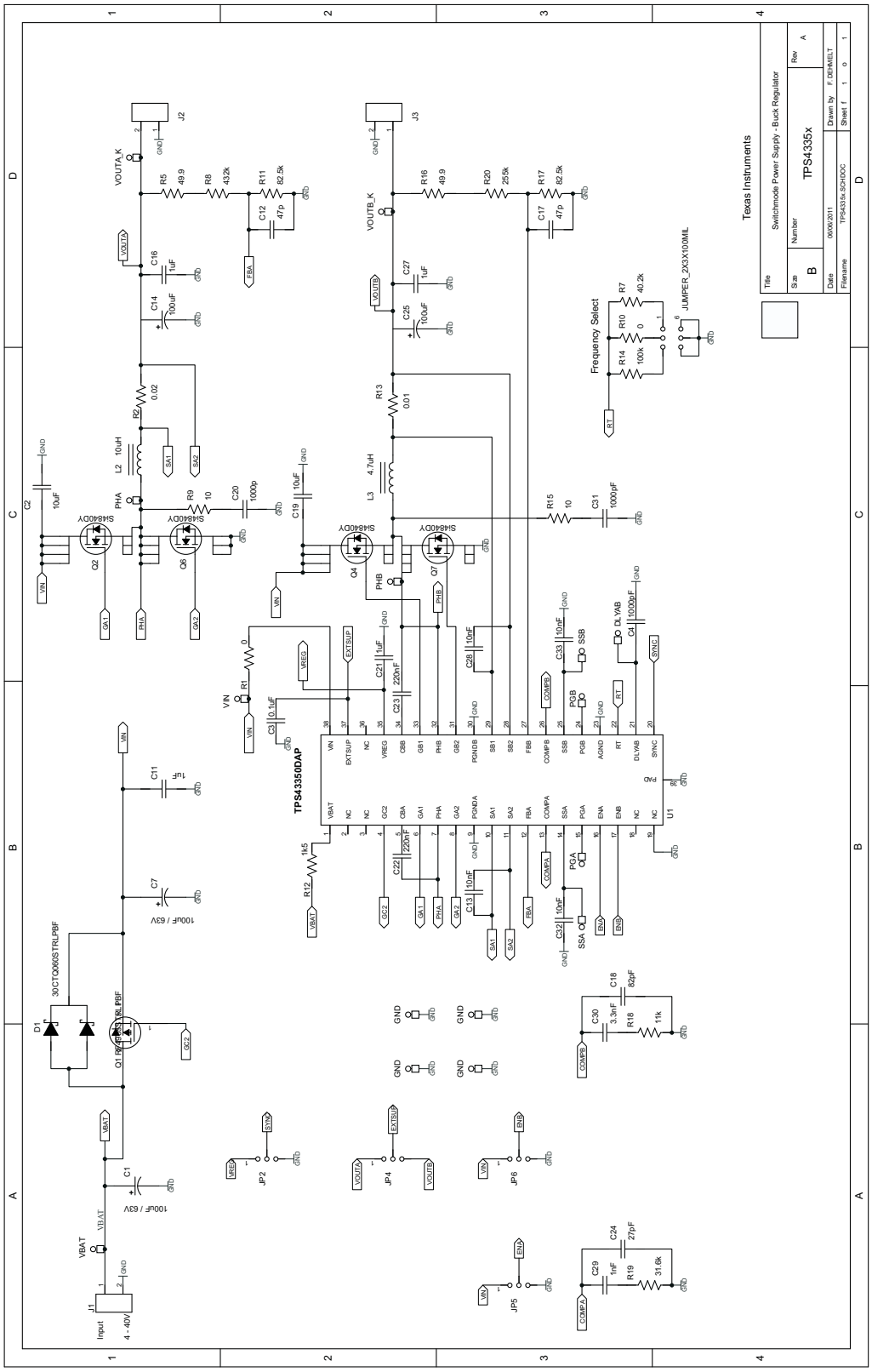


Figure 10. TPS4335xEVM Schematic

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Table 3. Bill of Materials

COMMENT	DESCRIPTION	DESIGNATOR	FOOTPRINT	QTY
TI Bug		*1	TI Bug New	1
G,100uF,63V,Al-El,EEE-FK1J101P	Capacitor, Aluminum, SM, ±20%, vvV,	C1, C7	ELKO-AL-G	2
2220,10uF,100V,ceramic	Capacitor, Ceramic, vvV, [temp], [tol]	C2, C19	CAP_2220	2
0603,0.1uF,50V,ceramic	Capacitor, Ceramic, vvV, [temp], [tol]	C3	C603	1
0603,1000pF,50V,ceramic	Capacitor, Ceramic, vvV, [temp], [tol]	C4, C29	C603	2
1206,1uF,100V,ceramic	Capacitor, Ceramic, vvV, [temp], [tol]	C11	C1206	1
0603,47pF,50V,ceramic	Capacitor, Ceramic, vvV, [temp], [tol]	C12, C17	0603	2
0603,0.01uF,50V,ceramic	Capacitor, Ceramic, vvV, [temp], [tol]	C13, C28, C32, C33	C603	4
7343,100uF,16V,tantal,TPSD107K016 R0060	Capacitor, Tantalum, vvV, [temp], [tol]	C14, C25	CAP_TPSD/E	2
0603,1uF,16V,ceramic	Capacitor, Ceramic, vvV, [temp], [tol]	C16, C21, C27	C603	3
0603,82pF,50V,ceramic	Capacitor, Ceramic, vvV, [temp], [tol]	C18	C603	1
0603,1000pF,50V,ceramic	Capacitor, Ceramic, vvV, [temp], [tol]	C20, C31	0603	2
0603,220nF,50V,ceramic	Capacitor, Ceramic, vvV, [temp], [tol]	C22, C23	C603	2
0603,27pF,50V,ceramic	Capacitor, Ceramic, vvV, [temp], [tol]	C24	C603	1
0603,3.3nF,50V,ceramic	Capacitor, Ceramic, vvV, [temp], [tol]	C30	C603	1
d2pak_30CTQ060STRLPBF		D1	D2PAK	1
OSTT7022150	Terminal Block, 2-pin, 32-A, 9.5mm	J1	TB_2X9.5MM	1
OSTTA024163	Terminal Block, 2-pin, 15-A, 5.1mm	J2, J3	TB_2X5.1MM	2
JUMPER_3X100MIL	JUMPER_3X100MIL	JP2, JP4, JP5, JP6	HDR100_1X3	4
JUMPER_2X3X100MIL	Header, 3-pin, 100mil spacing, (36-pin strip)	JP7	HDR100_2X3	1
MSS1278T-103ML	IND	L2	IND_DR127	1
74477004	IND	L3	IND_DR127	1
IRF4905STRLPBF	IRF4905STRLPBF	Q1	D2PAK	1
TR-SI4840DY	MOSFET, N-ch, 40V, 14A, 9milliohm	Q2, Q4, Q6, Q7	SO8	4
R0603_0R	R0603_0R, R0603_1%	R1, R10	0603	2
R2512_0.02R	Resistor, Chip, 2W, 0.1%	R2	R2512	1
R0603_49R9	R603	R5, R16	0603	2
R0603_40k2	R0603_1%	R7	0603	1
R0603_432k	R603	R8	0603	1
R0603_10R	R603	R9, R15	0603	2
R0603_82k5	R603	R11, R17	0603	2
R0603_1K5	Resistor, Chip, 1/8W, 1%	R12	0603	1
R2512_0.01R	Resistor, Chip, 2W, 0.1%	R13	R2512	1
R0603_100k	R0603_1%	R14	0603	1
R0603_11k	R0603_1%	R18	0603	1
R0603_31.6k	R0603_1%	R19	0603	1
R0603_255k	R603	R20	0603	1
PHA	Glass Beaded Test Point	TP1	TEST POINT 0.052	1
VOUTA_K	Glass Beaded Test Point	TP2	TEST POINT 0.052	1
SSA	Glass Beaded Test Point	TP3	TEST POINT 0.052	1
VBAT	Glass Beaded Test Point	TP4	TEST POINT 0.052	1
PGA	Glass Beaded Test Point	TP5	TEST POINT 0.052	1
PGB	Glass Beaded Test Point	TP6	TEST POINT 0.052	1
GND	Glass Beaded Test Point	TP7, TP14, TP15, TP16	TEST POINT 0.052	4
VIN	Glass Beaded Test Point	TP8	TEST POINT 0.052	1
VOUTB_K	Glass Beaded Test Point	TP10	TEST POINT 0.052	1

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Table 3. Bill of Materials (continued)

COMMENT	DESCRIPTION	DESIGNATOR	FOOTPRINT	QTY
PHB	Glass Beaded Test Point	TP11	TEST POINT 0.052	1
SSB	Glass Beaded Test Point	TP12	TEST POINT 0.052	1
DLYAB	Glass Beaded Test Point	TP13	TEST POINT 0.052	1
TPS43350DAP		U1	DAP (R-PDSO-G38)	1
PCB	Printed Circuit Board	PCB		1

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EVM Warnings and Restrictions

It is important to operate this EVM within the input voltage range of 2 V to 40 V (boost enabled) or 4 V to 40 V (boost disabled) and the output voltage range of 0.9 V to 11 V.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 85°C. The EVM is designed to operate properly with certain components above 60°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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