

MSC8122



The High-Performance DSP with Ethernet

Taking full advantage of the scalable StarCore™ architecture, the MSC8122 offers a "DSP-farm-on-a-chip" level of performance integration. The raw processing power of this highly integrated system-on-a-chip device enables developers to create next-generation networking products that offer tremendous channel densities, while maintaining system flexibility, scalability and upgradability. The MSC8122 is well suited for computation-intensive infrastructure DSP applications, including packet telephony

media gateways, multichannel modem banks and third-generation wireless systems.

For systems supporting the true convergence of circuit-switched voice, fax, modem and packet-based protocols, the MSC8122 multicore DSP is an ideal fit.

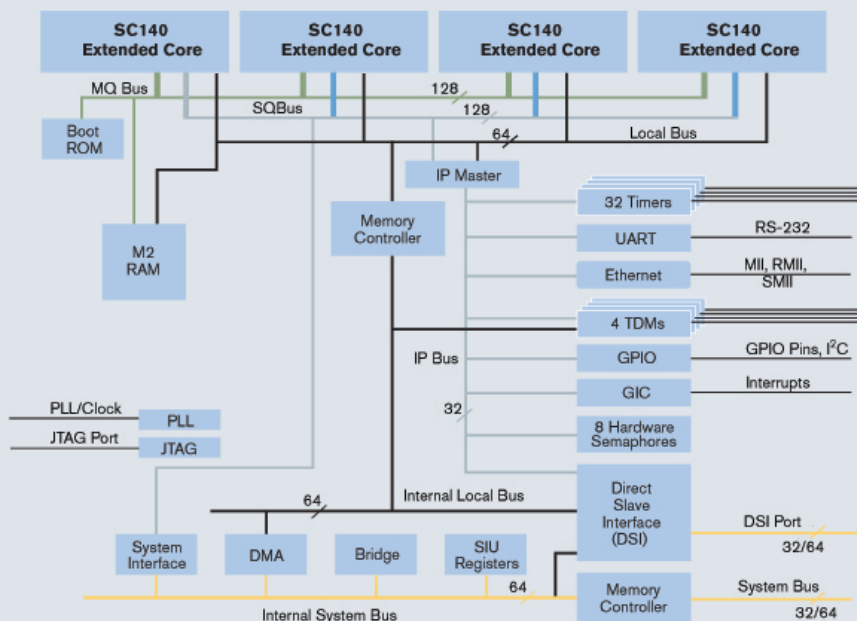
The MSC8122 multicore device signals a breakthrough in wireless infrastructure with the introduction of DSPs in advanced 90-nanometer process technology, which drives low core voltage and low power dissipation. Aimed at delivering industry-leading channel density and

scalable, low-power and cost-optimized design, the MSC8122 is offered at three core speed levels: 300 MHz, 400 MHz and 500 MHz. With four DSP extended cores based on StarCore technology, the MSC8122 is a highly integrated system-on-a-chip that can deliver up to 8000 DSP MMACS performance at up to 500 MHz, yielding an effective performance equal to 2.0 GHz. The MSC8122 comprises four time division multiplexing (TDM) serial interfaces, 32 general-purpose timers, a flexible system interface unit (SIU), a fully featured multichannel DMA controller, a sophisticated multilevel memory hierarchy with large on-chip SRAM, a high-speed Ethernet interface for different types of external memories, and high-speed host port and serial communication interfaces.

Why Ethernet?

Ethernet has become the de facto low-cost pervasive packet network interface between the DSP array, host processors and the network. The MII, RMII and SMII Ethernet interfaces for the MSC8122 provide direct access to packet networks and use a low pin count, providing a glueless interface to onboard Ethernet switches and PHYs that enables scalable, distributed, uncomplicated and low-cost board architecture.

MSC8122 BLOCK DIAGRAM



DIFFERENCES BETWEEN MSC8102 AND MSC8122

Feature	MSC8102	MSC8122
Core voltage	1.6V $\pm$ 0.1V	1.1V $\pm$ 0.5V (300 MHz/400 MHz) 1.2V $\pm$ 0.6V (300 MHz/400 MHz) 1.2V $\pm$ 0.4V (500 MHz)
Target operating frequency	250 MHz and 275 MHz	300 MHz, 400 MHz and 500 MHz
Pin definition differences	As defined in the MSC8102 Technical Data Sheet and the MSC8102 Reference Manual (MSC8102RM)*	Ethernet pins can be mixed with DSI pins, which enable the use of all four TDMs; 15 pins have new multiplexed signals required for Ethernet support; two power pins and one ground pin also are used to supply Ethernet signals
Ethernet controller	Not available	IEEE® Std. 802.3™, Std. 802.3u™, Std. 802.3x™ and Std. 802.3ac™; supports MII, RMII and SMII; direct access to internal memories via the DMA controller
Memory maps	As defined in the MSC8102 Reference Manual (MSC8102RM)*	Adds programmable registers for the Ethernet controller
I ² C interface	None	Engineered to support the standard I ² C signals (SDA and SCL); designed to permit boot from a slave memory device

*Available at www.freescale.com

Features

- > Four 300 MHz/400 MHz/500 MHz SC140 extended cores
- > 224 KB, of dedicated M1 memory for each extended core
- > 16 KB, 16-way instruction cache in each extended core
- > 476 KB of shared M2 memory between all extended cores
- > 4 KB bootstrap ROM
- > Ethernet interface designed to comply with IEEE Std. 802.3, Std. 802.3u, Std. 802.3x and Std. 802.3ac
- > Configurable dual bus architecture
- > 32- or 64-bit industry-standard external 60x-compatible bus interface at up to 166 MHz
- > 32- or 64-bit high-performance direct slave interface (DSI)
- > 476 KB of shared M2 four independent time division multiplexing (TDM) interfaces (256 channels each)

- > Flexible memory controller for various external memory types
- > 16-channel DMA engine that facilitates independent data transfers
- > 32 16-bit timers with watchdog mode support
- > 1.1V and 1.2V extended core; 3.3V I/O
- > 0.8 mm pitch 20 mm x 20 mm Flip-Chip Plastic Ball-Grid Array (FC-PBGA)
- > I²C port compatible with I²C bus standard and widespread I²C serial EEPROM access protocol

Benefits

- > Up to 4800/6400/8000 MMACS of DSP performance capability
- > Ethernet interface that provides direct access to internal memories
- > Excellent channel and power density ratio
- > Code-compatible with the existing MSC8102, MSC8101 and MSC8103

- > Pin-compatible with the MSC8102
- > C programming that helps speed time to market
- > High code density that results in low system costs

Software Development Tools

- > Tools integrated in an integrated development environment (IDE)
- > Real-time debug capability for each extended core
- > Optimized C compiler generates efficient control and DSP code
- > Real-time operating system (RTOS) that fully supports device architecture (multicore, memory, hierarchy, I-Cache, timers, DMA, interrupts, peripherals)

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