MP5610

2.7V to 5.5V Input, 1.2MHz, Dual-ch *LCD Bias Power Supply*

DESCRIPTION

The MP5610 is a dual-output converter with 2.7V-to-5.5V input for small size LCD panel bias supply. It uses peak-current mode to regulate the positive output voltage and uses a negative charge pump to provide negative output voltage. The MP5610 has very good efficiency performance because the negative charge pump draws power directly from the positive converter switching node which can save power loss much. Also, MP5610 provides good voltage tracking between positive and negative output by well matching the internal MOSFET on resistance value. The fully integrated synchronous rectification increases total efficiency and reduces PCB space requirements.

The MP5610 features as programmable output, fixed 1.2MHz switching frequency and rich protection modes, like input-output disconnection protection, cycle-by-cycle current limit protection, thermal shutdown protection, Output over voltage protection and Output under voltage protection.

The MP5610 is available in tiny QFN-10 (1.4mmx1.8mm) package.

FEATURES

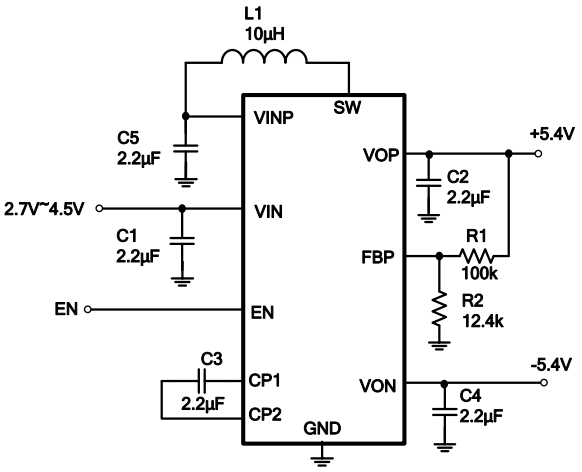
- 2.7V-to-5.5V Input Voltage
- Max. 50mA Output Current for Each Output
- Up to Programmable 5.8V Output Voltage
- 0.5% Line Regulation for Step-up Converter
- 0.5% Load Regulation for Step-up Converter
- 1% Voltage Tracking Between Dual-ch
- 600mV Feedback Voltage with ±1% Accuracy
- 270us Soft Start Time
- Input DC Current Limit Protection
- Output Over Voltage Protection
- Output Under Voltage Protection
- Input UVLO Protection
- Over Temperature Protection
- Available in a QFN-10 (1.4mm×1.8mm) Package

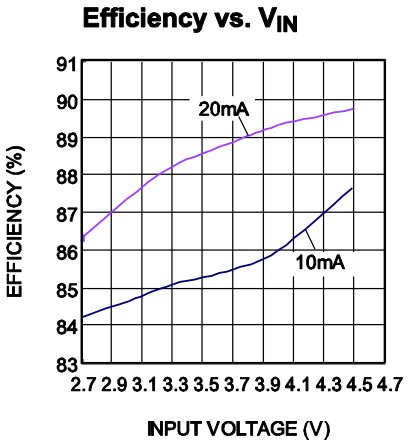
APPLICATIONS

- Feature Phones and Smart Phones
- Small Size LCD Displays

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TYPICAL APPLICATION





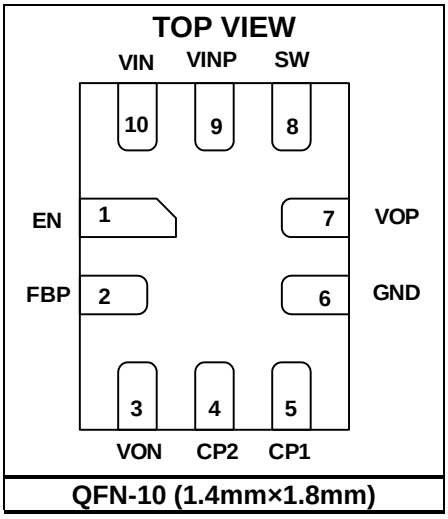
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ORDERING INFORMATION

Part Number*	Package	Top Marking
MP5610GQG	QFN-10 (1.4mm×1.8mm)	BZ

* For Tape & Reel, add suffix –Z (e.g. MP5610GQG–Z);

PACKAGE REFERENCE



QFN-10 (1.4mm×1.8mm)

ABSOLUTE MAXIMUM RATINGS (1)

V_{IN}, V_{INP} ..... -0.3V to +6.5V
V_{SW}, V_{OP}, V_{CP1} ..... -0.3V to +7V
V_{CP2}, V_{ON} ..... -7V to +0.3V
All Other Pins ..... -0.3V to +6.5V
Junction Temperature ..... 150°C
Lead Temperature ..... 260°C
Continuous Power Dissipation ... (T_A = 25°C) (2)
QFN-10 (1.4mm×1.8mm) 0.892W

Recommended Operating Conditions (3)

Supply Voltage V_{IN} ..... 2.7V to 5.5V
Operating Junction Temp. ..... -40°C to +125°C

Thermal Resistance (4)

	θ_{JA}	θ_{JC}	
QFN-10 (1.4mm×1.8mm)	140	30	°C/W

Notes:
1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

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ELECTRICAL CHARACTERISTICS

V_{IN} =3.7V, V_{EN} = V_{IN}, T_A = 25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
GENEARL						
Operating Input Voltage	V_{IN}		2.7		5.5	V
Supply Current (Quiescent)	I_Q	V_{IN}=3.7V, V_{EN}= V_{IN}, no switching		450	500	μA
Supply Current (Shutdown)	I_{ST}	V_{EN}=0V, V_{IN}=3.7V			0.2	μA
Input UVLO Threshold	V_{IN_UVLO}	Rising Edge	2.35	2.45	2.55	V
Input UVLO Hysteresis				260		mV
EN High Voltage	V_{EN_HIGH}	V_{EN} Rising	1.2			V
EN Low Voltage	V_{EN_LOW}	V_{EN} Falling			0.4	V
Switching Frequency	f_{SW}		0.96	1.2	1.44	MHz
Input Disconnect MOSFET On-Resistance	R_{ON_M5}	V_{IN}=3.7V		0.1		Ω
Input DC Current Limit	I_{LIM_IN}	V_{IN}=3.7V	200	245	290	mA
Input DC Current Ramp Time		V_{IN}=3.7V, V_{INP}=GND I_{LIM_IN}: 0 to 260mA		215		us
REF Soft Start Time		V_{IN}=3.7V		270		us
STEP-UP CONVERTER						
Maximum Duty Cycle	D_{MAX}		75	85		%
Minimum On Time	t_{ON_MIN}			110		ns
Feedback Regulation Voltage	V_{FBP}		594	600	606	mV
Feedback Input Bias Current					100	nA
Main Switch On-Resistance	R_{ON_M1}	V_{IN}=2.7V-3.7V,		0.5		Ω
High Side Switch On-Resistance	$R_{ON_M2\&M6}$	V_{IN}=2.7V-3.7V,		2.0		Ω
Cycle-by-Cycle Current Limit	I_{LIM}	Duty Cycle=0%	240	300	365	mA
High Side Switch Current ZCD Detection Threshold			5	10	15	mA
NEGATIVE CHARGE PUMP						
CP2 to GND MOSFET On-Resistance	R_{ON_M3}	V_{IN}=2.7V-3.7V,		0.6		Ω
CP2 to VON MOSFET On-Resistance	R_{ON_M4}	V_{IN}=2.7V-3.7V,		0.5		Ω
PROTECTION						
Positive Output Over Voltage Protection Threshold	V_{OVP}		5.9	6.1	6.4	V
Output Over Voltage Protection Hysteresis	V_{OVP_TH}			215		mV
Negative Output Over Voltage Protection Threshold	V_{OVN}		-6.7	-6.2	-5.8	V
Output Over Voltage Protection Hysteresis				165		mV

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ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} =3.7V, V_{EN} = V_{IN}, T_A = 25°C, unless otherwise noted.

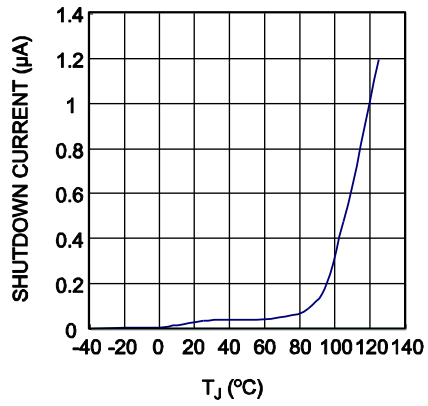
Parameters	Symbol	Condition	Min	Typ	Max	Units
PROTECTION *(continued)*						
Positive Output Under-Voltage Protection Threshold	V_{UVP_P}			52%		REF
Negative Output Under-Voltage Protection Threshold	V_{UVP_N}			60%		V_{OP}
OTP Protection Threshold	T_{j_SD}			150		℃

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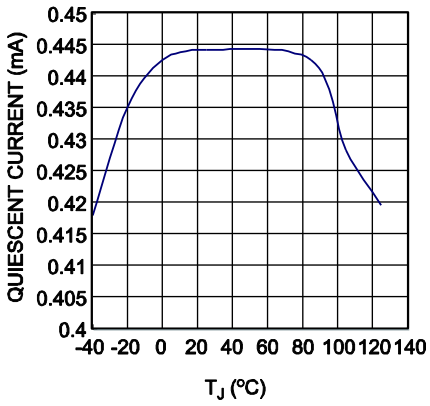
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 3.7V, V_{OP}=+5.4V, V_{ON}=-5.4V, L = 10µH, C_{OUT}=1µF, T_A = 25°C, unless otherwise noted.

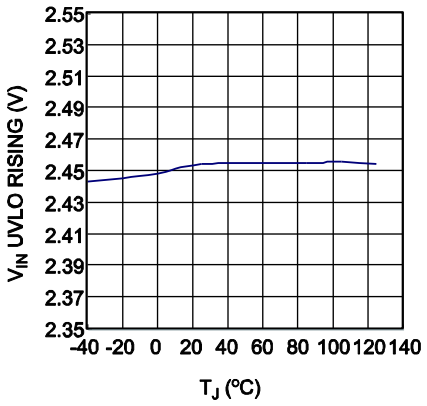
I_{ST} vs. T_J



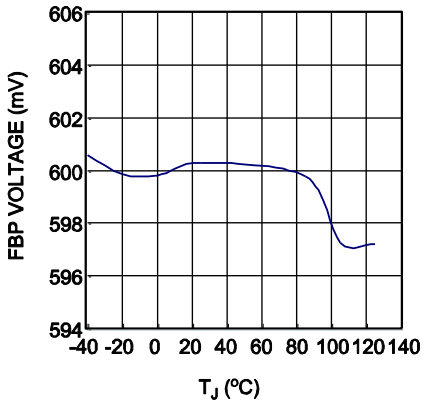
I_Q vs. T_J



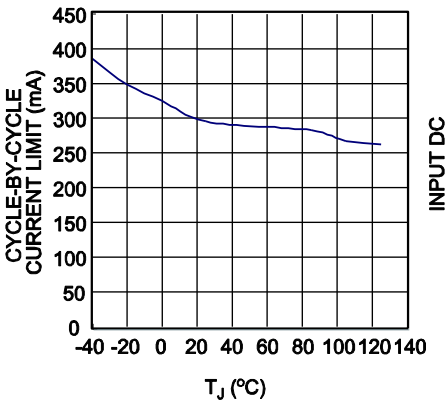
V_{IN_UVLO} vs. T_J



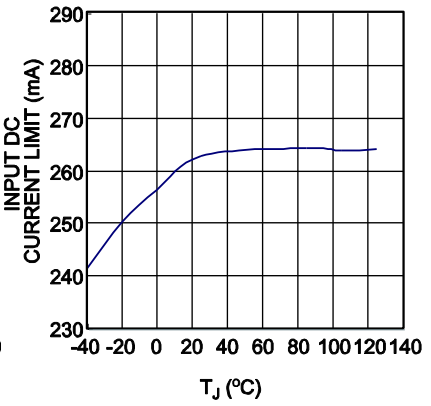
V_{FBP} vs. T_J



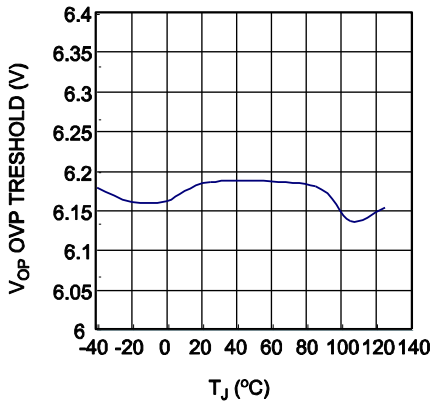
I_{LIM} vs. T_J



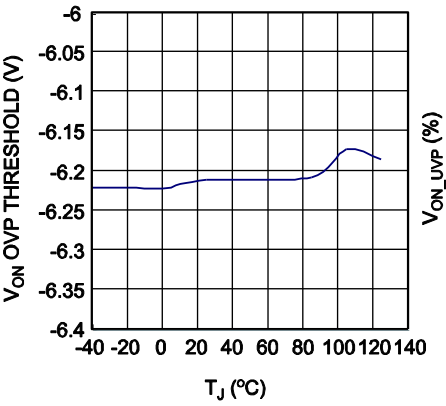
I_{LIM_IN} vs. T_J



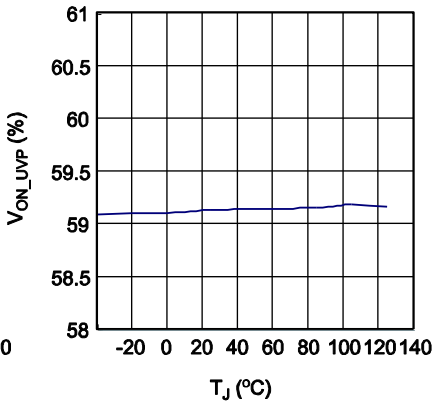
V_{OVP} vs. T_J



V_{OVN} vs. T_J



V_{UVP_N} vs. T_J

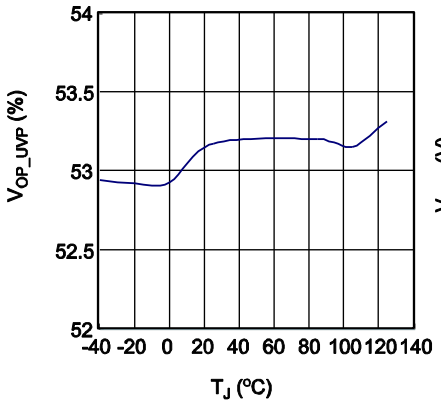


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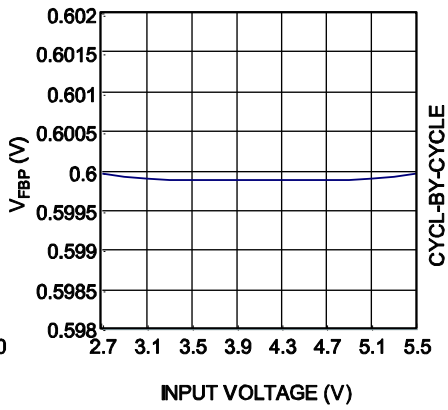
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 3.7V, V_{OP}=+5.4V, V_{ON}=-5.4V, L = 10µH, C_{OUT}=1µF, T_A = 25°C, unless otherwise noted.

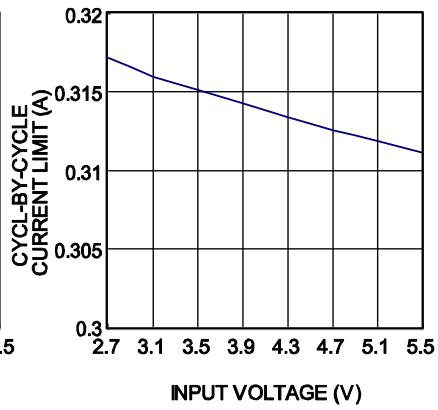
V_{UVP_P} vs. T_J



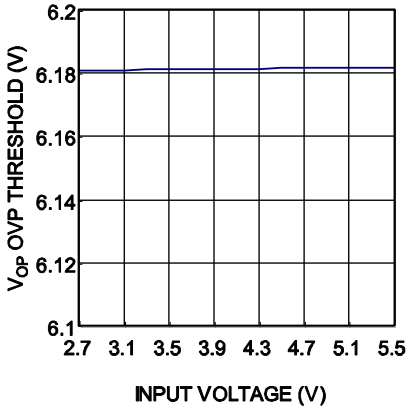
V_{FBP} vs. V_{IN}



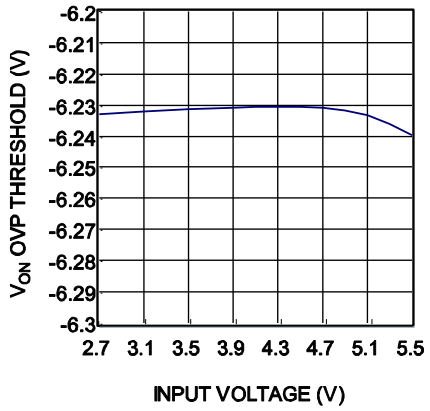
Current Limit vs. V_{IN}



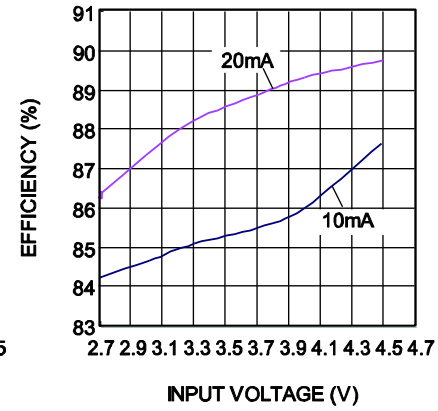
V_{OVP} vs. V_{IN}



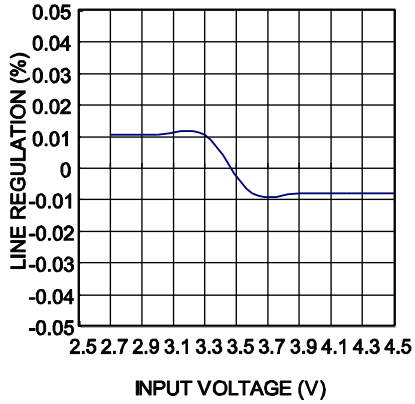
V_{OVN} vs. V_{IN}



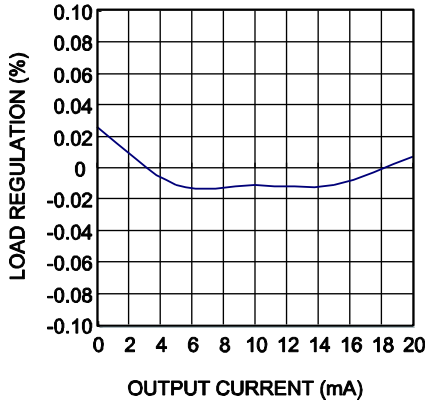
Efficiency vs. V_{IN}



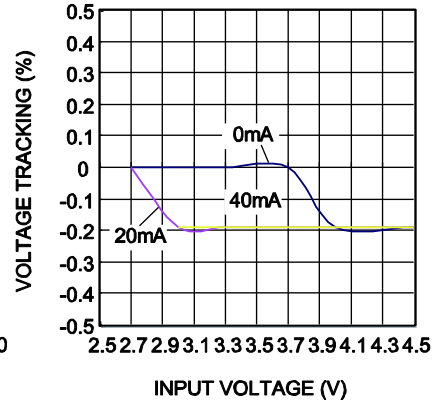
Line Regulation



Load Regulation



Voltage Tracking @ Symmetric Load

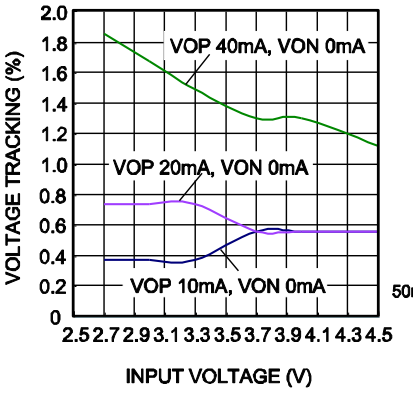


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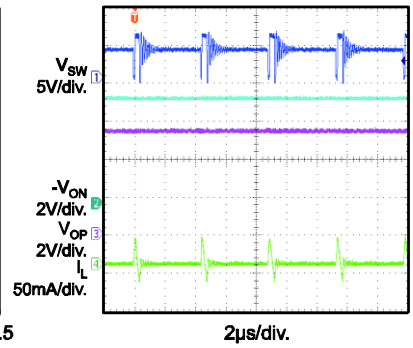
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 3.7V, V_{OP}=+5.4V, V_{ON}=-5.4V, L = 10µH, C_{OUT}=1µF, T_A = 25°C, unless otherwise noted.

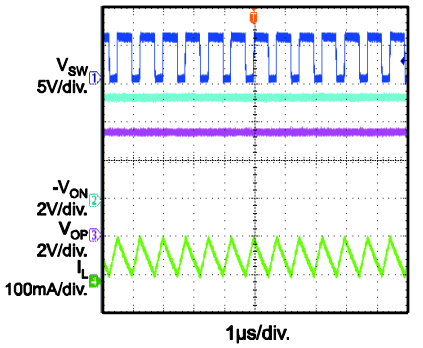
Voltage Tracking @ Asymmetric Load



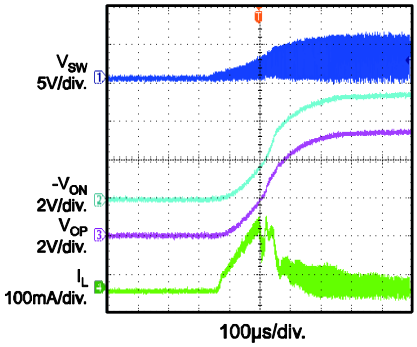
Steady State @ No Load



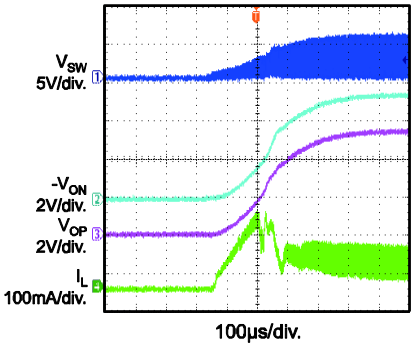
Steady State @ 20mA Symmetric Load



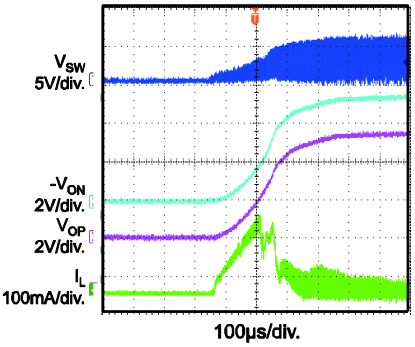
V_{IN} Startup @ No Load



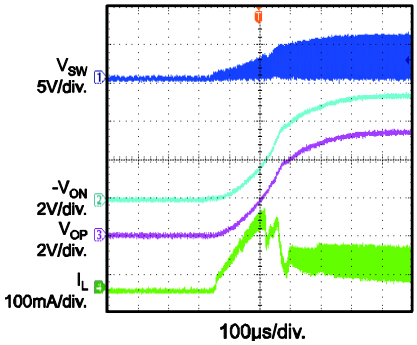
V_{IN} Startup @ 20mA Symmetric Load



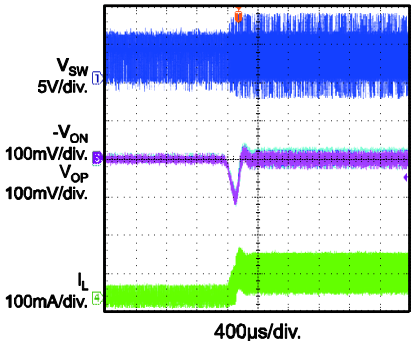
EN Startup @ No Load



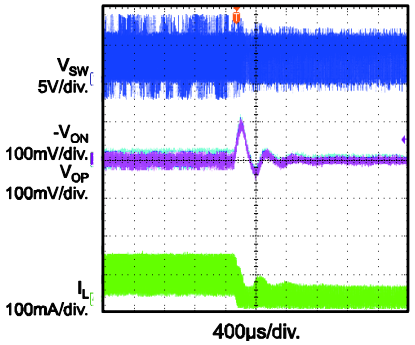
EN Startup @ 20mA Symmetric Load



Load Transient 0->20mA



Load Transient 20mA->0mA



Notes:

(a) Line/Load Regulation: (V_{OP}-V_{OP_AVG})/V_{OP_AVG}*100%.

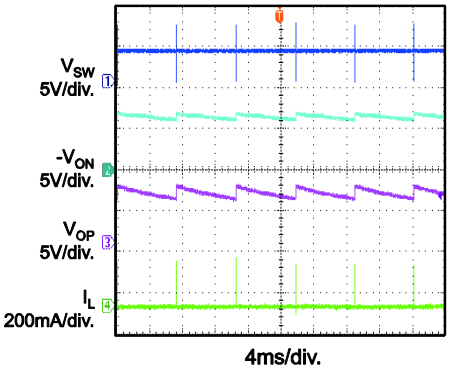
(b) Voltage Tracking: (|VON|-VOP)/VOP*100%.

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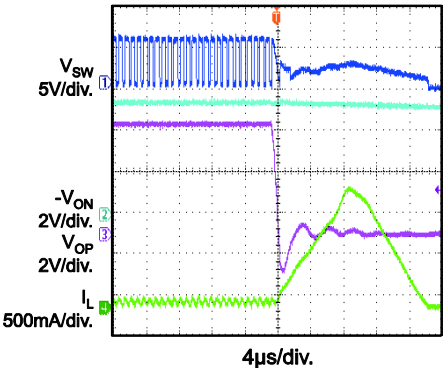
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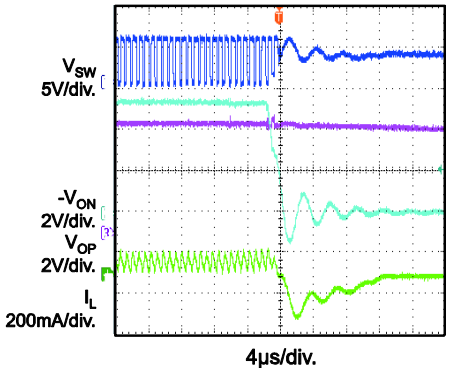
OVP



VOP UVP



VON UVP



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PIN FUNCTIONS

Package Pin #	Name	Description
1	EN	IC Enable Pin. A voltage higher than threshold voltage enables the IC. Disable the IC by pulling this pin to GND.
2	FBP	Positive Output Step-up Converter Feedback Pin.
3	VON	Charge Pump Negative Output Pin.
4	CP2	Negative Output Charge Pump Flying Capacitor Node 2
5	CP1	Negative Output Charge Pump Flying Capacitor Node 1. Connect a flying capacitor between this pin and CP2 pin.
6	GND	Ground Reference Pin.
7	VOP	Step-up Converter Positive Output Pin.
8	SW	Step-up Converter Power Switch Node. Drain of the internal low-side MOSFET. Connect the power inductor between SW and VINP pin.
9	VINP	Input Power Pin for Step-up Power Stage. Internally connected to the source node of internal N-MOSFET.
10	VIN	Input Power Pin. It provides power for internal logic and driver. Must be locally bypassed.

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FUNCTIONAL BLOCK DIAGRAM

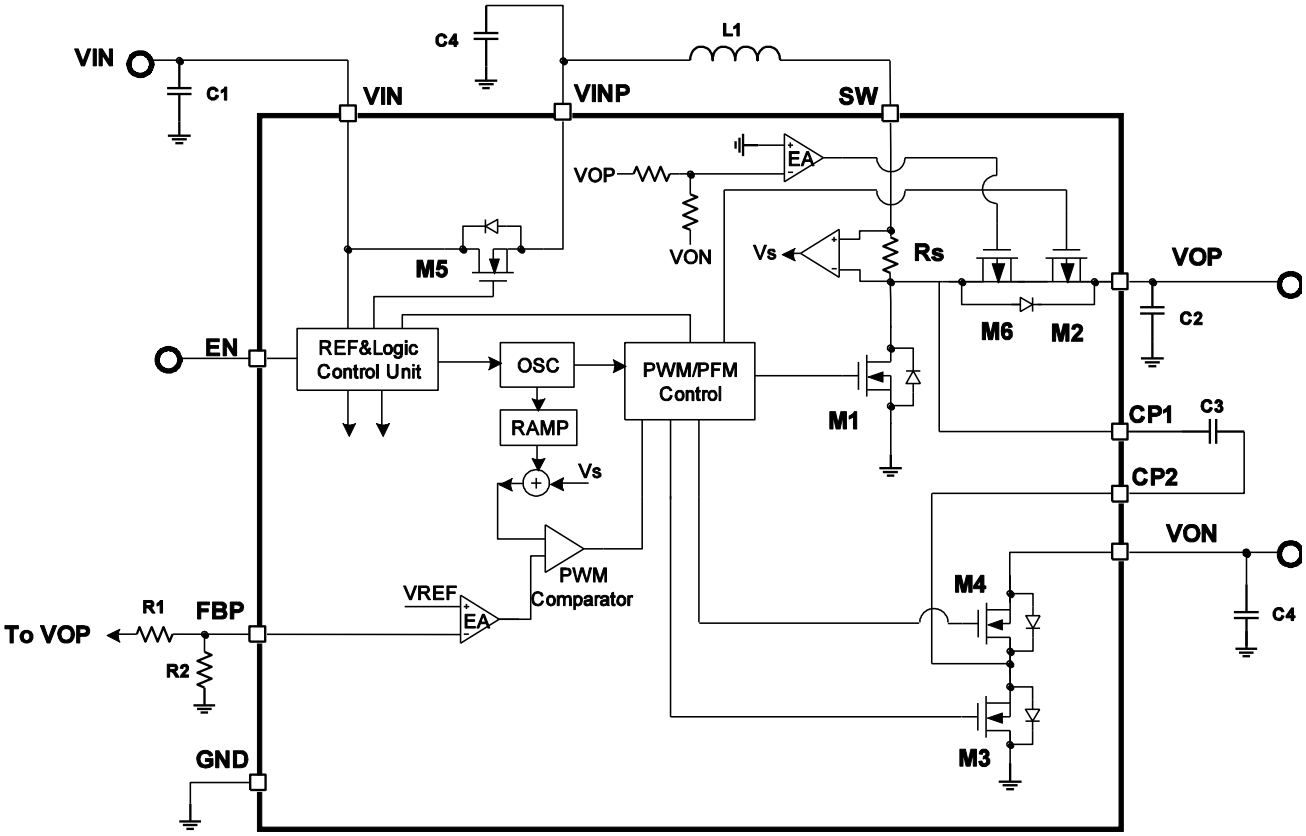


Figure 1: Functional Block Diagram

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OPERATION

Positive Step-up Converter

The MP5610 uses peak-current-mode control step up converter to regulate positive output voltage. The output voltage is accurately set a resistor divider. At the start of each oscillator cycle, the control circuit turns on the low-side MOSFET (M1) and the inductor current stars ramping up. A stabilizing ramp added to the output of the current-sense amplifier, which then feeds into the positive input of the PWM comparator, prevents sub-harmonic oscillations at duty cycles greater than 50%. When the input to the PWM comparator equals the output voltage of the error amplifier, M1 turns off. Then the inductor current flows through the synchronous power MOSFET which forces the inductor current to decrease.

Negative Charge Pump

The negative output is provided by a charge pump which directly draws power from the step-up converter switching node. When the M1 turns on, CP2-to-VON MOSFET (M4) turns on at the same time and then, the energy stored in flying capacitor is transferred to the output capacitor and load. When step-up rectifier MOSFET (M2) turns on, CP2-to-GND MOSFET (M3) turns on at the same time, the flying capacitor is charged from inductor and thus, energy is stored in flying capacitor. The negative output voltage tracks the positive output voltage by well matching the internal MOSFET on resistive. The negative voltage can be estimated as below,

$$V_{ON} = V_{OP} + \frac{I_{OP}}{1-D} * (R_{on_M2} + R_{on_M6}) - \frac{I_{ON}}{1-D} * R_{on_M3} - \frac{I_{ON}}{D} * R_{on_M4} - (I_L + \frac{I_{ON}}{D}) * (R_{on_M1} + R_s)$$

While,

V_{ON} is the negative output voltage,

V_{OP} is the positive output voltage,

I_{ON} is the negative output current,

I_{OP} is the positive output current,

D is the duty cycle of step-up converter,

I_L is the inductor average current,

R_s is the internal sensing resistor value of step-up converter,

R_{ON_M1} is the on resistance of MOSFET M1,

R_{ON_M2} is the on resistance of MOSFET M2,

R_{ON_M3} is the on resistance of MOSFET M3,

R_{ON_M4} is the on resistance of MOSFET M4,

R_{ON_M6} is the on resistance of MOSFET M6,

Enable

When the input voltage is larger than under-voltage-lock-out protection threshold, MP5610 can be enabled by pulling EN pin to higher than 1.2V. Leaving EN pin float or by pulling EN pin down to GND disables MP5610. There is a 1M Ω pulling down resistor from EN pin to GND.

System Startup

When enabled, the input disconnection MOSFET (M5) turns on and its DC current limit ramps up gradually and this function provides two merits,

1) To avoid large inrush current during startup,
2) To provide better voltage tracking starting from 0 between positive and negative output voltage.

After IC enabled, the internal reference starts ramping up linearly to provide linear voltage startup and avoid inrush current. The soft start time from 0 to 600mV is around 1ms.

Voltage Tracking

MP5610 does precise voltage tracking by adjusting the on resistance of PMOS M6 in close loop. If the sum of positive output voltage value and negative output voltage value is larger than 0, the gate driver voltage of M6 increases to increase the on resistance, thus more energy is dropped across M6. If the sum of positive output voltage value and negative output voltage value is lower than 0, the gate driver voltage of M6 reduces to reduces the on resistance, thus less energy is dropped across M6. Note that the minimum on resistance of M6 is 1Ω.

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Output Over-Voltage Protection

MP5610 provides over-voltage protection for step-up converter. If the positive output voltage is larger than 6.1V, IC stops switching and output starts dropping. When the voltage drops lower than OVP recover threshold, IC resumes to normal switching. The hysteresis is 215mV.

Since the negative output voltage is always tracking the positive output voltage, the negative output voltage can also be avoided to over-charging. In some unexpected cases, if the negative output voltage is lower than -6.2V, IC stops switching and output starts dropping. When the voltage drops larger than OVP recover threshold, IC resumes to normal switching. The hysteresis is 165mV.

V_{OP} Under Voltage Protection

After startup, if the output feedback voltage is lower than 52%*V_{REF}, IC stops switching and latches off to avoid any damage. This fault has to be cleared by reset the input power or enable signal. If V_{OP} and GND are shorted before the startup, larger current draws from the input power side and it can be limited by maximum input DC current limit, around 260mA.

V_{ON} Under Voltage Protection

MP5610 provides V_{ON} Under Voltage protection by sensing the negative output voltage. After the startup, if the V_{ON} is lower than 60%*$V_{OP,}$ the IC will stop switching and latch off to avoid any damage. If the V_{ON}-to-GND is shorted before startup, the positive output voltage will not be charged up and thus, the IC will be protected by limiting the input current limit switch.

Input UVLO Protection

To avoid IC operation in low input voltage, MP5610 has input UVLO protection. IC only starts operation when input voltage is larger than input under-voltage-lock-out protection threshold, V_{IN_UVLO}. There is a 260mV hysteresis when input voltage drops.

Over Heat Protection

When MP5610 junction temperature exceeds the thermal protection threshold, IC shuts down and latch off.

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APPLICATION INFORMATION

Setting the Positive Output Voltage

The external resistor divider is used to set the output voltage. Choose the high side feedback resistor R1 to 100k to 200k resistor, the low side feedback resistor R2 can be calculated as below,

$$R2 = \frac{R1}{\frac{V_{OUT}}{0.6} - 1}$$

Selecting the Input Capacitor

The input capacitor reduces the surge current drawn from the input supply and the switching noise from the device. The input capacitor impedance at the switching frequency should be less than the input source impedance to prevent the high-frequency switching current from passing through to the input. Use ceramic capacitors with X5R or X7R dielectrics for their low ESR and small temperature coefficients. For most applications, use a 1μF-to-4.7μF ceramic capacitor.

Selecting the Inductor

The MP5610 requires an inductor to boost its output voltage. A larger value inductor results in less ripple current, lowering both the peak-inductor current and the stress on the internal N-channel MOSFET. However, the larger inductor is physically larger, has a higher series resistance, and a lower saturation current.

Choose an inductor that does not saturate under the worst-case load conditions. Select the minimum inductor value to ensure that the boost converter works in continuous-conduction mode with high efficiency and good EMI performance.
Calculate the required inductance value using the equation:

$$L \geq \frac{\eta \times V_{OUT} \times D \times (1-D)^2}{2 \times f_{SW} \times I_{LOAD}}$$

$$D = 1 - \frac{V_{IN}}{V_{OUT}}$$

Where V_{IN} and V_{OUT} are the input and output voltages, f_{SW} is the switching frequency, I_{LOAD} is the load current, and η is the efficiency.

Selecting the Output Capacitor

The output capacitor keeps the output voltage ripple small and ensures feedback loop stability. The output capacitor impedance must be low at the switching frequency. Ceramic capacitors with X7R dielectrics are recommended for their low ESR characteristics. Selection must also account for the capacitance's dependence on the voltage rating; with a DC bias voltage, the capacitor can lose as much as 50% of its capacitance at its rated voltage rating. Leave a sufficient voltage rating margin when select the component.

Too-low or too-high capacitance will cause loop instability. For most applications, select a capacitor in the range of 1μF to 4.7μF.

Selecting Flying Capacitor

The flying capacitor between CP1 and CP2 is used to transfer energy from step-up converter switching node to negative output. Ceramic capacitors with X7R dielectrics are recommended for their low ESR characteristics. Usually, a 0.1μF to 1μF capacitor can cover most of the applications.

Layout Consideration

Careful attention must be paid to the PCB board layout and components placement. Proper layout of the high frequency switching path is critical to prevent noise and limit electromagnetic interference. The loop consisting of internal low-side MOSFET, synchronous MOSFET and output capacitor contains a high-frequency ripple current—minimize this loop. Place the input and output capacitor should as close to the IC as possible.

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TYPICAL APPLICATION CIRCUITS

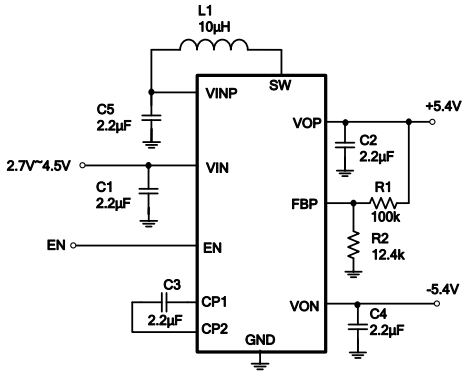
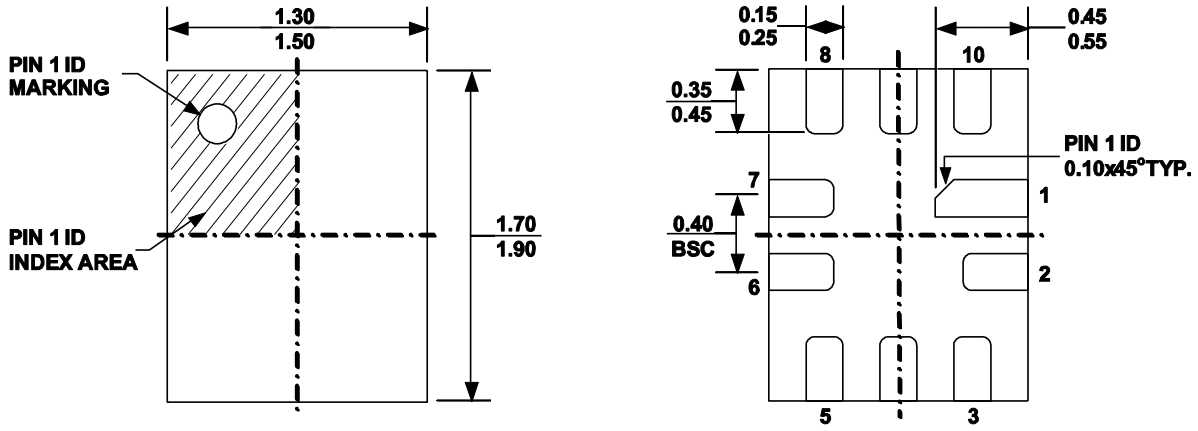


Figure 2: Application Circuit

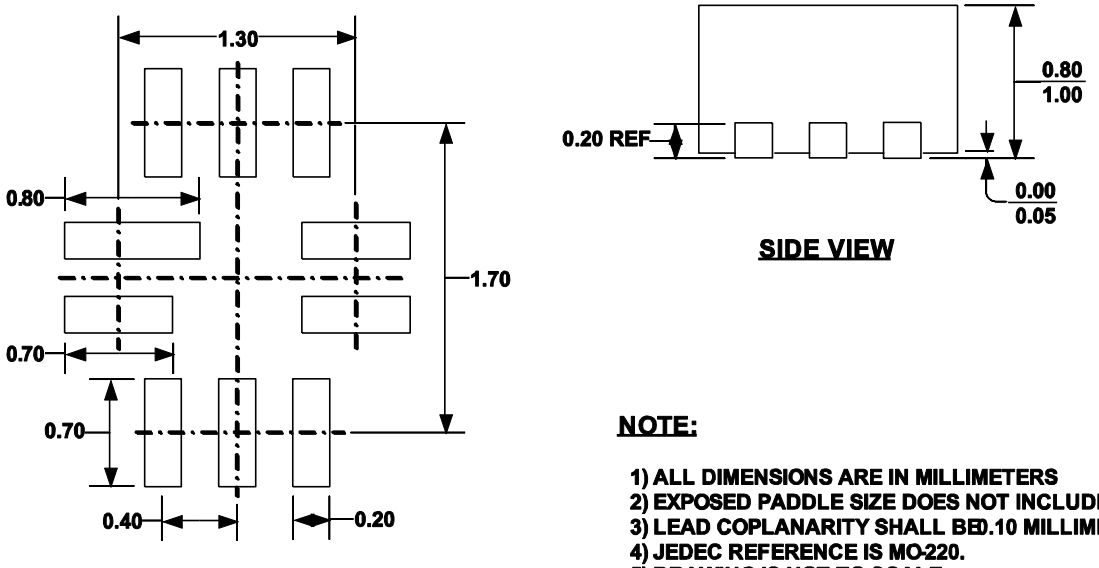
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PACKAGE INFORMATION

QFN-10 (1.4mm×1.8mm)



TOP VIEW **BOTTOM VIEW**



RECOMMENDED LAND PATTERN **SIDE VIEW**

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH
3) LEAD COPLANARITY SHALL BE0.10 MILLIMETER MAX
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE

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