4.3 GHz, Ultrahigh Dynamic Range, Dual Differential Amplifier

Data Sheet

ADL5567

FEATURES

–3 dB bandwidth of 4.3 GHz
High performance (HP), low power (LP), and power down modes
Preset 20 dB gain can be reduced by adding external resistors
Channel to channel gain error: 0.04 dB at 500 MHz
Channel to channel phase error: 0.6° at 500 MHz
Differential or single-ended input to differential output
Internally dc-coupled inputs and outputs
Low noise input stage: 7.4 dB noise figure at 500 MHz
Low broadband distortion for supply = 5 V, HP mode, and 2 V p-p
200 MHz: –94 dBc (HD2), –103 dBc (HD3)
500 MHz: –82 dBc (HD2), –82 dBc (HD3)
IMD3 of –104 dBc at 200 MHz and –90 dBc at 500 MHz
Low single-ended input distortion
Slew rate: 20 V/ns
Maintains low distortion for output common-mode voltage down to 1.25 V
Single-supply operation: 3.3 V or 5 V
Low dc power consumption: 148 mA at 5 V (HP mode), and 80 mA at 3.3 V (LP mode)

APPLICATIONS

Differential ADC drivers
Single-ended to differential conversions
RF/IF gain blocks
SAW filter interfacing

FUNCTIONAL BLOCK DIAGRAM

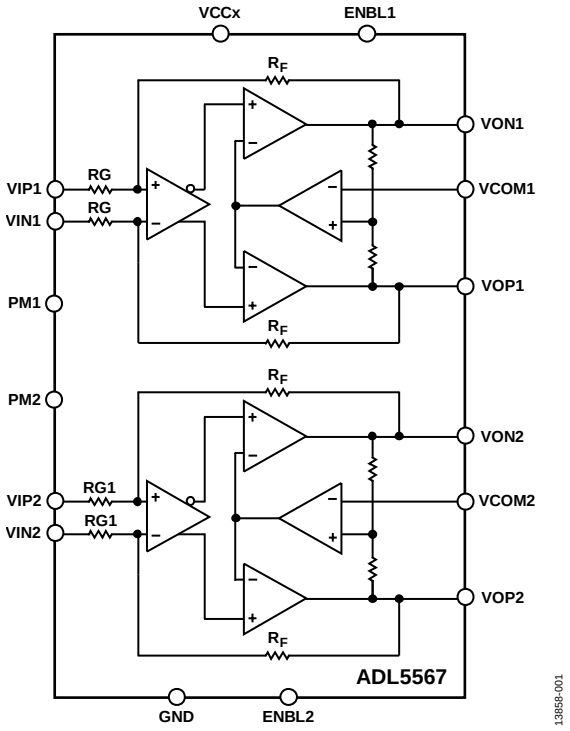


Figure 1.

GENERAL DESCRIPTION

The ADL5567 is a high performance, dual differential amplifier optimized for intermediate frequencies (IF) and dc applications. The amplifier offers a low noise of 1.29 nV/√Hz and excellent distortion performance over a wide frequency range, making it an ideal driver for high speed 16-bit analog-to-digital converters (ADCs). The ADL5567 is ideally suited for use in high performance zero-IF and complex IF receiver designs. In addition, this device has excellent low distortion for single-ended input driver applications.

The ADL5567 provides a gain of 20 dB. For the single-ended input configuration, the gain is reduced to 18 dB. Using two external series resistors for each amplifier expands the gain flexibility of the amplifier and allows for any gain selection from 0 dB to 20 dB for a differential input and 0 dB to 18 dB for a single-ended input. In addition, this device maintains low distortion down to output common-mode levels of 1.25 V, and therefore providing an added capability for driving CMOS ADCs at ac levels up to 2 V p-p.

The quiescent current of the ADL5567 using a 5 V supply is typically 74 mA per amplifier in high performance mode. When disabled, each amplifier consumes only 3.5 mA, and has 58 dB input to output isolation at 100 MHz.

The device is optimized for wideband, low distortion, and low noise operation, giving it unprecedented performance for overall spurious-free dynamic range (SFDR). These attributes, together with its adjustable gain capability, make this device the amplifier of choice for driving a wide variety of ADCs, mixers, pin diode attenuators, SAW filters, and multielement discrete devices.

Fabricated on an Analog Devices, Inc., high speed silicon germanium (SiGe) process, the ADL5567 is supplied in a compact 4 mm × 4 mm, 24-lead LFCSP package and operates over the −40°C to +85°C temperature.

Rev. A Document Feedback
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REVISION HISTORY

8/2018—Rev. 0 to Rev. A

Changes to Gain Adjustment and Interfacing Section ... 17
Updated Outline Dimensions ... 23

7/2016—Revision 0: Initial Version

SPECIFICATIONS

Supply voltage (V_S) = 3.3 V or 5 V, high performance (HP) mode, output common-mode voltage (V_{COM}) = V_S/2, source impedance (RS) = 100 Ω differential, load impedance (RL) = 200 Ω differential, output voltage (V_{OUT}) = 2 V p-p, frequency = 200 MHz, T_A = 25°C, parameters specified for differential input and differential output, signal spacing = 2 MHz for two-tone measurements, unless otherwise noted.

Table 1.

Parameter	Test Conditions/ Comments	V_S = 3.3 V			V_S = 5 V			Unit
		Min	Typ	Max	Min	Typ	Max	
DYNAMIC PERFORMANCE								
−3 dB Bandwidth	V_{OUT} ≤ 0.5 V p-p		4.3			4.3		GHz
Bandwidth, 0.1 dB Flatness	V_{OUT} ≤ 1.0 V p-p		410			420		MHz
Voltage Gain (A_V)								
Differential Input	RL = open		20			20		dB
	RL = 200 Ω differential		19			19		dB
Single-Ended Input	RL = 200 Ω differential		18			18		dB
Gain Accuracy			±0.2			±0.2		dB
Channel to Channel Gain Error	Frequency = 500 MHz, Channel A to Channel B		0.04			0.04		dB
Channel to Channel Phase Error	Frequency = 500 MHz, Channel A to Channel B		0.6			0.6		Degrees
Gain Supply Sensitivity	V_S ± 5%		7.1			13.9		mdB/V
Gain Temperature Sensitivity	T_A = −40°C to +85°C		1.5			1.3		mdB/°C
Slew Rate	Rising, V_{OUT} = 2 V step		18			19		V/ns
	Falling, V_{OUT} = 2 V step		19			20		V/ns
Settling Time	2 V step to 1%		380			380		ps
Overdrive Recovery Time	Differential input voltage step from 2 V to 0 V, for V_{OUT} ≤ ±10 mV		6			4		ns
Reverse Isolation (SDD12)			57			57		dB
Input to Output Isolation When Disabled	100 MHz; ENBLx = low		58			58		dB
Channel to Channel Isolation	Channel A to Channel B		69			69		dB
INPUT/OUTPUT CHARACTERISTICS								
Input Common-Mode Range		1.2		1.8	1.3		3.5	V
Input Resistance								
Differential			100			100		Ω
Single-Ended			91.7			91.7		Ω
Input Capacitance (Single-Ended)			0.25			0.25		pF
Common-Mode Rejection Ratio (CMRR)	Frequency = 500 MHz		48			48		dB
Output Common-Mode Range	VCOM1 and VCOM2 pins	1.25		1.8	1.25		3	V
Output Common-Mode Offset	Referenced to V_{COM} (V_S/2)	−25	±7	+25	−25	±8	+40	mV
Output Common-Mode Drift	T_A = −40°C to +85°C		1.61			1.42		mV/°C
Output Differential Offset Voltage		−20	±8	+20	−20	±8	+20	mV
Output Differential Offset Drift	T_A = −40°C to +85°C		±15			±6		µV/°C
Output Resistance (Differential)			10			10		Ω
Maximum Output Voltage Swing	1 dB compressed		5.4			8.6		V p-p
POWER INTERFACE								
Supply Voltage		3.15	3.3	3.45	4.75	5	5.25	V
Digital Input Voltage								
Logic High (V_{IH})	ENBL1/ENBL2, PM1/PM2	2.1		3.45	2.1		3.45	V
Logic Low (V_{IL})		0		1.0	0		1.0	V
ENBL1/ENBL2 Input Current	ENBLx = 3 V		−7			−7		µA
	ENBLx = 0 V		−70			−70		µA
PM1/PM2 Input Current	PMx = 3 V		62			62		µA
	PMx = 0 V		−0.1			−0.1		µA

Parameter	Test Conditions/ Comments	V_S = 3.3 V Min	Typ	Max	V_S = 5 V Min	Typ	Max	Unit
Supply Current (I_{SUPPLY})	Total for two channels							
High Performance Mode	ENBLx = high, PMx = low		138	150		148	160	mA
Low Power Mode	ENBLx = high, PMx = high		80			85		mA
Disabled (Power Down)	ENBLx = low, PMx = don't care		7			9		mA
NOISE/HARMONIC PERFORMANCE								
10 MHz								
Second Harmonic Distortion (HD2)			−88			−93		dBc
Third Harmonic Distortion (HD3)			−90			−94		dBc
Output Third-Order Intercept (OIP3)			42.6			46.3		dBm
Third-Order Intermodulation Distortion (IMD3)			−89			−97		dBc
Output Second-Order Intercept (OIP2)			90.2			90.9		dBm
Second-Order Intermodulation Distortion (IMD2)			−92			−93		dBc
Output 1 dB Compression Point (OP1dB)			12.8			16.6		dBm
Noise Figure (NF)			6.7			6.8		dB
Noise Spectral Density (NSD), Referred to Input (RTI)[1]			1.21			1.23		nV/√Hz
100 MHz								
HD2			−88			−94		dBc
HD3			−89			−101		dBc
OIP3			42.5			46.5		dBm
IMD3			−89			−97		dBc
OIP2			84.5			94.2		dBm
IMD2			−87			−96		dBc
OP1dB			13.0			16.9		dBm
NF			6.8			6.8		dB
NSD, RTI[1]			1.23			1.23		nV/√Hz
200 MHz								
HD2			−88			−94		dBc
HD3			−86			−103		dBc
OIP3			43.5			49.8		dBm
IMD3			−91			−104		dBc
OIP2			80.7			88.8		dBm
IMD2			−83			−91		dBc
OP1dB, Referred to Output (RTO)			12.6			16.7		dBm
NF			7.0			7.1		dB
NSD, RTI			1.27			1.29		nV/√Hz
500 MHz[2]								
HD2			−77			−82		dBc
HD3			−70			−82		dBc
OIP3			37			42.8		dBm
IMD3			−78			−90		dBc
OIP2			76.7			82.0		dBm
IMD2			−79			−84		dBc
NF			7.3			7.4		dB
NSD, RTI			1.32			1.34		nV/√Hz

Parameter	Test Conditions/ Comments	V_S = 3.3 V Min	Typ	Max	V_S = 5 V Min	Typ	Max	Unit
1000 MHz[2]								
HD2			−59			−70		dBc
HD3			−49			−55		dBc
OIP3			29			32		dBm
IMD3			−62			−68		dBc
OIP2			62.1			65.4		dBm
IMD2			−64			−67		dBc
NF			8.1			8.2		dB
NSD, RTI			1.48			1.50		nV/√Hz
1500 MHz[2]								
HD2			−44			−50		dBc
HD3			−47			−51		dBc
OIP3			21.3			25.3		dBm
IMD3			−47			−55		dBc
OIP2			50.2			51.8		dBm
IMD2			−52			−54		dBc
NF			8.3			8.4		dB
NSD, RTI			1.52			1.54		nV/√Hz
2000 MHz[2]								
HD2			−49			−50		dBc
HD3			−44			−44		dBc
OIP3			17.5			19		dBm
IMD3			−39			−42		dBc
OIP2			43.3			51.4		dBm
IMD2			−45			−53		dBc
NF			9.6			9.7		dB
NSD, RTI			1.8			1.83		nV/√Hz

[1] NSD RTI is calculated from NF, as follows:

$$NSD\ (RTI) = \tfrac{1}{2} \times \sqrt{4kT \times 10^{NF/10} - 1 \times R_{IN}}$$

where:
k is Boltzmann's constant, which equals 1.381×10^{-23} J/K.
T is the standard absoltute temperature for evaluating noise figure, which equals 290 K.
R_{IN} is the differential input impedance of each amplifier, which equals 100 Ω.

[2] OP1dB is not specified above 500 MHz, as the output level exceeds absolute maximum level allowed (see Table 2).

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Output Voltage Swing × Bandwidth Product	
High Performance Mode	5 V-GHz
Low Power Mode	3 V-GHz
Supply Voltage (V_S) at VCC1, VCC2	5.25 V
VIPx, VINx	V_S + 0.5 V
$\pm I_{OUT}$ Maximum (VIPx and VINx Pins)	±30 mA
Internal Power Dissipation	900 mW
Maximum Junction Temperature	135°C
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment.

Careful attention to PCB thermal design is required.

Table 3. Thermal Resistance

Package Type	θ_{JA}[1]	θ_{JC}[2]	Unit
CP-24-19	56	2.2	°C/W

[1] Measured on Analog Devices evaluation board.
[2] Based on simulation with JEDEC standard JESD51.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

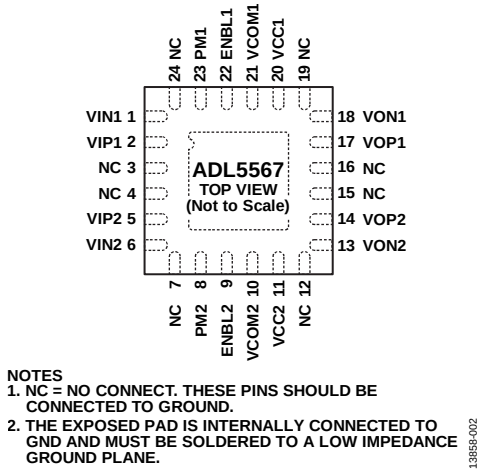


Figure 2. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	VIN1	Negative Side of Balanced Differential Inputs for Amplifier 1. This pin is biased to $V_{VCC1}/2$, and is typically ac-coupled.
2	VIP1	Positive Side of Balanced Differential Inputs for Amplifier 1. This pin is biased to $V_{VCC1}/2$, and is typically ac-coupled.
3, 4, 7, 12, 15, 16, 19, 24	NC	No Functional Connection. Connect these pins to ground.
5	VIP2	Positive Side of Balanced Differential Inputs for Amplifier 2. This pin is biased to $V_{VCC2}/2$, and is typically ac-coupled.
6	VIN2	Negative Side of Balanced Differential Inputs for Amplifier 2. This pin is biased to $V_{VCC2}/2$, and is typically ac-coupled.
8	PM2	Power Mode Control for Amplifier 2. This pin is internally pulled down to GND through a 30 kΩ resistor. A logic low on this pin sets the device to high performance mode, and a logic high ($2.1\ V < V_{PM2} < 3.3\ V$) sets the device to low power mode.
9	ENBL2	Enable for Amplifier 2. This pin is internally pulled up to about 2.8 V. A logic high on this pin ($2.1\ V < V_{ENBL2} < 3.3\ V$) enables the device.
10	VCOM2	Common-Mode Voltage. A voltage applied to this pin sets the common-mode voltage of the inputs and outputs of Amplifier 2. If left open, $V_{VCOM2} = V_{CC2}/2$. Decouple this pin to ground with a 0.1 µF capacitor.
11	VCC2	Positive Supply for Amplifier 2.
13	VON2	Negative Side of Balanced Differential Outputs for Amplifier 2. This pin is biased to V_{VCOM2}, and is typically ac-coupled.
14	VOP2	Positive Side of Balanced Differential Outputs for Amplifier 2. This pin is biased to V_{VCOM2}, and is typically ac-coupled.
17	VOP1	Positive Side of Balanced Differential Outputs for Amplifier 1. This pin is biased to V_{VCOM1}, and is typically ac-coupled.
18	VON1	Negative Side of Balanced Differential Outputs for Amplifier 1. This pin is biased to V_{VCOM1}, and is typically ac-coupled.
20	VCC1	Positive Supply for Amplifier 1.
21	VCOM1	Common-Mode Voltage. A voltage applied to this pin sets the common-mode voltage of the inputs and outputs of Amplifier 1. If left open, $V_{VCOM1} = V_{CC1}/2$. Decouple this pin ground with a 0.1 µF capacitor.
22	ENBL1	Enable for Amplifier 1. This pin is internally pulled up to about 2.8 V. A logic high on this pin ($2.1\ V < V_{ENBL1} < 3.45\ V$) enables the device.
23	PM1	Power Mode Control for Amplifier 1. This pin is internally pulled down to GND through a 30 kΩ resistor. A logic low on this pin sets the device to high performance mode, and a logic high ($2.1\ V < V_{PM1} < 3.45\ V$) sets the device to low power mode.
EP	GND	Exposed Pad. The exposed pad is internally connected to GND and must be soldered to a low impedance ground plane.

TYPICAL PERFORMANCE CHARACTERISTICS

V_S = 3.3 V or 5 V, HP mode, V_{COM} = V_S/2, R_S = 100 Ω differential, RL = 200 Ω differential, V_{OUT} = 2 V p-p, frequency = 200 MHz, T_A = 25°C, parameters specified for differential input and differential output, signal spacing = 2 MHz for two-tone measurements, unless otherwise noted.

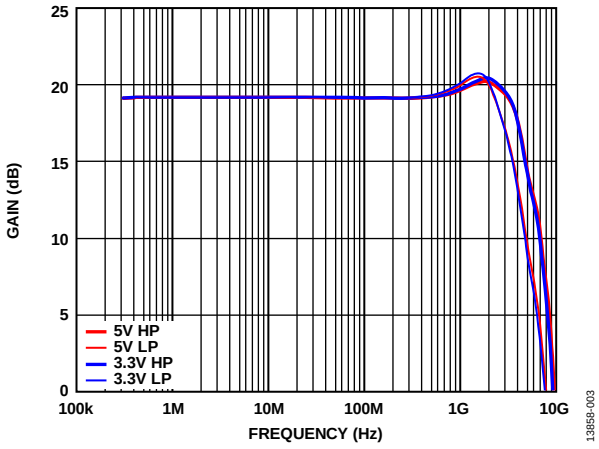


Figure 3. Gain vs. Frequency over Power Modes

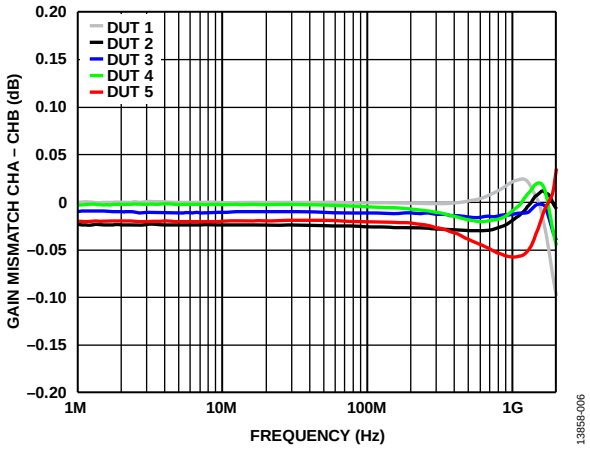


Figure 6. Channel to Channel Gain Mismatch CHA – CHB vs. Frequency

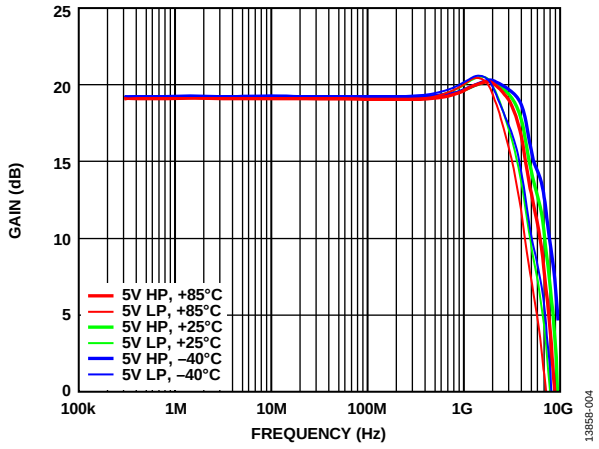


Figure 4. Gain vs. Frequency over Temperature at V_S = 5 V

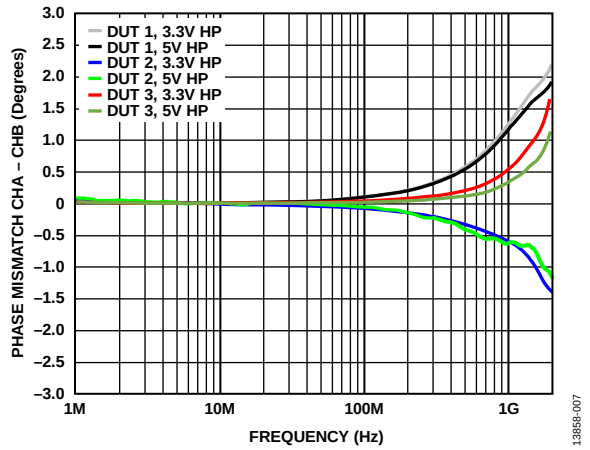


Figure 7. Channel to Channel Phase Mismatch CHA – CHB vs. Frequency

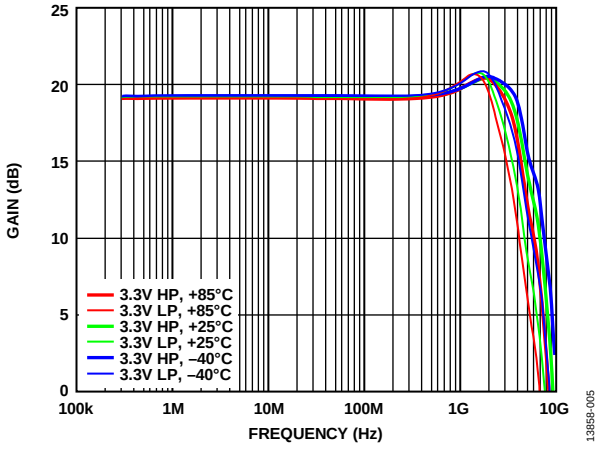


Figure 5. Gain vs. Frequency over Temperature at V_S = 3.3 V

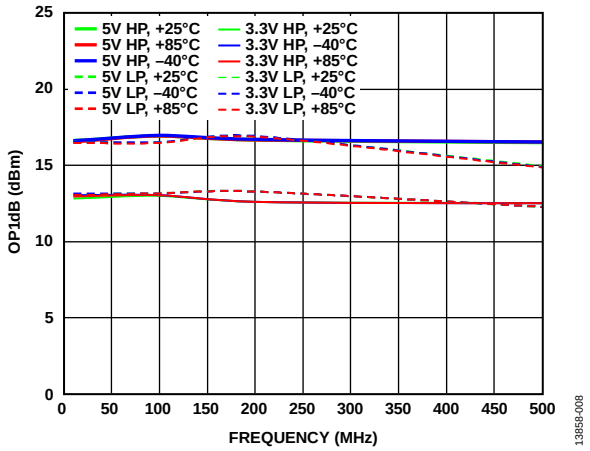


Figure 8. OP1dB vs. Frequency over Temperature

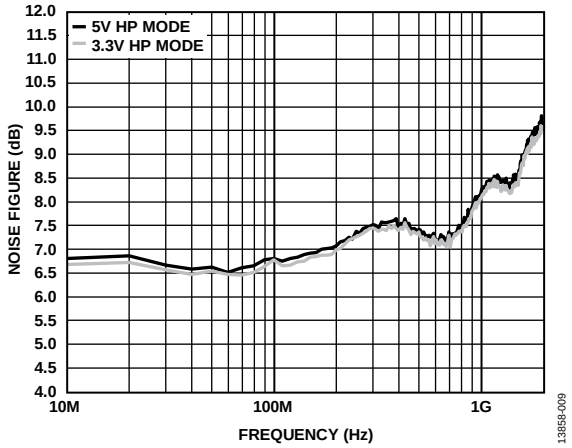


Figure 9. Noise Figure vs. Frequency over V_S, HP Mode

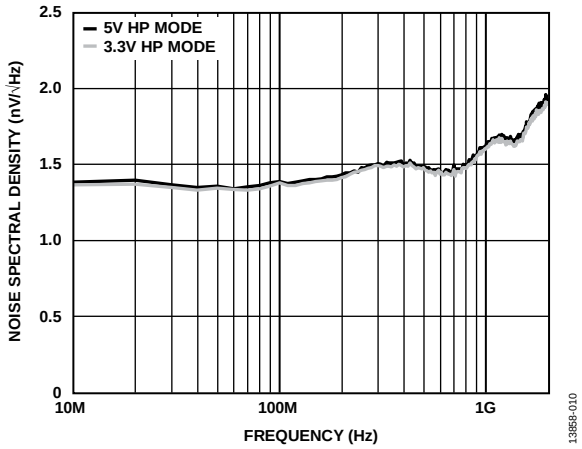


Figure 10. Noise Spectral Density (NSD) vs. Frequency over V_S, HP Mode

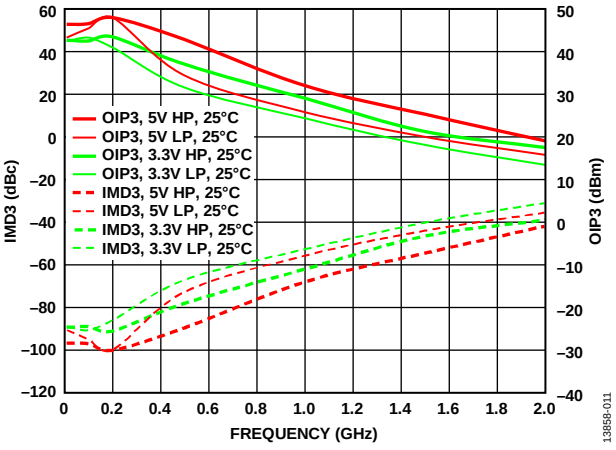


Figure 11. IMD3 and OIP3 vs. Frequency over Supply Voltage and Power Modes

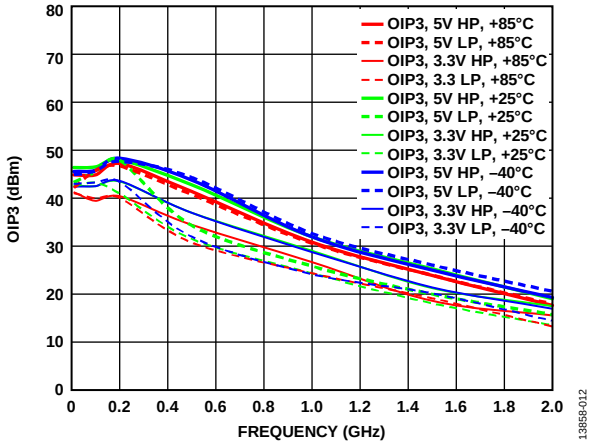


Figure 12. OIP3 vs. Frequency over Temperature, Supply Voltage, and Power Modes

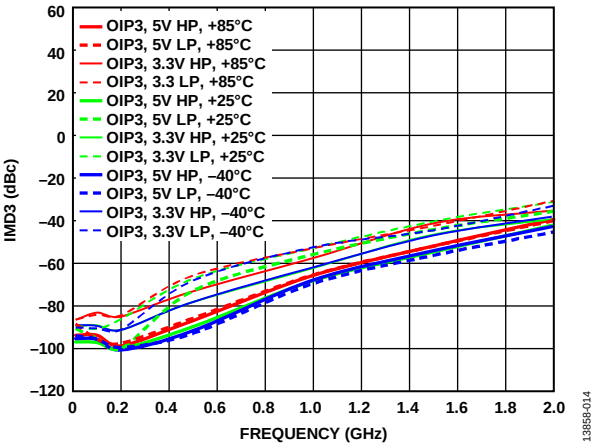


Figure 13. IMD3 vs. Frequency over Temperature, Supply Voltage, and Power Modes

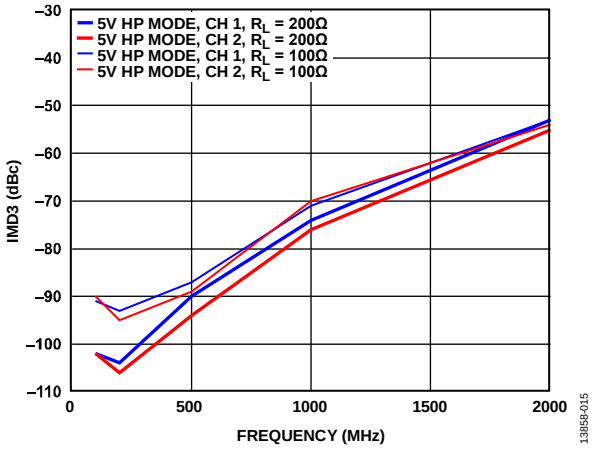


Figure 14. IMD3 vs. Frequency for R_L = 100 Ω

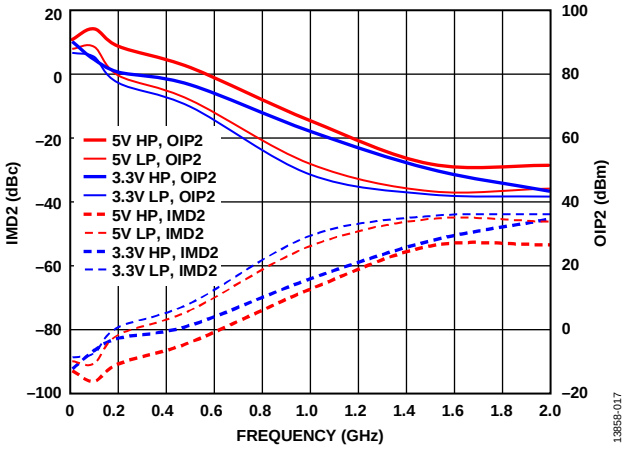


Figure 15. IMD2 and OIP2 vs. Frequency over Supply Voltage and Power Modes

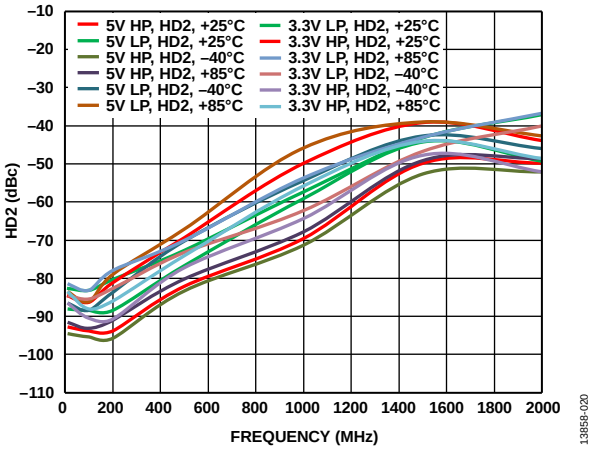


Figure 18. HD2 vs. Frequency over Temperature, Supply Voltage, and Power Modes

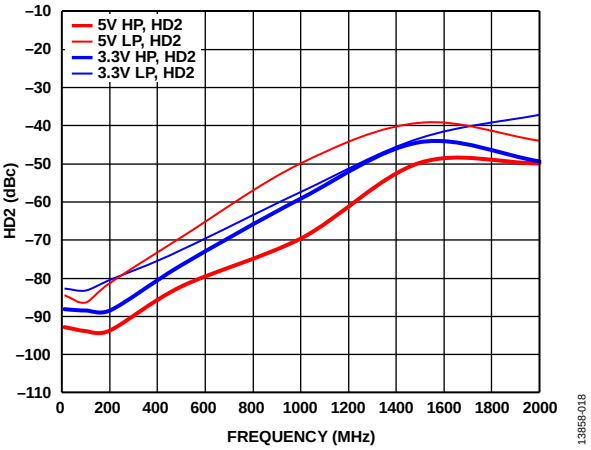


Figure 16. HD2 vs. Frequency over Supply Voltage and Power Modes

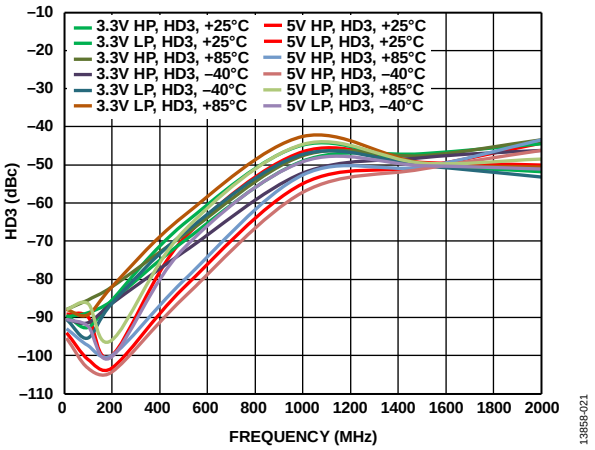


Figure 19. HD3 vs. Frequency over Temperature, Supply Voltage, and Power Modes

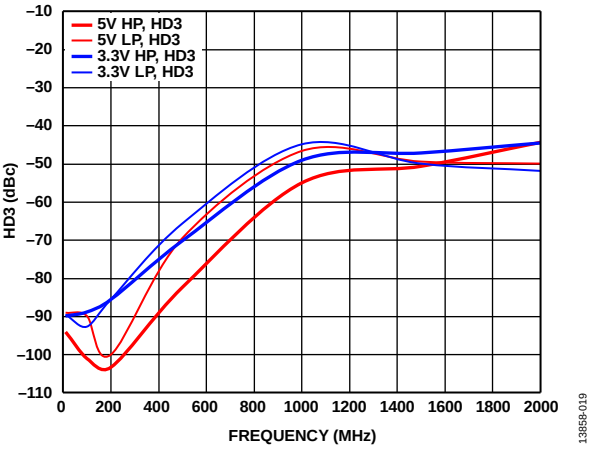


Figure 17. HD3 vs. Frequency over Supply Voltage and Power Modes

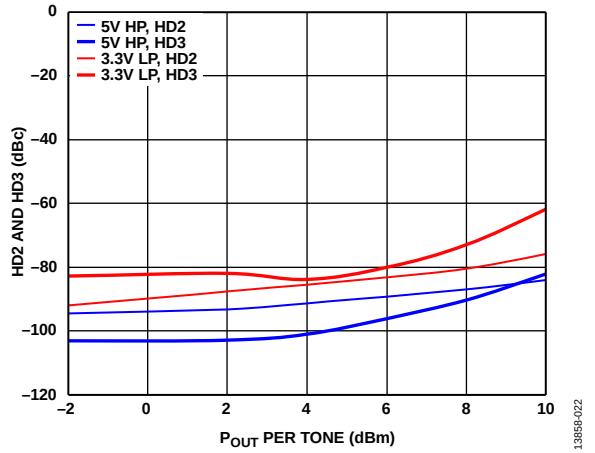


Figure 20. HD2 and HD3 vs. Output Power (P_{OUT}) per Tone, 3.3 V LP Mode and 5 V HP Mode

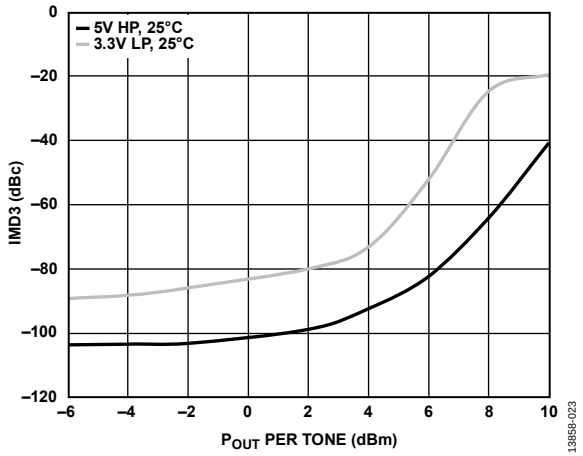


Figure 21. IMD3 vs. P_{OUT} per Tone for 3.3 V LP Mode and 5 V HP Modes

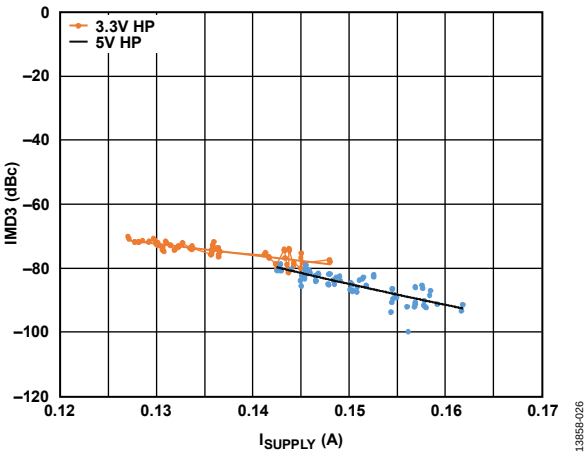


Figure 24. IMD3 vs. Supply Current (I_{SUPPLY}) Distribution, 200 MHz, V_S = 5 V

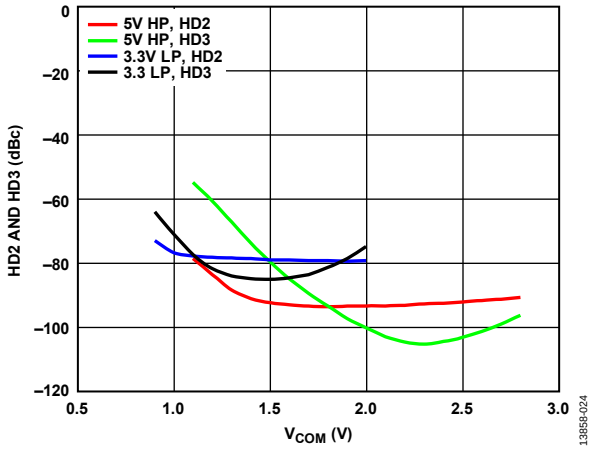


Figure 22. Harmonic Distortion (HD2 and HD3) vs. V_{COM} for V_S = 5 V, High Performance Mode and V_S = 3.3 V, Low Power Mode

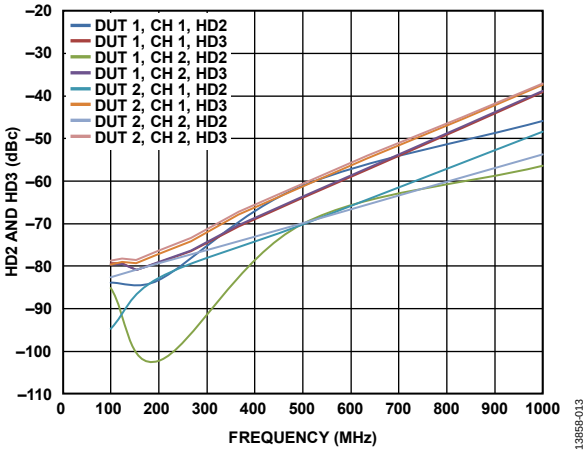


Figure 25. HD2 and HD3 vs. Frequency for V_S = 2.8 V, LP Mode (Two Devices)

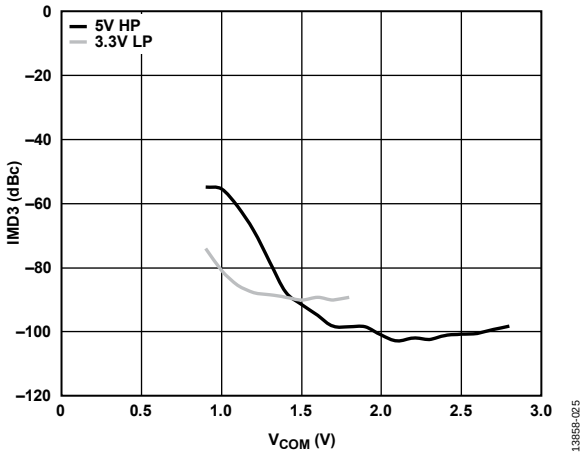


Figure 23. IMD3 vs. V_{COM} for 3.3 V LP Mode and 5 V HP Mode

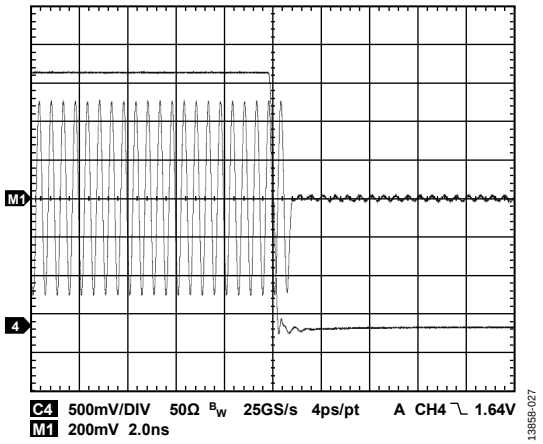


Figure 26. Disable Time Response, V_S = 3.3 V, Low Power Mode

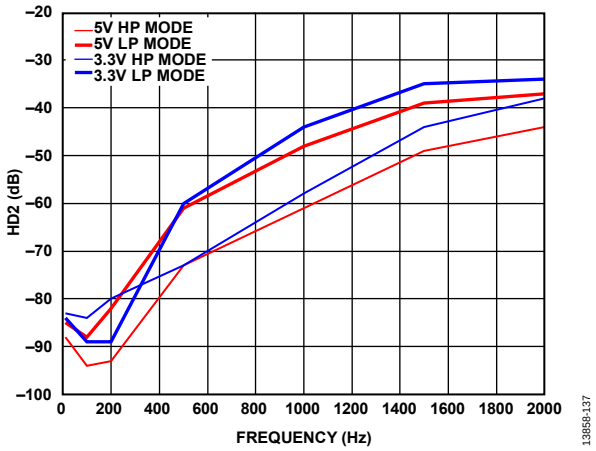


Figure 27. HD2 vs. Frequency for Single-Ended Input Circuit

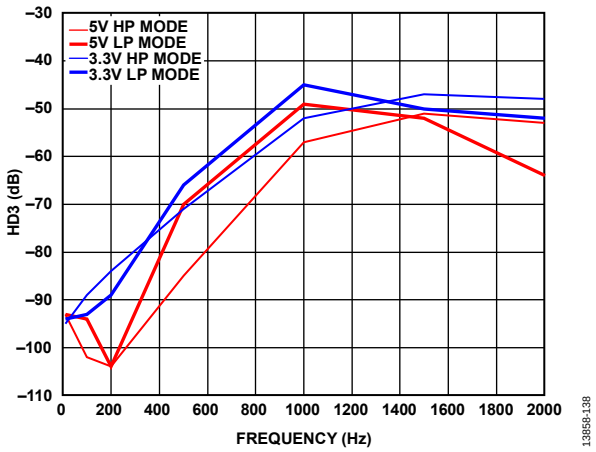


Figure 28. HD3 vs. Frequency for Single-Ended Input Circuit

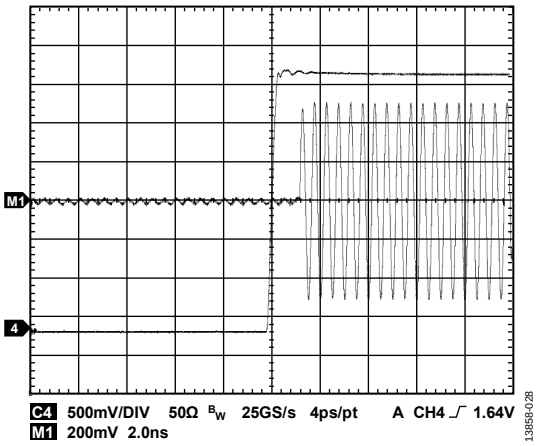


Figure 29. Enable Time Response, V_S = 3.3 V, Low Power Mode

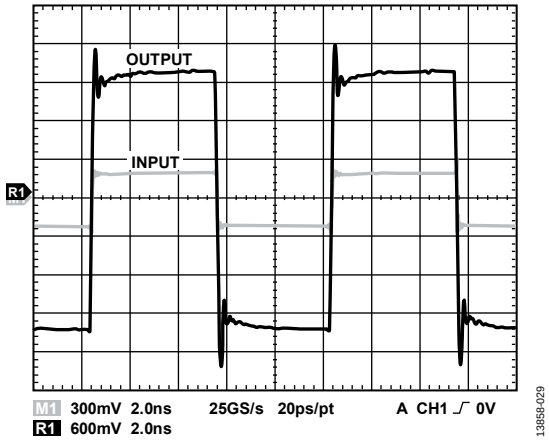


Figure 30. Large Signal Pulse Response, V_{OUT} = 4 V p-p, V_S = 3.3 V

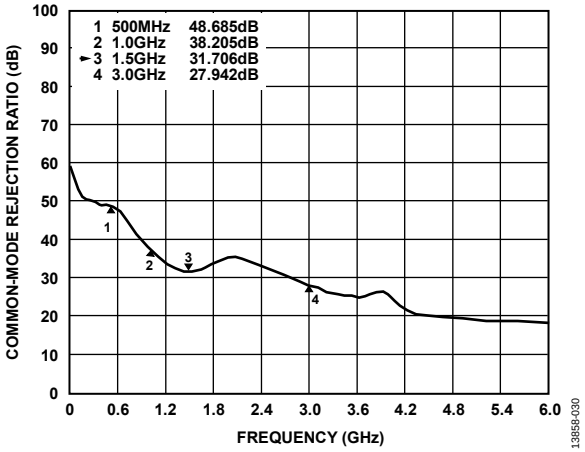


Figure 31. Common-Mode Rejection Ratio (CMRR) vs. Frequency, V_S = 5 V, High Performance Mode

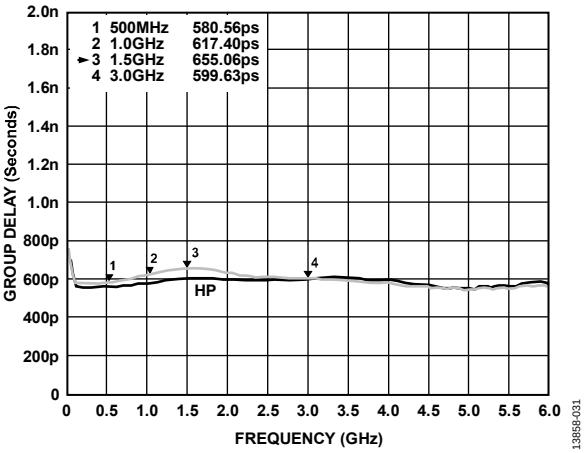


Figure 32. Group Delay vs. Frequency, V_S = 5 V, High Performance (HP) and Low Power (LP) Modes

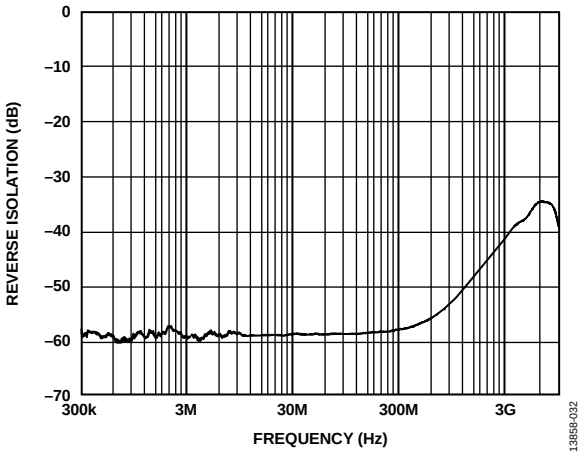


Figure 33. Reverse Isolation (SDD12) vs. Frequency

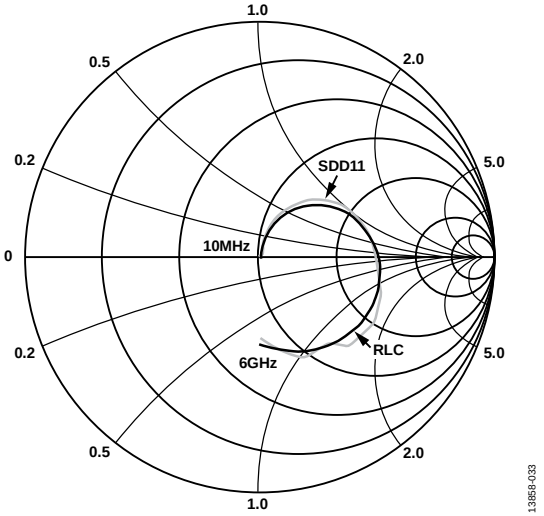


Figure 34. Differential Input Equivalent RLC Network vs. SDD11 (Z_O = 100 Ω)

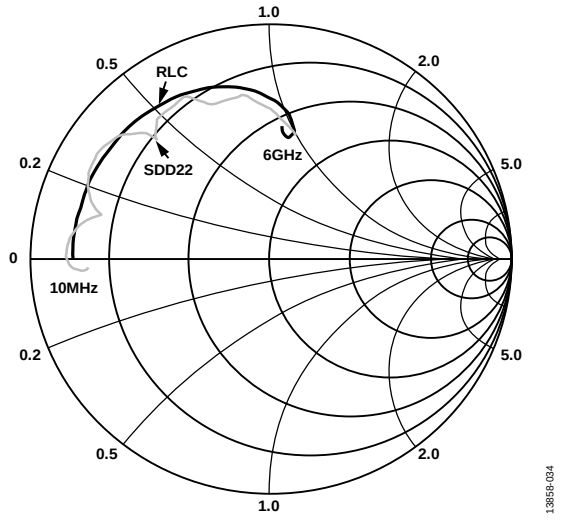


Figure 35. Differential Output Equivalent RLC Network vs. SDD22 (Z_O = 100 Ω)

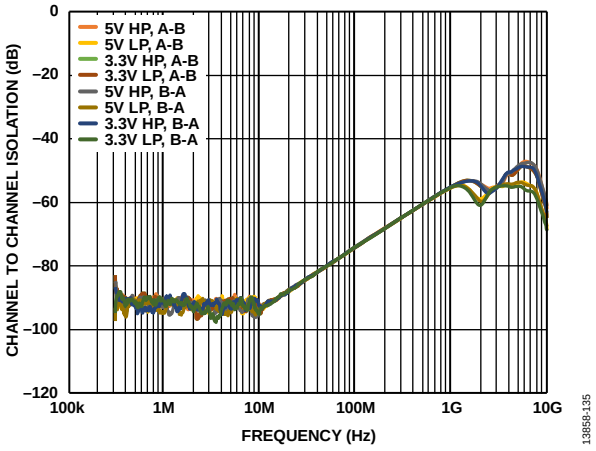


Figure 36. Channel to Channel Isolation vs. Frequency

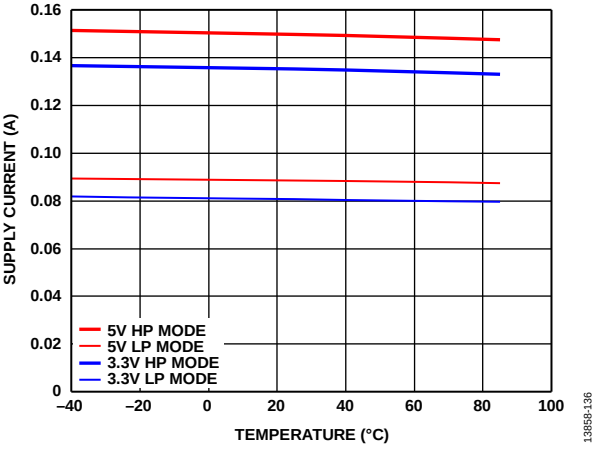


Figure 37. Supply Current vs. Temperature over V_S and Power Modes

THEORY OF OPERATION

The ADL5567 is a high gain, fully differential dual amplifier/ADC driver that operates on a single power supply voltage (V_S) of 3.3 V or 5 V. Internal resistors preset the gain to 20 dB, and external resistors can be added to reduce this gain. The −3 dB bandwidth is 4.3 GHz, and it has a differential input impedance of 100 Ω. It has a differential output impedance of 10 Ω and an operating output common-mode voltage range of 1.25 V to 3 V with 5 V supply.

The ADL5567 is composed of a pair of fully differential amplifiers with on-chip feedback and feedforward resistors. The gain is fixed at 20 dB, but it can be reduced by adding two resistors in series with the two inputs (see the Gain Adjustment and Interfacing section). The amplifier provides a high differential open-loop gain and has an output common-mode circuit that enables the user to change the output common-mode voltage by applying a voltage to a VCOMx pin.

Each amplifier provides superior low distortion for frequencies near dc to beyond 500 MHz, with low noise and low power consumption. The low distortion and noise are realized with a 3.3 V power supply at 140 mA. This amplifier achieves an IMD3 of −104 dBc at 200 MHz, and −90 dBc IMD3 at 500 MHz for 2 V p-p operation. In addition, the ADL5567 can deliver 5 V p-p operation under heavy loads. The internal gain is set at 20 dB, and the device has a noise figure of 7.1 dB and a RTI voltage NSD of 1.29 nV/√Hz at 200 MHz. When comparing noise figure and distortion performance, this amplifier delivers the best in category spurious-free dynamic range (SFDR).

The ADL5567 is very flexible in terms of input/output coupling. It can be ac-coupled or dc-couplied. For dc coupling, the output common-mode voltage can be adjusted (using the VCOMx pins) from 1.25 V to 1.8 V for V_S at 3.3 V, and up to 3 V with V_S at 5 V.

The distortion performance as a function of common-mode voltage is shown in Figure 22 and Figure 23. Note that the input common-mode voltage follows the output common-mode voltage when at the inputs are ac-coupled.

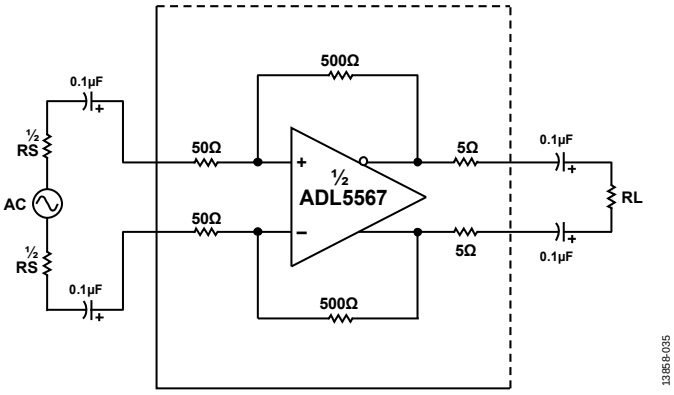


Figure 38. Basic Structure

For dc-coupled inputs, the input common-mode voltage must stay between 1.2 V and 1.8 V for a 3.3 V supply and 1.3 V to 3.5 V for a 5 V supply. Note again that for ac-coupled applications with series capacitors at the inputs, as shown in Figure 38, the input common-mode level is set to be the same as the voltage at VCOMx.

Due to the wide input common-mode range, this device can easily be dc-coupled to many types of mixers, demodulators, and amplifiers. Forcing a higher input common-mode level does not affect the output common-mode level in dc-coupled operations. If the outputs are ac-coupled, no external VCOMx voltage adjustment is required because the amplifier output common-mode level is set to $V_S/2$.

APPLICATIONS INFORMATION

BASIC CONNECTIONS

Figure 39 shows the basic connections for operating the ADL5567. Apply a voltage between 3 V and 5 V to the VCC1 and VCC2 pins through a 5.1 nH inductor and decouple the supply side of the inductor with at least one low inductance, 0.1 µF surface-mount ceramic capacitor. This inductor, together with the internal capacitance at the VCCx pins, results in a two-pole, low-pass network and reduces the noise from the power supply.

Decouple the VCOM1 and VCOM2 pins (Pin 21 and Pin 10) using a 0.1 µF capacitor. The ENBL1 and ENBL2 pins (Pin 22 and Pin 9) are tied to logic high, respectively, to enable each amplifier. A differential signal is applied to Amplifier 1 through Pin 1 (VIN1) and Pin 2 (VIP1) and to Amplifier 2 through Pin 5 (VIP2) and Pin 6 (VIN2). Each amplifier has a gain of 20 dB.

The Amplifier 1 input pins, Pin 1 (VIN1) and Pin 2 (VIP1), and output pins, Pin 18 (VON1) and Pin 17 (VOP1), are biased by applying a voltage to Pin 21 (VCOM1). If VCOM1 is left open, VCOM1 equals ½ of V_S. The Amplifier 2 input pins, Pin 5 (VIP2) and Pin 6 (VIN2), and the output pins, Pin 13 (VON2) and Pin 14 (VOP2), are biased by applying a voltage to VCOM2. If VCOM2 is left open, VCOM2 equals ½ of V_S.

The ADL5567 can be ac-coupled as shown in Figure 39, or can be dc-coupled if within the specified input and output common-mode voltage ranges. Pulling the ENBL1/ENBL2 pins low puts the ADL5567 in sleep mode, reducing the current consumption to 7 mA at ambient temperature.

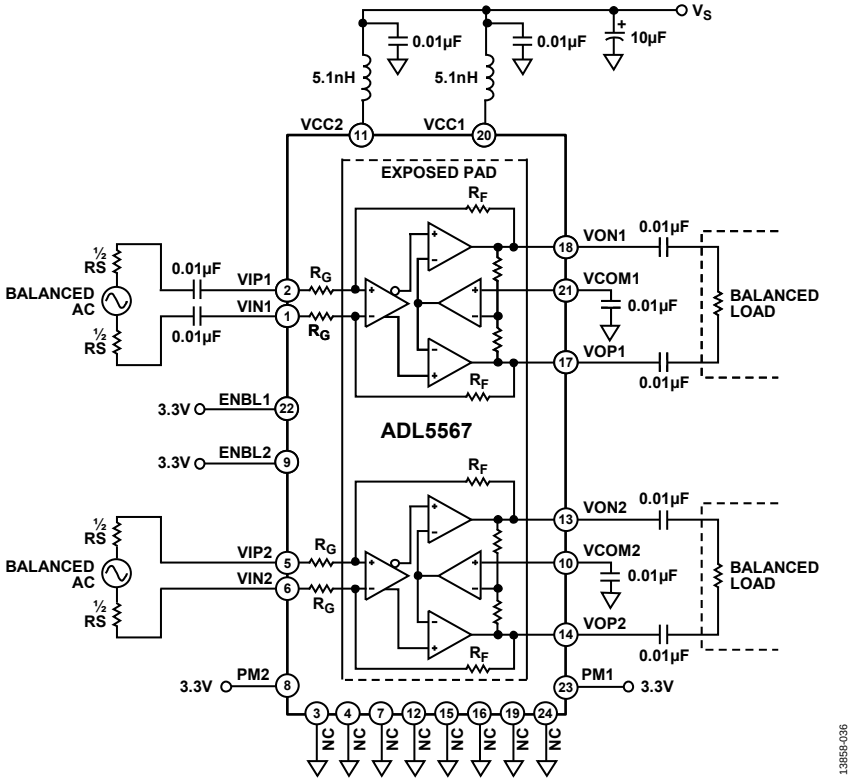


Figure 39. Basic Connections

INPUT AND OUTPUT INTERFACING

The ADL5567 can be configured as a differential input to differential output driver, as shown in Figure 40. The 50 Ω resistors, R1 and R2, combined with the input balun, provide a 50 Ω input match for the 100 Ω input impedance. The input and output 0.1 µF capacitors isolate the $V_{CCX}/2$ bias from the source and balanced load. The load equals 200 Ω to provide the expected ac performance (see the Specifications section).

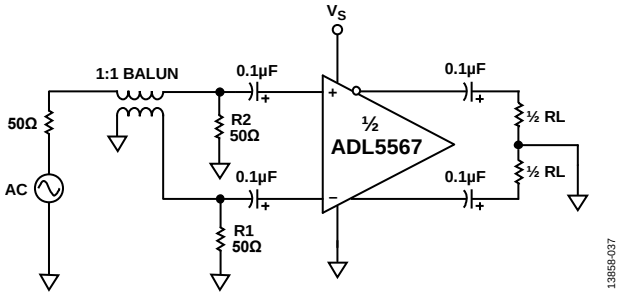


Figure 40. Differential Input to Differential Output Configuration

The differential gain of the ADL5567 is dependent on the source impedance and load, as shown in Figure 41. The differential gain (A_V) can be determined by

$$A_V = \frac{500}{50} \times \frac{RL}{10 + RL} \quad (1)$$

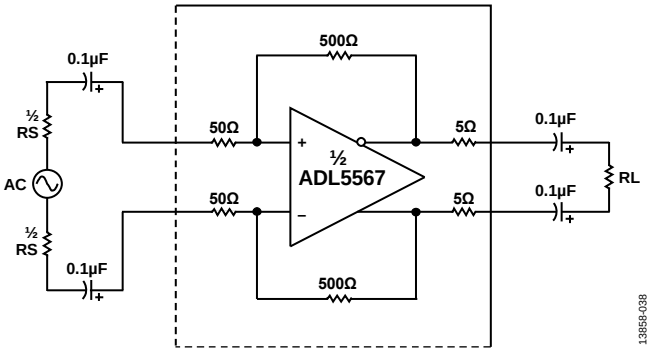


Figure 41. Differential Input Loading Circuit

Single-Ended Input to Differential Output

The ADL5567 can also be configured in a single-ended input to differential output driver, as shown in Figure 42. In this configuration, the gain of the device is reduced due to the application of the signal to only one side of the amplifier. The input and output 0.1 µF capacitors isolate the $V_{CCX}/2$ bias from the source and the balanced load.

The single-ended circuit configuration can be accomplished in three steps (see Figure 42), assuming a 50 Ω RS source. First, calculate the input impedance (R_{IN}) of the amplifier using the following formula:

$$R_{IN} = \frac{RG}{1 - \left(\frac{RF}{2 \times (RG + RF)} \right)} \quad (2)$$

Thus, R_{IN} = 91.7 Ω.

The next step is to calculate the termination of Resistor R2 (see Figure 42). Because RS must be equal to the parallel equivalent resistance of R2 and R_{IN},

$$RS = \frac{R2 \times R_{IN}}{R2 + R_{IN}}$$

Thus,

$$R2 = R_{IN} \times RS / (R_{IN} - RS) \quad (3)$$

When RS = 50 Ω and R_{IN} = 91.7 Ω, R2 = 109 Ω.

The last step is to calculate the gain path rebalancing resistor, R1 (see Figure 42), using the following formula:

$$R1 = \frac{RS \times R2}{RS + R2}$$

Thus, R1 = 34.0 Ω.

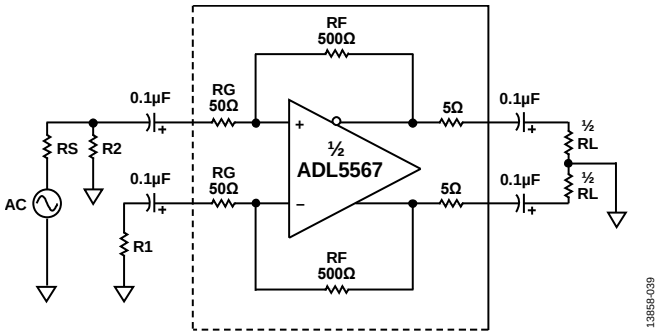


Figure 42. Single-Ended Input to Differential Output Configuration

See the AN-0990 Application Note for more information on terminating single-ended inputs. The single-ended gain configuration of the ADL5567 is dependent on the source impedance and load, as shown in Figure 43.

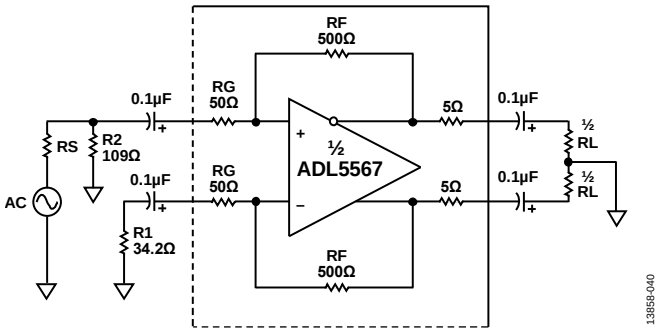


Figure 43. Single-Ended Input Loading Circuit

Determine the single-ended gain (A_{V1}) using the following two equations:

$$R_{MATCH} = \frac{R2 \times R_{IN}}{R2 + R_{IN}} \quad (4)$$

where R_{MATCH} is the input resistance value that matches R_S, calculated as follows:

$$A_{V1} = \frac{500}{50 + \left(\frac{RS \times R2}{RS + R2} \right)} \times \frac{R2}{RS + R2} \times \frac{R_{MATCH} + RS_S}{R_{MATCH}} \times \frac{RL}{10 + RL} \quad (5)$$

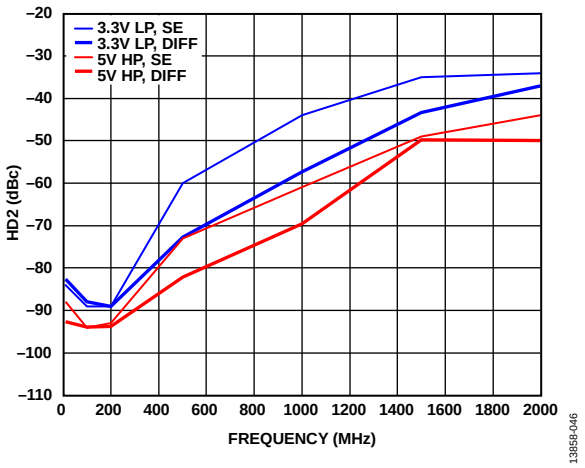


Figure 44. HD2 for Single-Ended (SE) and Differential (DIFF) Configurations vs. Frequency, V_{OUT} = 2 V p-p, RL = 200 Ω

INPUT AND OUTPUT EQUIVALENT CIRCUITS

The differential input and outptut impedance can be modeled by simple RLC equivalent circuits as shown in Figure 45. Figure 34 shows the comparison of the measured and modeled impedances for the input network. Likewise, Figure 35 shows the same comparison for the output network.

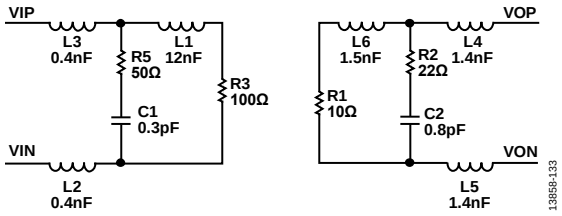


Figure 45. Model of Differential Input and Output Circuit

GAIN ADJUSTMENT AND INTERFACING

The effective gain of the ADL5567 can be reduced by adding two resistors in series with the inputs to reduce the gain.

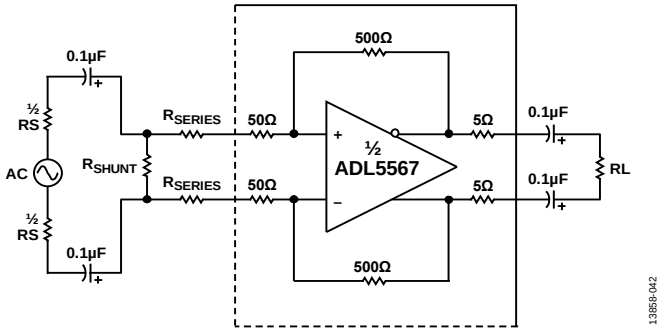


Figure 46. Gain Adjustment Using a Series Resistor

To find R_{SERIES} for a given A_V gain and RL, use the following equation:

$$R_{SERIES} = \frac{500}{A_V} \times \left(\frac{RL}{10 + RL} \right) - 50 \quad (6)$$

The necessary shunt component, R_{SHUNT}, to match to the source impedance, RS, can be expressed as

$$R_{SHUNT} = \frac{1}{\frac{1}{RS} - \frac{1}{2R_{SERIES} + 100}} \quad (7)$$

The shunt resistor values for multiple target voltage gains are listed in Table 5. The source resistance and input impedance need careful attention when using Equation 5. The input impedance of the ADL5567 and the reactance of the ac coupling capacitors must be considered before assuming that they make a negligible contribution.

To calculate the gain (A_V) for a given R_{SERIES} and RL, use the following equation:

$$A_V = \left(\frac{500}{R_{SERIES} + 50} \right) \times \left(\frac{RL}{10 + RL} \right) \quad (8)$$

Note that Equation 8 only gives the absolute gain and does not take into account that the circuit introduces a 180° phase shift. To account for this phase shift, multiply the product of Equation 8 by −1.

Table 5. Differential Gain Adjustment Using Series Resistor

Target Voltage Gain (dB)	RS (Ω)	R_{SERIES} (Ω)	R_{SHUNT} (Ω)
0	50	426.1	52.7
1	50	374.4	53.1
2	50	328.2	53.5
3	50	287.1	54
4	50	250.4	54.5
5	50	217.7	55.1
6	50	188.6	55.8
7	50	162.7	56.6
8	50	139.5	57.5
9	50	118.9	58.6
10	50	100.5	59.9
11	50	84.2	61.4
12	50	69.6	63.2
13	50	56.6	65.3
14	50	45	67.8
15	50	34.6	70.9
16	50	25.4	74.7
17	50	17.2	79.5
18	50	9.9	85.7
19	50	3.4	93.7

EFFECT OF LOAD CAPACITANCE

Load capacitance, including stray capacitance from PCB traces, affect the bandwidth and flatness of the ADL5567 frequency response, resulting in excessive peaking. Adding external series resistors to each output isolates the load capacitance from the outputs, and reduces the peaking effectively. Respective frequency responses resulting from the addition of 1.5 pF and 3 pF differential load capacitance (C_{LD}) as well as series resistance (R_{SE}) of 15 Ω are shown in Figure 47.

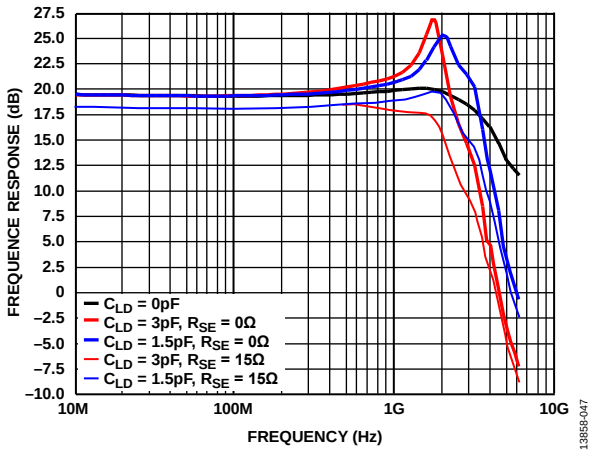


Figure 47. Frequency Response for Various Load Capacitances, V_S = 5 V, High Performance Mode, RL = 200 Ω

ADC INTERFACING

A wideband data acquisition system (AD-FMCADC7-EBZ) using the ADL5567 together with the AD9625 2.6 GSPS, 12-bit ADC is shown in Figure 51. The RC filter after the amplifier works with the pole formed by the ADC input capacitance to attenuate the broadband noise and out-of-band harmonics generated by the amplifier, as well as blocking the sharp switching pulses from reaching the amplifier outputs and creating nonlinear effects. Component values for different acquisition bandwidth are listed in Table 6. An additional filter more specific to the system rejection requirements is also needed ahead of the ADL5567 amplifier to prevent unwanted signals from compressing the amplifier as well as from reaching the ADC.

The signal-to-noise ratios with respect to full scale of the ADC system (SNR FS), using various sources for sampling clock on several circuit boards (such as the BRD-2, BRD-4, or BRD-5) are shown in Figure 48. Two-tone intermodulation distortion performance is shown in Figure 49, and the relative frequency responses for this ADC system with different output filter capacitors, are shown in Figure 50.

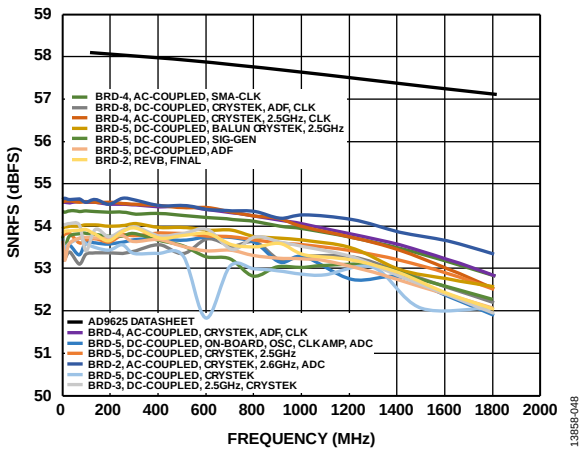


Figure 48. ADC System SNR (Referred to Full Scale)

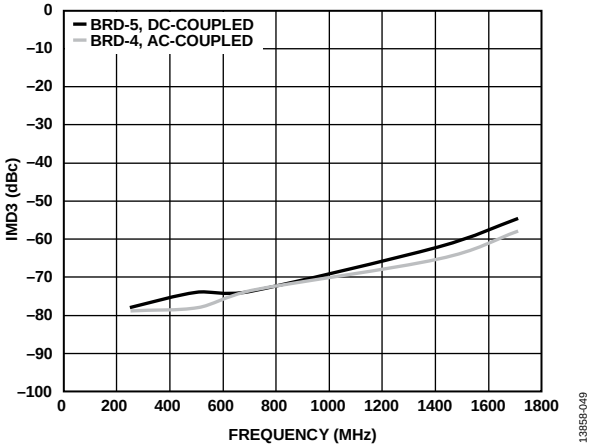


Figure 49. Measured Two-Tone IMD3 Performance

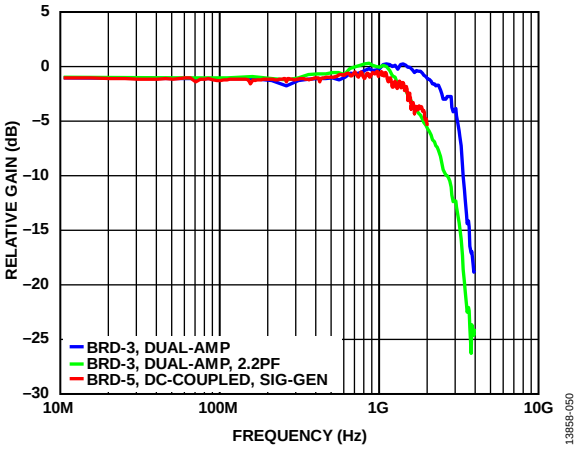


Figure 50. Measured Relative Frequency Response

Table 6. Example RC Values for Various Bandwidth Limits

Component	Value/Device	Description/Comments
Amplifier	½ ADL5567	One channel
R_{SERIES}	10 Ω	Small value to minimize loss
Wideband Configuration		
BW	3 GHz	Wide BW allows undersampling operation
C_{FILTER} (See Figure 51)	1 pF	Final value depends on PCB parasitics
Nyquist Band Configuration		
BW	1.8 GHz	Filters noise and harmonics above Nyquist frequency
C_{FILTER} (See Figure 51)	2.2 pF	Final value depends on PCB parasitics
ADC	AD9625	2.6 GSPS, 12-bit ADC

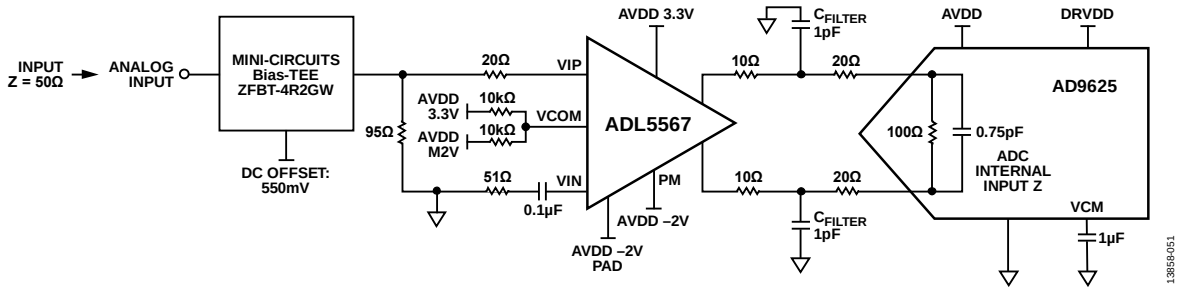


Figure 51. Wideband ADC Interfacing Example: ADL5567 Driving the AD9625

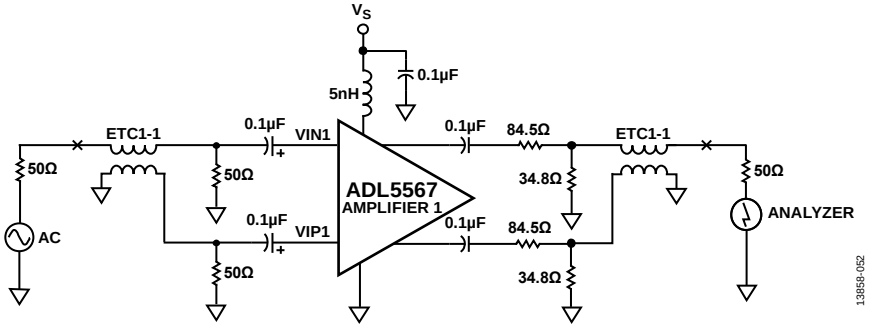


Figure 52. General-Purpose Characterization Circuit

SOLDERING INFORMATION AND RECOMMENDED LAND PATTERN

Figure 53 shows the recommended land pattern for the ADL5567. The ADL5567 is contained in a 4 mm × 4 mm LFCSP package, which has an exposed ground pad (EP). This pad is internally connected to the ground of the chip. To minimize thermal impedance and ensure electrical performance, solder the pad to the low impedance ground plane on the PCB. To further reduce thermal impedance, it is recommended that the ground planes on all layers under the paddle be stitched together with vias.

For more information on land pattern design and layout, refer to the AN-772 Application Note, *A Design and Manufacturing Guide for the Lead Frame Chip Scale Package (LFCSP)*.

The land pattern on the ADL5567 evaluation board provides a simulated thermal resistance (θ_{JA}) of 56 °C/W.

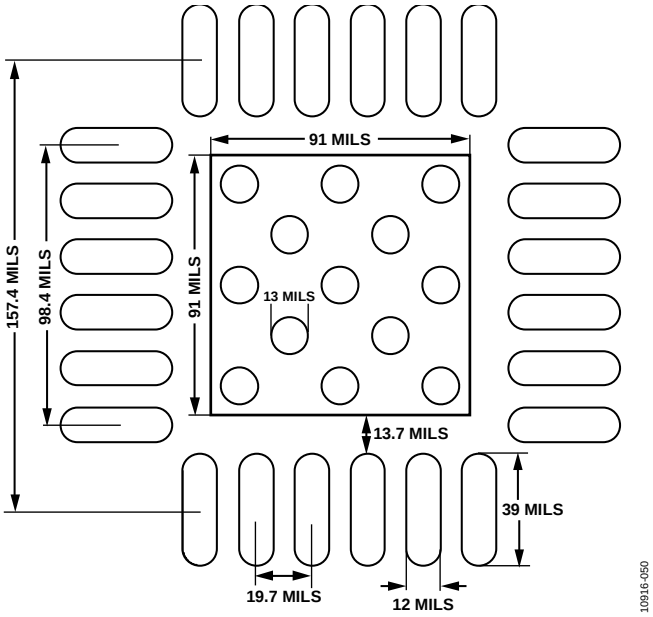


Figure 53. Recommended Land Pattern

EVALUATION BOARD

Figure 54 shows the schematic of the ADL5567 evaluation board. The evaluation board is powered by a single supply in the 3 V to 5 V range. The power supply is decoupled by 10 µF and 0.1 µF capacitors. Inductors L1 and L2 decouple the ADL5567 from the power supply. Table 7 details the various configuration options of the evaluation board.

Figure 55 and Figure 56 show the component and circuit side layouts of the evaluation board.

The balanced input and output interfaces are converted to single-ended with a pair of baluns (Mini-Circuits TCM1-43X+). The baluns at the input, T1 and T2, provide a 50 Ω single-ended to differential transformation. The output baluns, T3 and T4, and the matching components are configured to provide a 200 Ω to 50 Ω impedance transformation with an insertion loss of about 11 dB.

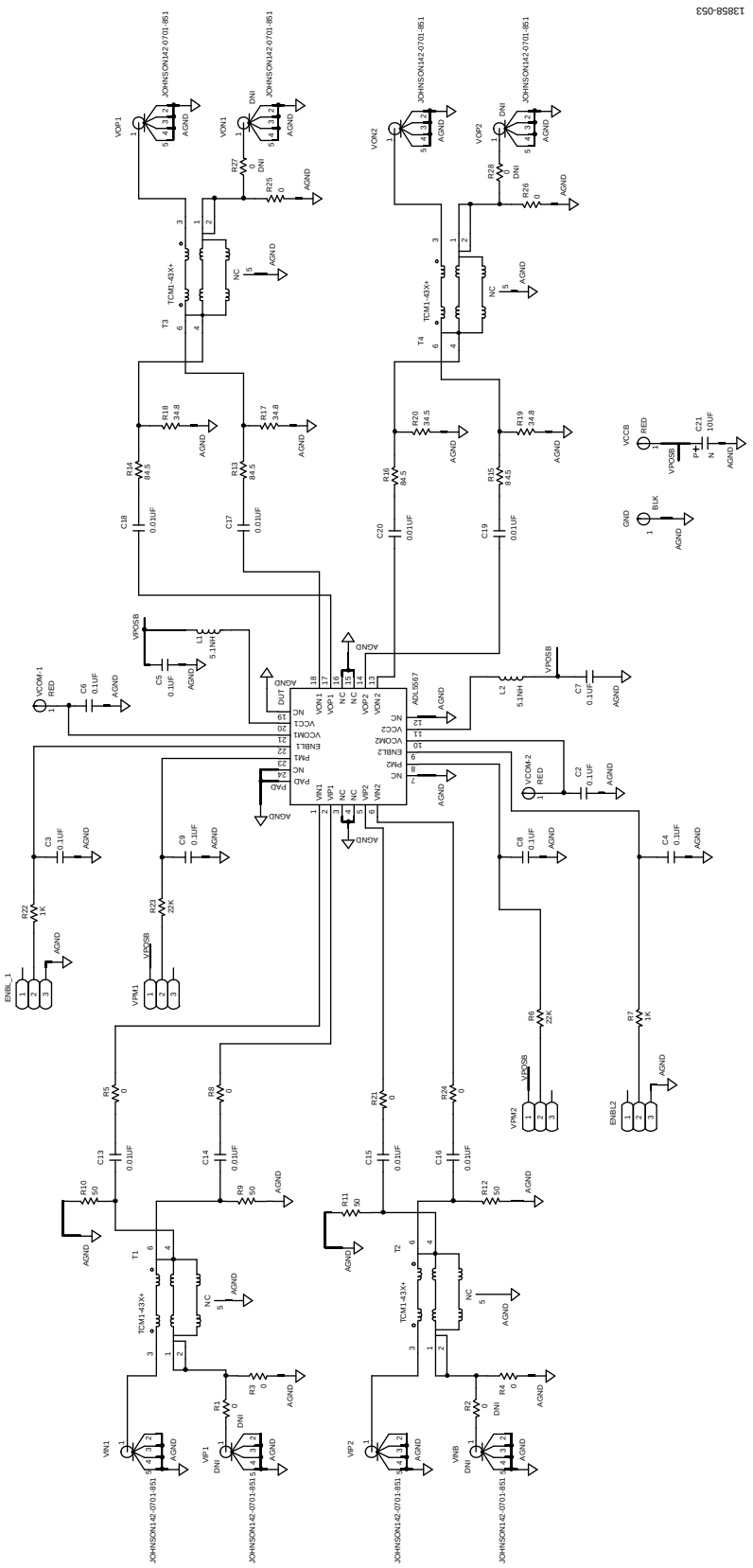


Figure 54. Evaluation Board Schematic

Table 7. Evaluation Board Configuration Options

Component	Description	Default Condition
VCCB, GND	Supply and ground test loops.	VCCB, GND = installed
C5, C7, C21, L1, L2	Power supply decoupling. The supply decoupling consists of a 10 µF capacitor (C21) and two 0.1 µF capacitors, C5 and C7, connected between the supply lines and ground. L1 and L2 decouple the ADL5567 from the power supply.	C21 = 10 µF (Size D), C5, C7 = 0.1 µF (Size 0402), L1, L2 = 5.1 nH (Size 0603)
VIN1, VIP1, VIP2, VIN2, R1, R2, R3, R4, R5, R8, R9, R10, R11, R12, R21, R24, C13, C1, C12, C14, C15, C16, T1, T2	Input interface. The SMA labeled VIN1 is the input to Amplifier 1. T1 is a 1:1 impedance ratio balun to transform a single-ended input into a balanced differential signal. Removing R3, installing R1 (0 Ω), and installing an SMA connector (VIP1) allows driving from a differential source. C13 and C14 provide ac coupling. C12 is an optional bypass capacitor. R9 and R10 provide a differential 50 Ω input termination. The SMA labeled VIP2 is the input to Amplifier 2. T2 is a 1:1 impedance ratio balun to transform a single-ended input into a balanced differential signal. Removing R4, installing R2 (0 Ω), and installing an SMA connector (VIN2) allows driving from a differential source. C15 and C16 provide ac coupling. C1 is an optional bypass capacitor. R11 and R12 provide a differential 50 Ω input termination.	VIN1, VIP2 = installed, VIP1, VIN2 = not installed, R1, R2 = do not install (DNI), R3, R4, R5, R8, R21, R24 = 0 Ω (Size 0402), R9, R10, R11, R12 = 50 Ω (Size 0402), C13, C14, C15, C16 = 0.01 µF (Size 0402), C1, C12 = DNI, T1, T2 = TCM1-43+ (Mini-Circuits®)
VOP1, VON1, VON2, VOP2, C10, C11, C17, C18, C19, C20, R13, R14, R15, R16, R17, R18, R19, R20, R25, R26, R27, R28, T3, T4	Output interface. The SMA labeled VOP1 is the output for Amplifier 1. T3 is a 1:1 impedance ratio balun used to transform a balanced differential signal to a single-ended signal. Removing R25, installing R27 (0 Ω), and installing an SMA connector (VON1) allows differential loading. C10 is an optional bypass capacitor. C17 and C18 provide ac coupling. R13, R14, R17, and R16 are provided for generic placement of matching components. The SMA labeled VON2 is the output for Amplifier 2. T4 is a 1:1 impedance ratio balun used to transform a balanced differential signal to a single-ended signal. Removing R26, installing R28 (0 Ω), and installing an SMA connector (VOP2) allows differential loading. C11 is an optional bypass capacitor. C19 and C20 provide ac coupling. R15, R16, R19, and R20 are provided for generic placement of matching components. The evaluation board is configured to provide a 50 Ω source impedance to the external output, as well as a 200 Ω load to the device, with a voltage divide ratio of 17 dB.	VOP1, VON2 = installed, VON1, VOP2 = not installed, R13, R14, R15, R16 = 84.5 Ω (Size 0402), R17, R18, R19, R20 = 34.8 Ω (Size 0402), R25, R26 = 0 Ω (Size 0402), R27, R28 = DNI (Size 0402), C10, C11 = DNI (Size 0402), C17, C18 = 0.01 µF (Size 0402), C19, C20 = 0.01 µF (Size 0402), T3, T4 = TCM1-43+ (Mini-Circuits)
ENBL_1, ENBL_2, C3, C4	Device enable. ENBL_1 is the enable input for Amplifier 1. Placing the jumper between Position 1 and Position 2 enables Amplifier 1. C3 is a bypass capacitor for the ENBL_1 input. ENBL_2 is the enable for Amplifier 2. Placing the jumper between Position 1 and Position 2 enables Amplifier 2. C4 is a bypass capacitor for the ENBL_2 pin.	ENBL_1, ENBL_2 = installed, C3, C4 = 0.1 µF (Size 0402)
VCOM-1, VCOM-2, C2, C6	Common-mode voltage interface. VCOM-1 is the common-mode interface for Amplifier 1. A voltage applied to this pin sets the common-mode voltage of the output of Amplifier 1. VCOM-2 is the common-mode interface for Amplifier 2. A voltage applied to this pin sets the common-mode voltage of the output of Amplifier 2. Typically decoupled to ground with a 0.1 µF capacitor (C2 and C6). With no reference applied, input and output common mode levels float to midsupply (V_S/2).	VCOM-1, VCOM-2 = installed C2, C6 = 0.1 µF (Size 0402)
PM1, PM2	Power mode control. Each amplifier has a power mode control that lowers the current in the amplifier to lower the power consumption.	PM1, PM2 = installed

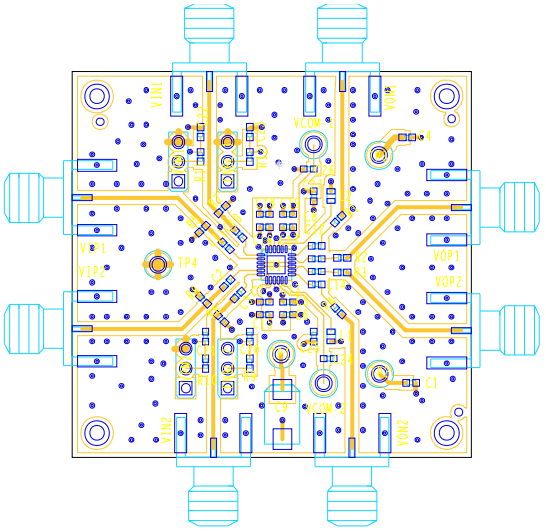


Figure 55. Layout of Evaluation Board, Component Side

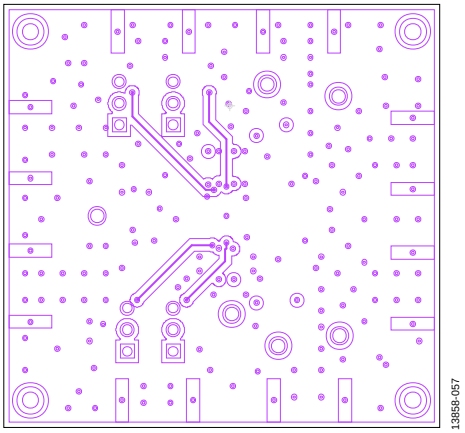
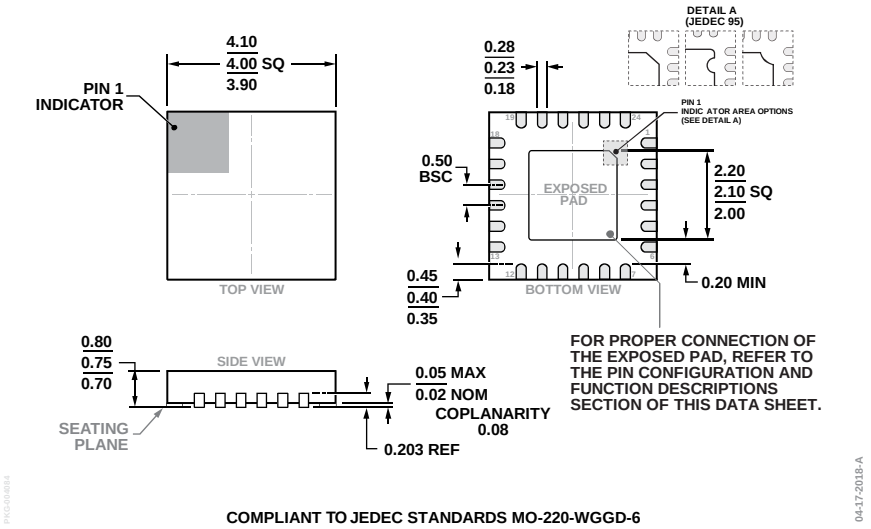


Figure 56. Layout of Evaluation Board, Circuit Side

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-WGGD-6

Figure 57. 24-Lead Lead Frame Chip Scale Package [LFCSP]
4 mm × 4 mm Body and 0.75 mm Package Height
(CP-24-19)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADL5567ACPZN-R7	−40°C to + 85°C	24-Lead Lead Frame Chip Scale Package [LFCSP], 7″ Tape and Reel	CP-24-19
ADL5567-EVALZ		Evaluation Board	

[1] Z = RoHS Compliant Part.

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