CSD13202Q2 12-V N-Channel NexFET™ Power MOSFETs

1 Features

- Ultra-Low Q_g and Q_{gd}
- Low Thermal Resistance
- Avalanche Rated
- Lead-Free Terminal Plating
- RoHS Compliant
- Halogen Free
- SON 2-mm × 2-mm Plastic Package

2 Applications

- Optimized for Load Switch Applications
- Storage, Tablets, and Handheld Devices
- Optimized for Control FET Applications
- Point of Load Synchronous Buck Converters

3 Description

This 12-V, 7.5-mΩ NexFET™ power MOSFET has been designed to minimize losses in power conversion and load management applications. The SON 2 × 2 offers excellent thermal performance for the size of the package.

Product Summary

T_A = 25°C		TYPICAL VAUE		UNIT
V_{DS}	Drain-to-Source Voltage	12		V
Q_g	Gate Charge Total (4.5 V)	5.1		nC
Q_{gd}	Gate Charge Gate-to-Drain	0.76		nC
$R_{DS(on)}$	Drain-to-Source On-Resistance	V_{GS} = 2.5 V	9.1	mΩ
		V_{GS} = 4.5 V	7.5	
$V_{GS(th)}$	Threshold Voltage	0.8		V

Device Information

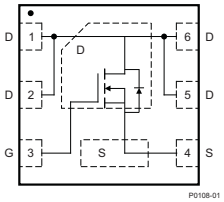
DEVICE	MEDIA	QTY	PACKAGE	SHIP
CSD13202Q2	7-Inch Reel	3000	SON 2.00-mm × 2.00-mm Plastic Package	Tape and Reel

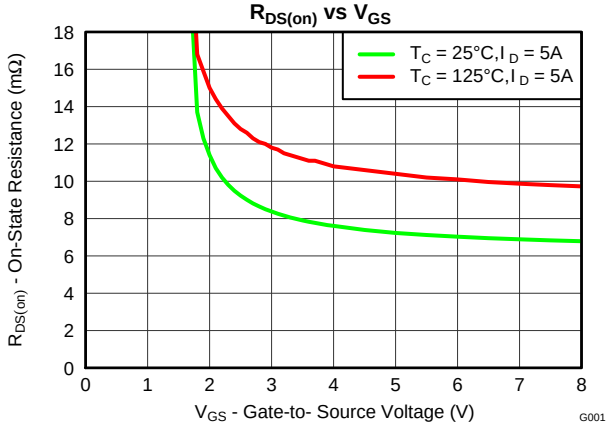
Absolute Maximum Ratings

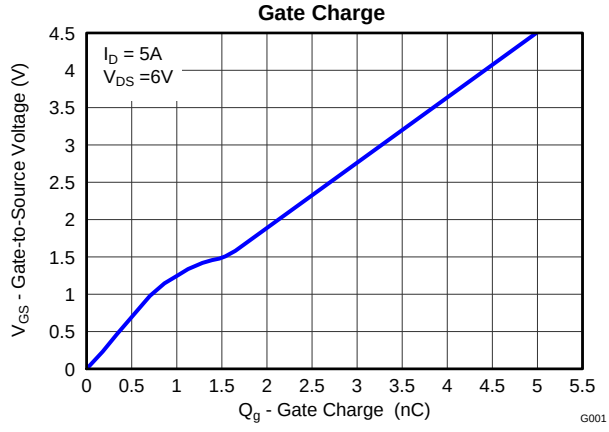
T_A = 25°C		VALUE	UNIT
V_{DS}	Drain-to-Source Voltage	12	V
V_{GS}	Gate-to-Source Voltage	±8	V
I_D	Continuous Drain Current (Package Limit)	22	A
	Continuous Drain Current(1)	14.4	
I_{DM}	Pulsed Drain Current, T_A = 25°C(2)	76	A
P_D	Power Dissipation(1)	2.7	W
T_J, T_{STG}	Operating Junction, Storage Temperature	–55 to 150	°C
E_{AS}	Avalanche Energy, Single Pulse I_D = 20 A, L = 0.1 mH, R_G = 25 Ω	20	mJ

(1) $R_{\theta JA}$ = 45°C/W on 1-in^2 Cu (2-oz) on 0.06-in thick FR4 PCB.
(2) Pulse duration 10 µs, duty cycle ≤ 2%.

Top View







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4 Revision History

Changes from Original (September 2013) to Revision A **Page**

- Added *Device Information* table, *Specifications* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Updated the mechanical drawings ... 8

5 Specifications

5.1 Electrical Characteristics

T_A = 25°C, unless otherwise specified

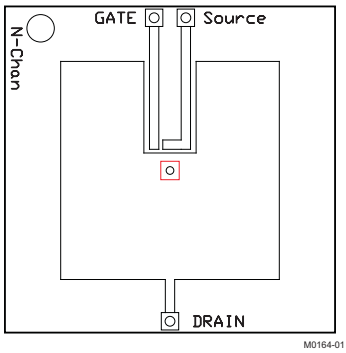
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC CHARACTERISTICS						
BV_{DSS}	Drain-to-source voltage	V_{GS} = 0 V, I_D = 250 µA	12			V
I_{DSS}	Drain-to-source leakage current	V_{GS} = 0 V, V_{DS} = 9.6 V			1	µA
I_{GSS}	Gate-to-source leakage current	V_{DS} = 0 V, V_{GS} = 8 V			100	nA
$V_{GS(th)}$	Gate-to-source threshold voltage	V_{DS} = V_{GS}, I_{DS} = 250 µA	0.58	0.80	1.10	V
$R_{DS(on)}$	Drain-to-source on-resistance	V_{GS} = 2.5 V, I_{DS} = 5 A		9.1	11.6	mΩ
		V_{GS} = 3 V, I_{DS} = 5 A		8.4	10.4	
		V_{GS} = 4.5 V, I_{DS} = 5 A		7.5	9.3	
g_{fs}	Transconductance	V_{DS} = 6 V, I_{DS} = 5 A		44		S
DYNAMIC CHARACTERISTICS						
C_{ISS}	Input capacitance	V_{GS} = 0V, V_{DS} = 6 V, f = 1 MHz		767	997	pF
C_{OSS}	Output capacitance			506	657	pF
C_{RSS}	Reverse transfer capacitance			43	56	pF
R_g	Series gate resistance			0.7	1.4	Ω
Q_g	Gate charge total (4.5 V)	V_{DS} = 6 V, I_{DS} = 5 A		5.1	6.6	nC
Q_{gd}	Gate charge gate-to-drain			0.76		nC
Q_{gs}	Gate charge gate-to-source			0.98		nC
$Q_{g(th)}$	Gate charge at Vth			0.57		nC
Q_{OSS}	Output charge	V_{DS} = 6 V, V_{GS} = 0 V		5.7		nC
$t_{d(on)}$	Turnon delay time	V_{DS} = 6 V, V_{GS} = 4.5 V, I_{DS} = 5 A R_G = 2 Ω		4.5		ns
t_r	Rise time			28		ns
$t_{d(off)}$	Turnoff delay time			11.0		ns
t_f	Fall time			13.6		ns
DIODE CHARACTERISTICS						
V_{SD}	Diode forward voltage	I_{DS} = 5 A, V_{GS} = 0 V		0.75	1	V
Q_{rr}	Reverse recovery charge	V_{DD} = 6 V, I_F = 5 A, di/dt = 200 A/µs		13		nC
t_{rr}	Reverse recovery time			28		ns

5.2 Thermal Characteristics

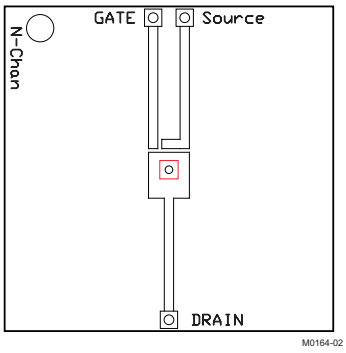
T_A = 25°C unless otherwise stated

PARAMETER		MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Thermal resistance junction-to-case (1)			6.4	°C/W
$R_{\theta JA}$	Thermal resistance junction-to-ambient (1) (2)			60	°C/W

(1) $R_{\theta JC}$ is determined with the device mounted on a 1-in^2 (6.45-cm^2), 2-oz (0.071-mm) thick Cu pad on a 1.5-in × 1.5-in (3.81-cm × 3.81-cm), 0.06-in (1.52-mm) thick FR4 PCB. $R_{\theta JC}$ is specified by design, whereas $R_{\theta JA}$ is determined by the user's board design.
(2) Device mounted on FR4 material with 1-in^2 (6.45-cm^2), 2-oz (0.071-mm) thick Cu.



Max $R_{\theta JA}$ = 60 when mounted on 1 in^2 (6.45 cm^2) of 2-oz (0.071-mm) thick Cu.



Max $R_{\theta JA}$ = 210 when mounted on minimum pad area of 2-oz (0.071-mm) thick Cu.

5.3 Typical MOSFET Characteristics

T_A = 25°C unless otherwise stated

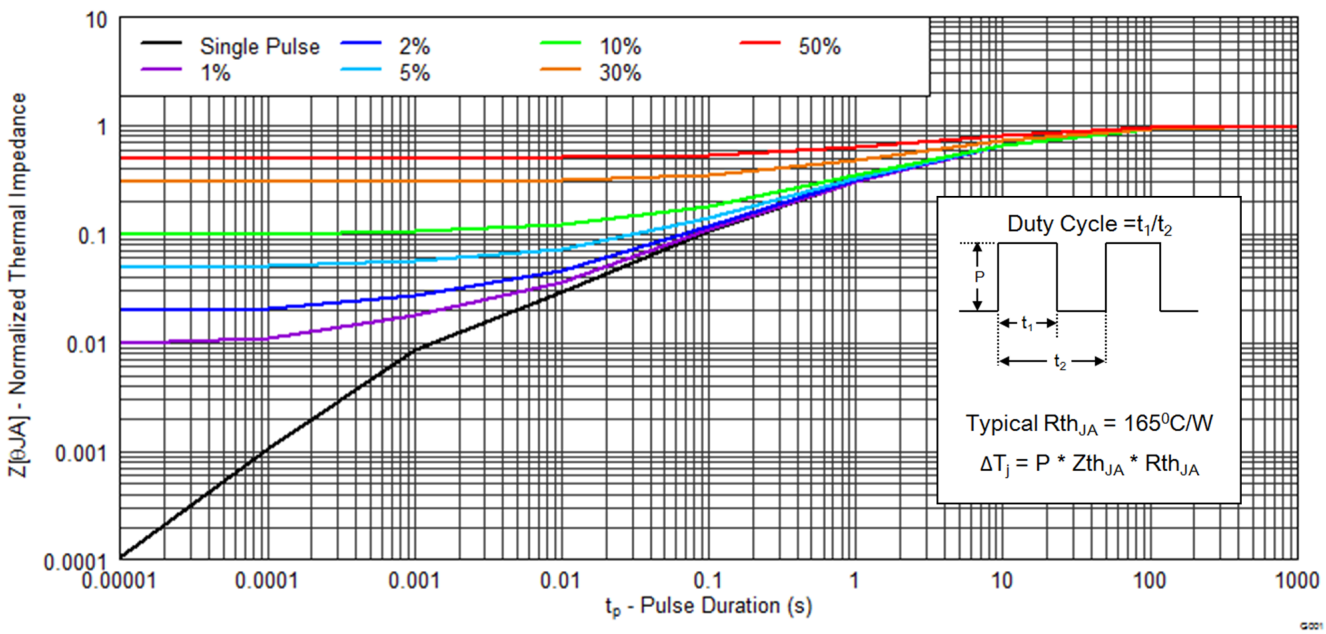


Figure 1. Transient Thermal Impedance

Typical MOSFET Characteristics (continued)

T_A = 25°C unless otherwise stated

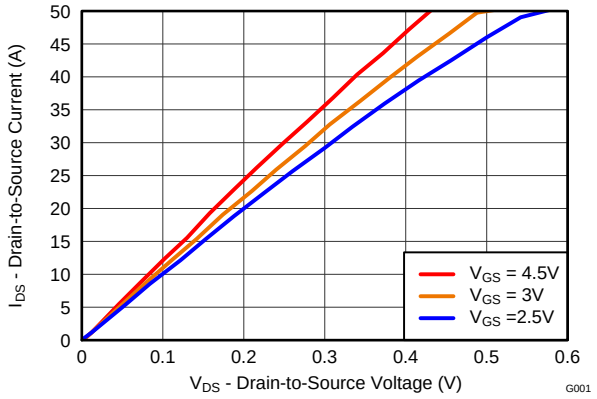


Figure 2. Saturation Characteristics

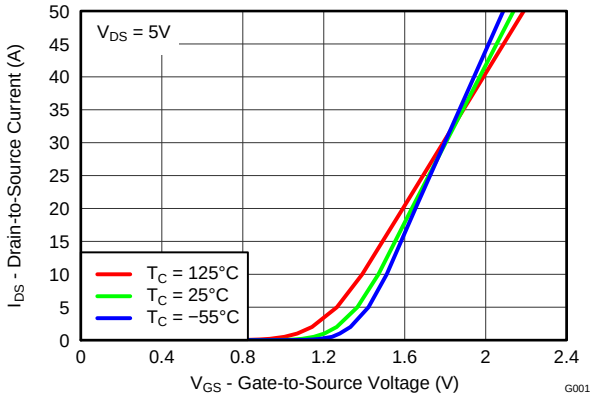


Figure 3. Transfer Characteristics

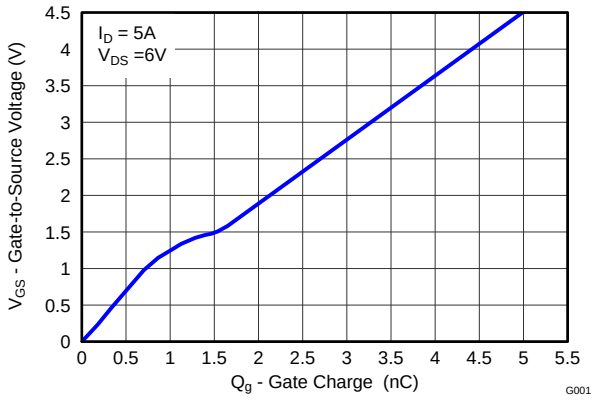


Figure 4. Gate Charge

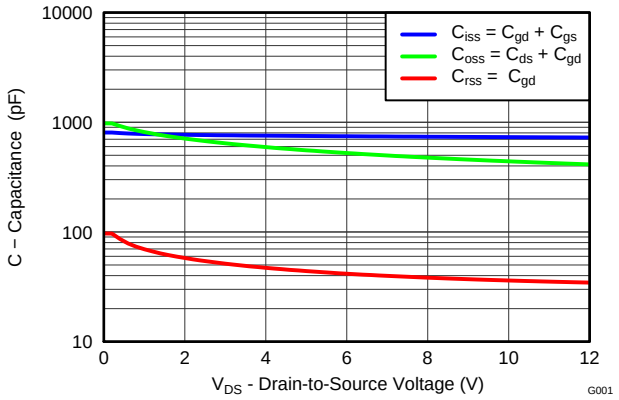


Figure 5. Capacitance

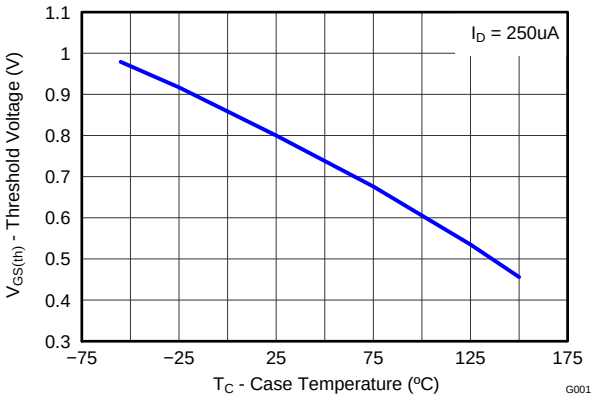


Figure 6. Threshold Voltage vs Temperature

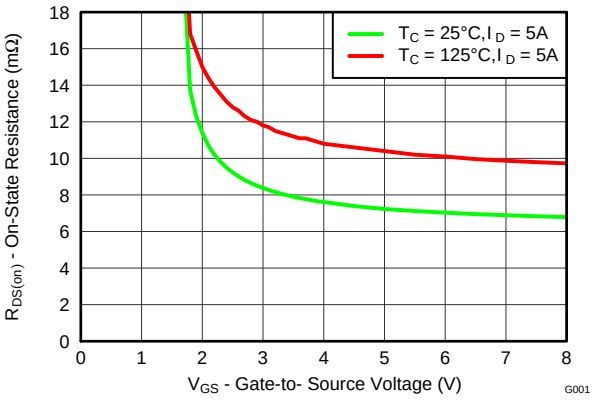


Figure 7. On-State Resistance vs Gate-to-Source Voltage

Typical MOSFET Characteristics (continued)

T_A = 25°C unless otherwise stated

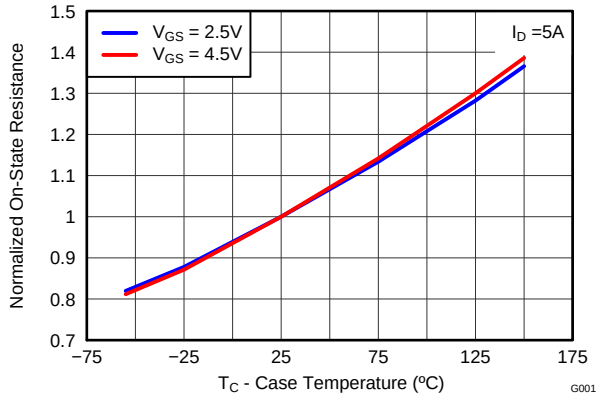


Figure 8. Normalized On-State Resistance vs Temperature

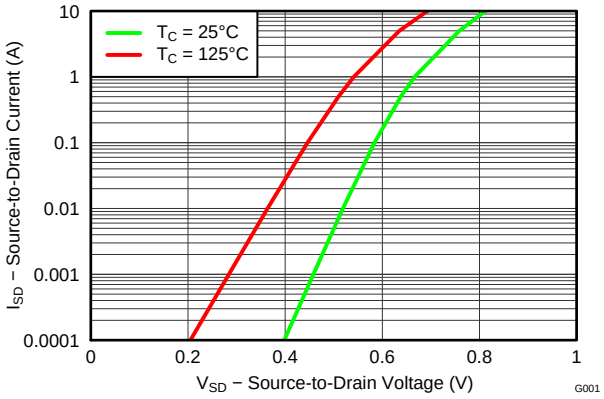


Figure 9. Typical Diode Forward Voltage

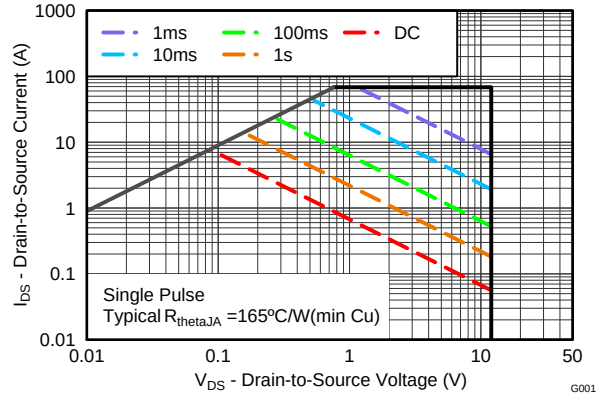


Figure 10. Maximum Safe Operating Area

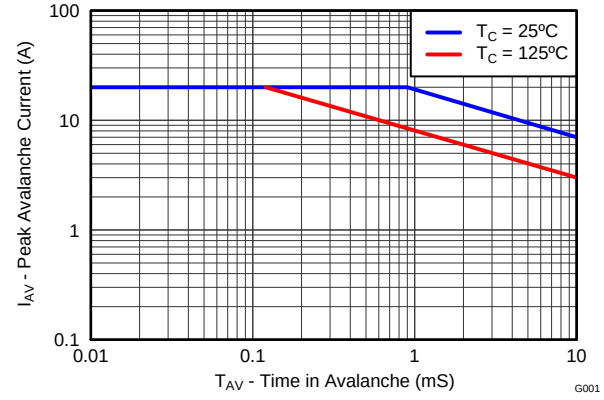


Figure 11. Single Pulse Unclamped Inductive Switching

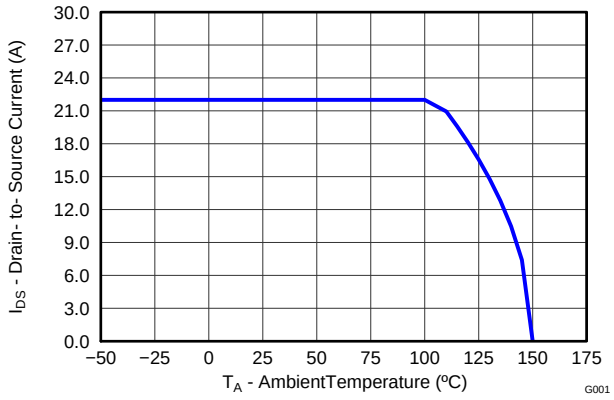


Figure 12. Maximum Drain Current vs Temperature

6 Device and Documentation Support

6.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

6.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

6.3 Trademarks

NexFET, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

6.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

6.5 Glossary

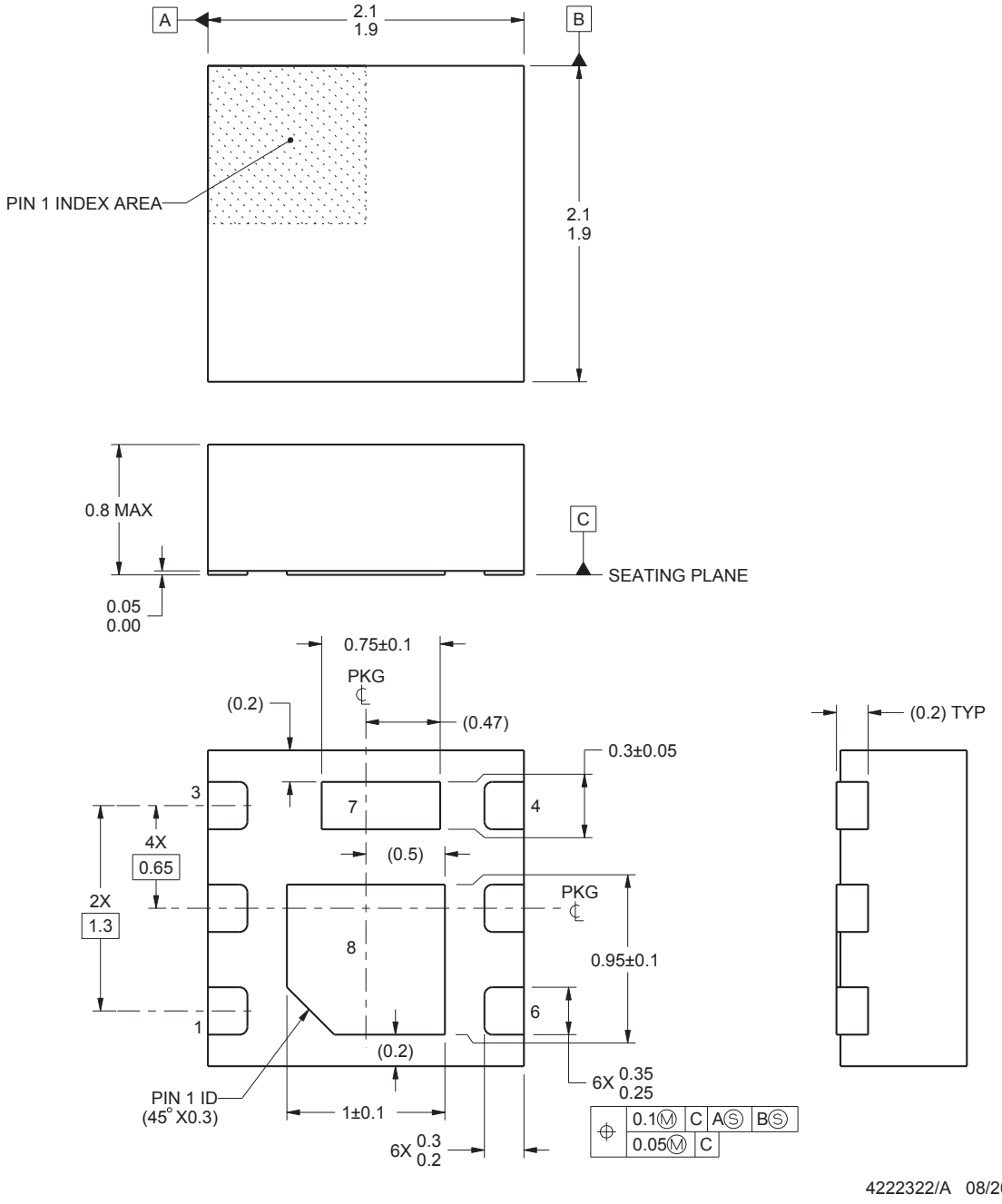
SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

7 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

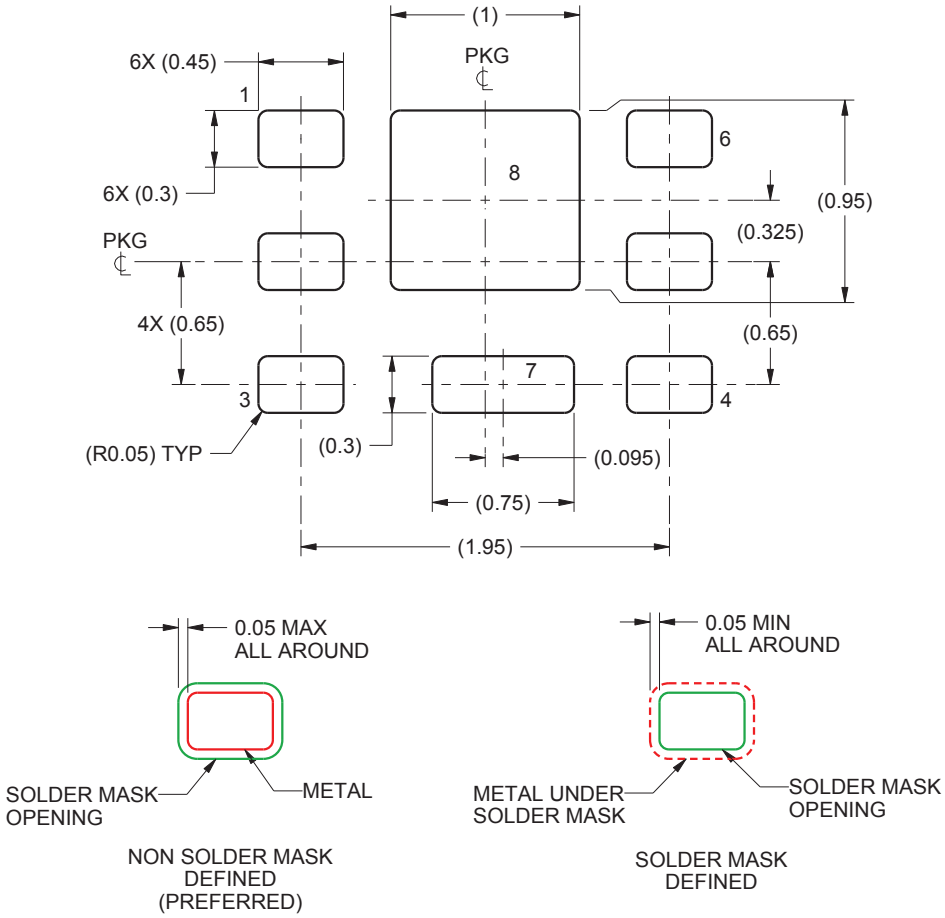
7.1 Q2 Package Dimensions



1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pads must be soldered to the printed circuit board for thermal and mechanical performance.

Q2 Package Dimensions (continued)

7.1.1 Recommended PCB Pattern

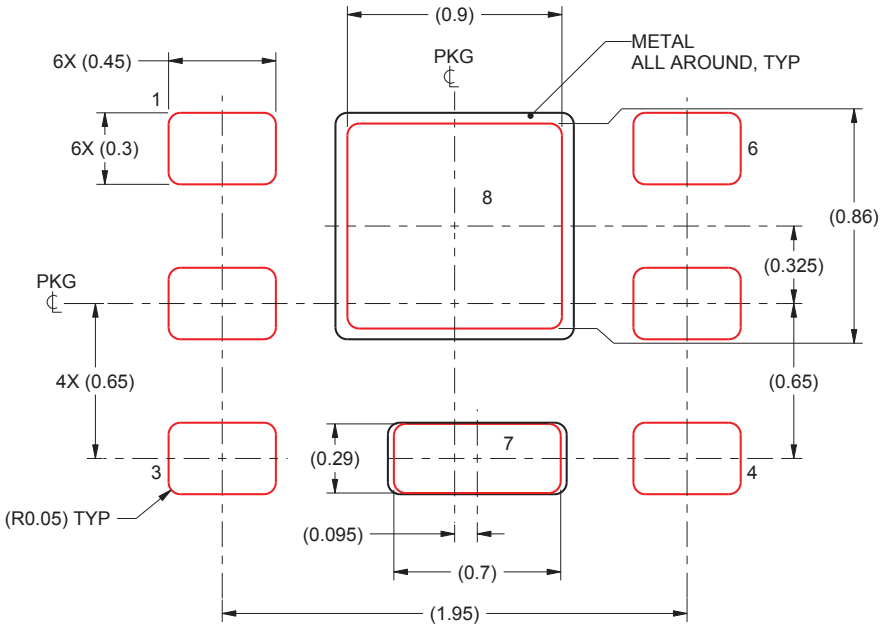


SOLDER MASK DETAILS

1. This package is designed to be soldered to a thermal pad on the board. For more information, see *QFN/SON PCB Attachment* (SLUA271).

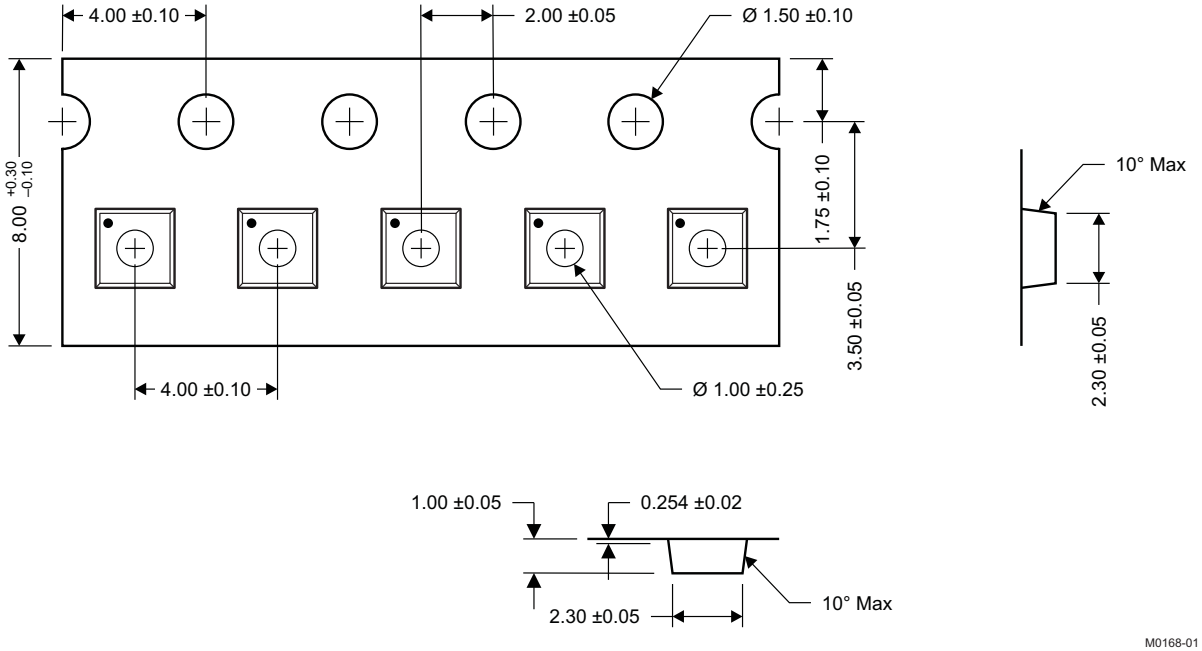
Q2 Package Dimensions (continued)

7.1.2 Recommended Stencil Pattern



1. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

7.2 Q2 Tape and Reel Information



Notes:
1. Measured from centerline of sprocket hole to centerline of pocket.
2. Cumulative tolerance of 10 sprocket holes is ±0.2.
3. Other material available.
4. Typical SR of form tape max 10^9 OHM/SQ.
5. All dimensions are in mm, unless otherwise specified.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD13202Q2	ACTIVE	WSON	DQK	6	3000	Green (RoHS & no Sb/Br)	NIPDAU | SN	Level-1-260C-UNLIM	-55 to 150	1322	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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