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USER GUIDE 3910

User's Guide for the MAX2769 GPS Receiver

By: David Weber, Strategic Applications Engineer
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Abstract: This note describes the MAX2769, a low-cost, single-conversion, low-IF GPS receiver chip that offers more flexibility and performance than its predecessors. Also included is a test procedure for the MAX2769 evaluation kit (EV kit) and some suggested SPI™ register settings for evaluation purposes.

Introduction

The MAX2769 is a low-cost, single-conversion, low-IF GPS receiver chip that offers more flexibility and performance than its predecessors. This device covers a wide range of GPS applications such as mobile handsets, PDAs and embedded PC, and automotive applications. It represents the most flexible, high-performance, low-power GPS receiver on the market.

Click here for an overview of the wireless components used in a typical radio transceiver.

IC Features

Low DC Power Consumption

Power required is typically 16mA to 23mA at 3V. Using SPI control, the device can be placed in idle mode, in which only the clock buffer and temperature sensor are active and the current consumption drops to 0.5mA.

Low Associated BOM Cost and Reduced Size

The MAX2769 is a direct down-conversion design with internal filtering that eliminates the need for external filtering components. An excellent noise figure (NF) of 1.4dB for the cascaded chain (with a 0.8dB typical first-stage NF) allows this device to be used with a passive antenna. No external LNA is required. Because the design removes intermediate frequency filtering and preamplification, the MAX2769 requires less board space to implement a receiver.

Flexibility for Applications Involving Active Antennas

A designer can use this device with an active antenna, as in an automotive application. For an active-antenna application, a second internal path can be selected, which leads to a different LNA (LNA2) with lower gain (13dB vs. 19dB) and a slightly higher NF (1.1dB vs. 0.8dB). This approach results in a power savings of 16mA to 19mA vs. 23mA to 21mA at 3V in default mode.

A voltage is provided at pin 3 specifically to bias the active device. This voltage can be turned off through the SPI interface for passive-antenna applications. If, however, the voltage is enabled, then LNA selection can be done automatically depending on whether there is an active antenna present. In the LNA-gated mode, the receiver is configured to automatically switch between the two LNAs contingent on whether a load current in excess of 1.5mA is detected at the antenna bias pin. A user does not need separate designs for applications using active and passive antennas; the chip automatically selects the appropriate LNA

for any application. If automatic LNA selection is not desired, it can be disabled through the Config1 register <14:13>.

Internal Capacitive Load Trimming for Crystal References

When using the MAX2769 with a crystal reference, no tuning of external load capacitors is required to match devices—a bank of internal crystal load capacitors can be programmed through the SPI interface to trim the load to yield the correct reference frequency. The internal bank can be programmed over a range of about 11pF to 17pF (settings plus 9pF of parasitic capacitance). A single series capacitor is placed between the crystal and the crystal/reference input. If the desired load value is between 11pF and 17pF, the value of this coupling capacitor can be made large (e.g., 10nF), so as not to affect the programmed value. For crystals with load capacitances below 11pF, the coupling capacitor can be made small to add in series with the internal bank, reducing the load seen at the device. Either way, the final frequency trimming can be done internally through the SPI interface.

Reference and IF Frequency Flexibility

The design accommodates a wide range of reference frequencies between 8MHz and 44MHz with a default setting of 16.328MHz. The IF frequency is adjustable in 63 steps between 0 and 12.5MHz, with a default setting of 4.092MHz. (It is recommended that the IF frequency be kept at or below 4.092MHz, as additional steps may need to be taken to assure stability at higher frequencies.) Because of a fractional-N synthesizer that permits small step size while maintaining excellent phase noise, this flexibility does not compromise performance. No other product on the market has this degree of flexibility.

IF Filter Flexibility

Filtering at IF is important as it limits the noise bandwidth and improves sensitivity while eliminating interference. The MAX2769's IF filtering is highly flexible. The design uses a complex polyphase Butterworth configuration that can be set to 3rd or 5th order, and either bandpass or lowpass as the application dictates. The center frequency is also programmable to match the selected IF. The 3dB bandwidths can be selected as 2.5MHz, 4.2MHz, 8.0MHz, or 18MHz. Users can choose a design that optimizes performance for their application. (Note: These are two-sided 3dB bandwidths. When the lowpass option is selected, the bandwidths are cut in half and become 1.25MHz, 2.1MHz, 4.0MHz, and 9MHz. In fact, the highest setting should only be used in a lowpass configuration.) In the predecessor to this part, a 4.8MHz lowpass filter was required to pass the fixed-IF frequency data. In this design, a 2.6MHz bandpass design could be employed, thus reducing the noise bandwidth by nearly 3dB and enhancing system sensitivity. Filters (in bandpass mode) are designed to have no more than 1dB droop at F_C ±1.023MHz.

High System Gain with a Wide Range of Level Control

To use the MAX2769 without an active antenna in a low-signal-strength environment, it is imperative that the receiver have sufficient gain. This device typically has up to 110dB available gain (in analog mode) with 60dB to 65dB of gain adjustment.

Access to the Amplified RF Signal for Coexistence Filtering

While no external filtering is required for stand-alone applications, coexistence with cellular or WiLAN transmissions in close proximity may require additional filtering to prevent overdriving the GPS receiver front-end. On the MAX2769, the RF signal has been made accessible between the first LNA stage output and mixer input (pins 2 and 5 respectively). If filtering is not desired, these ports can be connected through a coupling capacitor. However, filtering introduced at this point has minimal effect on the excellent sensitivity of the receiver. (For example, for typical device parameters, a SAW filter with 1dB insertion loss would degrade cascaded NF (and thus GPS sensitivity) by only about 0.15dB.

Flexibility of Output Modes

Most GPS devices provide only a single-output mode. The MAX2769's output can be programmed to be analog, CMOS, or limited differential logic in unsigned or complimentary binary format with 1- to 3-bit output from the ADC.

Temperature Sensor and Status Monitoring

A temperature sensor is included, which can be calibrated externally if desired. While lock-detect status can be obtained at the

LD pin, the part can be programmed to instead provide the output signal, the reference clock, or results from a sigma-delta test. It can also be programmed to provide a short to the active antenna or to be an independent test point for voltage.

The part is programmed through ten registers across a 3-wire SPI interface. Registers are described in **Table 1**. For further details, please refer to the MAX2769 data sheet.

Table 1. Description of SPI Configuration Registers

Register	Address	Function	Default
CONF1<31:0>	0000	Configures Rx and IF sections, sets antenna bias and LNA autoselect	A2919A3
CONF2<31:0>	0001	Configures AGC and output format	055028C
CONF3<31:0>	0010	Configures PGA, and details of AGC, filtering, and data streaming	EAFE1DC
PLLCONFIG<31:0>	0011	Sets PLL, VCO, and CLK settings	9EC0008
DIV<31:0>	0100	Sets PLL main and reference division ratios	0C00080
FDIV<31:0>	0101	Sets PLL fractional division ratios	8000070
STRM<31:0>	0110	Configures DSP interface frame streaming	8000000
CLK<31:0>	0111	Sets fractional clock divider values	10061B2
TEST1<31:0>	1000	Sets up test mode	1E0D401
TEST2<31:0>	1001	Sets up test mode	14C0002

For initial characterization in a MAX2769 EV kit, the parameters listed in **Table 2** can be measured with the suggested procedures that follow. The MAX2769 EV kit data sheet should be consulted for more details. Some settings differ from default values to facilitate testing; users are free to select different settings.

Table 2. Parameters to be Tested in Suggested Procedure

Parameter	Pins at which measurements are made on the MAX2769	Connectors at which measurements are made on the MAX2769 EV kit	Target value
LNA1 Gain	27–2	J7–J8	19dB
LNA2 Gain	25–2	J6–J8	13dB
System IP3 with LNA1	27–18	J7–J2	-26dBm
System IP3 with LNA2	25–18	J6–J2	-20dBm
LNA1 NF (Default Mode)	27–2	J7–J8	0.8dB
LNA2 NF	25–2	J6–J8	1.5dB
LNA1 P1dB (Output)	27–2	J7–J8	8dBm
LNA2 P1dB (Output)	25–2	J6–J8	10dB
Cascaded System NF, LNA1	27–18	J7–J2	1.4dB
Cascaded System NF, LNA2	25–18	J6–J2	2.7dB
Current Consumption (Default Mode,	11, 13, 14, 19, 23	W19, W20, W11, W12	19mA (default mode device only) (36mA at 3V, 140mA at ±5V for entire

LNA1)			EV kit)
IF Output Gain Range (4.092MHz IF)	27–18	J6 or J7–J2	55dB to 110dB
3dB IF Filter Passband	27–18	J7–J2	2.5MHz (default)
4MHz Offset Filter Rejection	18	J7–J2	29dB (3rd-order BPF), 48dB (5th-order BPF)
Digital Output	25, 27–17, 18, 20, 21	J12–J9	CMOS square wave with 50% duty cycle
AGC Function	25, 27–17, 18, 20, 21	J12–J9	Flat, -105dBm to -65dBm input

Suggested Test Procedures for Initial Device Characterization

U8 should be installed—make sure only U8 or Y2 is installed. The software assumes a reference frequency of 16.368MHz. If another frequency is used, change PLLCONFIG<22:21>. On the EV kit, remove U28, R61, R62, R63, R64, R65, C68, and C69. C26 should be installed, but U11 should not be installed on the board. For cascaded measurements, connect J8 to J12 using an RF cable.

For analog measurements (see steps 1 through 14 below), make certain that R47, R48, R52, and R54 have been inserted. This connects the output path through the two (MAX4444) differential-to-single-ended line receivers to ports J3 (I out) and J2 (Q out) where measurements can be made. A 50Ω load (such as a cable to a spectrum analyzer) should be placed on the ports for correct loading. (Note that baluns T2 and T3 are not required and should not be loaded.)

Jumpers should be set as follows:

- Connect W1–W9.
- Connect top two pins of W16, W17 (connecting signal paths) and W23, which shorts the signal to ground.
- Do not connect W13–W15, W18, and W28 (note that W13–W15 set up preconfigured states and will disable SPI commands).

LNA1 Tests (Default Current Mode)

1. Apply 3V, ±5V, and GND at W19, W20, W11, and W12.

2. Run the software to set up new default register configurations, as shown below and described in the appendix. (Note that these are not the default values.)

Config1:	A2959A3
Config2:	85502AC
Config3:	EAFF1DC
PLL Config:	9EC0008
PLL Integer Division:	0C00080
PLL Fractional Division Ratio:	8000070
DSP Interface:	8000000
CLK Fractional Division Ratio:	10061B2

TEST1:	1E0F401
TEST2:	14C0002

Make sure SHDN and IDLE are set to 1, the disabled state for both.

3. Measure +3V current consumption at W19 and W20.

4. Input a -60dBm, 1575.42MHz CW signal at J7. Measure the signal at J8 and record the LNA1 gain. Take into account the loss on the board traces at 1575MHz around 0.35dB.

5. Raise the input level until you get 1dB of compression (P1dB). (This is not a specified parameter, but you should get a number around +8dBm.) Be sure to gain correct any line losses.

6. Connect a short, low-loss cable from J8 to J12 to connect the LNA1 output to the mixer. Decrease the input to -110dBm and measure the system gain by monitoring the 4.092MHz output at J2. It should be around 110dB, resulting in a 0dBm output.

7. Set the maximum GAININ level by setting <3:27-22> to 63 (CONF2: 85512AC and CONF3: FEFF1DC). Decrease the input to -115dBm and measure the gain—it should be around 115dB. The input level should be adjustable through changes in GAININ. Decrease GAININ to the minimum by setting CONF3: 02FF1DC and once again measure the gain. It should be around 55dB.

8. Measure IP3 using LNA1. Combine two input sources (perhaps around -55dBm input), at F1 = 1587.42MHz and F2 = 1599.42MHz (where 2 × F1 - F2 falls in-band at 1575.42MHz) and inject into J7. Measure the strength of the 4.092MHz product at J2 (Q out). Drop both inputs by 1dB, and note that the product drops by 3dB. (If not, you are compressing and need to use a lower input level.) OIP3 = (3 × P_{OUT} - product)/2, so IIP3 = (3 × P_{OUT} - product)/2 - gain. This reduces to (3 × (P_{IN} + gain) - product)/2 - gain = (3 × P_{OUT} - product + gain)/2. With a minimum (55dB) gain, P_{OUT} = 5dBm. A typical 3rd-order product seen on the output spectrum at minimum gain might be -5dBm, in which case IIP3 = (3 × (-55) + 5 + 110)/2 = -25dBm.

9. Measure the LNA1 NF with an NF meter. The NF of the mixer stage can be measured using the gain method: by setting gain to max (see step 8), reducing the spectrum analyzer resolution bandwidth, and measuring the output S/N ratio. You need to have measured the exact system gain. For example, the input noise is -174dBm/Hz. Using an input of -100dBm and assuming around 90dB gain for the mixer stage, the receiver will not be in compression. The input S/N in a 1Hz bandwidth would be -74dB (S = 100dB/Hz, N = 174dBm/Hz). We might measure an output noise floor at J2 of -73dBm/Hz, yielding (with a -10dBm output) an SNR around 63dB. The NF of the system would then be the degradation in the S/N ratio, or 11dB. The result is approximate because measurement precision is poor. However, as the result is large and precision for this value is not critical, this approximate result is sufficient. Once again, subtract the input losses on the board (roughly 0.35dB) from all measured results. Knowing the gain of LNA1, you can then calculate cascaded NF.

You could use the gain method or the y-factor method to measure the NF for the entire cascaded chain, but this result would once again be approximate.

10. Return to the test register settings from step 2 and use an input level at J12 that is at least 10dB below the value that leads to 1dB compression, typically -110dB. Sweep the input frequency from 1572.9MHz to 1577.9MHz to yield a passband of 2.6MHz for the IF bandpass filter. This measurement can be made by using the maximum hold option on the spectrum analyzer.

11. Set up the AGC in the autonomous mode (AGC on with independent I and Q), where CONF2<12:11> = 00. Feed a signal into the LNA1 input at -150dBm and select LNA1. Note the tone power at the output while raising

the input level to -65dBm. It should remain approximately the same (indicating AGC is working).

LNA2 Tests

12. Switch to LNA2 (CONF1<14:13> = 01). Input a -60dBm, 1575.42MHz CW signal at J6. Measure LNA2 gain at J8 and record. Raise the input level until you get 1dB compression (P1dB). This is a repeat of steps 4 and 5 with LNA2. (Note again that the cascaded P1dB is determined by the mixer stage.) Cascaded gain is the linear gain measured here plus the gain from the mixer-in port to J2 from step 7.

13. If an NF meter is available, measure the LNA2 NF between J6 and J8. Then measure the NF following the procedure in step 9. Be sure that the AGC control is turned off so you can control the output level, CONF2<12:11> = 10.

14. With default settings, measure IP3 using LNA2. Combine two sources of -55dBm input at F1 = 1587.42MHz and F2 = 1599.42MHz (where 2 × F1 - F2 falls in-band at 1575.42MHz) and inject into J6. Measure the strength of the 4.092MHz product at J2 (Q out)—analog mode must be selected. Drop both inputs by 1dB and note that the product drops by 3dB. (If not, you are compressing the signal and need to use a lower input level.) Calculate IIP3 as in step 8.

Digital Tests

Digital measurements should be made at J9 A, B, C, and D. It has been discovered that the 74LV07 driver chip (U28) originally designed onto the board does not properly buffer these signals to allow them to be passed back to the computer on connector JDR1. To use these output signals to drive other circuitry off board, they may need to first be separately buffered.

15. Change to a digital output (CONF2<5:4> = 00) so that CONF2 = 855028C, and monitor the signal on an oscilloscope. You should have a square-wave CMOS output (2.8V amplitude) at J9. With CONF2<27> = 1, both I and Q signals should be present.

Appendix: Suggested Register Settings for Initial Test

CONF1: Test: A2959A3
This register:

- Enables the chip (default)
- Disables the idle (default)
- Sets default current programming
- Sets non-default LO current programming
- Sets default mixer current programming
- Selects 13MHz passive filter pole at mixer output (default)
- Selects LNA1 active (default; equivalent to grated mode when there is no current load on the ANT BIAS pin)
- Enables mixer (default)
- Turns off bias to external active antenna (default is bias on)
- Selects F_C = 4.092MHz
- Selects 2.5MHz polyphase IF bandpass filter
- Selects 26dB IF filter gain (default is 17dB)

CONF2: Test: 85502AC
This register:

- Selects both I and Q channels (default is I only)

- Sets AGC gain to 170 (default)
- Sets bit-counter length to 1024 bits (default)
- Selects sign/magnitude output format (default)
- Selects 1-bit AGC (default is 1 bit)
- Selects analog output driver (default is CMOS logic)
- Disables LO buffer (default)
- Enables temperature sensor (default)

CONF3: Test: EAFF15C
This register:

- Sets the PGA gain for level/LSB at 58 (default; used only when AGC is disabled and gain is set up over SPI lines)
- Chooses the nominal ADC input scale (default)
- Selects the nominal loading for the output driver (default)
- Enables the ADC (default)
- Enables the output driver (default)
- Enables the filter DC-offset cancellation circuitry (default)
- Enables the IF filter (default)
- Enables AGC for both channels (default is I enabled only)
- Enables highpass coupling between the filter and AGC (default)
- Sets a 50kHz highpass pole corner frequency (default is 20kHz)
- Selects no DSP interface for data streaming (default)
- Sets the default data-counter length (16394 bits/frame)
- Selects 2-bit streaming (default)
- Enables sync pulse outputs (default)
- Enables frame sync pulse outputs (default)
- Disables data sync pulse outputs (default)
- Disables DSP interface reset (default)

PLLCONFIG: Test: 9EC0008
This register:

- Enables the VCO in normal current mode (default)
- Disables external VCO bias compensation (default)
- Sets clock output driver to CMOS mode (default)
- Sets clock frequency to XTAL frequency
- Selects buffer nominal current of 130mA for crystal (default; range is 130mA to 700mA)
- Sets capacitive load programming to 3.6pF (default; nominal for C_L > 12pF)
- Selects PLL lock detect as output at LD pin (default)
- Selects nominal charge-pump operation with 0.5mA current (default)
- Selects 2ns charge-pump on-time selection (default)
- Selects integer-N PLL (default)
- Disables power save (default is power-save enable)
- Selects low-current mode for prescalar E2Cs (default is high-current mode)

DIV: Test: 0C00080
This register:

- Sets N = 1536 for low-side injection (default; LO = 1536 × 1.023MHz = 1571.328MHz)
- Sets R = 16 (default; step size = 16.368MHz/16 = 1.023MHz)

FDIV: Test: 8000070

This register:

- Sets fractional division ratio = 80000 (default)
- Selects nominal current and filter trim values

STRM: Test: 8000000
This register:

- Sets nominal stream interface control to start at a frame given by FRAME_COUNT

CLK: Test: 10061B2
This register:

- Sets the L counter to 256
- Sets the M counter to 1563
- Selects a fractional clock input to the fractional clock divider to come after the reference divider
- Selects the serializer clock to come from the reference divider

(When integer-N is selected in the PLL Config register, these settings are not used.)

TEST1: Test: 1E0F401
This register is reserved for Test

TEST2: Test: 14C0002
This register is reserved for Test

The screen format for setting configurations is shown in **Figure 1**.

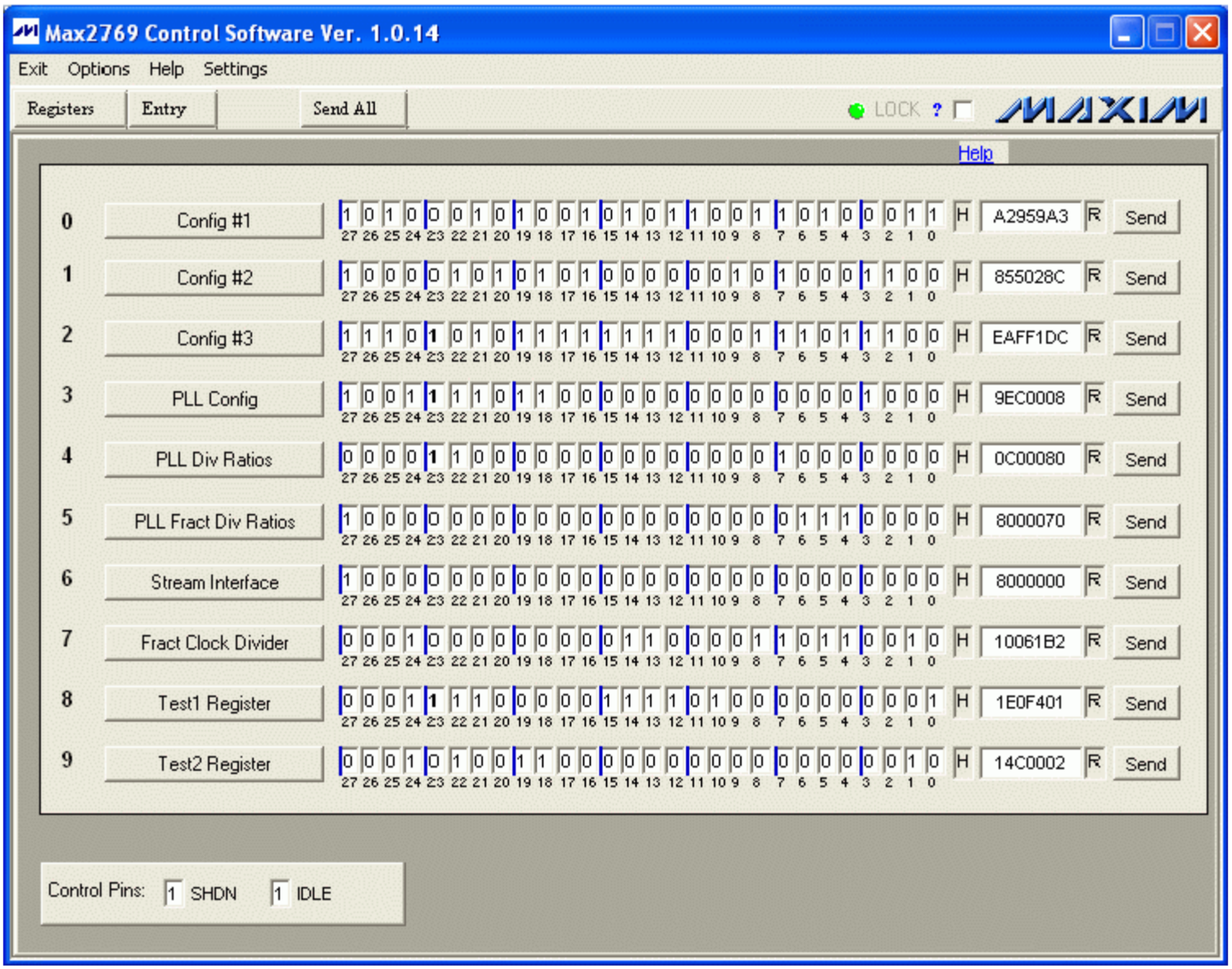

Figure 1. The MAX2769 EV kit test software screen format shows suggested settings.

Related Parts		
MAX2769	Universal GPS Receiver	Free Samples
MAX4444	Ultra-High-Speed, Low-Distortion, Differential-to-Single-Ended Line Receivers with Enable	Free Samples

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