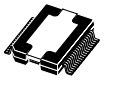
# STA506

## 40V 4A QUAD POWER HALF BRIDGE

## 1 FEATURES

- MINIMUM INPUT OUTPUT PULSE WIDTH DISTORTION
- 200mΩ $R_{dsON}$ COMPLEMENTARY DMOS OUTPUT STAGE
- CMOS COMPATIBLE LOGIC INPUTS
- THERMAL PROTECTION
- THERMAL WARNING OUTPUT
- UNDER VOLTAGE PROTECTION
- SHORT CIRCUIT PROTECTION

**Figure 1. Package**



**PowerSO36**

**Table 1. Order Codes**

| Part Number | Package |
|---|---|
| STA506 | PowerSO36 |
| STA50613TR | Tape & Reel |

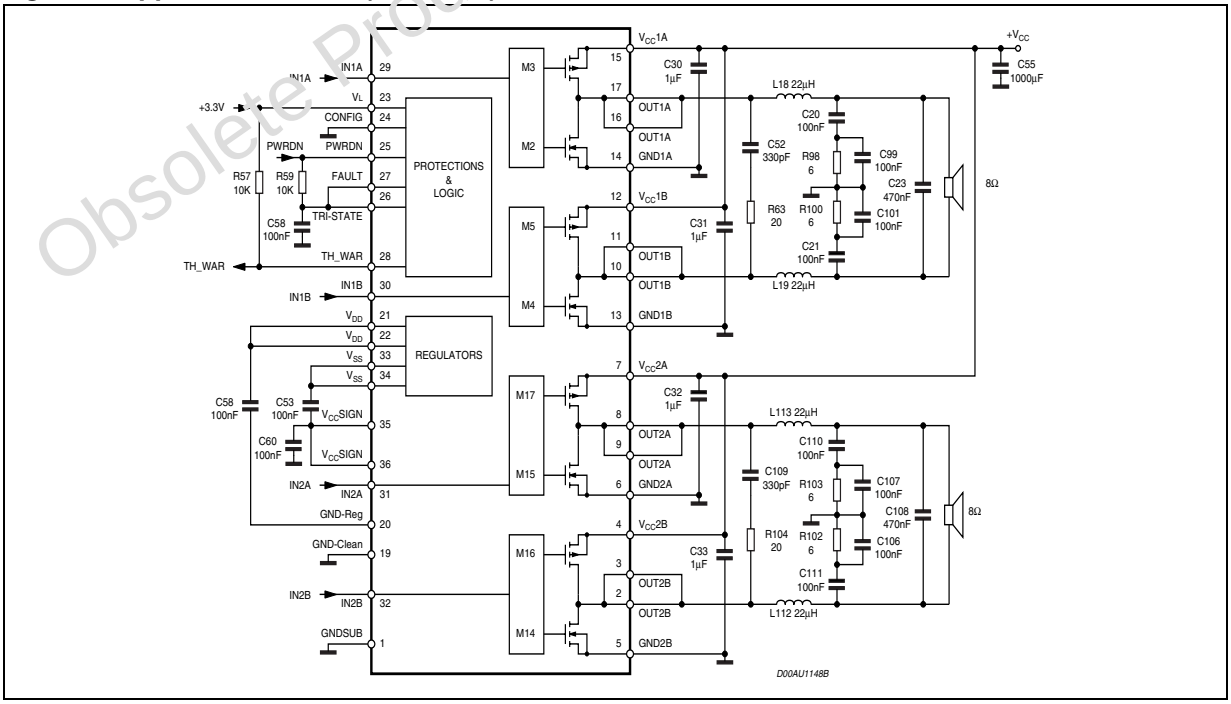
## 2 DESCRIPTION

STA506 is a monolithic quad half bridge stage in Multipower BCD Technology.

The device can be used as dual bridge or reconfigured, by connecting CONFIG pin to Vdd pin, as single bridge with double current capability, and as half bridge (Binary mode) with half current capability.

The device is particularly designed to make the output stage of a stereo All-Digital High Efficiency (DDX™) amplifier capable to deliver 60 + 60W @ THD = 10% at $V_{cc}$ 32V output power on 8Ω load and 80W @ THD = 10% at $V_{CC}$ 36V on 8Ω load in single BTL configuration. In single BTL configuration is also capable to deliver a peak of 120W @THD = 10% at $V_{CC}$ = 32V on 4Ω load. The input pins have threshold proportional to $V_L$ pin voltage.

**Figure 2. Application Circuit (Dual BTL)**




Obsolete Product(s)

**Table 2. Pin Function**

| Pin n. | Pin Name | Description |
|---|---|---|
| 1 | GND-SUB | Substrate Ground |
| 2 ; 3 | OUT2B | Output Half Bridge 2B |
| 4 | $V_{CC}$ 2B | Positive Supply |
| 5 | GND2B | Negative Supply |
| 6 | GND2A | Negative Supply |
| 7 | $V_{CC}$ 2A | Positive Supply |
| 8 ; 9 | OUT2A | Output Half Bridge 2A |
| 10 ; 11 | OUT1B | Output Half Bridge 1B |
| 12 | $V_{CC}$1B | Positive Supply |
| 13 | GND1B | Negative Supply |
| 14 | GND1A | Negative Supply |
| 15 | $V_{CC}$1A | Positive Supply |
| 16 ; 17 | OUT1A | Output Half Bridge 1A |
| 18 | NC | Not Connected |
| 19 | GND-clean | Logical Ground |
| 20 | GND-Reg | Ground for Regulator $V_{dd}$ |
| 21 ; 22 | $V_{dd}$ | 5V Regulator Referred to Ground |
| 23 | VL | Logic Reference Voltage |
| 24 | CONFIG | Configuration pin |
| 25 | PWRDN | Stand-by pin |
| 26 | TRI-STATE | High-Z pin |
| 27 | FAULT | Fault pin advisor |
| 28 | TH-WAR | Thermal warning advisor |
| 29 | IN1A | Input of Half Bridge 1A |
| 30 | IN1B | Input of Half Bridge 1B |
| 31 | IN2A | Input of Half Bridge 2A |
| 32 | IN2B | Input of Half Bridge 2B |
| 33 ; 34 | $V_{SS}$ | 5V Regulator Referred to +$V_{CC}$ |
| 35 ; 36 | $V_{CC}$ Sign | Signal Positive Supply |

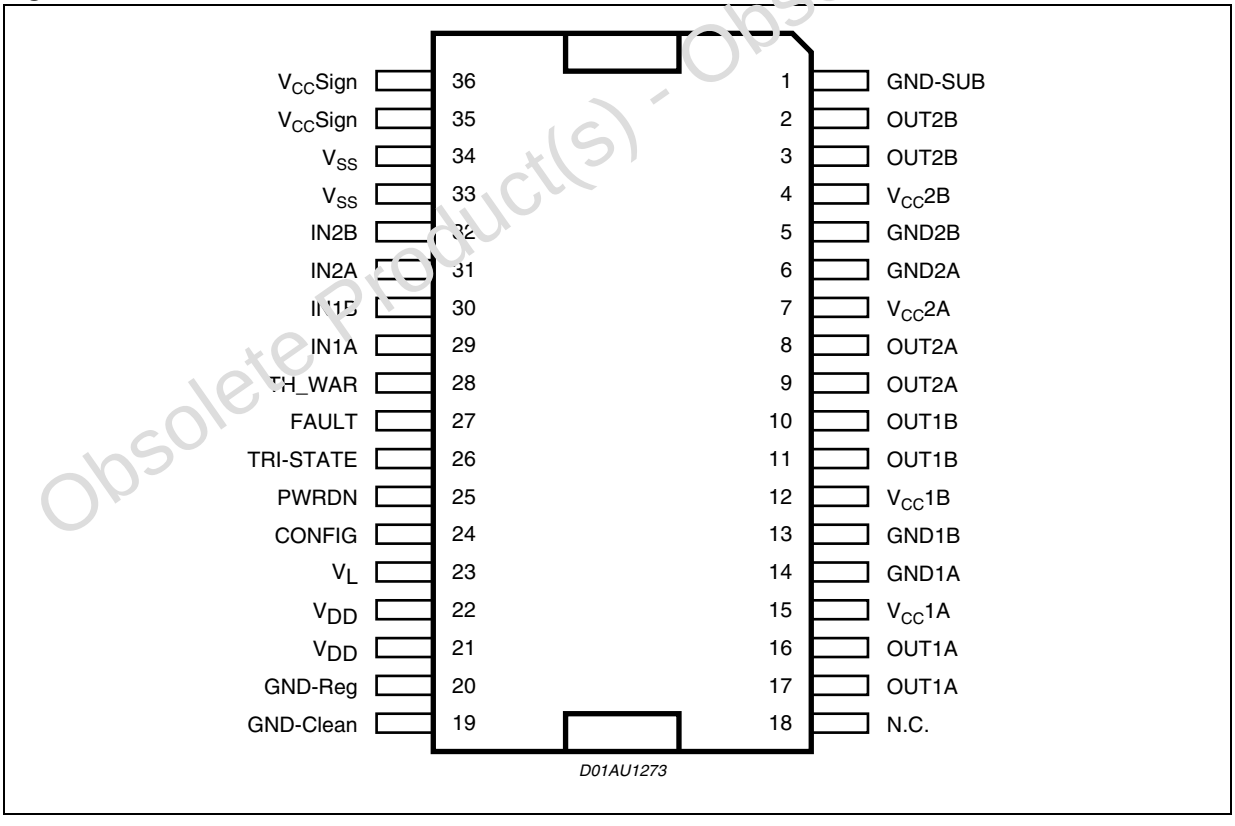
Obsolete Product(s) - Obsolete Product(s)

**Table 3. Functional Pin Status**

| Pin name | Pin n. | Logical value | IC -STATUS |
|---|---|---|---|
| FAULT | 27 | 0 | Fault detected (Short circuit, or Thermal ..) |
| FAULT (*) | 27 | 1 | Normal Operation |
| TRI-STATE | 26 | 0 | All powers in Hi-Z state |
| TRI-STATE | 26 | 1 | Normal operation |
| PWRDN | 25 | 0 | Low absorpion |
| PWRDN | 25 | 1 | Normal operation |
| THWAR | 28 | 0 | Temperature of the IC =130°C |
| THWAR(*) | 28 | 1 | Normal operation |
| CONFIG | 24 | 0 | Normal Operation |
| CONFIG(**) | 24 | 1 | OUT1A = OUT1B ; OUT2A=OUT2B (IF IN1A = IN1B; IN2A = IN2B) |

(*) : The pin is open collector. To have the high logic value, it needs to be pulled up by a resistor.
(**): To put CONFIG = 1 means connect Pin 24 (CONFIG) to Pins 21, 22 (Vdd) to implement single BTL (mono mode) operation for high current.

**Figure 3. Pin Connection**




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**Table 4. Absolute Maximum Ratings**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{CC}$ | DC Supply Voltage (Pin 4,7,12,15) | 40 | V |
| $V_{max}$ | Maximum Voltage on pins 23 to 32 (logic reference) | 5.5 | V |
| $P_{tot}$ | Power Dissipation ($T_{case}$ = 70°C) | 50 | W |
| $T_{op}$ | Operating Temperature Range | -40 to 90 | °C |
| $T_{stg}$, $T_j$ | Storage and Junction Temperature | -40 to 150 | °C |

**Table 5. (*) Recommended Operating Conditions**

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $V_{CC}$ | DC Supply Voltage | 10 | | 36.0 | V |
| $V_L$ | Input Logic Reference | 2.7 | 3.3 | 5.0 | V |
| $T_{amb}$ | Ambient Temperature | 0 | | 70 | °C |

(*) performances not guaranteed beyond recommended operating conditions

**Table 6. Thermal Data**

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $T_{j\text{-}case}$ | Thermal Resistance Junction to Case (thermal pad) | | | 1.5 | °C/W |
| $T_{jSD}$ | Thermal shut-down junction temperature | | 150 | | °C |
| $T_{warn}$ | Thermal warning temperature | | 130 | | °C |
| $t_{hSD}$ | Thermal shut-down hysteresis | | 25 | | °C |

**Table 7. Electrical Characteristcs:** refer to circuit in Fig.1 ($V_L$ = 3.3V; $V_{CC}$ = 32V; $R_L$ = 8Ω; fsw = 384KHz; $T_{amb}$ = 25°C unless otherwise specified)

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $R_{dsON}$ | Power Pchannel/Nchannel MOSFET RdsON | Id=1A | | 200 | 270 | mΩ |
| $I_{dss}$ | Power Pchannel/Nchannel leakage Idss | $V_{CC}$ =35V | | | 50 | µA |
| $g_N$ | Power Pchannel RdsON Matching | Id=1A | 95 | | | % |
| $g_P$ | Power Nchannel RdsON Matching | Id=1A | 95 | | | % |
| Dt_s | Low current Dead Time (static) | see test circuit no.1; see fig. 3 | | 10 | 20 | ns |
| Dt_d | High current Dead Time (dinamic) | L=22µH; C = 470nF; $R_L$ = 8 Ω Id=3.5A; see fig. 5 | | | 50 | ns |
| $t_{d\ ON}$ | Turn-on delay time | Resistive load | | | 100 | ns |
| $t_{d\ OFF}$ | Turn-off delay time | Resistive load | | | 100 | ns |
| $t_r$ | Rise time | Resistive load; as fig.3 | | | 25 | ns |
| $t_f$ | Fall time | Resistive load; as fig. 3 | | | 25 | ns |
| $V_{CC}$ | Supply voltage operating voltage | | 10 | | 36 | V |
| $V_{IN\text{-}H}$ | High level input voltage | | | | $V_L$/2 +300mV | V |

Obsolete Product(s) - Obsolete Product(s)

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{IN-L}$ | Low level input voltage | | $V_L$/2 - 300mV | | | V |
| $I_{IN-H}$ | High level Input current | Pin Voltage = $V_L$ | | 1 | | µA |
| $I_{IN-L}$ | Low level input current | Pin Voltage = 0.3V | | 1 | | µA |
| $I_{PWRDN-H}$ | High level PWRDN pin input current | $V_L$ = 3.3V | | 35 | | µA |
| $V_{LOW}$ | Low logical state voltage VLow (pin PWRDN, TRISTATE) (note 1) | $V_L$ = 3.3V | 0.8 | | | V |
| $V_{HIGH}$ | High logical state voltage VHigh (pin PWRDN, TRISTATE) (note 1) | $V_L$ = 3.3V | | | 1.7 | V |
| $I_{VCC-PWRDN}$ | Supply CURRENT from Vcc in Power Down | PWRDN = 0 | | | 3 | mA |
| $I_{FAULT}$ | Output Current pins FAULT -TH-WARN when FAULT CONDITIONS | Vpin = 3.3V | | 1 | | mA |
| $I_{VCC-hiz}$ | Supply Current from Vcc in Tri-state | $V_{CC}$ = 30V; Tri-state = 0 | | 22 | | mA |
| $I_{VCC}$ | Supply Current from Vcc in operation both channel switching) | $V_{CC}$ =30V; Input Pulse width = 50% Duty; Switching Frequency = 384KHz; No LC filters; | | 50 | | mA |
| $I_{VCC-q}$ | Isc (short circuit current limit) (note 2) | | 4 | 6 | 8 | A |
| $V_{UV}$ | Undervoltage protection threshold | | | 7 | | V |
| $t_{pw-min}$ | Output minimum pulse width | No load | 70 | | 150 | ns |

Notes: 1. The following table explains the $V_{LOW}$, $V_{HIGH}$ variation with $V_L$

**Table 8.**

| $V_L$ | $V_{LOW\ min}$ | $V_{HIGH\ max}$ | Unit |
|---|---|---|---|
| 2.7 | 0.7 | 1.5 | V |
| 3.3 | 0.8 | 1.7 | V |
| 5 | 0.85 | 1.85 | V |

Note 2: See relevant Application Note AN1994

**Table 9. Logic Truth Table (see fig. 4)**

| TRI-STATE | INxA | INxB | Q1 | Q2 | Q3 | Q4 | OUTPUT MODE |
|---|---|---|---|---|---|---|---|
| 0 | x | x | OFF | OFF | OFF | OFF | Hi-Z |
| 1 | 0 | 0 | OFF | OFF | ON | ON | DUMP |
| 1 | 0 | 1 | OFF | ON | ON | OFF | NEGATIVE |
| 1 | 1 | 0 | ON | OFF | OFF | ON | POSITIVE |
| 1 | 1 | 1 | ON | ON | OFF | OFF | Not used |

Obsolete Product(s) - Obsolete Product(s)

**Figure 4. Test Circuit.**

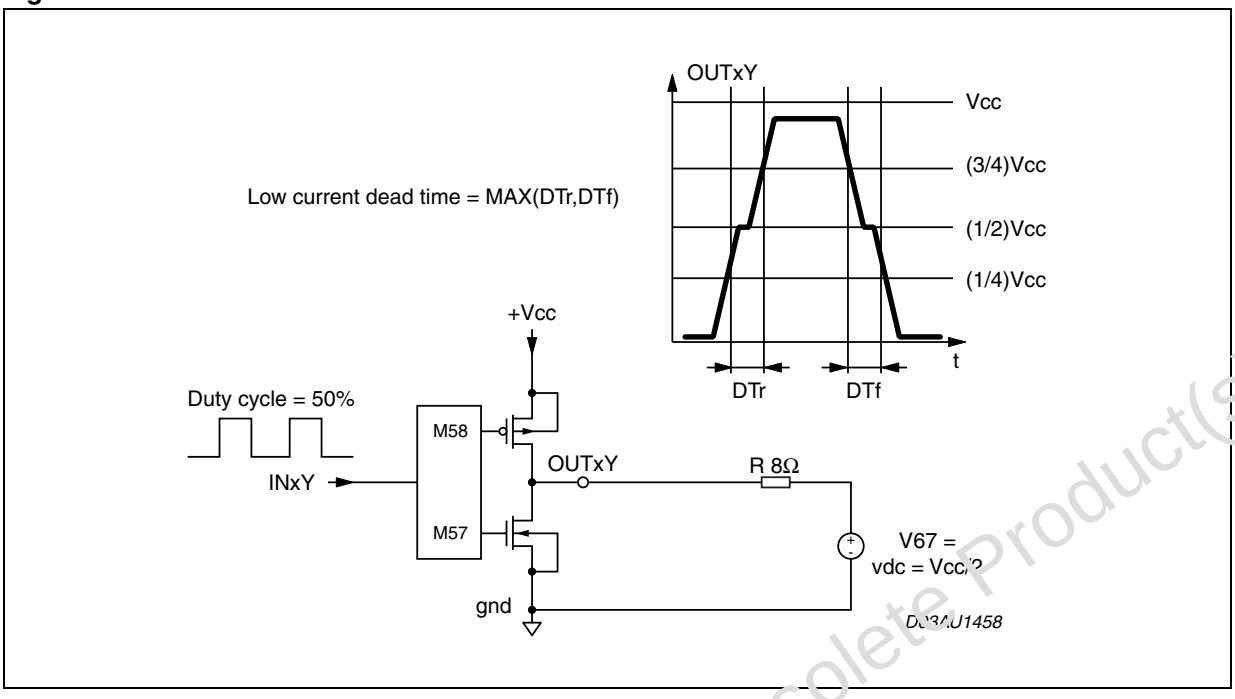



**Figure 5.**

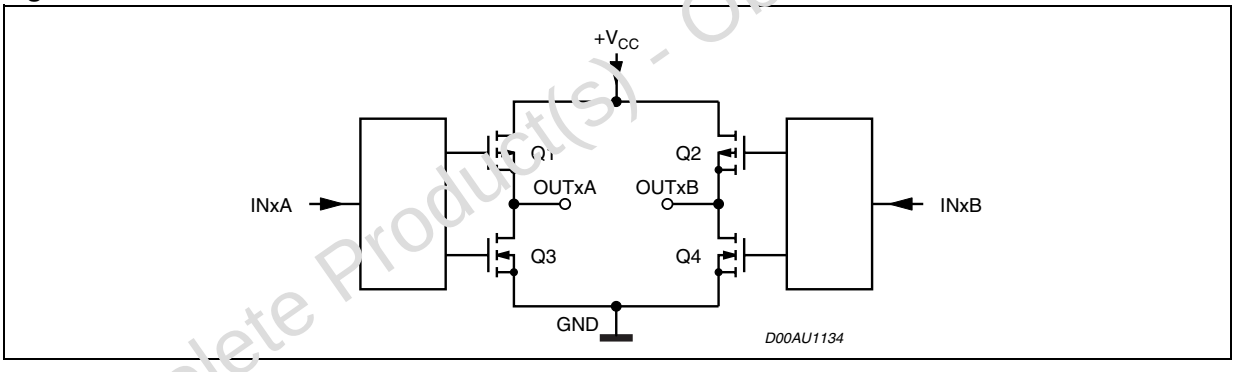
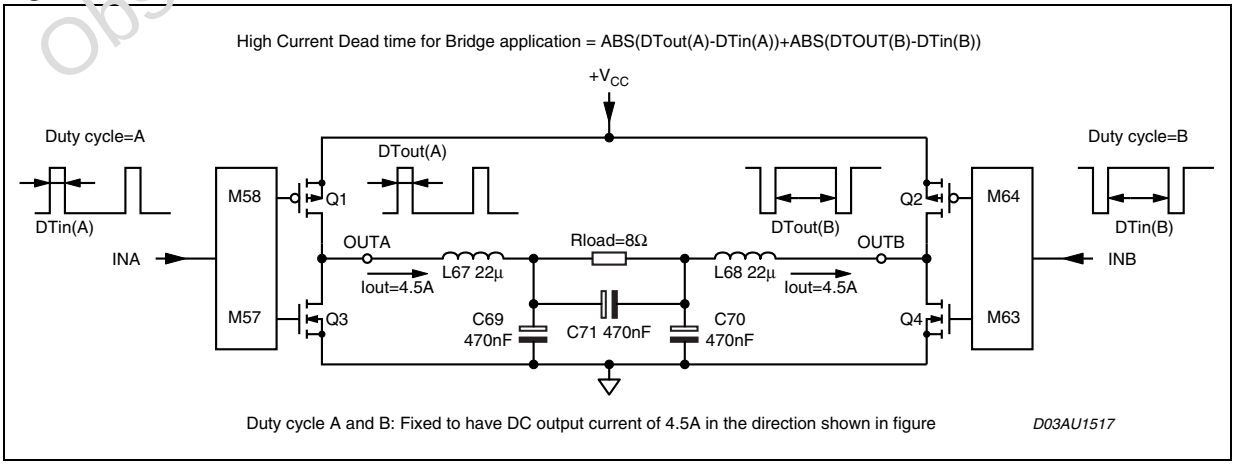



**Figure 6.**




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# 3 TECHNICAL INFO:

The STA506 is a dual channel H-Bridge that is able to deliver more than 60W per channel (@ THD=10%) of audio output power in high efficiency.

The STA506 converts both DDX and binary-controlled PWM signals into audio power at the load. It includes a logic interface , integrated bridge drivers, high efficiency MOSFET outputs and thermal and short circuit protection circuitry.

In DDX mode, two logic level signals per channel are used to control high-speed MOSFET switches to connect the speaker load to the input supply or to ground in a Bridge configuration, according to the damped ternary Modulation operation.

In Binary Mode operation , both Full Bridge and Half Bridge Modes are supported. The STA506 includes overcurrent and thermal protection as well as an under-voltage

Lockout with automatic recovery. A thermal warning status is also provided.

**Figure 7. STA506 Block Diagram Full-Bridge DDX® or Binary Modes**

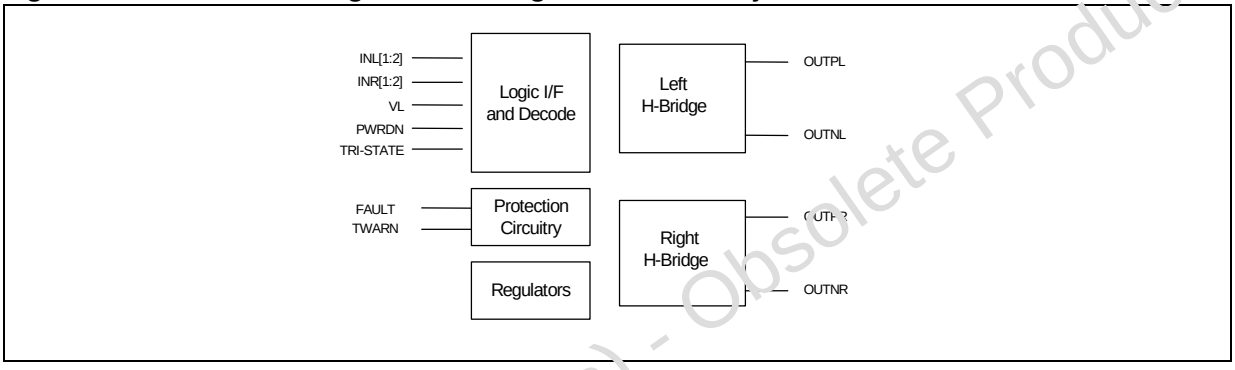
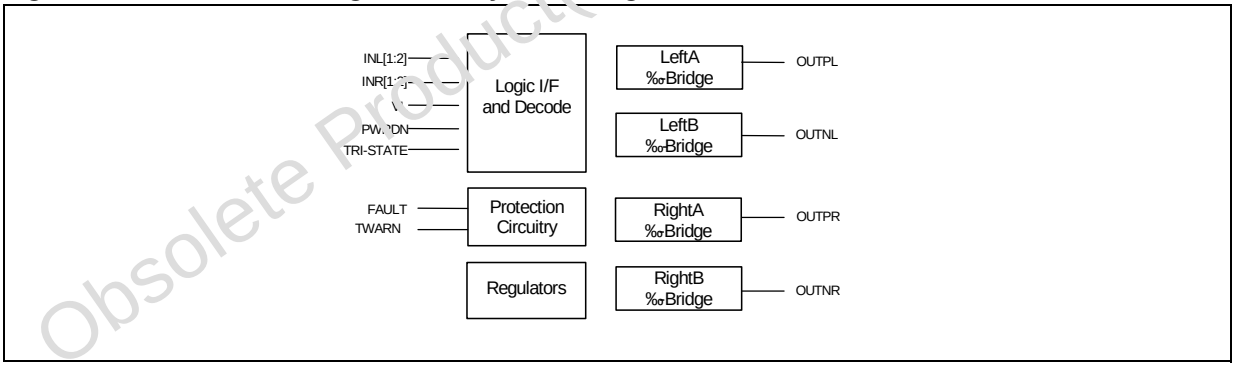



**Figure 8. STA506 Block Diagram Binary Half-Bridge Mode**




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## 3.1 Logic Interface and Decode:

The STA506 power outputs are controlled using one or two logic level timing signals. In order to provide a proper logic interface, the Vbias input must operate at the dame voltage as the DDX control logic supply.

## 3.2 Protection Circuitry:

The STA506 includes protection circuitry for over-current and thermal overload conditions. A thermal warning pin (pin.28) is activated low (open drain MOSFET) when the IC temperature exceeds 130C, in advance of the thermal shutdown protection. When a fault condition is detected , an internal fault signal acts to immediately disable the output power MOSFETs, placing both H-Bridges in high impedance state. At the same time an open-drain MOSFET connected to the fault pin (pin.27) is switched on.

There are two possible modes subsequent to activating a fault:

– **1) SHUTDOWN mode**: with FAULT (pull-up resistor) and TRI-STATE pins independent, an activated fault will disable the device, signaling low at the FAULT output.
The device may subsequently be reset to normal operation by toggling the TRI-STATE pin from High to Low to High using an external logic signal.

– **2) AUTOMATIC recovery mode:** This is shown in the Application Circuit of fig.1.
The FAULT and TRI-STATE pins are shorted together and connected to a time constant circuit comprising R59 and C58.
An activated FAULT will force a reset on the TRI-STATE pin causing normal operation to resume following a delay determined by the time constant of the circuit.
If the fault condition is still present , the circuit operation will continue repeating until the fault condition is removed .
An increase in the time constant of the circuit will produce a longer recovery interval. Care must be taken in the overall system design as not to exceed the protection thesholds under normal operation.

### 3.3 Power Outputs:

The STA506 power and output pins are duplicated to provide a low impedance path for the device's bridged outputs .

All duplicate power, ground and output pins must be connected for proper operation.

The PWRDN or TRI-STATE pins should be used to set all MOSFETS to the Hi-Z state during power-up until the logic power supply, $V_L$ , is settled.

### 3.4 Parallel Output / High Current Operation:

When using DDX Mode output , the STA506 outputs can be connected in parallel in order to increase the output current capability to a load.

In this configuration the STA506 can provide 80W into 8 ohm or up to 120W into 4ohm.

This mode of operation is enabled with the CONFIG pin (pin.24) connected to VREG1 and the inputs combined INLA=INLB, INRA=INRB and the outputs combined OUTLA=OTLB, OUTRA=OUTRB.

### 3.5 Additional Informations:

Output Filter: A passive 2nd-order passive filter is used on the STA506 power outputs to reconstruct an analog Audio Signal .

System performance can be significantly affected by the output filter design and choice of passive components. A filter design for 6ohm/8ohm loads is shown in the Typical Application circuit of fig.1. Figure 9 shows a filter design suitable for 4ohm loads.

Figure 10 shows a filter for ½ bridge mode , 4 ohm loads.

**Power Dissipation & Heat Sink requirements:** The power dissipated within the device will depend primarily on the supply voltage, load impedance and output modulation level.

The PowerSO36 package of the STA506 includes an exposed thermal slug on the top of the device to provide a direct thermal path from the IC to the heatsink.

Careful consideration must be given to the overall thermal design . See figure 8 for power derating

versus Slug temperature using different heatsinks and considering the Rth-jc =1.5°C/W.

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**Figure 9. STA506 Power Derating Curve**

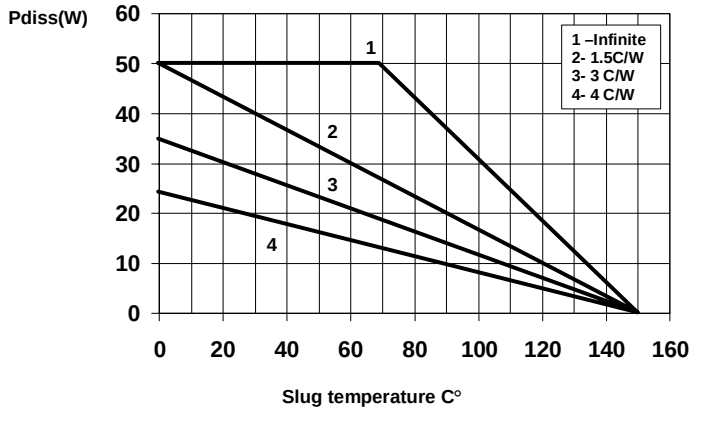
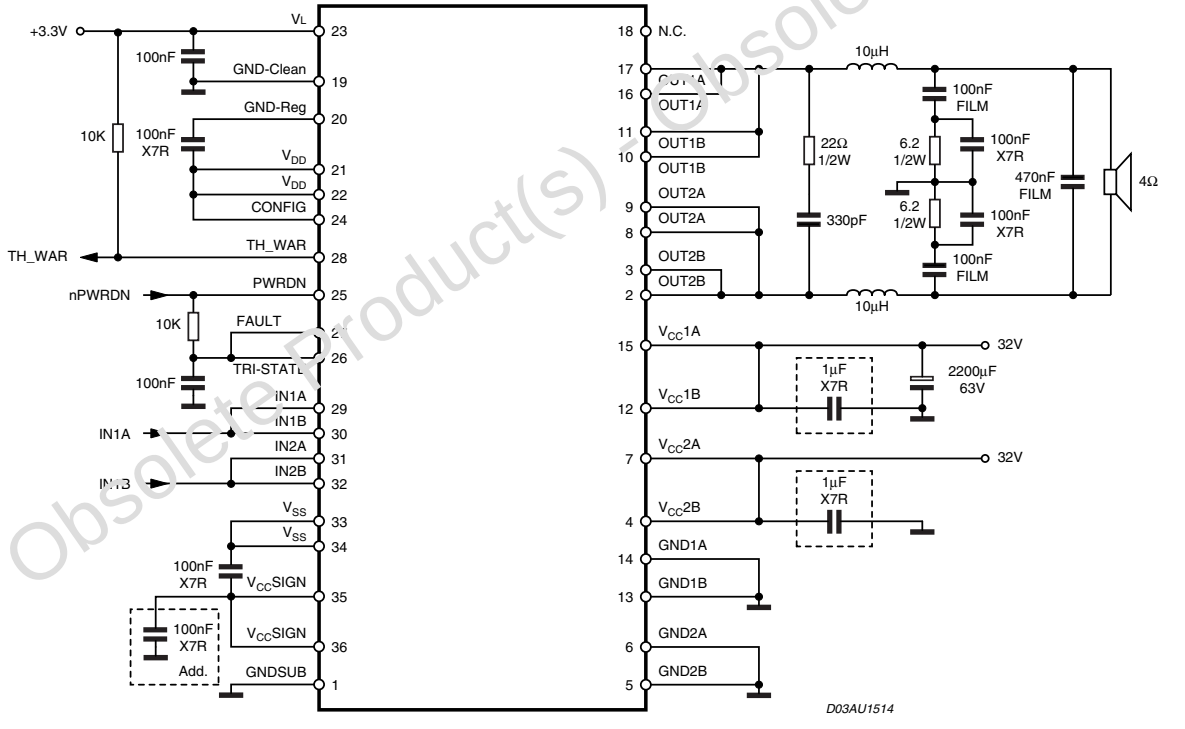


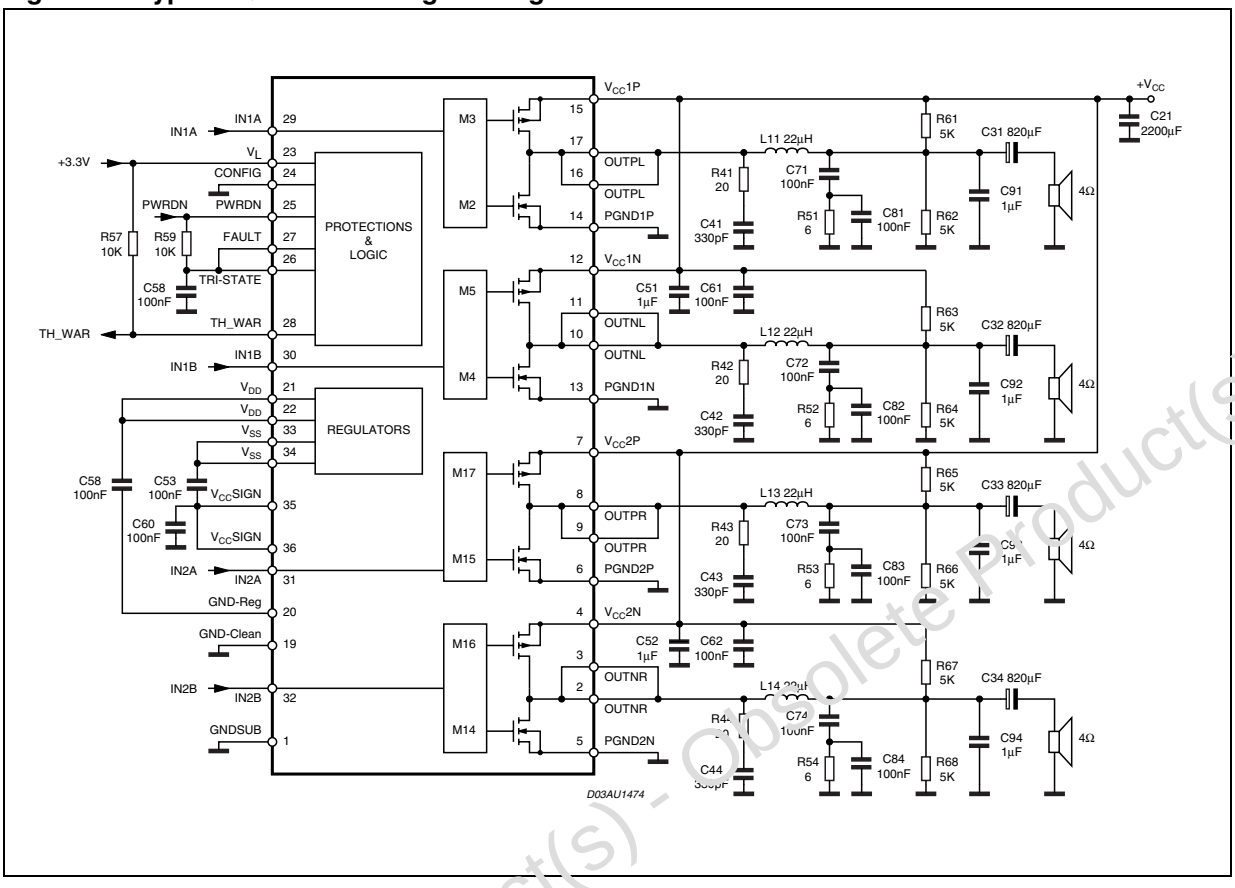

**Figure 10. Typical Single BTL Configurationto Obtain 120W @ THD 10%, $R_L$= 4Ω, $V_{CC}$ = 32V** (note 1))




Note: 1. "A PWM modulator as driver is needed . In particular, this result is performed using the STA30X+STA50X demo board". Peak Power for t ≤1sec

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**Figure 11. Typical Quad Half Bridge Configuration**




For more information refer to the application notes AN1456 and AN1661

Obsolete Product(s) - Obsolete Product(s)

**Figure 12. THD+N vs Frequency**

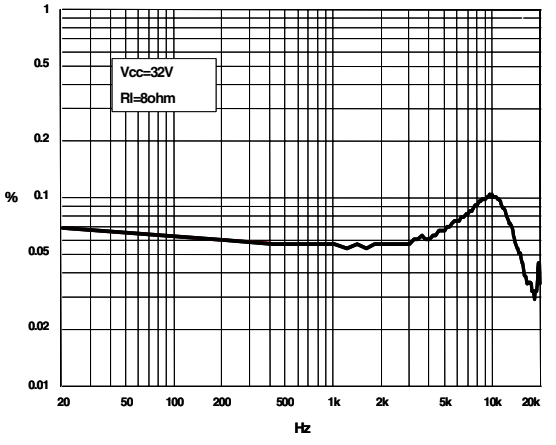



**Figure 13. Output Power vs Vsupply**

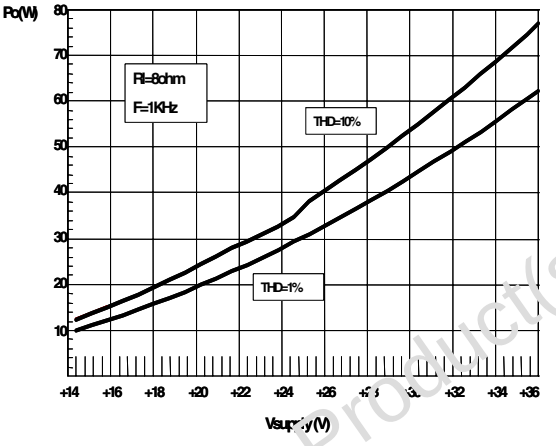



**Figure 14. THD+N vs Output Power**

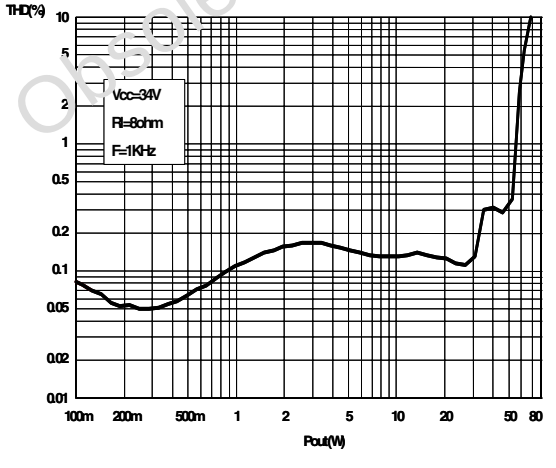



**Figure 15. THD+N vs Output Power**

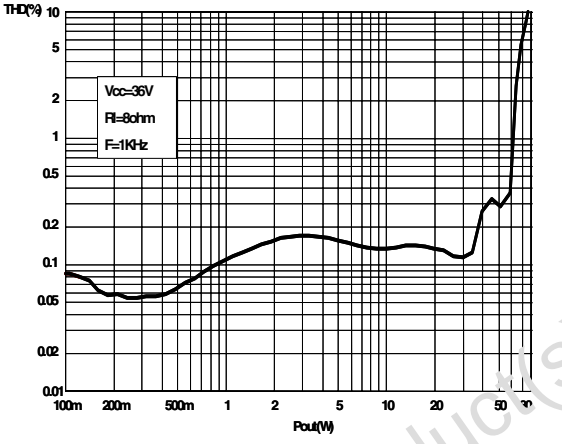
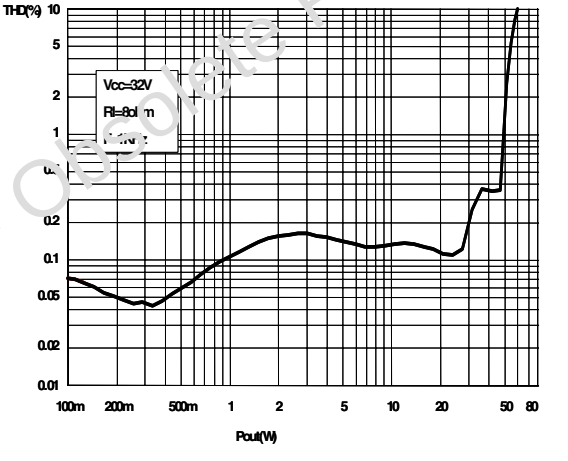



**Figure 16. THD+N vs Output PowerRevision**



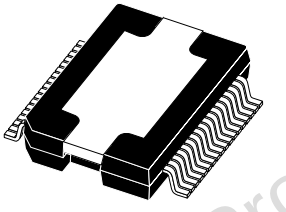

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**Figure 17. PowerSO36 (Slug Up) Mechanical Data & Package Dimensions**

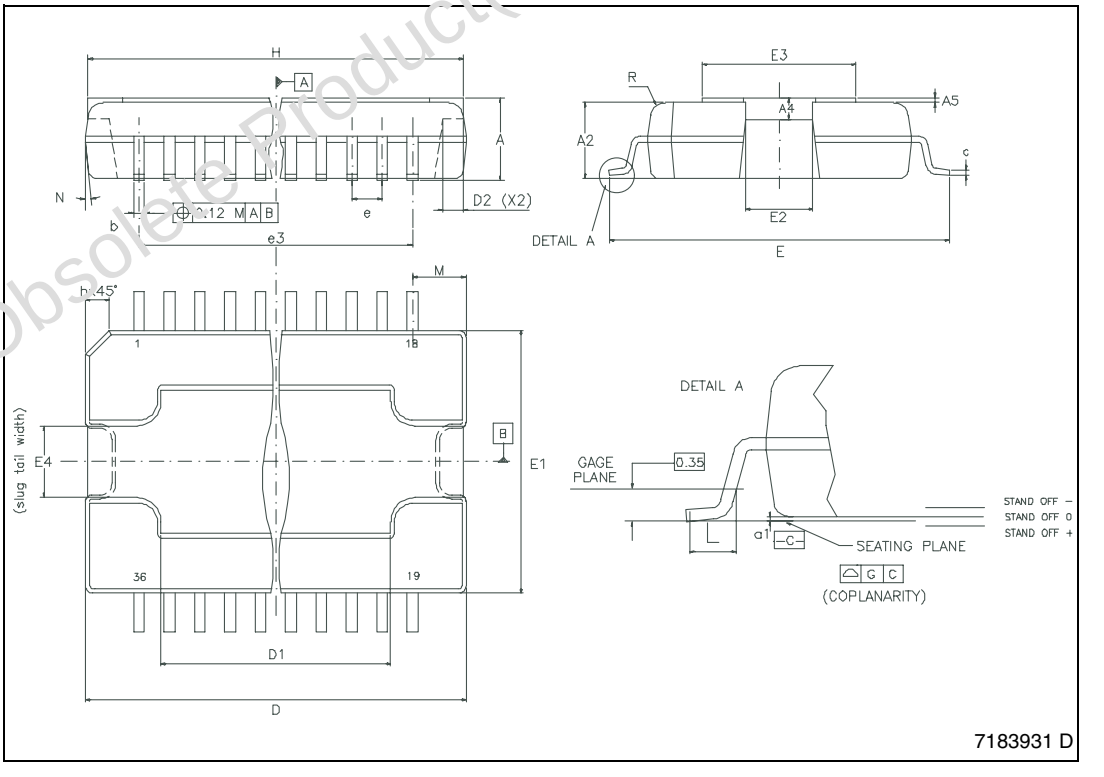
| DIM. | mm | | | inch | | |
|---|---|---|---|---|---|---|
| | MIN. | TYP. | MAX. | MIN. | TYP. | MAX. |
| A | 3.25 | | 3.43 | 0.128 | | 0.135 |
| A2 | 3.1 | | 3.2 | 0.122 | | 0.126 |
| A4 | 0.8 | | 1 | 0.031 | | 0.039 |
| A5 | | 0.2 | | | 0.008 | |
| a1 | 0.030 | | -0.040 | 0.0011 | | -0.0015 |
| b | 0.22 | | 0.38 | 0.008 | | 0.015 |
| c | 0.23 | | 0.32 | 0.009 | | 0.012 |
| D | 15.8 | | 16 | 0.622 | | 0.630 |
| D1 | 9.4 | | 9.8 | 0.37 | | 0.38 |
| D2 | | 1 | | | 0.039 | |
| E | 13.9 | | 14.5 | 0.547 | | 0.57 |
| E1 | 10.9 | | 11.1 | 0.429 | | 0.437 |
| E2 | | | 2.9 | | | 0.114 |
| E3 | 5.8 | | 6.2 | 0.228 | | 0.244 |
| E4 | 2.9 | | 3.2 | 0.114 | | 1.259 |
| e | | 0.65 | | | 0.026 | |
| e3 | | 11.05 | | | 0.435 | |
| G | 0 | | 0.075 | 0 | | 0.003 |
| H | 15.5 | | 15.9 | 0.61 | | 0.625 |
| h | | | 1.1 | | | 0.043 |
| L | 0.8 | | 1.1 | 0.031 | | 0.043 |
| N | | | 10° | | | 10° |
| s | | | 8° | | | 8° |

(1) "D and E1" do not include mold flash or protusions.
Mold flash or protusions shall not exceed 0.15mm (0.006")
(2) No intrusion allowed inwards the leads.

**OUTLINE AND MECHANICAL DATA**



**PowerSO36 (SLUG UP)**




Obsolete Product(s) - Obsolete Product(s)

**Table 10. Revision History**

| Date | Revision | Description of Changes |
|---|---|---|
| December 2003 | 1 | First Issue |
| April 2004 | 2 | Inserted Technical Info and Graphics |
| April 2004 | 3 | Small changes in pag 4 and 5 |
| June 2004 | 4 | Note 2: See relevant Application Note AN1994 |
| November 2004 | 5 | Changed Vcc from 9 min to 10 min |
| February 2006 | 6 | Changed $T_{op}$ value on Table 4. |

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