

NB3L8533

2.5V/3.3V Differential 2:1 MUX to 4 LVPECL Fanout Buffer

Description

The NB3L8533 is a low skew 1:4 LVPECL Clock fanout buffer designed explicitly for low output skew applications.

The NB3L8533 features a multiplexed input which can be driven by either a differential or single-ended input to allow for the distribution of a lower speed clock along with the high speed system clock.

The CLK_SEL pin will select the differential clock inputs, CLK and $\overline{\text{CLK}}$, when LOW (or left open and pulled LOW by the internal pull-down resistor). When CLK_SEL is HIGH, the Differential PCLK and $\overline{\text{PCLK}}$ inputs are selected.

The common enable (CLK_EN) is synchronous so that the outputs will only be enabled/disabled when they are already in the LOW state. This avoids any chance of generating a runt clock pulse when the device is enabled/disabled as can happen with an asynchronous control. The internal flip flop is clocked on the falling edge of the input clock, therefore, all associated specification limits are referenced to the negative edge of the clock input.

Features

- 650 MHz Maximum Clock Output Frequency
- CLK/ $\overline{\text{CLK}}$ can Accept LVPECL, LVDS, HCSL, STTL and HSTL
- PCLK/ $\overline{\text{PCLK}}$ can Accept LVPECL, LVDS, CML and SSTL
- Four Differential LVPECL Clock Outputs
- 1.5 ns Maximum Propagation Delay
- Operating Range: $V_{CC} = 2.375 \text{ V}$ to 3.630 V
- LVCMOS Compatible Control Inputs
- Selectable Differential Clock Inputs
- Synchronous Clock Enable
- 30 ps Max. Skew Between Outputs
- -40°C to $+85^{\circ}\text{C}$ Ambient Operating Temperature Range
- TSSOP-20 Package
- These are Pb-Free Devices

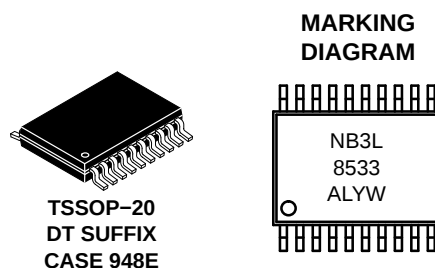
Applications

- Computing and Telecom
- Routers, Servers and Switches
- Backplanes



ON Semiconductor®

www.onsemi.com



TSSOP-20
DT SUFFIX
CASE 948E

A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb-Free Package

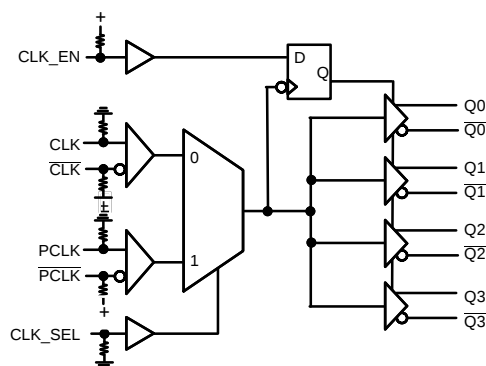


Figure 1. Simplified Logic Diagram of NB3L8533

ORDERING INFORMATION

See detailed ordering and shipping information on page 8 of this data sheet.

NB3L8533

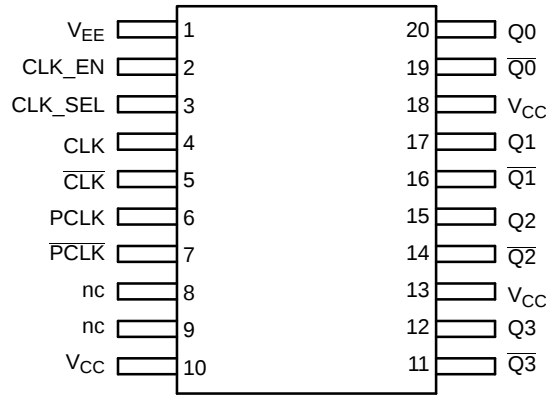


Figure 2. Pinout Diagram (Top View)

Table 1. FUNCTIONS

Inputs			Outputs		
CLK_EN	CLK_SEL	Input Function	Output Function	Qx	Qx
0	0	CLK input selected	Disabled	LOW	HIGH
0	1	PCLK Inputs Selected	Disabled	LOW	HIGH
1	0	CLK input selected	Enabled	CLK	Invert of CLK
1	1	PCLK Inputs Selected	Enabled	PCLK	Invert of PCLK

1. After CLK_EN switches, the clock outputs are disabled or enabled following a rising and falling input clock edge as show in Figure 3.

Table 2. PIN DESCRIPTION

Pin Number	Name	I/O	Open Default	Description
1	VEE	Power		Negative (Ground) Power Supply pin must be externally connected to power supply to guarantee proper operation.
2	CLK_EN	LVCMOS/LVTTL Input	Pull-up	Synchronized Clock Enable when HIGH. When LOW, outputs are disabled (Qx HIGH, Qx LOW)
3	CLK_SEL	LVCMOS/LVTTL Input	Pull-down	Clock Input Select (HIGH selects PCLK, LOW selects CLK input)
4	CLK	Input	Pull-down	Non-inverted Differential Clock Input. Float open when unused.
5	CLK	Input	Pull-up	Inverted Differential Clock Input. Float open when unused.
6	PCLK	Input	Pull-down	Non-inverted Differential Clock Input. Float open when unused.
7	PCLK	Input	Pull-up	Inverted Differential Clock Input. Float open when unused.
8	NC			No Connect
9	NC			No Connect
10	VCC	Power		Positive Power Supply pins must be externally connected to power supply to guarantee proper operation.
11	Q3	LVPECL Output		Complement Differential Output
12	Q3	LVPECL Output		True Differential Output
13	VCC	Power		Positive Power Supply pins must be externally connected to power supply to guarantee proper operation.
14	Q2	LVPECL Output		Complement Differential Output
15	Q2	LVPECL Output		True Differential Output
16	Q1	LVPECL Output		Complement Differential Output
17	Q1	LVPECL Output		True Differential Output
18	VCC	Power		Positive Power Supply pins must be externally connected to power supply to guarantee proper operation.
19	Q0	LVPECL Output		Complement Differential Output
20	Q0	LVPECL Output		True Differential Output

Table 3. ATTRIBUTES (Note 2)

Characteristics		Value
ESD Protection	Human Body Model Machine Model	> 2 kV > 200 V
R _{PU} – Pull-up Resistor		50 kΩ
R _{PD} – Pull-down Resistor		50 kΩ
Moisture Sensitivity (Note 2)	TSSOP-20	Level 1
Flammability Rating	Oxygen Index: 28 to 34	UL 94 V-0 @ 0.125 in
Transistor Count		289
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test		

2. For additional information, see Application Note AND8003/D.

Table 4. MAXIMUM RATINGS

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
V _{CC}	Positive Power Supply Voltage	V _{EE} = 0 V		4.6	V
V _I	Input Voltage	V _{EE} = 0 V	V _I ≤ V _{CC}	–0.5 to V _{CC} + 0.5	V
I _{out}	Output Current	Continuous Surge		50 100	mA mA
T _A	Operating Temperature Range			–40 to +85	°C
T _{stg}	Storage Temperature Range			–65 to +150	°C
θ _{JA}	Thermal Resistance (Junction-to-Ambient)	0 lfpm 500 lfpm	TSSOP-20 TSSOP-20	140 50	°C/W
θ _{JC}	Thermal Resistance (Junction-to-Case)	Standard Board	TSSOP-20	23 to 41	°C/W
T _{sol}	Wave Solder			265	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Table 5. DC CHARACTERISTICS $V_{CC} = 2.375\text{ V to }3.630\text{ V}$; $V_{EE} = 0\text{ V}$; $T_A = -40^\circ\text{C to }+85^\circ\text{C}$ (Note 3)

Symbol	Characteristic	Min	Typ	Max	Unit
POWER SUPPLY					
V_{CC}	Power Supply Voltage	2.375		3.630	V
I_{EE}	Power Supply Current (Outputs Open)			40	mA
LVPECL OUTPUTS (Note 4)					
V_{OH}	Output HIGH Voltage	$V_{CC}-1.4$		$V_{CC}-0.9$	V
V_{OL}	Output LOW Voltage	$V_{CC}-2.0$		$V_{CC}-1.7$	V
V_{SWING}	Output Voltage Swing, Peak-to-Peak	0.6		1.0	V
DIFFERENTIAL INPUTS DRIVEN DIFFERENTIALLY (see Figure 5) (Note 7)					
V_{IHD}	Differential Input HIGH Voltage CLK PCLK	0.5 1.5		$V_{CC}-0.85$	V
V_{ILD}	Differential Input LOW Voltage CLK PCLK	0 0.5		$V_{IHD}-0.15$ $V_{IHD}-0.30$	V
V_{CMR}	Common Mode Input Voltage; (Note 8) CLK/CLKb PCLK/PCLKb	0.5 1.5		$V_{CC}-0.85$	V
V_{ID}	Differential Input Voltage ($V_{IHD}-V_{ILD}$) CLK/CLKb PCLK/PCLKb	0.15 0.3		1.3 1.0	V
I_{IH}	Input HIGH Current $V_{IN} = V_{CC} = 3.630\text{ V}$ CLK, PCLK CLKb, PCLKb			150 5	μA
I_{IL}	Input LOW Current $V_{IN} = 0\text{ V}$, $V_{CC} = 3.630\text{ V}$ CLK, PCLK CLKb, PCLKb	-5 -150			μA
LVC MOS/LVTTL INPUTS (CLK_EN, CLK_SEL)					
V_{IH}	Input HIGH Voltage	2.0		$V_{CC}+0.3$	V
V_{IL}	Input LOW Voltage	-0.3		0.8	V
I_{IH}	Input HIGH Current $V_{IN} = V_{CC} = 3.630\text{ V}$ CLK_EN CLK_SEL			5 150	μA
I_{IL}	Input Low Current $V_{IN} = 0\text{ V}$, $V_{CC} = 3.630\text{ V}$ CLK_EN CLK_SEL	-150 -5			μA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

- Input and Output parameters vary 1:1 with V_{CC} .
- LVPECL outputs loaded with $50\ \Omega$ to $V_{CC} - 2\text{ V}$ for proper operation.
- V_{IH} , V_{IL} , V_{th} and V_{ISE} parameters must be complied with simultaneously.
- V_{th} is applied to the complementary input when operating in single-ended mode.
- V_{IHD} , V_{ILD} , V_{ID} and V_{CMR} parameters must be complied with simultaneously.
- The common mode voltage is defined as V_{IH} .

Table 6. AC CHARACTERISTICS, $V_{CC} = 2.375\text{ V to }3.630\text{ V}$, $T_A = -40^\circ\text{C to }+85^\circ\text{C}$ (Note 9)

Symbol	Characteristic		Min	Typ	Max	Unit
f_{MAX}	Maximum Input Clock Frequency: $V_{OUTpp} \geq 300\text{ mV}$				650	MHz
Φ_N	Phase Noise, $f_C = 156.25\text{ MHz}$	100 Hz 1 kHz 10 kHz 100 kHz 1 MHz 10 MHz 20 MHz	Offset from Carrier	-124.4 -136.1 -144.2 -153.3 -156.2 -156.2 -156.4		dBc/Hz
t_{PLH} , t_{PHL}	Propagation Delay to Differential Outputs, @ 50 MHz (Figures 6 and 7) ($V_{CC} = 3.3\text{ V}$)	Note 10 Note 11	CLK/ $\overline{\text{CLK}}$ to Q/ $\overline{\text{Q}}$ PCLK/PCLK to Q/ $\overline{\text{Q}}$	1.0	1.55	ns
$t_{j\Phi N}$	Additive Phase Jitter, RMS; $f_C = 156.25\text{ MHz}$, Integration Range: 12 kHz – 20 MHz			0.05		ps
$tsk(o)$	Output-to-output skew; (Note 12)				30	ps
$tsk(pp)$	Part-to-Part Skew; (Note 13)				150	ps
V_{INpp}	Input Voltage Swing/Sensitivity (Differential Configuration) (Note 15)		150		1300	mV
t_r/t_f	Output rise and fall times, 20% to 80%, @ 50 MHz		$Q_n, \overline{Q}_n$	250	600	ps
ODC	Output Clock Duty Cycle		47		53	%

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

All parameters measured at f_{MAX} unless noted otherwise.

The cycle-to-cycle jitter on the input will equal the jitter on the output. The part does not add jitter

9. Measured using a $V_{INPPmin}$ source, Reference Duty Cycle = 50% duty cycle clock source. All output loading with external $50\ \Omega$ to $V_{CC} - 2\text{ V}$.

10. Measured from the differential input crossing point to the differential output crossing point.

11. Measured from $V_{CC}/2$ input crossing point to the differential output crossing point.

12. Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the output differential cross points.

13. Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.

14. Output voltage swing is a single-ended measurement operating in differential mode.

15. Input voltage swing is a single-ended measurement operating in differential mode.

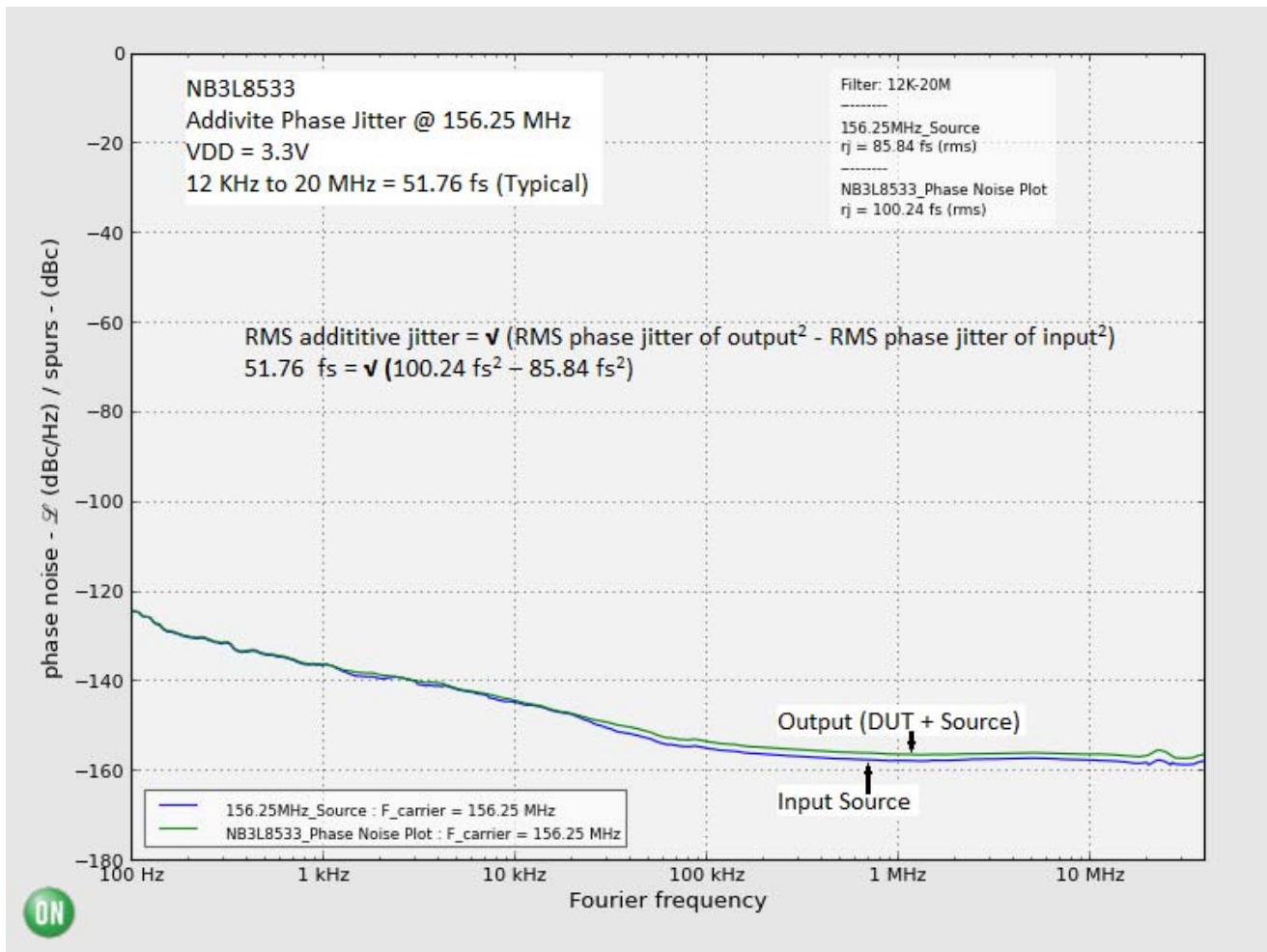


Figure 3. Typical Phase Noise Plot at $f_{\text{carrier}} = 156.25 \text{ MHz}$ at an Operating Voltage of 3.3 V, Room Temperature

The above phase noise data was captured using Agilent E5052A/B. The data displays the input phase noise and output phase noise used to calculate the additive phase jitter at a specified integration range. The RMS Phase Jitter contributed by the device (integrated between 12 kHz and 20 MHz) is 51.76 fs.

The additive phase jitter performance of the fanout buffer is highly dependent on the phase noise of the input source.

To obtain the most accurate additive phase noise measurement, it is vital that the source phase noise be notably lower than that of the DUT. If the phase noise of the source is greater than the device under test output, the source noise will dominate the additive phase jitter calculation and lead to an artificially low result for the additive phase noise measurement within the integration range.

$$\text{RMS additive jitter} = \sqrt{\text{RMS phase jitter of output}^2 - \text{RMS phase jitter of input}^2}$$

$$51.76 \text{ fs} = \sqrt{100.24 \text{ fs}^2 - 85.84 \text{ fs}^2}$$

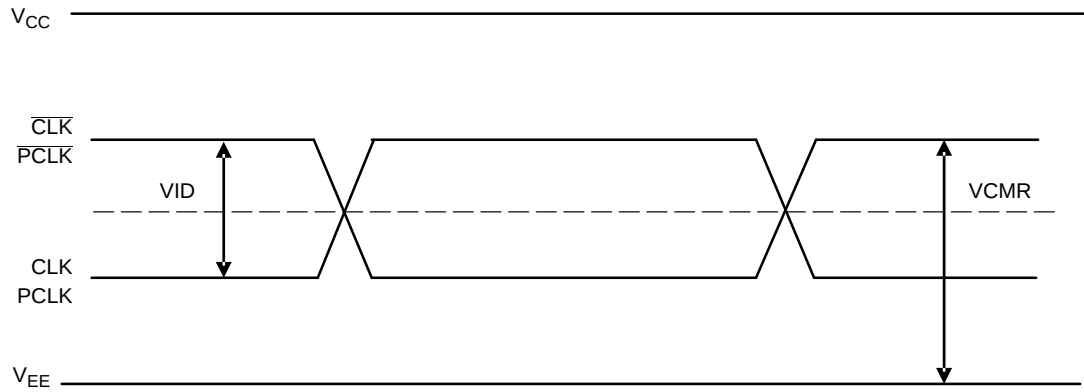


Figure 4. VCMR Diagram

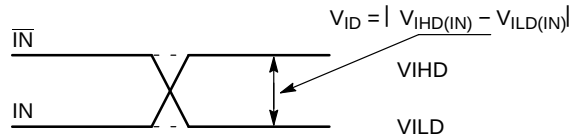


Figure 5. Differential Inputs Driven Differentially

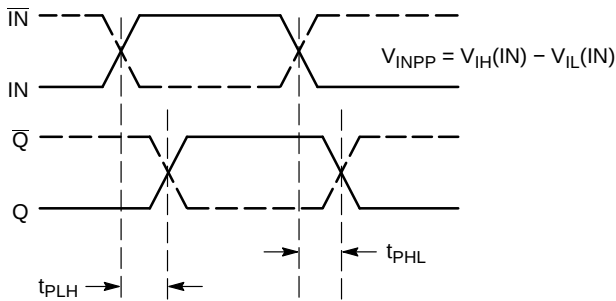


Figure 6. AC Reference Measurement

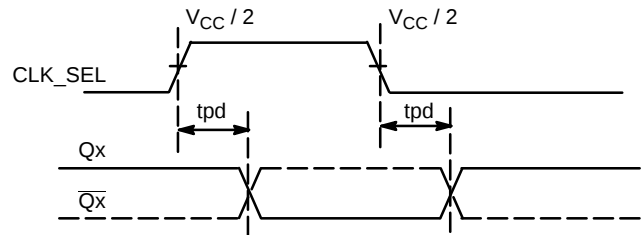


Figure 7. CLK_SEL to Qx Timing Diagram

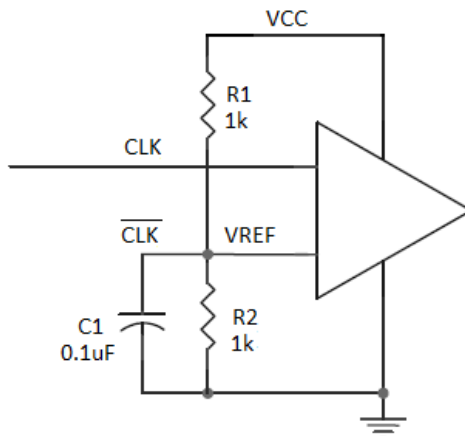


Figure 8. Differential Input Driven Single-ended

Differential Clock Input to Accept Single-ended Input

Figure 8 shows how the CLK input can be driven by a single-ended Clock signal. C1 is connected to the V_{ref} node

as a bypass capacitor. Locate these components close the device pins. R1 and R2 must be adjusted to position V_{ref} to the center of the input swing on CLK.

NB3L8533

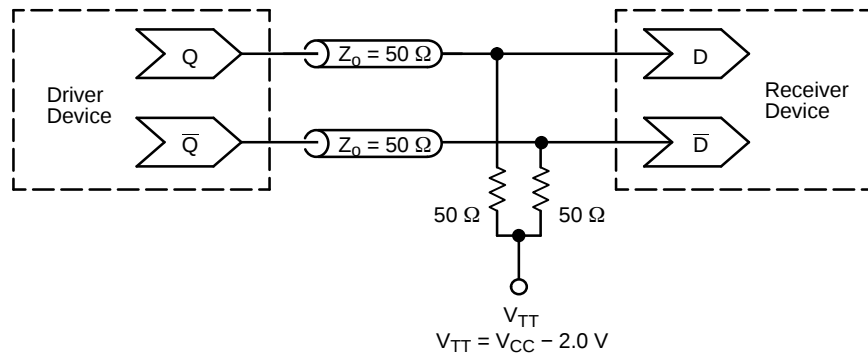


Figure 9. Typical Termination for Output Driver and Device Evaluation
 (See Application Note AND8020/D – Termination of ECL Logic Devices.)

ORDERING INFORMATION

Device	Package	Shipping [†]
NB3L8533DTG	TSSOP-20 (Pb-Free)	75 Units / Rail
NB3L8533DTR2G	TSSOP-20 (Pb-Free)	2500 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

ON Semiconductor and the  are registered trademarks of Semiconductor Components Industries, LLC (SCILLC) or its subsidiaries in the United States and/or other countries. SCILLC owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of SCILLC's product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free
USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81-3-5817-1050

ON Semiconductor Website: www.onsemi.com

Order Literature: <http://www.onsemi.com/orderlit>

For additional information, please contact your local Sales Representative