NSS40300MZ4

Bipolar Power Transistors 40 V, 3.0 A, Low $V_{CE(sat)}$ PNP Transistor

ON Semiconductor's e^2PowerEdge family of low $V_{CE(sat)}$ transistors are surface mount devices featuring ultra low saturation voltage ($V_{CE(sat)}$) and high current gain capability. These are designed for use in low voltage, high speed switching applications where affordable efficient energy control is important.

Typical applications are DC−DC converters and power management in portable and battery powered products such as cellular and cordless phones, PDAs, computers, printers, digital cameras and MP3 players. Other applications are low voltage motor controls in mass storage products such as disc drives and tape drives. In the automotive industry they can be used in air bag deployment and in the instrument cluster. The high current gain allows e^2PowerEdge devices to be driven directly from PMU's control outputs, and the Linear Gain (Beta) makes them ideal components in analog amplifiers.

Features

- Complement to NSS40301MZ4 Series
- NSV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q101 Qualified and PPAP Capable
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Collector−Emitter Voltage	V_{CEO}	40	Vdc
Collector−Base Voltage	V_{CB}	40	Vdc
Emitter−Base Voltage	V_{EB}	6.0	Vdc
Base Current − Continuous	I_B	1.0	Adc
Collector Current − Continuous	I_C	3.0	Adc
Collector Current − Peak	I_{CM}	5.0	Adc
Total Power Dissipation Total P_D @ T_A = 25°C (Note 1) Total P_D @ T_A = 25°C (Note 2)	P_D	 2.0 0.80	W
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−55 to +150	°C

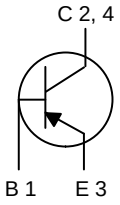
Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Mounted on 1" sq. (645 sq. mm) Collector pad on FR−4 bd material.
2. Mounted on 0.012" sq. (7.6 sq. mm) Collector pad on FR−4 bd material.

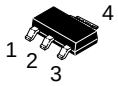
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http://onsemi.com

PNP TRANSISTOR
3.0 AMPERES
40 VOLTS, 2.0 WATTS

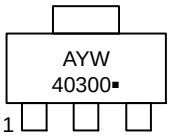


Schematic



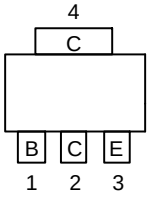
SOT−223
CASE 318E
STYLE 1

MARKING DIAGRAM



A	= Assembly Location
Y	Year
W	= Work Week
40300	= Specific Device Code
▪	= Pb−Free Package

PIN ASSIGNMENT



Top View Pinout

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

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THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction−to−Case Junction−to−Ambient on 1” sq. (645 sq. mm) Collector pad on FR−4 bd material Junction−to−Ambient on 0.012” sq. (7.6 sq. mm) Collector pad on FR−4 bd material	 $R_{\theta JA}$ $R_{\theta JA}$	 64 155	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8” from case for 5 seconds	T_L	260	°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector−Emitter Sustaining Voltage (I_C = 10 mAdc, I_B = 0 Adc)	$V_{CEO(sus)}$	40	−	−	Vdc
Emitter−Base Voltage (I_E = 50 μAdc, I_C = 0 Adc)	V_{EBO}	6.0	−	−	Vdc
Collector Cutoff Current (V_{CB} = 40 Vdc)	I_{CBO}	−	−	100	nAdc
Emitter Cutoff Current (V_{BE} = 6.0 Vdc)	I_{EBO}	−	−	100	nAdc
ON CHARACTERISTICS (Note 3)					
Collector−Emitter Saturation Voltage (I_C = 0.5 Adc, I_B = 50 mAdc) (I_C = 1.0 Adc, I_B = 20 mAdc) (I_C = 3.0 Adc, I_B = 0.3 Adc)	$V_{CE(sat)}$	 − − −	 − − −	 0.070 0.150 0.400	Vdc
Base−Emitter Saturation Voltage (I_C = 1.0 Adc, I_B = 0.1 Adc)	$V_{BE(sat)}$	−	−	1.0	Vdc
Base−Emitter On Voltage (I_C = 1.0 Adc, V_{CE} = 2.0 Vdc)	$V_{BE(on)}$	−	−	0.9	Vdc
DC Current Gain (I_C = 0.5 Adc, V_{CE} = 1.0 Vdc) (I_C = 1.0 Adc, V_{CE} = 1.0 Vdc) (I_C = 3.0 Adc, V_{CE} = 1.0 Vdc)	h_{FE}	 200 175 100	 − − −	 − 350 −	−
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 10 Vdc, f = 1.0 MHz)	C_{ob}	−	40	−	pF
Input Capacitance (V_{EB} = 5.0 Vdc, f = 1.0 MHz)	C_{ib}	−	130	−	pF
Current−Gain − Bandwidth Product (Note 4) (I_C = 500 mA, V_{CE} = 10 V, F_{test} = 1.0 MHz)	f_T	 −	 160	 −	MHz

3. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
4. $f_T = |h_{FE}| \bullet f_{test}$

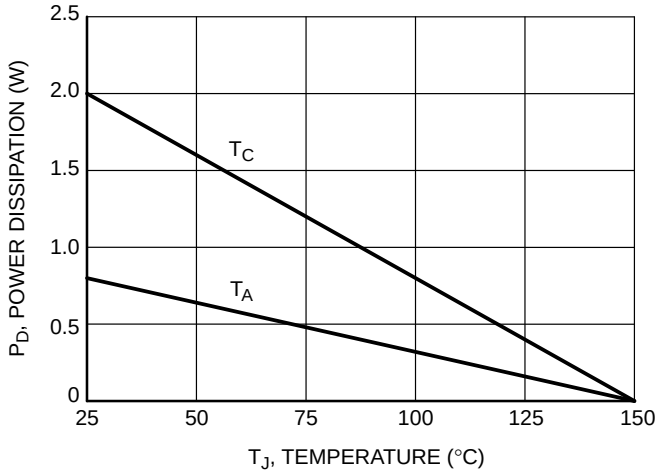


Figure 1. Power Derating

TYPICAL CHARACTERISTICS

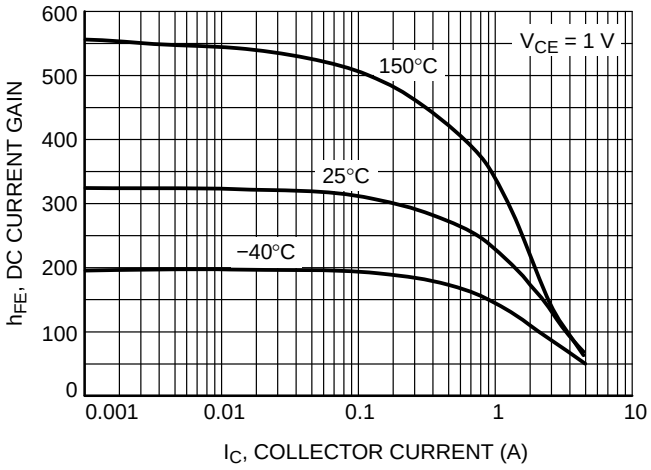


Figure 2. DC Current Gain

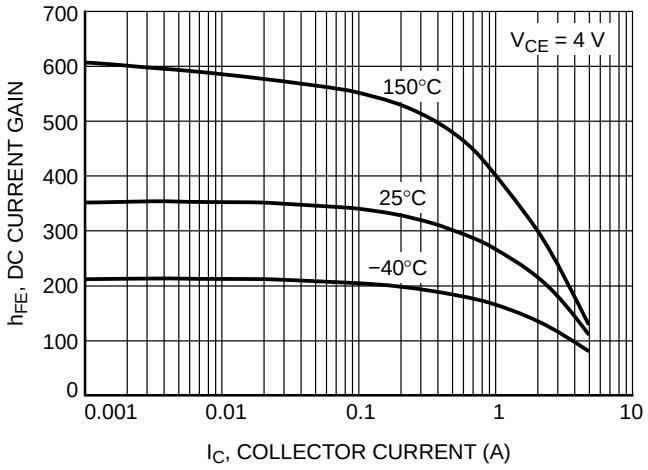


Figure 3. DC Current Gain

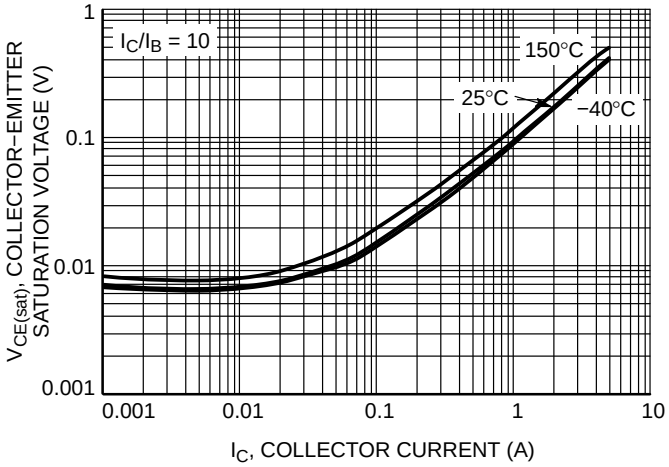


Figure 4. Collector−Emitter Saturation Voltage

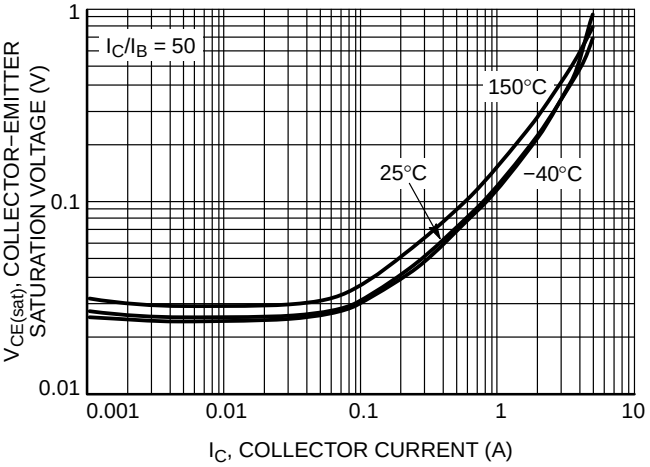


Figure 5. Collector−Emitter Saturation Voltage

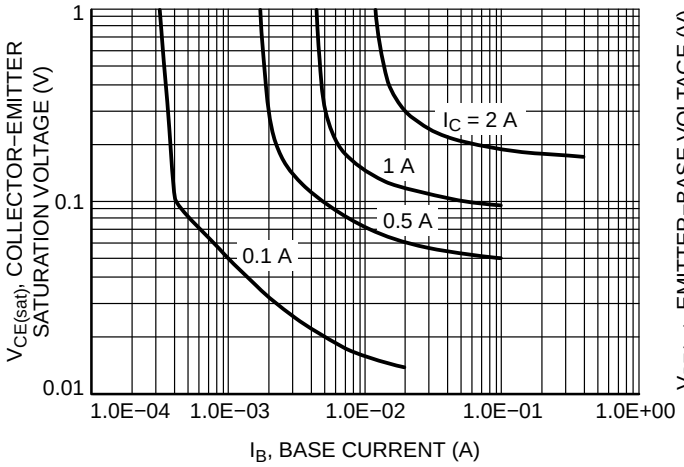


Figure 6. Collector Saturation Region

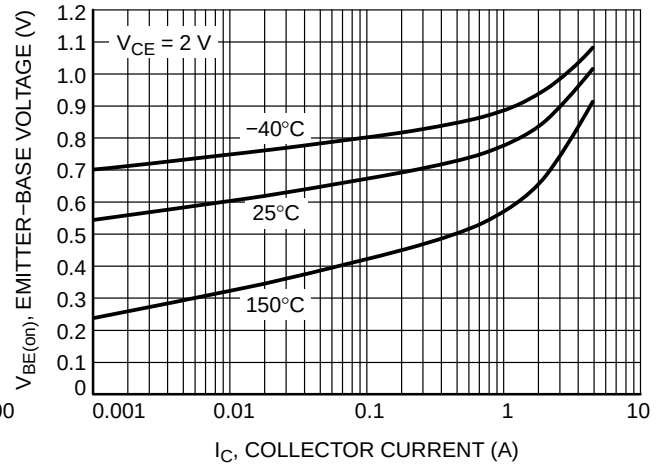


Figure 7. $V_{BE(on)}$ Voltage

TYPICAL CHARACTERISTICS

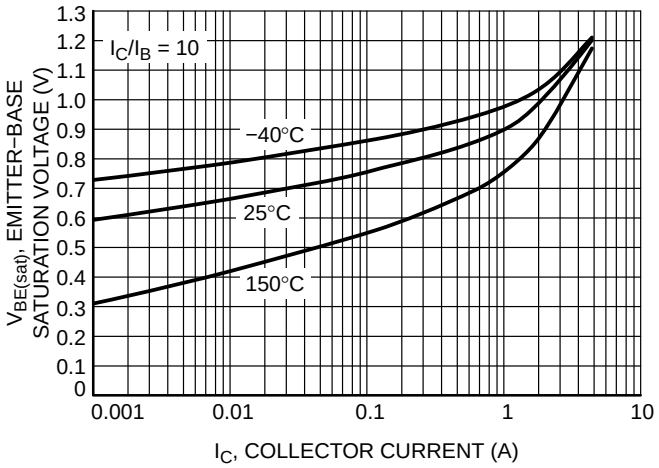


Figure 8. Base−Emitter Saturation Voltage

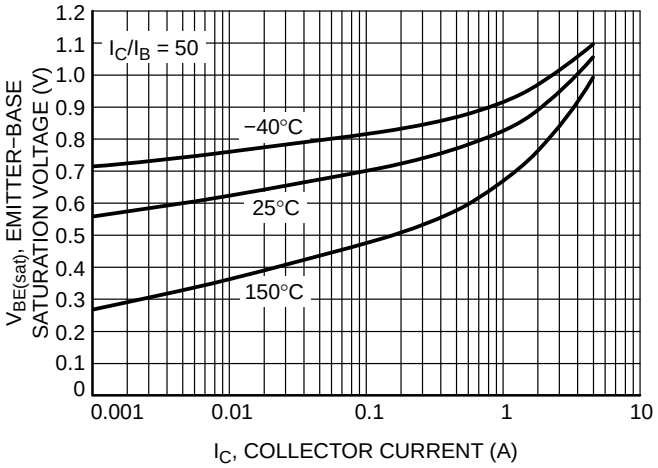


Figure 9. Base−Emitter Saturation Voltage

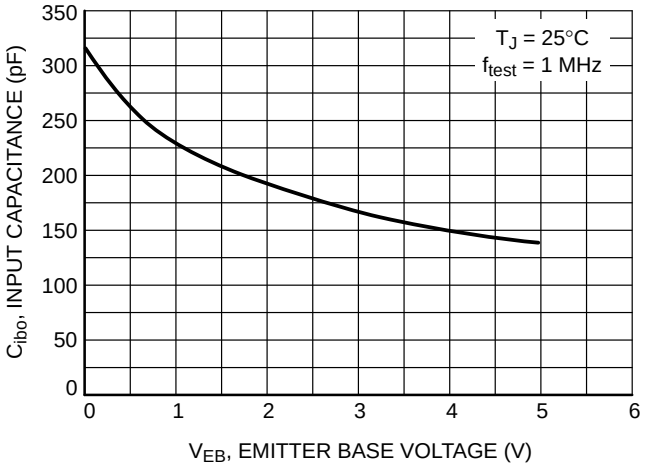


Figure 10. Input Capacitance

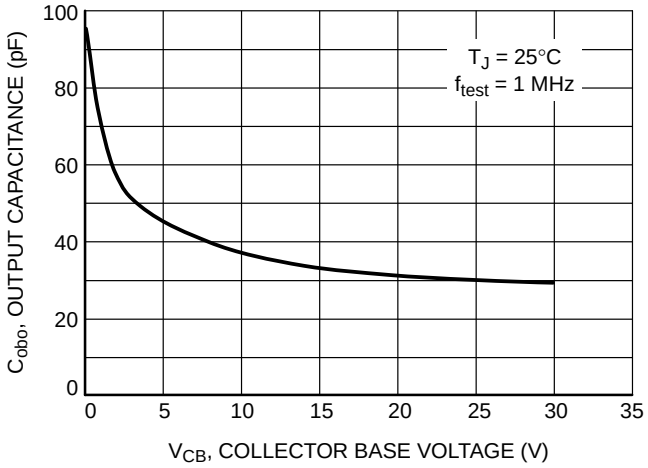


Figure 11. Output Capacitance

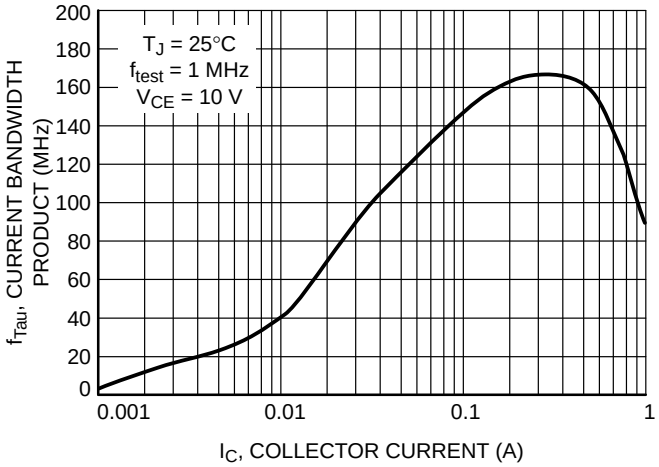


Figure 12. Current−Gain Bandwidth Product

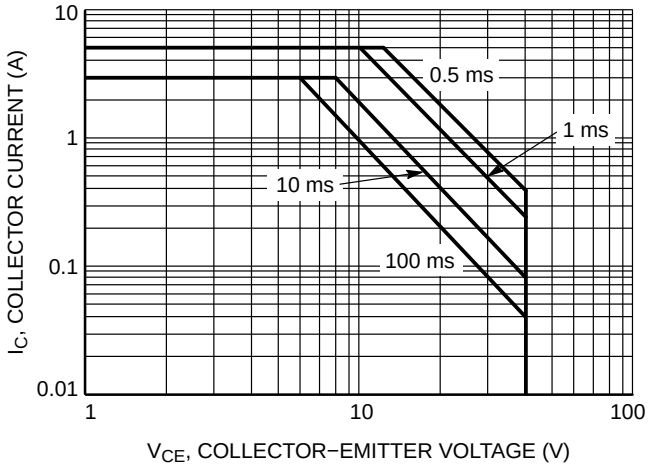


Figure 13. Safe Operating Area

ORDERING INFORMATION

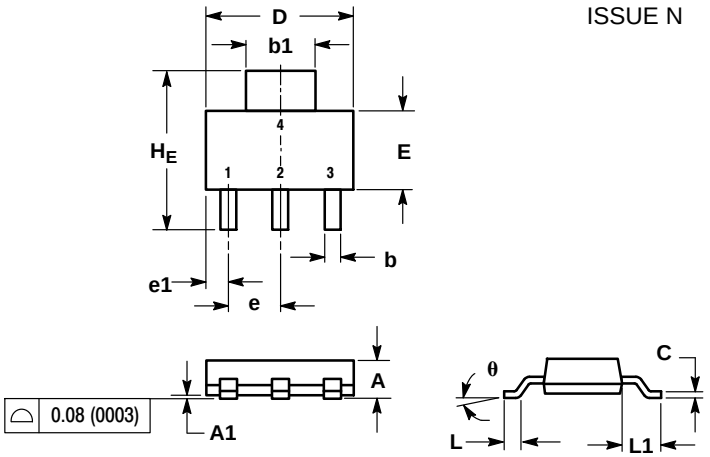
Device	Package	Shipping†
NSS40300MZ4T1G	SOT−223 (Pb−Free)	1,000 / Tape & Reel
NSV40300MZ4T1G*	SOT−223 (Pb−Free)	1,000 / Tape & Reel
NSS40300MZ4T3G	SOT−223 (Pb−Free)	4,000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*NSV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q101 Qualified and PPAP Capable

PACKAGE DIMENSIONS

SOT−223 (TO−261)
CASE 318E−04
ISSUE N

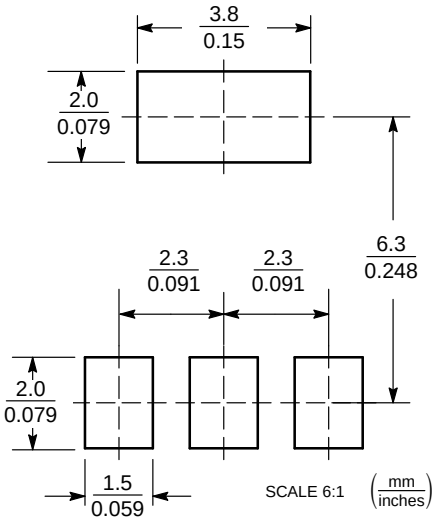


NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCH.

	MILLIMETERS			INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
A	1.50	1.63	1.75	0.060	0.064	0.068
A1	0.02	0.06	0.10	0.001	0.002	0.004
b	0.60	0.75	0.89	0.024	0.030	0.035
b1	2.90	3.06	3.20	0.115	0.121	0.126
c	0.24	0.29	0.35	0.009	0.012	0.014
D	6.30	6.50	6.70	0.249	0.256	0.263
E	3.30	3.50	3.70	0.130	0.138	0.145
e	2.20	2.30	2.40	0.087	0.091	0.094
e1	0.85	0.94	1.05	0.033	0.037	0.041
L	0.20	−−−	−−−	0.008	−−−	−−−
L1	1.50	1.75	2.00	0.060	0.069	0.078
H_E	6.70	7.00	7.30	0.264	0.276	0.287
θ	0°	–	10°	0°	–	10°

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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