NC7S86

TinyLogic HS 2-Input Exclusive-OR Gate

ON Semiconductor®

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Description

The NC7S86 is a single 2−Input high performance CMOS Exclusive−OR Gate. Advanced Silicon Gate CMOS fabrication assures high speed and low power circuit operation over a broad V_{CC} range. ESD protection diodes inherently guard both inputs and output with respect to the V_{CC} and GND rails. Inputs are well buffered from the output to assure high noise immunity and reduced sensitivity to input edge rate.

Features

- Space Saving SC−74A and SC−88A 5−Lead Package
- Ultra Small MicroPak™ Leadless Package
- High Speed: t_{PD} = 4.5 ns Typ
- Low Quiescent Power: I_{CC} < 1 μA
- Balanced Output Drive: 2 mA I_{OL}, −2 mA I_{OH}
- Broad V_{CC} Operating Range: 2 V – 6 V
- Balanced Propagation Delays
- Specified for 3 V Operation
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

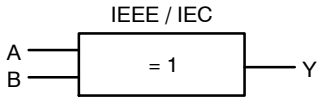
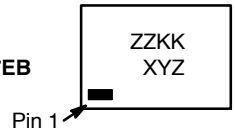


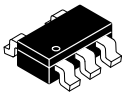
Figure 1. Logic Symbol

MARKING DIAGRAMS

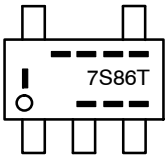


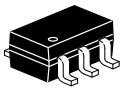
SIP6
CASE 127EB



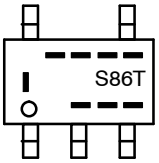


SC−74A
CASE 318BQ





SC−88A
CASE 419AC−01



ZZ, 7S86, S86	= Specific Device Code
KK	= 2−Digit Lot Run Traceability Code
XY	= 2−Digit Date Code Format
Z	= Assembly Plant Code
T	= Die Run Code
▬▬▬	= Year Coding Scheme
▮▪▬	= Plant Code Identifier
▬▬▬	= Eight−Week Datacoding Scheme

ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 5 of this data sheet.

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Pin Configurations

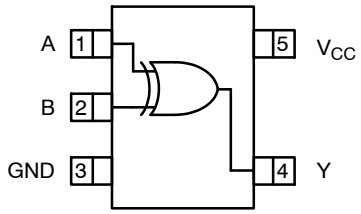


Figure 2. SC−88A and SC−74A (Top View)

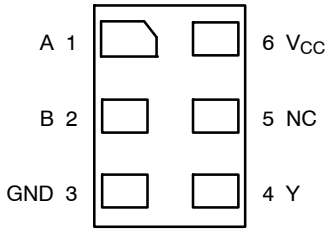


Figure 3. MicroPak (Top Through View)

PIN DESCRIPTIONS

Pin Name	Description
A, B	Input
Y	Output
NC	No Connect

FUNCTION TABLE (Y = A ⊕ B)

Inputs		Output
A	**B**	**Y**
L	L	L
L	H	H
H	L	H
H	H	L

H = HIGH Logic Level
L = LOW Logic Level

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Min	Max	Unit
V_{CC}	Supply Voltage		−0.5	6.5	V
I_{IK}	DC Input Diode Current	$V_{IN} \le -0.5$ V	−	−20	mA
		$V_{IN} \ge V_{CC} + 0.5$ V	−	+20	
V_{IN}	DC Input Voltage		−0.5	V_{CC} + 0.5	V
I_{OK}	DC Output Diode Current	$V_{OUT} < -0.5$ V	−	−20	mA
		$V_{OUT} > V_{CC} + 0.5$ V	−	+20	
V_{OUT}	DC Output Voltage		−0.5	V_{CC} + 0.5	V
I_{OUT}	DC Output Source or Sink Current		−	±12.5	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current per Output Pin		−	±25	mA
T_{STG}	Storage Temperature		−65	+150	°C
T_J	Junction Temperature		−	+150	°C
T_L	Lead Temperature (Soldering, 10 Seconds)		−	+260	°C
P_D	Power Dissipation in Still Air	SC−74A	−	225	mW
		SC−88A	−	190	
		MicroPak	−	327	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply Voltage		2.0	6.0	V
V_{IN}	Input Voltage		0	V_{CC}	V
V_{OUT}	Output Voltage		0	V_{CC}	V
T_A	Operating Temperature		−40	+85	°C
t_r, t_f	Input Rise and Fall Times	V_{CC} at 2.0 V	0	20	ns
		V_{CC} at 3.0 V	0	20	
		V_{CC} at 4.5 V	0	10	
		V_{CC} at 6.0 V	0	5	
θ_{JA}	Thermal Resistance	SC−74A	–	555	°C/W
		SC−88A	–	659	
		MicroPak	–	382	

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

1. Unused inputs must be held HIGH or LOW. They may not float.

DC ELECTICAL CHARACTERISTICS

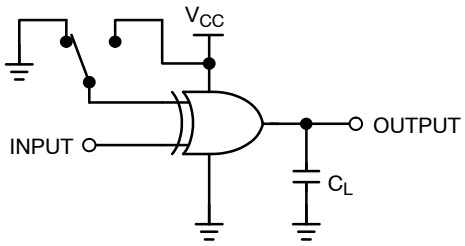
Symbol	Parameter	V_{CC} (V)	Conditions	T_A = +25°C			T_A = −40 to +85°C		Unit
				Min	Typ	Max	Min	Max	
V_{IH}	HIGH Level Input Voltage	2.0 3.0 – 6.0		1.50 0.7 V_{CC}	– –	– –	1.50 0.7 V_{CC}	– –	V
V_{IL}	LOW Level Input Voltage	2.0 3.0 – 6.0		– –	– –	0.50 0.3 V_{CC}	– –	0.50 0.3 V_{CC}	V
V_{OH}	HIGH Level Output Voltage	2.0 3.0 4.5 6.0	I_{OH} = −20 μA V_{IN} = V_{IH}, V_{IL}	1.90 2.90 4.40 5.90	2.0 3.0 4.5 6.0	– – – –	1.90 2.90 4.40 5.90	– – – –	V
		 3.0 4.5 6.0	V_{IN} = V_{IH}, V_{IL} I_{OH} = −1.3 mA I_{OH} = −2.0 mA I_{OH} = −2.6 mA	 2.68 4.18 5.68	 2.85 4.35 5.85	 – – –	 2.63 4.13 5.63	 – – –	V
V_{OL}	LOW Level Output Voltage	2.0 3.0 4.5 6.0	I_{OL} = 20 μA V_{IN} = V_{IH} or V_{IL}	– – – –	0.0 0.0 0.0 0.0	0.10 0.10 0.10 0.10	– – – –	0.10 0.10 0.10 0.10	V
		 3.0 4.5 6.0	V_{IN} = V_{IL} or V_{IL} I_{OL} = 1.3 mA I_{OL} = 2.0 mA I_{OL} = 2.6 mA	 – – –	 0.1 0.1 0.1	 0.26 0.26 0.26	 – – –	 0.33 0.33 0.33	V
I_{IN}	Input Leakage Current	6.0	V_{IN} = V_{CC}, GND	–	–	±0.1	–	±1.0	μA
I_{CC}	Quiescent Supply Current	6.0	V_{IN} = V_{CC}, GND	–	–	1.0	–	10.0	μA

AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	V_{CC} (V)	Conditions	T_A = +25°C			T_A = −40 to +85°C		Unit
				Min	Typ	Max	Min	Max	
t_{PLH}, t_{PHL}	Propagation Delay (Figure 4, 6)	5.0	C_L = 15 pF	–	4.5	17	–	–	ns
		2.0 3.0 4.5 6.0	C_L = 50 pF	– – – –	22 12 8.5 7	100 27 20 17	– – – –	125 35 25 21	ns
t_{TLH}, t_{THL}	Output Transition Time (Figure 4, 6)	5.0	C_L = 15 pF	–	3	8	–	–	ns
		2.0 3.0 4.5 6.0	C_L = 50 pF	– – – –	25 16 11 9	125 35 25 21	– – – –	155 45 31 26	ns
C_{IN}	Input Capacitance	Open		–	2	10	–	10	pF
C_{PD}	Power Dissipation Capacitance (Figure 5)	5.0	(Note 2)	–	8	–	–	–	pF

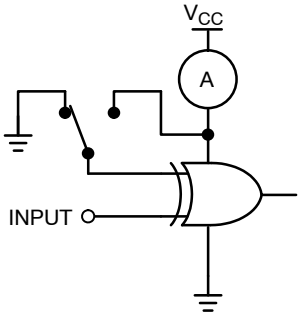
2. C_{PD} is defined as the value of the internal equivalent capacitance which is derived from dynamic operating current consumption (I_{CCD}) at no output loading and operating at 50% duty cycle. C_{PD} is related to I_{CCD} dynamic operating current by the expression: $I_{CCD} = (C_{PD})\ (V_{CC})\ (f_{IN}) + (I_{CC}static)$.

AC Loading and Waveforms



C_L includes load and stray capacitance
Input PRR = 1.0 MHz; t_W = 500 ns

Figure 4. AC Test Circuit



Input = AC Waveform;
PRR = Variable; Duty Cycle = 50%.

Figure 5. I_{CCD} Test Circuit

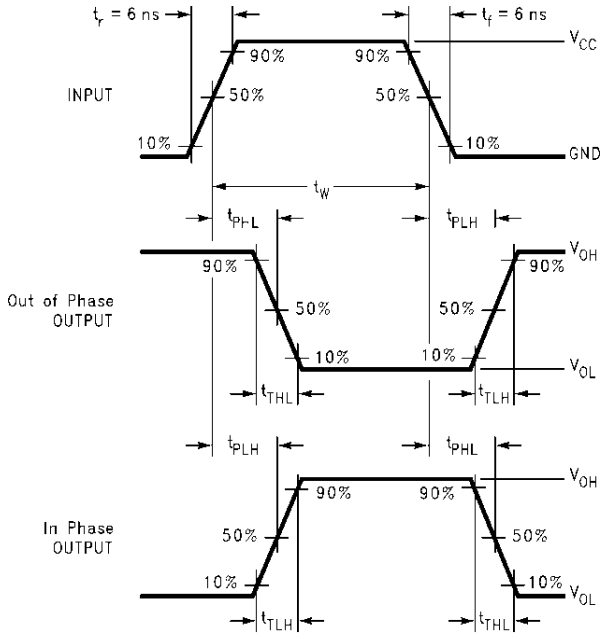


Figure 6. AC Waveforms

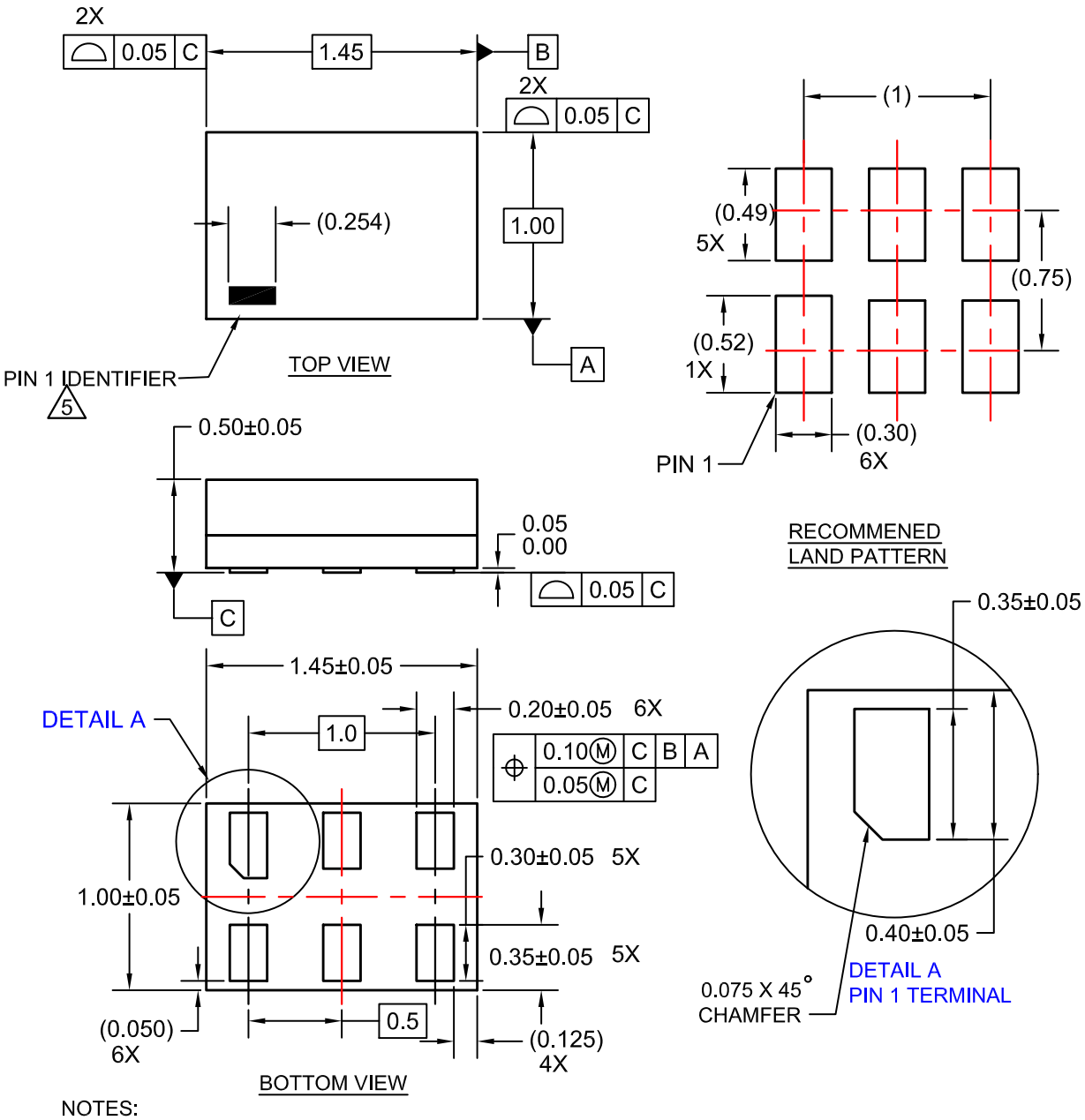
ORDERING INFORMATION

Order Number	Top Mark	Package Description	Shipping†
NC7S86M5X	7S86	SC−74A	3000 / Tape & Reel
NC7S86P5X	S86	SC−88A	3000 / Tape & Reel
NC7S86L6X	ZZ	SIP6, MicroPak	5000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

SIP6 1.45X1.0
CASE 127EB
ISSUE O

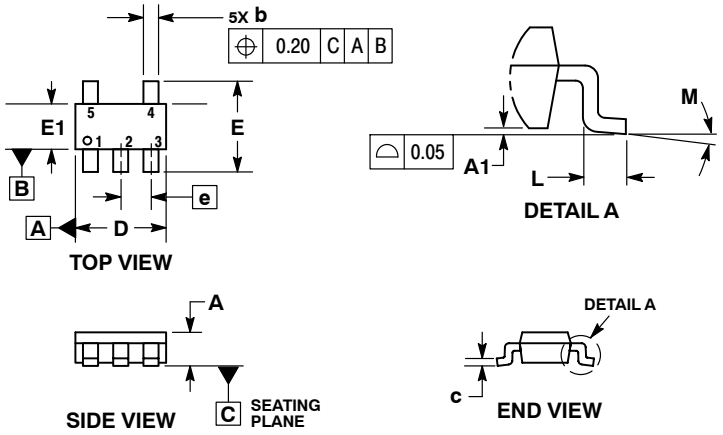


NOTES:

1. CONFORMS TO JEDEC STANDARD MO-252 VARIATION UAAD
2. DIMENSIONS ARE IN MILLIMETERS
3. DRAWING CONFORMS TO ASME Y14.5M-2009
4. PIN ONE IDENTIFIER IS 2X LENGTH OF ANY OTHER LINE IN THE MARK CODE LAYOUT.

PACKAGE DIMENSIONS

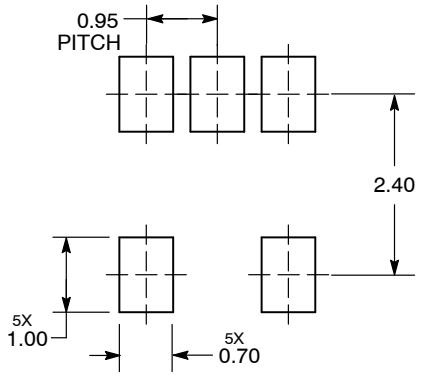
SC−74A
CASE 318BQ
ISSUE B



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE.

	MILLIMETERS	
DIM	MIN	MAX
A	0.90	1.10
A1	0.01	0.10
b	0.25	0.50
c	0.10	0.26
D	2.85	3.15
E	2.50	3.00
E1	1.35	1.65
e	0.95 BSC	
L	0.20	0.60
M	0 °	10 °

RECOMMENDED SOLDERING FOOTPRINT*

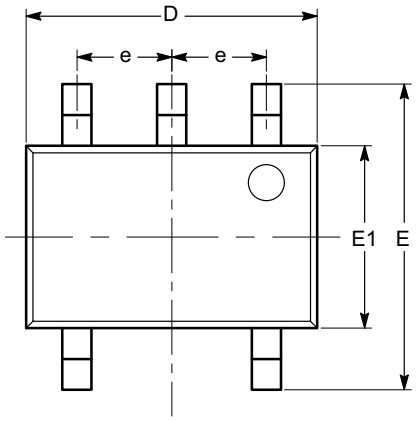


DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

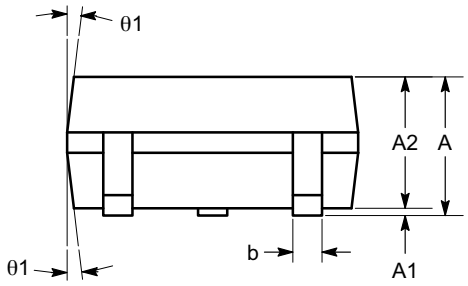
PACKAGE DIMENSIONS

SC−88A (SC−70 5 Lead), 1.25x2
CASE 419AC−01
ISSUE A

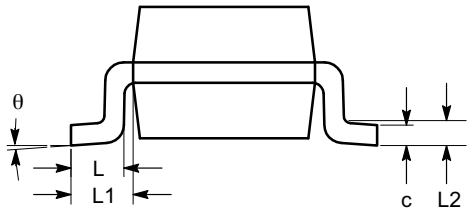


TOP VIEW

SYMBOL	MIN	NOM	MAX
A	0.80		1.10
A1	0.00		0.10
A2	0.80		1.00
b	0.15		0.30
c	0.10		0.18
D	1.80	2.00	2.20
E	1.80	2.10	2.40
E1	1.15	1.25	1.35
e		0.65 BSC	
L	0.26	0.36	0.46
L1		0.42 REF	
L2		0.15 BSC	
θ	0°		8°
θ1	4°		10°



SIDE VIEW



END VIEW

Notes:
(1) All dimensions are in millimeters. Angles in degrees.
(2) Complies with JEDEC MO-203.

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