I²C TOUCH SCREEN CONTROLLER

FEATURES

- **Qualified for Automotive Applications**
- **2.5-V To 5.25-V Operation**
- **Internal 2.5-V Reference**
- **Direct Battery Measurement (0.5 V To 6 V)**
- **On-Chip Temperature Measurement**
- **Touch-Pressure Measurement**
- **I²C Interface Supports: Standard, Fast, And High-Speed Modes**
- **Auto Power Down**
- **TSSOP-16 Package**

APPLICATIONS

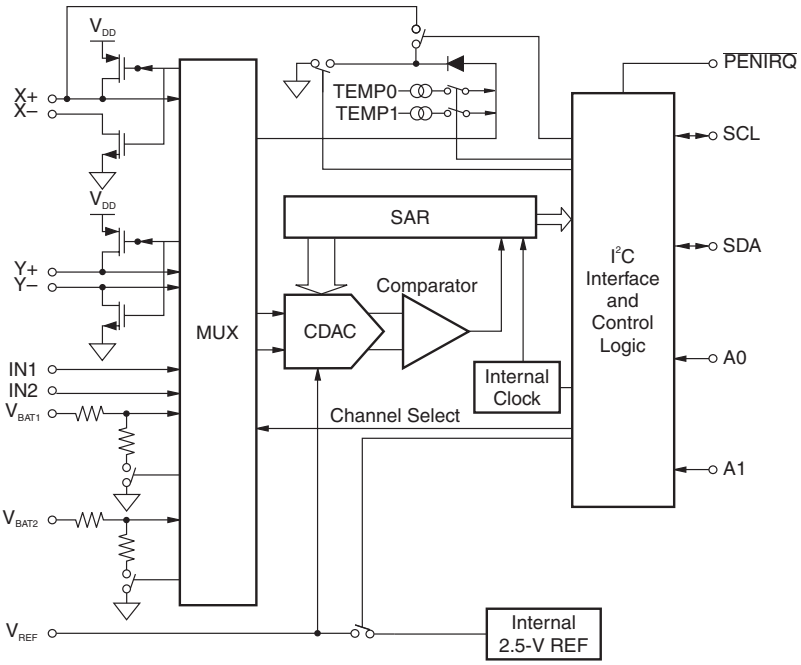
- **Personal Digital Assistants**
- **Portable Instruments**
- **Point-of-Sale Terminals**
- **Pagers**
- **Touch Screen Monitors**
- **Cellular Phones**

DESCRIPTION

The TSC2003 is a 4-wire resistive touch screen controller. It also features direct measurement of two batteries, two auxiliary analog inputs, temperature measurement, and touch-pressure measurement.

The TSC2003 has an on-chip 2.5-V reference that can be utilized for the auxiliary inputs, battery monitors, and temperature-measurement modes. The reference can also be powered down when not used to conserve power. The internal reference operates down to 2.7-V supply voltage while monitoring the battery voltage from 0.5 V to 6 V.

The TSC2003 is available in the small TSSOP-16 package and is specified over the –40°C to 85°C temperature range.



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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

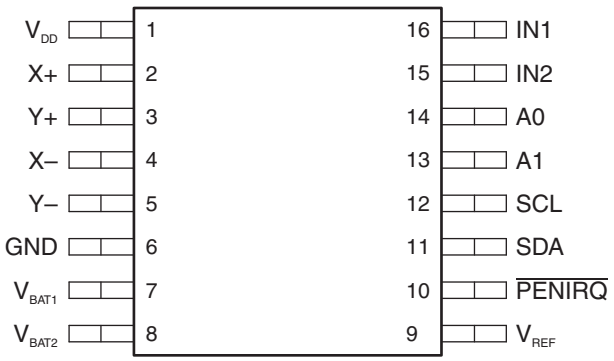
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

T_A	PACKAGE(2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	TSSOP – PW	Reel of 2000	TSC2003IPWRQ1	T2003Q1

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

PW PACKAGE
(TOP VIEW)



TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
V_{DD}	1		Power supply
X+	2	I	X+ position
Y+	3	I	Y+ position
X–	4	I	X– position
Y–	5	I	Y– position
GND	6		Ground
V_{BAT1}	7	I	Battery monitor 1
V_{BAT2}	8	I	Battery monitor 1
V_{REF}	9	I/O	Voltage reference
$\overline{PENIRQ}$	10	O	Pen interrupt. Open-drain, requires 30-kΩ to 100-kΩ external pullup resistor.
SDA	11	I/O	Serial data
SCL	12	I	Serial clock
A1	13	I	I^2C bus address A1
A0	14	I	I^2C bus address A0
IN2	15	I	Auxiliary analog-to-digital converter input 2
IN1	16	I	Auxiliary analog-to-digital converter input 1

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ABSOLUTE MAXIMUM RATINGS(1)(2)

over operating free-air temperature range (unless otherwise noted)

V_{DD}	Supply voltage range		–0.3 V to 6 V
V_I	Input voltage range	Digital inputs	–0.3 V to V_{DD} + 0.3 V
		All analog inputs except pins 7 and 8	–0.3 V to V_{DD} + 0.3 V
		Analog input pins 7 and 8	–0.3 V to 6 V
P_D	Power dissipation		$(T_{J(max)} – T_A)/\theta_{JA}$
θ_{JA}	Package thermal impedance, junction to free air		115.2°C
T_A	Operating free-air temperature range		–40°C to 85°C
T_J	Maximum junction temperature		150°C
T_{stg}	Storage temperature range		–65°C to 150°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are referenced to GND.

ELECTRICAL CHARACTERISTICS

T_A = –40°C to 85°C, V_{DD} = 2.7 V, V_{REF} = 2.5-V external voltage, I^2C bus frequency = 3.4 MHz, 12-bit mode, digital inputs = GND or V_{DD} (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Analog Input						
V_I	Full-scale input voltage span		0		V_{REF}	V
V_I	Absolute input voltage		–0.2		V_{DD} + 0.2	V
C_i	Capacitance			25		pF
I_{leak}	Leakage current			0.1		µA
System Performance						
	Resolution			12		bits
	No missing codes	Standard and fast modes	11			bits
		High-speed mode	10			
	Integral linearity error	Standard and fast modes			±2	LSB(1)
		High-speed mode			±4	
	Offset error				±6	LSB
	Gain error				±4	LSB
V_n	Noise	Including internal V_{REF}, RMS		70		µV
PSRR	Power-supply rejection ratio			70		dB
Sampling Dynamics						
	Throughput rate			50		ksps
	Channel-to-channel isolation	V_{IN} = 2.5 V_{pp} at 50 kHz		100		dB
Switch Drivers						
	Y+, X+ on-resistance			5.5		Ω
	Y–, X– on-resistance			7.3		Ω
	Drive current(2)	Duration 100 ms			50	mA

(1) LSB = least significant bit. With V_{REF} equal to 2.5 V, one LSB is 610 µV.
(2) Specified by design. Exceeding 50-mA source current may result in device degradation.

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ELECTRICAL CHARACTERISTICS (continued)

T_A = –40°C to 85°C, V_{DD} = 2.7 V, V_{REF} = 2.5-V external voltage, I^2C bus frequency = 3.4 MHz, 12-bit mode, digital inputs = GND or V_{DD} (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Reference Output						
	Internal reference voltage		2.45	2.50	2.55	V
	Internal reference drift			25		ppm/°C
Z_O	Output impedance	Internal reference on		300		Ω
		Internal reference off		1		GΩ
I_Q	Quiescent current	PD1 = 1, PD0 = 0, SDA and SCL high		750		µA
Reference Input						
V_I	Input voltage		2		V_{DD}	V
R_I	Resistance	PD1 = PD0 = 0		1		GΩ
Battery Monitor						
V_I	Input voltage		0.5		6	V
Z_I	Input impedance	Sampling battery		10		kΩ
		Battery monitor off		1		GΩ
	Accuracy	External V_{REF} = 2.5 V	–2		+2	%
		Internal reference	–3		+3	
Temperature Measurement						
	Temperature range		–40		85	°C
	Resolution	Differential method(3)		1.6		°C
		TEMP0(4)		0.3		
	Accuracy	Differential method(3)		±2		°C
		TEMP0(4)		±3		
Digital Input/Output						
V_{IH}	High-level input voltage, all except $\overline{PENIRQ}$(5)	| I_{IH} | ≤ 5 µA	0.7 × V_{DD}		V_{DD} + 0.3	V
V_{IL}	Low-level input voltage, all except $\overline{PENIRQ}$(5)	| I_{IL} | ≤ 5 µA	–0.3		0.3 × V_{DD}	V
V_{OH}	High-level output voltage, all except $\overline{PENIRQ}$	I_{OH} = –250 µA	0.8 × V_{DD}			V
V_{OL}	Low-level output voltage, all except $\overline{PENIRQ}$	I_{OL} = 250 µA			0.4	V
V_{OL}	Low-level output voltage, $\overline{PENIRQ}$	30-kΩ pullup			0.4	V
C_i	Input capacitance	SDA, SCL			10	pF

(3) Difference between TEMP0 and TEMP1 measurement. No calibration necessary.
(4) Temperature drift is –2.1 mV/°C
(5) Specified by design

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ELECTRICAL CHARACTERISTICS (continued)

T_A = –40°C to 85°C, V_{DD} = 2.7 V, V_{REF} = 2.5-V external voltage, I^2C bus frequency = 3.4 MHz, 12-bit mode, digital inputs = GND or V_{DD} (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Power Supply Requirements							
V_{DD}	Supply voltage	Specified performance		2.7		3.6	
		Operating range		2.5		5.25	
I_Q	Quiescent current	Internal reference off, PD1 = PD0 = 0	High-speed mode (SCL = 3.4 MHz)		254	650	µA
			Fast mode (SCL = 400 kHz)		95		
			Standard mode (SCL = 100 kHz)		63		
		Internal reference on, PD0 = 0			1005		
I_{PD}	Power-down current when part is not addressed	Internal reference off, PD1 = PD0 = 0	High-speed mode (SCL = 3.4 MHz)		90		µA
			Fast mode (SCL = 400 kHz)		21		
			Standard mode (SCL = 100 kHz)		4		
		PD1 = PD0 = 0, SDA = SCL = V_{DD}				3	
P_D	Power dissipation	V_{DD} = 2.7 V				1.8	mW
Temperature Range							
T_A	Operating free-air temperature	Specified performance		–40		85	°C

TIMING CHARACTERISTICS(1)(2)

T_A = –40°C to 85°C, V_{DD} = 2.7 V (unless otherwise noted) (see Figure 1)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
f_{SCL}	SCL clock frequency	Standard mode	0	100	kHz
		Fast mode	0	400	
		High-speed mode, C_b = 100 pF max	0	3.4	MHz
		High-speed mode, C_b = 400 pF max	0	1.7	
t_{BUF}	Bus free time between Stop and Start conditions	Standard mode	4.7		µs
		Fast mode	1.3		
$t_{HD;\ STA}$	Hold time (repeated) Start condition	Standard mode	4		µs
		Fast mode	600		ns
		High-speed mode	160		
t_{low}	Low period of the SCL clock	Standard mode	4.7		µs
		Fast mode	1.3		
		High-speed mode, C_b = 100 pF max	160		ns
		High-speed mode, C_b = 400 pF max	320		
t_{high}	High period of the SCL clock	Standard mode	4		µs
		Fast mode	600		ns
		High-speed mode, C_b = 100 pF max	60		
		High-speed mode, C_b = 400 pF max	120		
$t_{SU;\ STA}$	Setup time for a repeated Start condition	Standard mode	4.7		µs
		Fast mode	600		ns
		High-speed mode	160		

(1) All values referred to V_{IHMIN} and V_{ILMAX} levels.
(2) Not production tested

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TIMING CHARACTERISTICS (continued)

T_A = –40°C to 85°C, V_{DD} = 2.7 V (unless otherwise noted) (see Figure 1)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$t_{SU;\ DAT}$	Data setup time	Standard mode	250		ns
		Fast mode	100		
		High-speed mode	10		
$t_{HD;\ DAT}$	Data hold time	Standard mode	0	3.45	µs
		Fast mode	0	0.9	
		High-speed mode, C_b = 100 pF max	0	70	ns
		High-speed mode, C_b = 400 pF max	0	150	
t_{rCL}	Rise time of SCL signal	Standard mode		1000	ns
		Fast mode	20 + 0.1C_b	300	
		High-speed mode, C_b = 100 pF max	10	80	
		High-speed mode, C_b = 400 pF max	20	160	
t_{rCL1}	Rise time of SCL signal after a repeated Start condition and after an acknowledge bit	Standard mode		1000	ns
		Fast mode	20 + 0.1C_b	300	
		High-speed mode, C_b = 100 pF max	10	80	
		High-speed mode, C_b = 400 pF max	20	160	
t_{fCL}	Fall time of SCL signal	Standard mode		300	ns
		Fast mode	20 + 0.1C_b	300	
		High-speed mode, C_b = 100 pF max	10	80	
		High-speed mode, C_b = 400 pF max	20	160	
t_{rDA}	Rise time of SDA signal	Standard mode		1000	ns
		Fast mode	20 + 0.1C_b	300	
		High-speed mode, C_b = 100 pF max	10	80	
		High-speed mode, C_b = 400 pF max	20	160	
t_{fDA}	Fall time of SDA signal	Standard mode		300	ns
		Fast mode	20 + 0.1C_b	300	
		High-speed mode, C_b = 100 pF max	10	80	
		High-speed mode, C_b = 400 pF max	20	160	
$t_{SU;\ STO}$	Setup time for Stop condition	Standard mode	4		µs
		Fast mode	600		ns
		High-speed mode	160		
C_b	Capacitive load for SDA or SCL	Standard mode		400	pF
		Fast mode		400	
		High-speed mode, SCL = 1.7 MHz		400	
		High-speed mode, SCL = 3..4 MHz		100	
t_{SP}	Pulse width of spike suppressed	Fast mode	0	50	ns
		High-speed mode	0	10	
V_{nH}	Noise margin at the high level for each connected device (including hysteresis)	Standard mode	0.2 × V_{DD}		V
		Fast mode			
		High-speed mode			
V_{nL}	Noise margin at the low level for each connected device (including hysteresis)	Standard mode	0.1 × V_{DD}		V
		Fast mode			
		High-speed mode			

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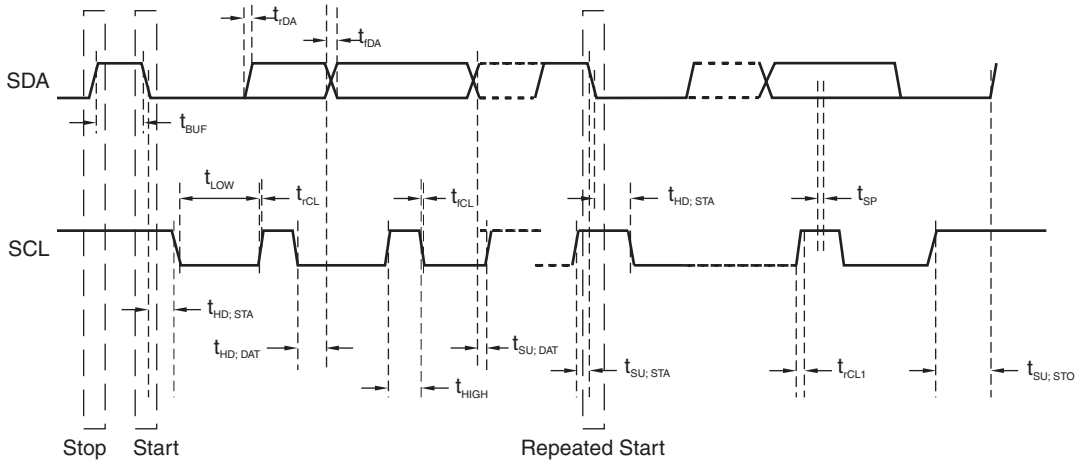


Figure 1. Timing Diagram

Power-On Sequence Timing

During TSC2003 power-up, the I^2C bus should be idle. In other words, the SDA and SCL lines must be high before the TSC2003 supply (V_{DD}) ramps up greater than 0.9 V. If the TSC2003 uses the same supply as the I^2C bus pullup resistors (V_{I2C}), then a 1-µF capacitor placed very close to the TSC2003 supply pin causes the TSC2003 supply to ramp up more slowly (see Figure 2). If the TSC2003 supply (V_{DD}) is different than the supply to the I^2C bus pullup resistors (V_{I2C}), then V_{I2C} should be turned on before the TSC2003 supply (V_{DD}) is powered up.

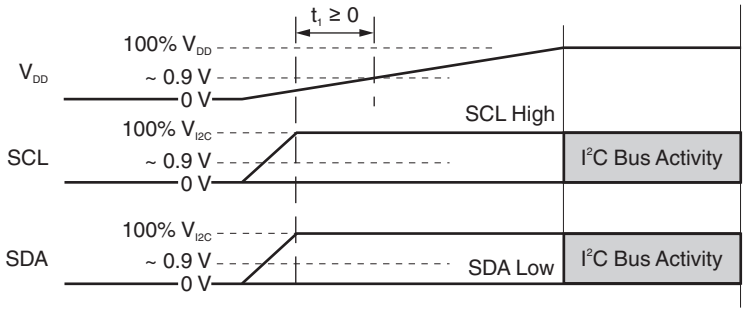
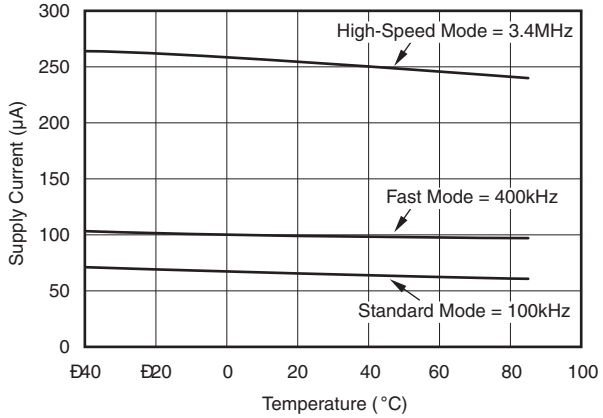


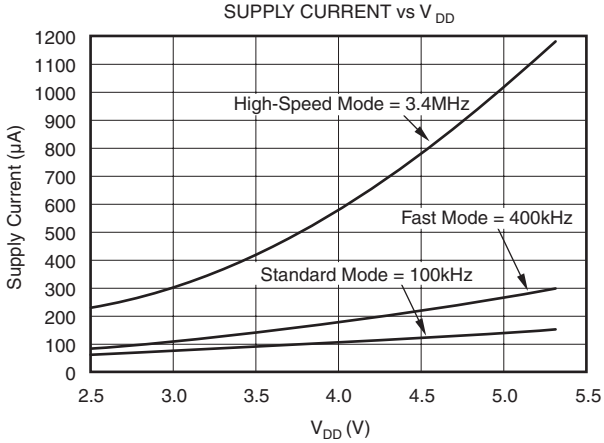
Figure 2. Power-On Sequence Timing Diagram

TYPICAL CHARACTERISTICS

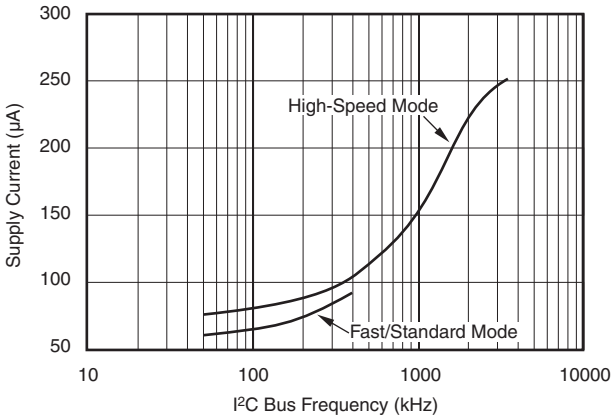
SUPPLY CURRENT vs TEMPERATURE



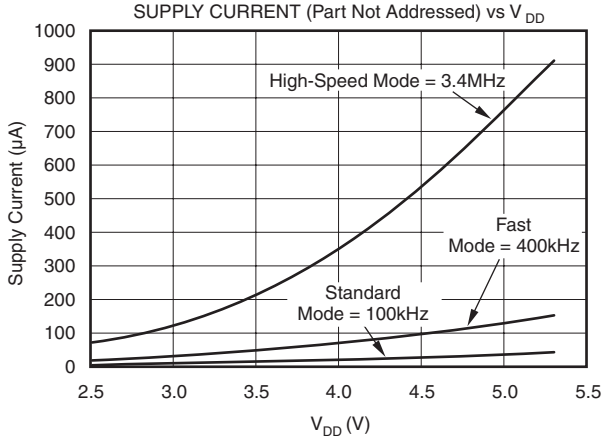
SUPPLY CURRENT vs V_{DD}



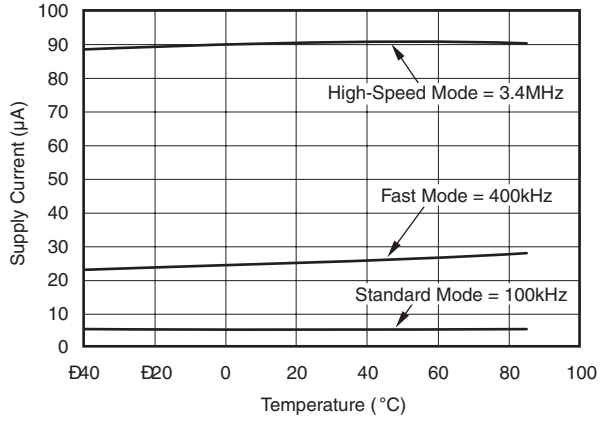
SUPPLY CURRENT vs I²C BUS FREQUENCY



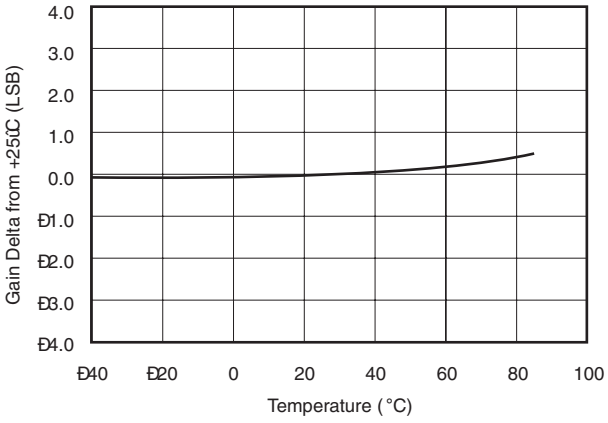
SUPPLY CURRENT (Part Not Addressed) vs V_{DD}



SUPPLY CURRENT (Part Not Addressed) vs TEMPERATURE



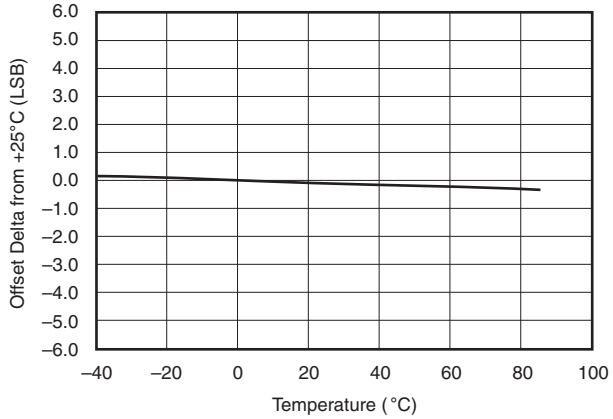
CHANGE IN GAIN vs TEMPERATURE



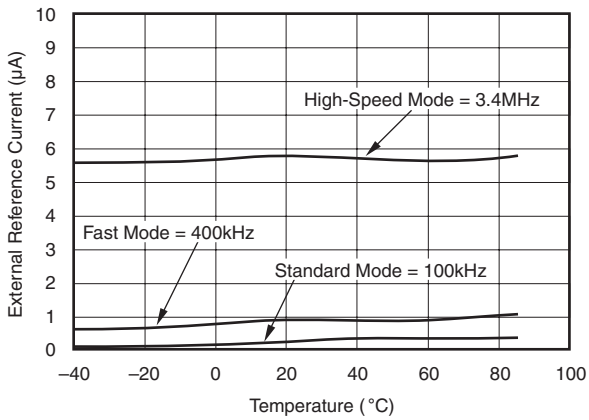
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TYPICAL CHARACTERISTICS (continued)

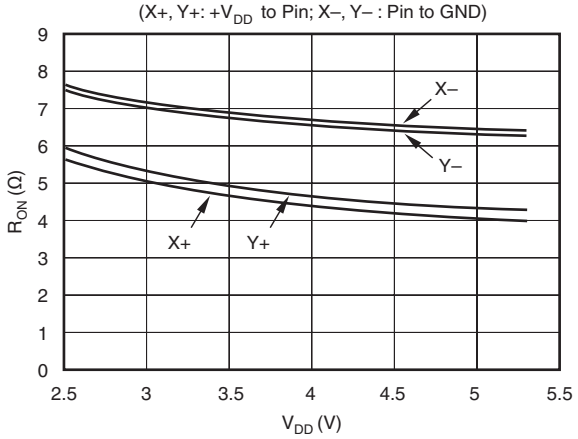
CHANGE IN OFFSET vs TEMPERATURE



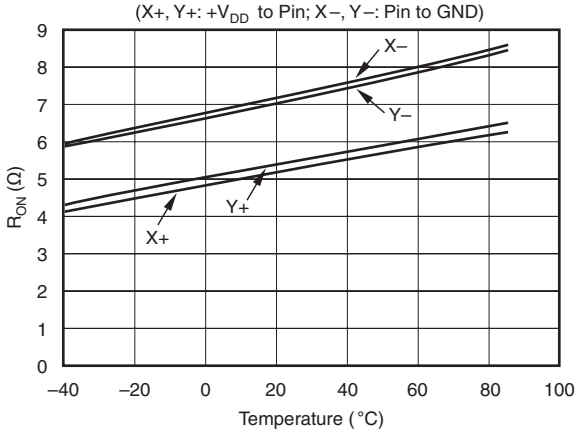
EXTERNAL REFERENCE CURRENT vs TEMPERATURE



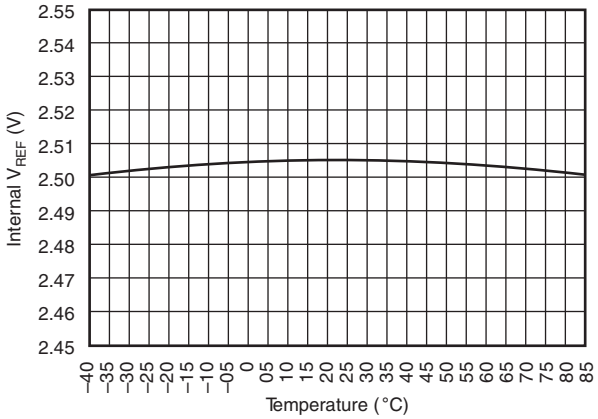
SWITCH-ON RESISTANCE vs V_{DD}
($X+$, $Y+$: $+V_{DD}$ to Pin; $X-$, $Y-$: Pin to GND)



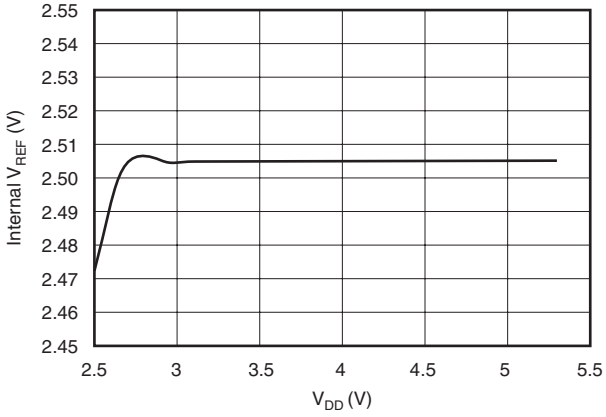
SWITCH-ON RESISTANCE vs TEMPERATURE
($X+$, $Y+$: $+V_{DD}$ to Pin; $X-$, $Y-$: Pin to GND)



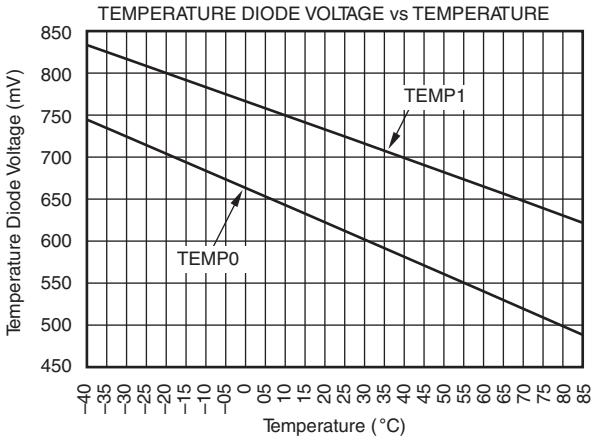
INTERNAL V_{REF} vs TEMPERATURE

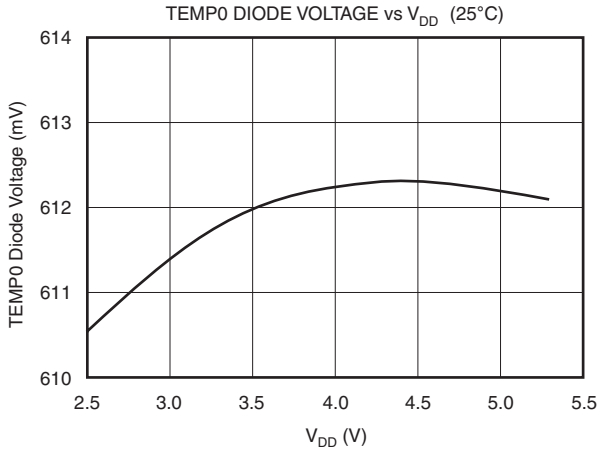


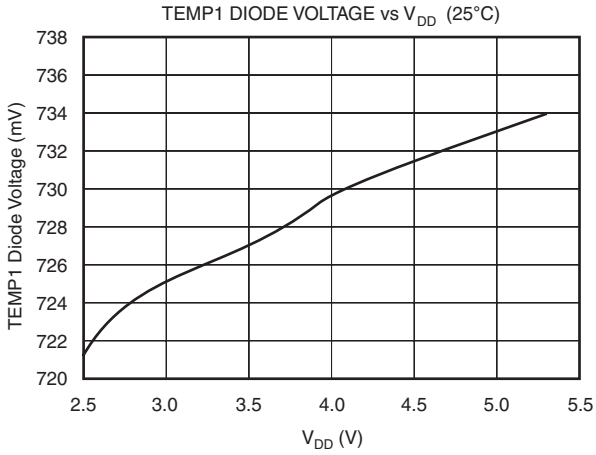
INTERNAL V_{REF} vs V_{DD}



TYPICAL CHARACTERISTICS (continued)







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DEVICE INFORMATION

The TSC2003 is a classic Successive Approximation Register (SAR) analog-to-digital converter (ADC). The architecture is based on capacitive redistribution which inherently includes a sample-and-hold function. The converter is fabricated on a 0.6µ CMOS process.

The basic operation of the TSC2003 is shown in Figure 3. The device features an internal 2.5-V reference and an internal clock. Operation is maintained from a single supply of 2.7 V to 5.25 V. The internal reference can be overdriven with an external, low-impedance source between 2 V and V_{DD}. The value of the reference voltage directly sets the input range of the converter.

The analog input (X, Y, and Z parallel coordinates, auxiliary inputs, battery voltage, and chip temperature) to the converter is provided via a multiplexer. A unique configuration of low on-resistance switches allows an unselected ADC input channel to provide power and an accompanying pin to provide ground for an external device. By maintaining Figure 3, a differential input to the converter, and a differential reference architecture, it is possible to negate the switch's on-resistance error (should this be a source of error for the particular measurement).

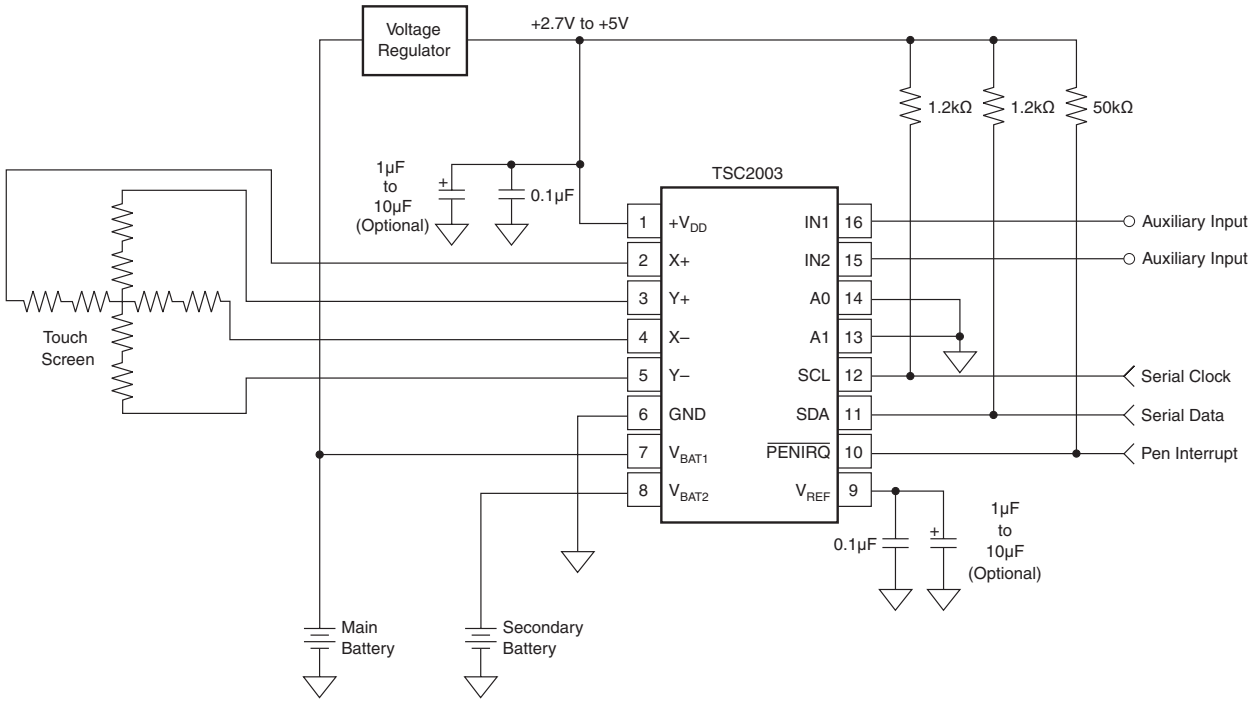


Figure 3. Basic Operation of the TSC2003

Analog Input

See Figure 4 for a block diagram of the input multiplexer on the TSC2003, the differential input of the ADC, and the converter's differential reference.

When the converter enters the Hold mode, the voltage difference between the +IN and –IN inputs (see Figure 4) is captured on the internal capacitor array. The input current on the analog inputs depends on the conversion rate of the device. During the sample period, the source must charge the internal sampling capacitor (typically 25 pF). After the capacitor has been fully charged, there is no further input current. The amount of charge transfer from the analog source to the converter is a function of conversion rate.

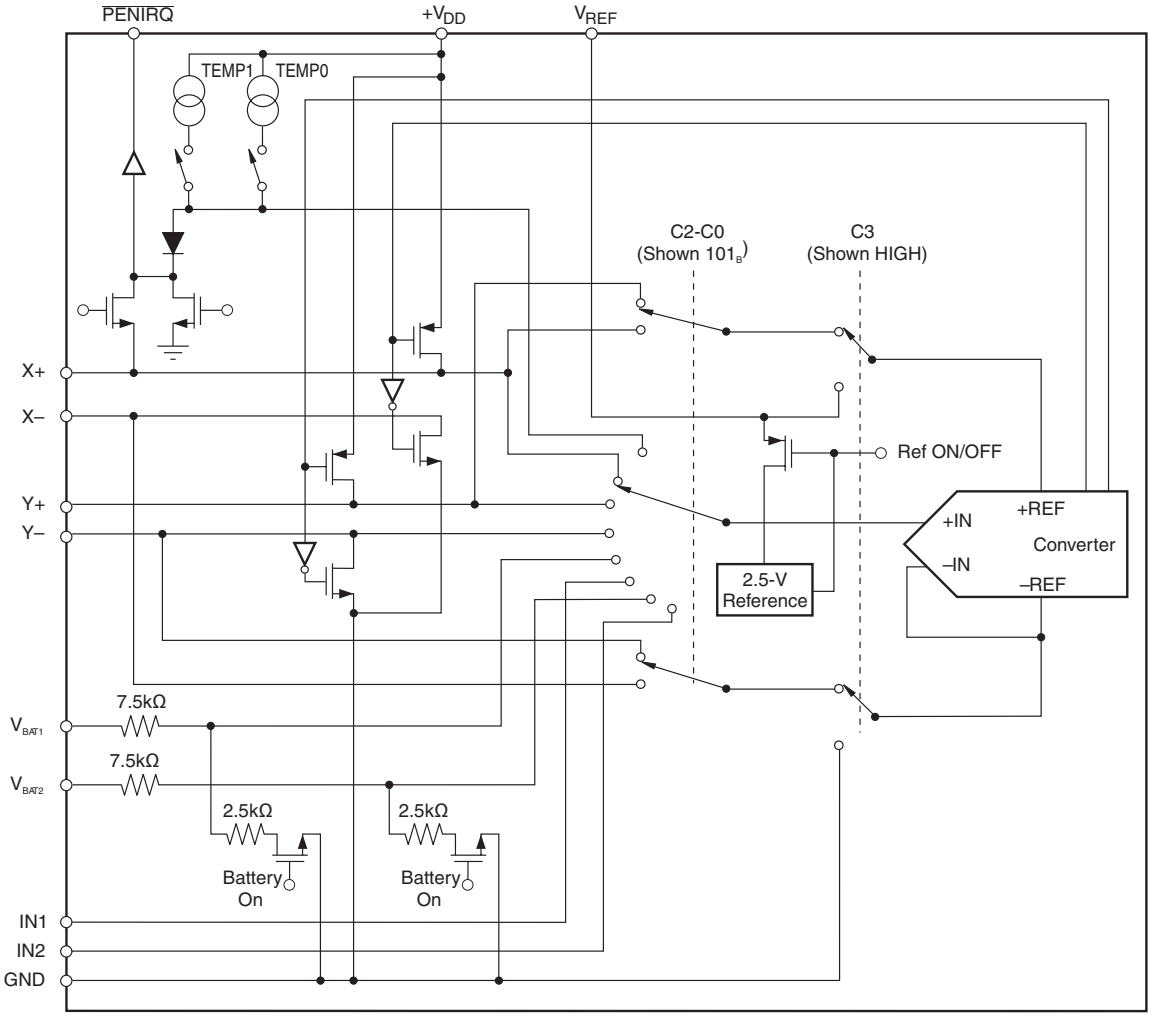


Figure 4. Simplified Diagram of the Analog Input

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Internal Reference

The TSC2003 has an internal 2.5-V voltage reference that can be turned on or off with the power-down control bits, PD0 and PD1 (see Table 2 and Figure 5). The internal reference is powered down when power is first applied to the device.

The internal reference voltage is only used in the single-ended reference mode for battery monitoring, temperature measurement, and for measuring the auxiliary input. Optimal touch screen performance is achieved when using a ratiometric conversion; thus, all touch screen measurements are done automatically in the differential mode.

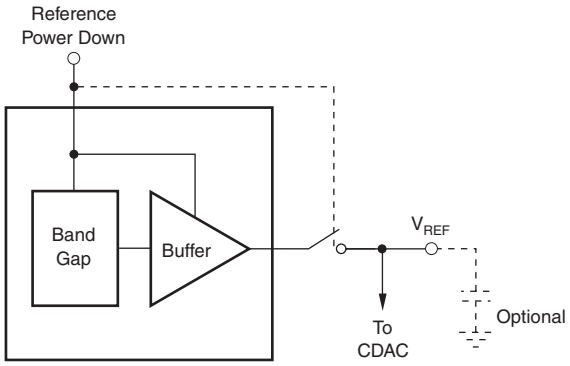


Figure 5. Simplified Diagram of the Internal Reference

Reference Input

The voltage difference between +REF and –REF (see Figure 4) sets the analog input range. The TSC2003 operates with a reference in the range of 2 V to V_{DD}. There are several critical items concerning the reference input and its wide-voltage range. As the reference voltage is reduced, the analog voltage weight of each digital output code is also reduced. This is often referred to as the LSB (least significant bit) size, and is equal to the reference voltage divided by 4096 (256 if in 8-bit mode). Any offset or gain error inherent in the ADC appears to increase, in terms of LSB size, as the reference voltage is reduced. For example, if the offset of a given converter is 2 LSBs with a 2.5-V reference, it is typically 2.5 LSBs with a 2-V reference. In each case, the actual offset of the device is the same, 1.22 mV. With a lower reference voltage, more care must be taken to provide a clean layout including adequate bypassing, a clean (low noise, low ripple) power supply, a low-noise reference (if an external reference is used), and a low-noise input signal.

The voltage into the V_{REF} input is not buffered, and directly drives the capacitor digital-to-analog converter (CDAC) portion of the TSC2003. Therefore, the input current is very low, typically < 6 μA.

Reference Mode

There is a critical item regarding the reference when making measurements while the switch drivers are on. For this discussion, it is useful to consider the basic operation of the TSC2003 (see Figure 3). This particular application shows the device being used to digitize a resistive touch screen. A measurement of the current Y position of the pointing device is made by connecting the X+ input to the ADC, turning on the Y+ and Y– drivers, and digitizing the voltage on X+, as shown in Figure 6. For this measurement, the resistance in the X+ lead does not affect the conversion; it does, however, affect the settling time, but the resistance is usually small enough that this is not a concern. However, because the resistance between Y+ and Y– is fairly low, the on-resistance of the Y drivers does make a small difference. Under the situation outlined so far, it would not be possible to achieve a 0-V input or a full-scale input regardless of where the pointing device is on the touch screen because some voltage is lost across the internal switches. In addition, the internal switch resistance is unlikely to track the resistance of the touch screen, providing an additional source of error.

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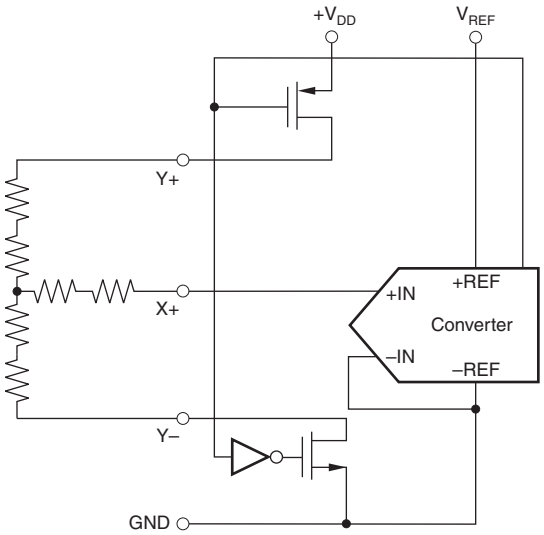


Figure 6. Simplified Diagram of Single-Ended Reference

This situation is remedied, as shown in Figure 7, by using the differential mode: the +REF and –REF inputs are connected directly to Y+ and Y–, respectively. This makes the ADC ratiometric. The result of the conversion is always a percentage of the external reference, regardless of how it changes in relation to the on-resistance of the internal switches.

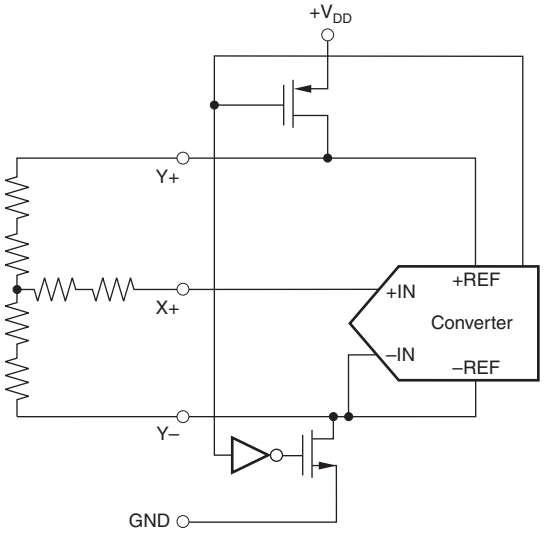


Figure 7. Simplified Diagram of Differential Reference (Y Switches Enabled, X+ is Analog Input)

Differential reference mode always uses the supply voltage, through the drivers, as the reference voltage for the ADC. V_{REF} cannot be used as the reference voltage in differential mode.

It is possible to use a high-precision reference on V_{REF} in single-ended reference mode for measurements which do not need to be ratiometric (i.e., battery voltage, temperature measurement, etc.). In some cases, it could be possible to power the converter directly from a precision reference. Most references can provide enough power for the TSC2003, but they might not be able to supply enough current for the external load, such as a resistive touch screen.

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Touch Screen Settling

In some applications, external capacitors may be required across the touch screen for filtering noise picked up by the touch screen (i.e., noise generated by the LCD panel or backlight circuitry). These capacitors provide a low-pass filter to reduce the noise, but they also cause a settling time requirement when the panel is touched. The settling time typically shows as a gain error. The problem is that the input and/or reference has not settled to its final steady-state value prior to the ADC sampling the input(s) and providing the digital output. Additionally, the reference voltage may still be changing during the measurement cycle.

To resolve these settling time problems, the TSC2003 can be commanded to turn on the drivers only without performing a conversion (see Table 1). Time can then be allowed before the command is issued to perform a conversion. Generally, the time it takes to communicate the conversion command over the I^2C bus is adequate for the touch screen to settle.

Temperature Measurement

In some applications, such as battery recharging, a measurement of ambient temperature is required. The temperature measurement technique used in the TSC2003 relies on the characteristics of a semiconductor junction operating at a fixed current level to provide a measurement of the temperature of the TSC2003 chip. The forward diode voltage (V_{BE}) has a well-defined characteristic versus temperature. The temperature can be predicted in applications by knowing the 25°C value of the V_{BE} voltage and then monitoring the delta of that voltage as the temperature changes. The TSC2003 offers two modes of temperature measurement.

The first mode requires calibrations at a known temperature, but only requires a single reading to predict the ambient temperature. A diode is used during this measurement cycle. The voltage across the diode is connected through the MUX for digitizing the diode forward bias voltage by the ADC with an address of C3 = 0, C2 = 0, C1 = 0, and C0 = 0 (see Table 1 and Figure 8 for details). This voltage is typically 600 mV at 25°C, with a 20-µA current through it. The absolute value of this diode voltage can vary a few millivolts; the temperature coefficient (TC) of this voltage is very consistent at –2.1 mV/°C. During the final test of the end product, the diode voltage would be stored at a known room temperature, in memory, for calibration purposes by the user. The result is an equivalent temperature measurement resolution of 0.3°C/LSB.

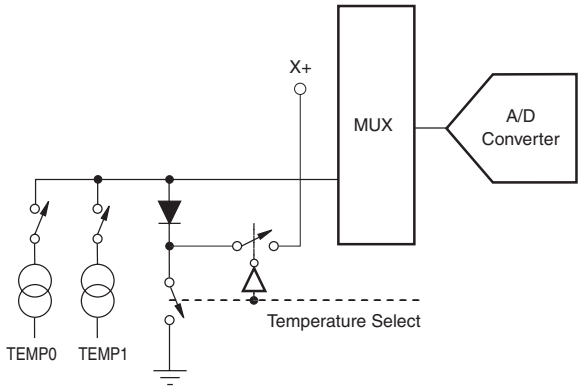


Figure 8. Temperature Measurement Mode Functional Block Diagram

The second mode does not require a test temperature calibration, but instead uses a two-measurement method to eliminate the need for absolute temperature calibration and for achieving 2°C/LSB accuracy. This mode requires a second conversion with an address of C3 = 0, C2 = 1, C1 = 0, and C0 = 0, with a 91 times larger current. The voltage difference between the first and second conversion using 91 times the bias current is represented by kT/q × 1n (N), where N is the current ratio (91), k is Boltzmann's constant (1.38054×10^{-23} electron-volts/degree Kelvin), q is the electron charge (1.602189×10^{-19} C), and T is the temperature in degrees Kelvin. This mode can provide improved absolute temperature measurement over the first mode, but at the cost of less resolution (1.6°C/LSB).

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The equation to solve for °K is shown in Equation 1:

$$°K = \frac{q \bullet \Delta V}{k \bullet 1n(N)} \quad (1)$$

Where:

ΔV $V(I_{91}) - V(I_1)$ (in mV)

$\therefore$ °K 2.573 × ΔV°K/mV

°C = 2.573 × ΔV(mV) – 273°K

NOTE:

The bias current for each diode temperature measurement is only turned on during the acquisition mode, and, therefore, does not add any noticeable increase in power, especially if the temperature measurement only occurs occasionally.

Battery Measurement

An added feature of the TSC2003 is the ability to monitor the battery voltage on the other side of the voltage regulator (dc/dc converter), as shown in Figure 9. The battery voltage can vary from 0.5 V to 6 V, while the voltage regulator maintains the voltage to the TSC2003 at 2.7 V, 3.3 V, etc. The input voltage (V_{BAT1} or V_{BAT2}) is divided down by 4 so that a 6-V battery voltage is represented as 1.5 V to the ADC. The simplifies the multiplexer and control logic. To minimize the power consumption, the divider is only on during the sample period which occurs after control bits C3 = 0, C2 = 0, C1 = 0, and C0 = 1 (V_{BAT1}) or C3 = 0, C2 = 1, C1 = 0, and C0 = 1 (V_{BAT2}) are received. See Table 1 and Table 2 for the relationship between the control bits and configuration of the TSC2003.

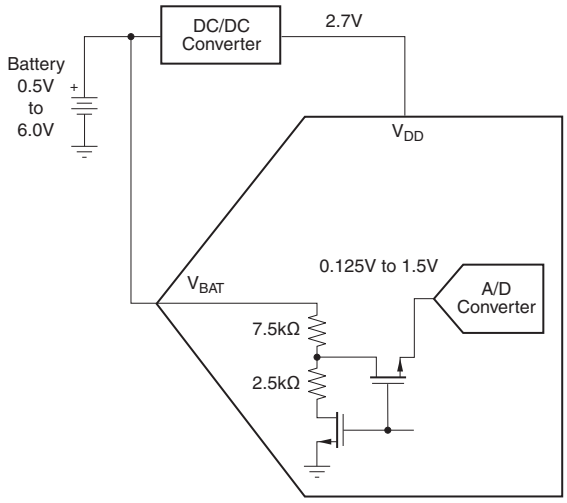


Figure 9. Battery Measurement Functional Block Diagram

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Pressure Measurement

Measuring touch pressure can also be done with the TSC2003. To determine pen or finger touch, the pressure of the "touch" needs to be determined. Generally, it is not necessary to have high accuracy for this test, therefore, the 8-bit resolution mode is recommended. However, calculations are shown with the 12-bit resolution mode. There are several different ways of performing this measurement, and the TSC2003 supports two methods.

The first method requires knowing the X-Plate resistance, measurement of the X-Position, and two additional cross-panel measurements (Z2 and Z1) of the touch screen, as shown in Figure 10. Use Equation 2 to calculate the touch resistance:

$$R_{TOUCH} = R_{X\text{-}Plate} \bullet \frac{X\text{-}Position}{4096} \left[\frac{Z_2}{Z_1} - 1 \right] \quad (2)$$

The second method requires knowing both the X-Plate and Y-Plate resistance, measurement of X-Position and Y-Position, and Z1. Equation 3 calculates the touch resistance using the second method:

$$R_{TOUCH} = \frac{R_{X-Plate} \bullet X\text{-}Position}{4096} \left[\frac{4096}{Z_1} - 1 \right] - R_{Y-Plate} \bullet \left[1 - \frac{Y\text{-}Position}{4096} \right] \quad (3)$$

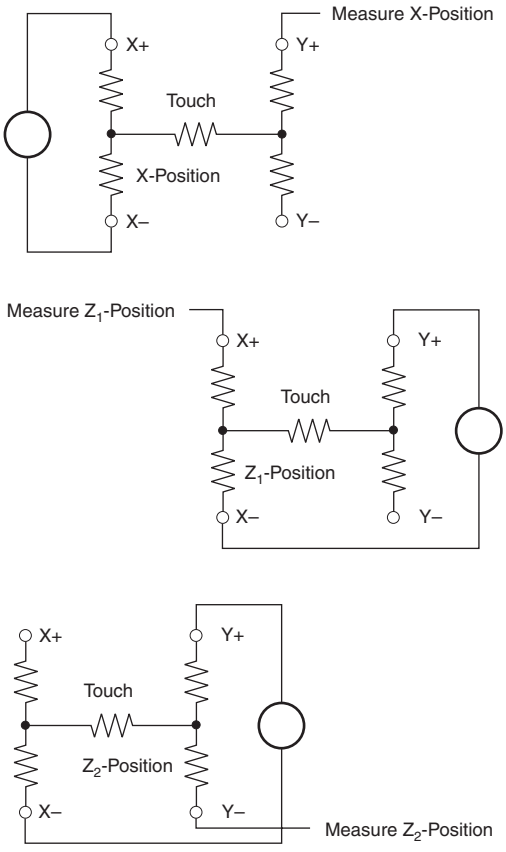


Figure 10. Pressure Measurement Block Diagrams

Digital Interface

The TSC2003 supports the I²C serial bus and data transmission protocol in all three defined modes: standard, fast, and high-speed. A device that sends data onto the bus is defined as a transmitter, and a device receiving data as a receiver. The device that controls the message is called a master. The devices that are controlled by the master are slaves. The bus must be controlled by a master device which generates the serial clock (SCL), controls the bus access, and generates the Start and Stop conditions. The TSC2003 operates as a slave on the I²C bus. Connections to the bus are made via the open-drain I/O lines SDA and SDL.

The following bus protocol has been defined, as shown in Figure 11:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is high. Changes in the data line while the clock line is high are interpreted as control signals.

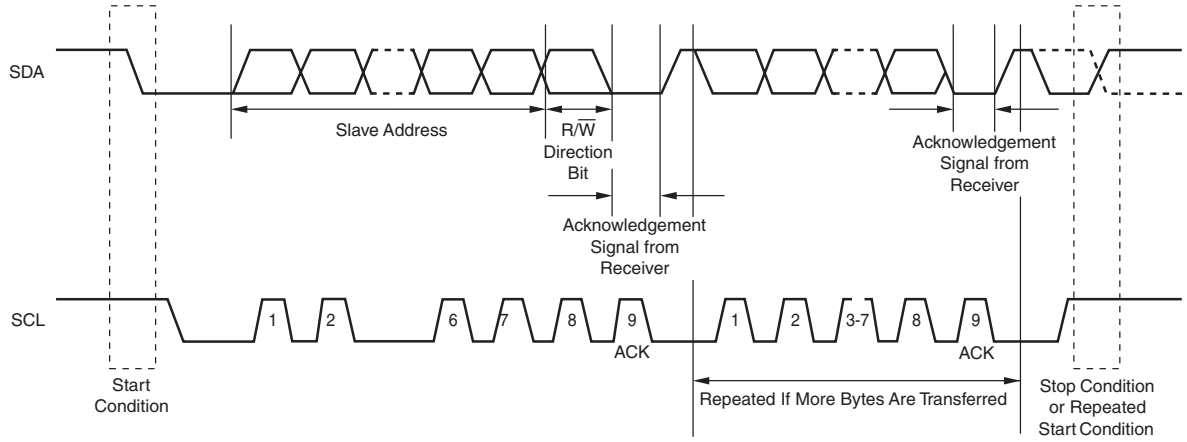


Figure 11. I²C Bus Protocol

Accordingly, the following bus conditions have been defined:

Bus Not Busy: Both data and clock lines remain high.

Start Data Transfer: A change in the state of the data line, from high to low, while the clock is high defines a Start condition.

Stop Data Transfer: A change in the state of the data line, from low to high, while the clock line is high defines a Stop condition.

Data Valid: The state of the data line represents valid data when, after a Start condition, the data line is stable for the duration of the high period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a Start condition and terminated with a Stop condition. The number of data bytes transferred between Start and Stop conditions is not limited, and is determined by the master device. The information is transferred byte-wise, and each receiver acknowledges with a ninth-bit.

Within the I²C bus specifications, a standard mode (100-kHz clock rate), a fast mode (400-kHz clock rate), and a high-speed mode (3.4-MHz clock rate) are defined. The TSC2003 works in all three modes.

Acknowledge: Each receiving device, when accessed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse, which is associated with this acknowledge bit.

A device that acknowledges must pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable low during the high period of the acknowledge clock pulse. Of course, setup and hold times must be taken into account. A master must signal an end of data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave must leave the data line high to enable the master to generate the Stop condition.

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Figure 11 details how data transfer is accomplished on the I^2C bus. Depending upon the state of the R/$\overline{W}$ bit, two types of data transfer are possible:

- Data transfer from a master transmitter to a slave receiver. The first byte transmitted by the master is the slave address. Next follows a number of data bytes. The slave returns an acknowledge bit after the slave address and each received byte.
- Data transfer from a slave transmitter to a master receiver. The first byte (the slave address) is transmitted by the master. The slave then returns an acknowledge bit. Next, a number of data bytes are transmitted by the slave to the master. The master returns an acknowledge bit after all received bytes other than the last one. At the end of the last received byte, a 'not acknowledge' is returned.

The master device generates all of the serial clock pulses and the Start and Stop conditions. A transfer is ended with a Stop condition or a repeated Start condition. Because a repeated Start condition is also the beginning of the next serial transfer, the bus is not released.

The TSC2003 may operate in the following two modes:

- Slave receiver mode: Serial data and clock are received through SDA and SCL. After each byte is received, an acknowledge bit is transmitted. Start and Stop conditions are recognized as the beginning and end of a serial transfer. Address recognition is performed by hardware after reception of the slave address and direction bit.
- Slave transmitter mode: The first byte (the slave address) is received and handled as in the slave receiver mode. However, in this mode the direction bit indicates that the transfer direction is reversed. Serial data is transmitted on SDA by the TSC2003 while the serial clock is input on SCL. Start and Stop conditions are recognized as the beginning and end of a serial transfer.

Address Byte

The address byte, as shown in Figure 12, is the first byte received following the Start condition from the master device. The first five bits (MSBs) of the slave address are factory preset to 10010. The next two bits of the address byte are the device select bits: A1 and A0. Input pins (A1 and A0) on the TSC2003 determine these two bits of the device address for a particular TSC2003. Therefore, a maximum of four devices with the same preset code can be connected on the same bus at one time.

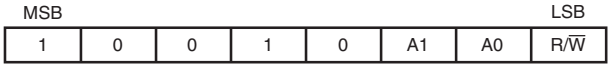


Figure 12. Address Byte

The A1–A0 address inputs can be connected to V_{DD} or digital ground. The last bit of the address byte (R/$\overline{W}$) defines the operation to be performed. When set to a "1", a read operation is selected; when set to a "0", a write operation is selected. Following the Start condition, the TSC2003 monitors the SDA bus and checks the device type identifier being transmitted. Upon receiving the 10010 code, the appropriate device select bits, and the R/$\overline{W}$ bit, the slave device outputs an acknowledge signal on the SDA line.

Command Byte

The TSC2003 operating mode is determined by a command byte, which is shown in Figure 13.

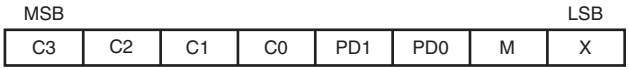


Figure 13. Command Byte

The bits in the device command byte are defined as follows:

- C3–C0: Configuration bits. These bits set the input multiplexer address and functions that the TSC2003 will perform, as shown in Table 1.
- PD1–PD0: Power-down bits. These two bits select the power-down mode that the TSC2003 will enter after the current command completes, as shown in Table 2.

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Table 1. Possible Input Configurations

C3	C2	C1	C0	FUNCTION	INPUT TO ADC	X DRIVERS	Y DRIVERS	REFERENCE MODE
0	0	0	0	Measure TEMP0	TEMP0	Off	Off	Single ended
0	0	0	1	Measure V_{BAT1}	V_{BAT1}	Off	Off	Single ended
0	0	1	0	Measure IN1	IN1	Off	Off	Single ended
0	0	1	1	Reserved	—	—	—	Single ended
0	1	0	0	Measure TEMP1	TEMP1	Off	Off	Single ended
0	1	0	1	Measure V_{BAT2}	V_{BAT2}	Off	Off	Single ended
0	1	1	0	Measure IN2	IN2	Off	Off	Single ended
0	1	1	1	Reserved	—	—	—	Single ended
1	0	0	0	Activate X– Drivers	—	On	Off	Differential
1	0	0	1	Activate Y– Drivers	—	Off	On	Differential
1	0	1	0	Activate Y+, X– Drivers	—	X– On	Y+ On	Differential
1	0	1	1	Reserved	—	—	—	Differential
1	1	0	0	Measure X Position	Y+	On	Off	Differential
1	1	0	1	Measure Y Position	X+	Off	On	Differential
1	1	1	0	Measure Z1 Position	X+	X– On	Y+ On	Differential
1	1	1	1	Measure Z2 Position	Y–	X– On	Y+ On	Differential

Table 2. Power-Down Bit Functions

PD1	PD0	$\overline{\text{PENIRQ}}$	DESCRIPTION
0	0	Enabled	Power-down between conversions
0	1	Disabled	Internal reference off, ADC on
1	0	Enabled	Internal reference on, ADC off
1	1	Disabled	Internal reference on, ADC on

The internal reference voltage can be turned on or off independently of the ADC. This can allow extra time for the internal reference voltage to settle to its final value prior to making a conversion. Allow this extra wakeup time if the internal reference was powered down. Also note that the status of the internal reference power down is latched into the part (internally) when a Stop or repeated Start occurs at the end of a command byte (see Figure 14 and Figure 16). Therefore, to turn off the internal reference, an additional write to the TSC2003 with PD1 = 0, is required after the channel has been converted.

It is recommended to set PD0 = 0 in each command byte to get the lowest power consumption possible. If multiple X-, Y-, and Z-position measurements are done one right after another, such as when averaging, PD0 = 1 leaves the touch screen drivers on at the end of each conversion cycle.

- M: Mode bit. If M is 0, the TSC2003 is in 12-bit mode. If M is 1, 8-bit mode is selected.
- X: Don't care

When the TSC2003 powers up, the power-down mode bits need to be written to ensure that the part is placed into the desired mode to achieve lowest power. Therefore, immediately after power-up, a command byte should be sent which sets PD1 = PD0 = 0, so that the device is in the lowest power mode, powering down between conversions.

Start Conversion/Write Cycle

A conversion/write cycle begins when the master issues the address byte containing the slave address of the TSC2003, with the eighth bit equal to a 0 (R/$\overline{W}$ = 0), as shown in Figure 12. Once the eighth bit has been received, and the address matches the A1–A0 address input pin setting, the TSC2003 issues an acknowledge.

Once the master receives the acknowledge bit from the TSC2003, the master writes the command byte to the slave (see Figure 13). After the command byte is received by the slave, the slave issues another acknowledge bit. The master then ends the write cycle by issuing a repeated Start or a Stop condition, as shown in Figure 14.

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If the master sends additional command bytes after the initial byte, before sending a Stop or repeated Start condition, the TSC2003 does not acknowledge those bytes.

The input multiplexer for the ADC has its channel selected when bits C3 through C0 are clocked in. If the selected channel is an X-,Y-, or Z-position measurement, the appropriate drivers turn on once the acquisition period begins.

When R/$\overline{W}$ = 0, the input sample acquisition period starts on the falling edge of SCL once the C0 bit of the command byte has been latched, and ends when a Stop or repeated Start condition has been issued. A/D conversion starts immediately after the acquisition period. The multiplexer inputs to the ADC are disabled once the conversion period starts. However, if an X-, Y-, or Z-position is being measured, the respective touch screen drivers remain on during the conversion period. A complete write cycle is shown in Figure 14.

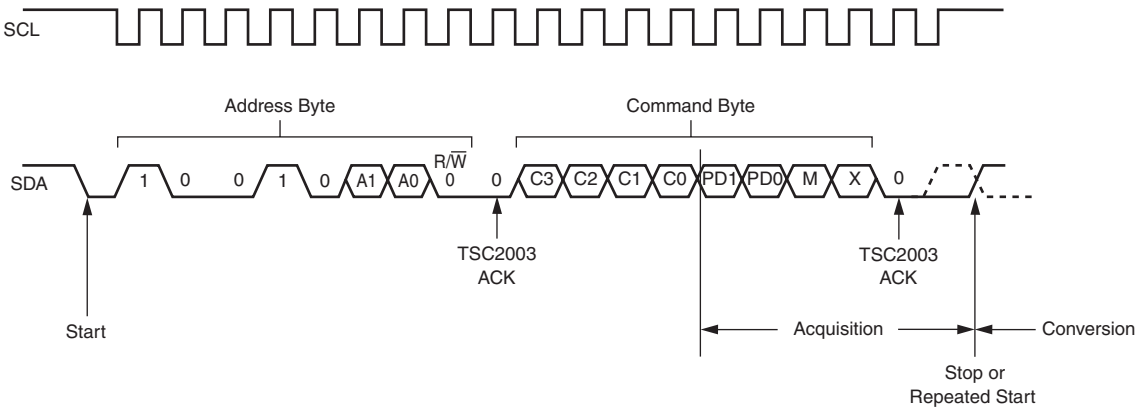


Figure 14. Complete I²C Serial Write Transmission

Read a Conversion/Read Cycle

For best performance, the I²C bus should remain in an idle state while an A/D conversion is taking place. This prevents digital clock noise from affecting the bit decisions being made by the TSC2003. The master should wait for at least 10 µs before attempting to read data from the TSC2003 to realize this best performance. However, the master does not need to wait for a completed conversion before beginning a read from the slave, if full 12-bit performance is not necessary.

Data access begins with the master issuing a Start condition followed by the address byte (see Figure 12) with R/$\overline{W}$ = 1. Once the eighth bit has been received, and the address matches, the slave issues an acknowledge. The first byte of serial data follows (D11 to D4, MSB first).

After the first byte has been sent by the slave, it releases the SDA line for the master to issue an acknowledge. The slave responds with the second byte of serial data upon receiving the acknowledge from the master (D3-D0, followed by four 0 bits). The second byte is followed by a NOT acknowledge bit (ACK = 1) from the master to indicate that the last data byte has been received. If the master acknowledges the second data byte, then the data repeats on subsequent reads with ACKs between bytes. This is true in both 12-bit and 8-bit mode. The master then issues a Stop condition, which ends the read cycle, as shown in Figure 15.

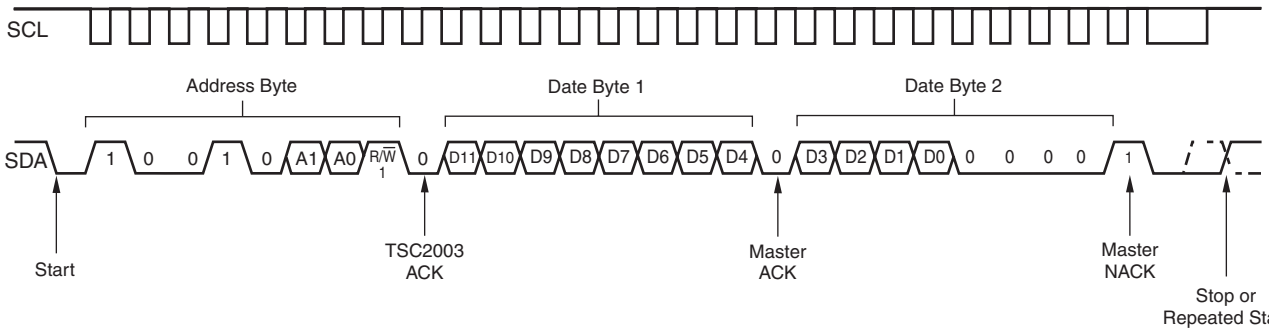


Figure 15. Complete I²C Serial Read Transmission

I²C High-Speed Operation

The TSC2003 can operate with high-speed I²C masters. To do so, the simple resistor pullup on SCL must be changed to the active pullup, as recommended in the I²C specification.

The I²C bus operates in standard or fast mode initially. Following a Start condition, the master sends the code 00001xxx, which the slave does not acknowledge. The bus now operates in high-speed mode and remains in high-speed mode until a Stop condition occurs. Therefore, to maximize throughput, only repeated Starts should be used to separate transactions.

Because the TSC2003 may not have completed a conversion before a read to the part can be requested, the TSC2003 is capable of stretching the clock until the converted data is stored in its internal shift register. Once the data is latched, the TSC2003 releases the clock line so that the master can receive the converted data. A complete high-speed conversion cycle is shown in Figure 16.

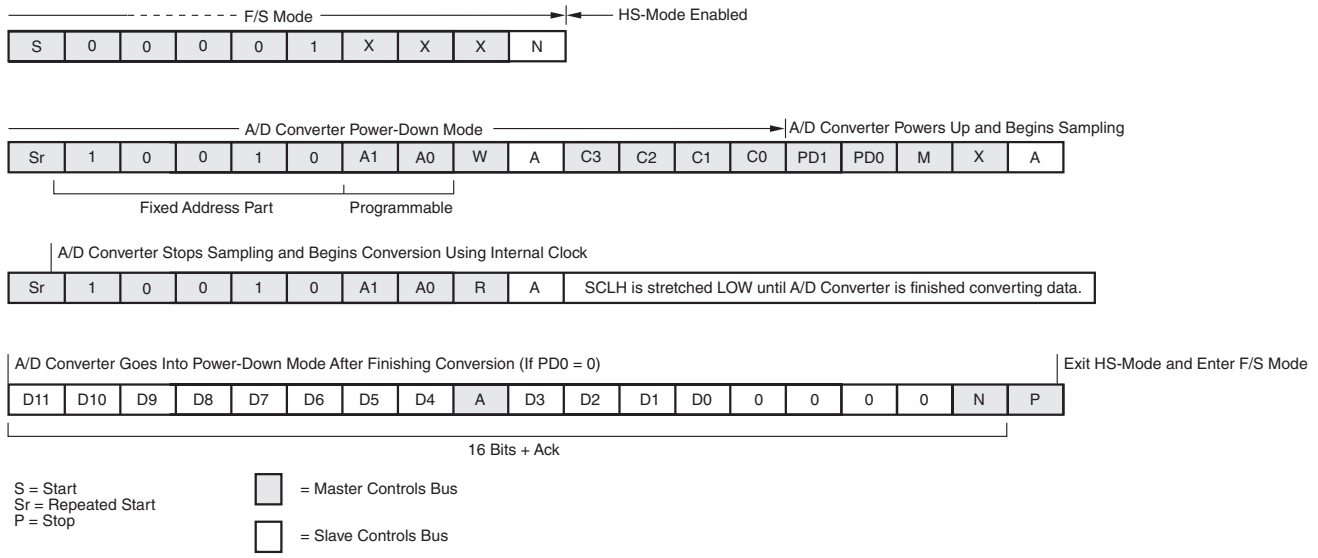
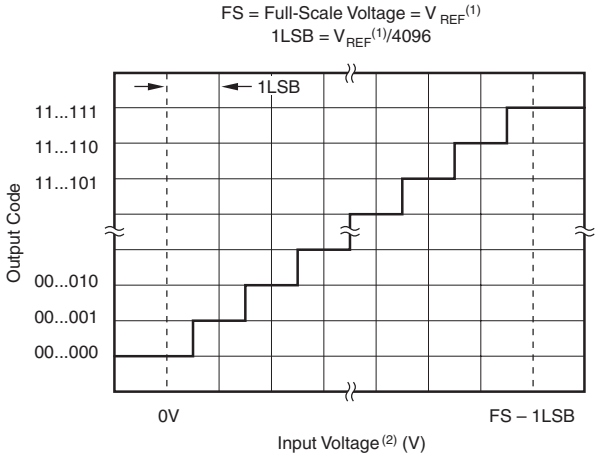


Figure 16. High-Speed I²C Mode Conversion Cycle

Data Format

The TSC2003 output data is in straight binary format, as shown in Figure 17. This shows the ideal output code for the given input voltage, and does not include the effects of offset, gain, or noise.



NOTES: (1) Reference voltage at converter: +REF – (–REF). See Figure 2.
(2) Input voltage at converter, after multiplexer: +IN – (–IN). See Figure 2

Figure 17. Ideal Input Voltages and Output Codes

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8-Bit Conversion

The TSC2003 provides an 8-bit conversion mode (M = 1) that can be used when faster throughput is needed, and the digital result is not as critical (for example, measuring pressure). By switching to the 8-bit mode, a conversion result can be read by transferring only one data byte.

This shortens each conversion by four bits and reduces data transfer time which results in fewer clock cycles and provides lower power consumption.

Layout

The following layout suggestions should provide optimum performance from the TSC2003. However, many portable applications have conflicting requirements concerning power, cost, size, and weight. In general, most portable devices have fairly "clean" power and grounds because most of the internal components are very low power. This situation would mean less bypassing for the converter's power, and less concern regarding grounding. Still, each situation is unique, and the following suggestions should be reviewed carefully.

For optimum performance, care should be taken with the physical layout of the TSC2003 circuitry. The basic SAR architecture is sensitive to glitches or sudden changes on the power supply, reference, ground connections, and digital inputs that occur just prior to latching the output of the analog comparator. Therefore, during any single conversion for an n-bit SAR converter, there are n "windows" in which large external transient voltages can easily affect the conversion result. Such glitches might originate from switching power supplies, nearby digital logic, and high-power devices. The degree of error in the digital output depends on the reference voltage, layout, and the exact timing of the external event. The error can change if the external event changes in time with respect to the SCL input.

With this in mind, power to the TSC2003 should be clean and well bypassed. A 0.1-µF ceramic bypass capacitor should be placed as close to the device as possible. In addition, a 1-µF to 10-µF capacitor may also be needed if the impedance of the connection between V_{DD} and the power supply is high.

A bypass capacitor is generally not needed on the V_{REF} pin because the internal reference is buffered by an internal op amp. If an external reference voltage originates from an operational amplifier, ensure that it can drive any bypass capacitor that is used without oscillation.

The TSC2003 architecture offers no inherent rejection of noise or voltage variation in regards to using an external reference input. This is of particular concern when the reference input is tied to the power supply. Any noise and ripple from the supply appears directly in the digital results. While high-frequency noise can be filtered out, voltage variation due to line frequency (50 Hz or 60 Hz) can be difficult to remove.

The GND pin should be connected to a clean ground point. In many cases, this is the "analog" ground. Avoid connections which are too near the grounding point of a microcontroller or digital signal processor. If needed, run a ground trace directly from the converter to the power-supply entry point. The ideal layout includes an analog ground plane dedicated to the converter and associated analog circuitry.

In the specific case of use with a resistive touch screen, care should be taken with the connection between the converter and the touch screen. Because resistive touch screens have fairly low resistance, the interconnection should be as short and robust as possible. Longer connections can be a source of error, much like the on-resistance of the internal switches. Likewise, loose connections can be a source of error when the contact resistance changes with flexing or vibrations.

As indicated previously, noise can be a major source of error in touch screen applications (e.g., applications that require a backlit LCD panel). This EMI noise can be coupled through the LCD panel to the touch screen and cause "flickering" of the converted data. Several things can be done to reduce this error, such as utilizing a touch screen with a bottom-side metal layer connected to ground. This couples the majority of noise to ground. Additionally, filtering capacitors from Y+, Y–, X+, and X– to ground can also help.

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$\overline{\text{PENIRQ}}$ Output

The pen-interrupt output function is shown in Figure 18. By connecting a pullup resistor to V_{DD} (typically 100 kΩ), the $\overline{\text{PENIRQ}}$ output is high. While in the power-down mode, with PD0 = 0, the Y– driver is on and connected to GND, and the $\overline{\text{PENIRQ}}$ output is connected to the X+ input. When the panel is touched, the X+ input is pulled to ground through the touch screen, and $\overline{\text{PENIRQ}}$ output goes low due to the current path through the panel to GND, initiating an interrupt to the processor. During the measurement cycle for X, Y, and Z positions, the X+ input is disconnected from the $\overline{\text{PENIRQ}}$ pulldown transistor to eliminate any leakage current from the pullup resistor to flow through the touch screen, thus causing no errors.

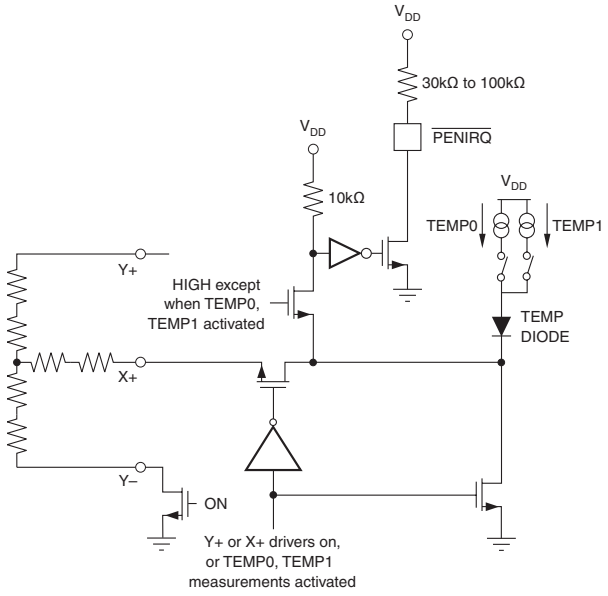


Figure 18. $\overline{\text{PENIRQ}}$ Functional Block Diagram

In addition to the measurement cycles for X-, Y-, and Z-position, commands which activate the X-drivers, Y-drivers, Y+ and X-drivers without performing a measurement also disconnect the X+ input from the $\overline{\text{PENIRQ}}$ pulldown transistor and disable the pen-interrupt output function regardless of the value of the PD0 bit. Under these conditions, the $\overline{\text{PENIRQ}}$ output is forced low. Furthermore, if the last command byte written to the TSC2003 contains PD0 = 1, the pen-interrupt output function is disabled and is not able to detect when the panel is touched. To re-enable the pen-interrupt output function under these circumstances, a command byte needs to be written to the TSC2003 with PD0 = 0.

Once the bus master sends the address byte with R/$\overline{\text{W}}$ = 0 (see Figure 12) and the TSC2003 sends an acknowledge, the pen-interrupt function is disabled. If the command that follows the address byte has PD0 = 0, then the pen-interrupt function is enabled at the end of a conversion. This is approximately 10 μs (12-bit mode) or 7 μs (8-bit mode) after the TSC2003 receives a Stop/Start condition following the reception of a command byte (see Figure 14 and Figure 16 for further details of when the conversion cycle begins).

In both cases listed above, it is recommended that the master processor mask the interrupt which the $\overline{\text{PENIRQ}}$ is associated with whenever the host writes to the TSC2003. This prevents false triggering of interrupts when the $\overline{\text{PENIRQ}}$ line is disabled in the cases listed above.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TSC2003IPWRQ1	ACTIVE	TSSOP	PW	16	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	T2003Q1	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF TSC2003-Q1 :

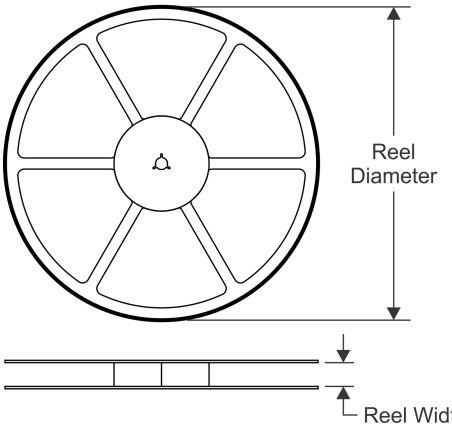
- Catalog: TSC2003

NOTE: Qualified Version Definitions:

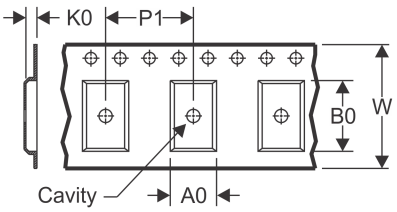
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

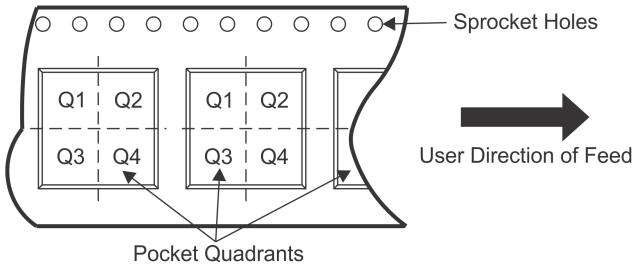


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

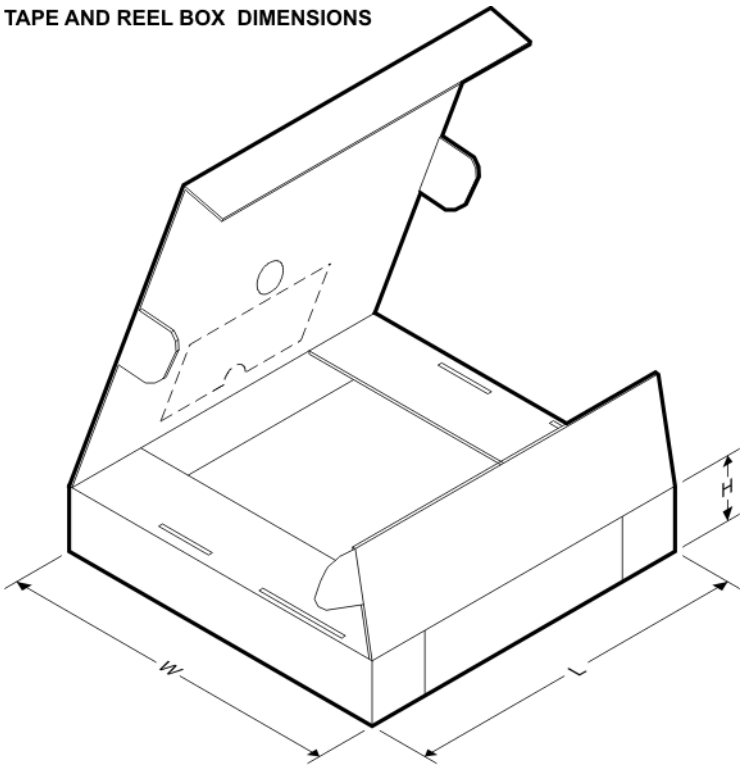
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TSC2003IPWRQ1	TSSOP	PW	16	2500	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

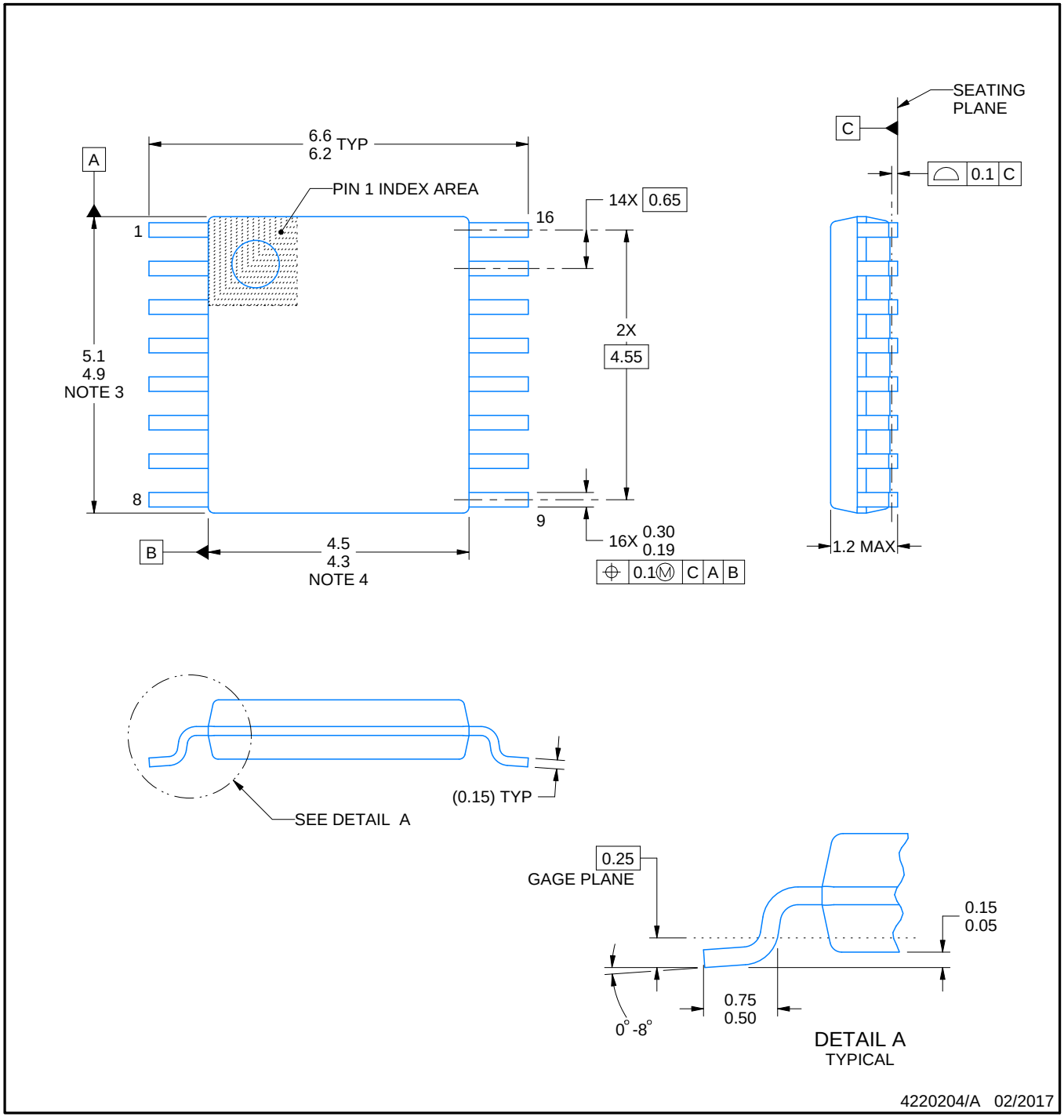
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TSC2003IPWRQ1	TSSOP	PW	16	2500	350.0	350.0	43.0

PACKAGE OUTLINE

PW0016A

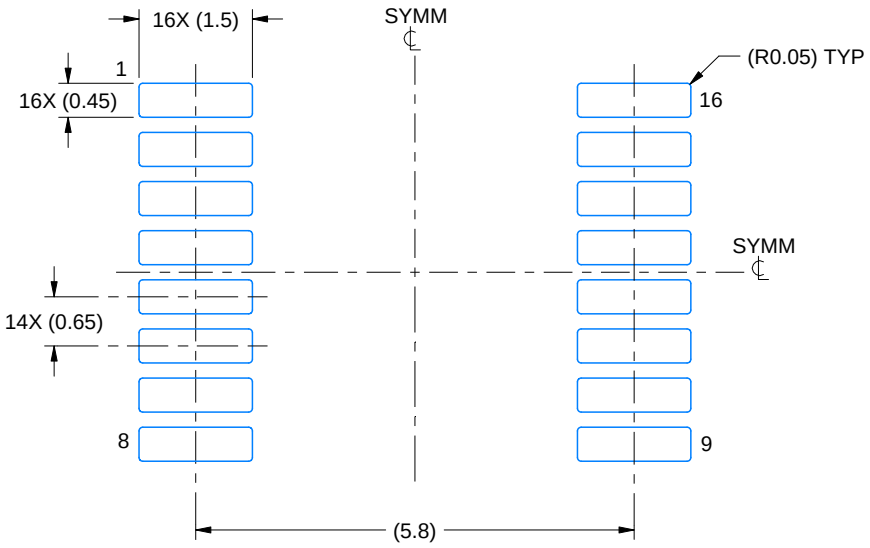
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

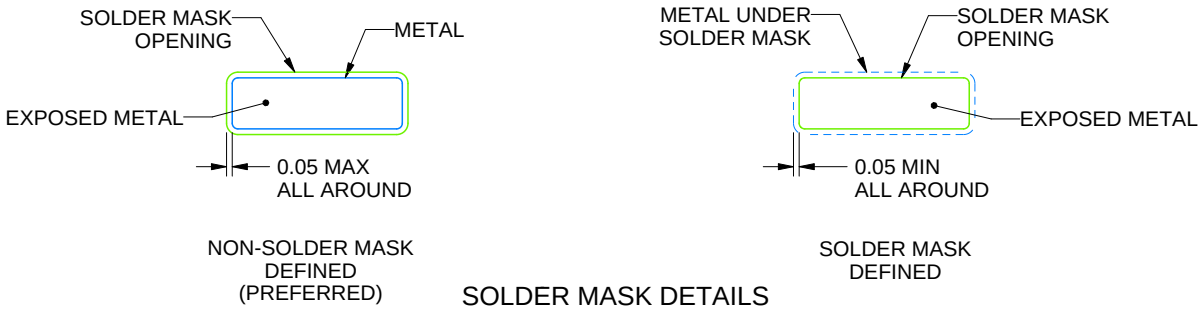


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

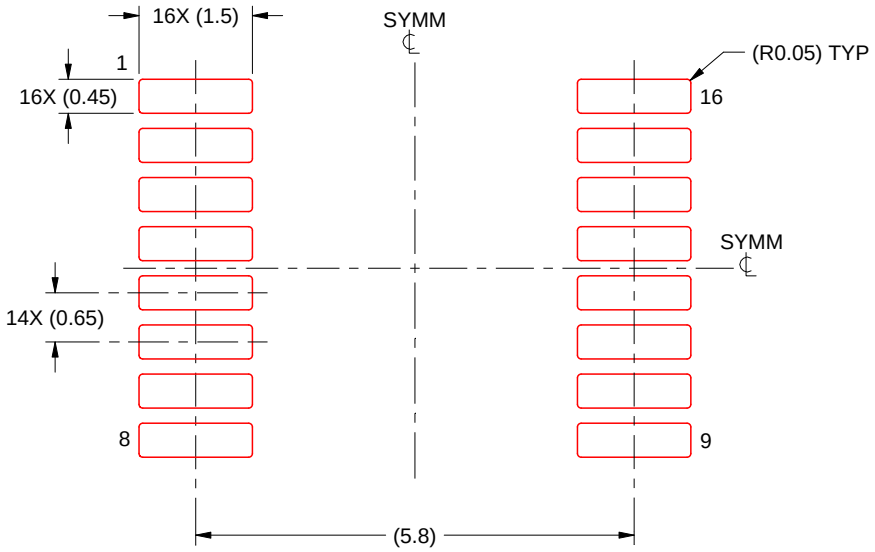


SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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