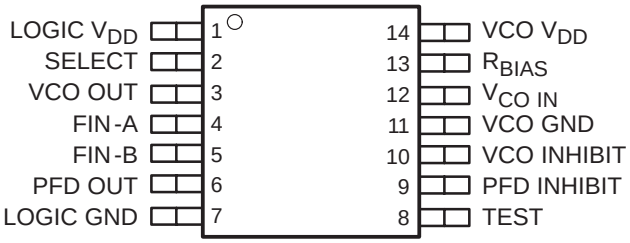
- **Voltage-Controlled Oscillator (VCO)**
  - **Ring Oscillator Using Only One External Biasing Resistor (R_{BIAS})**
- **Recommended Lock Frequency**
  - **100 MHz to 130 MHz**
  - **(V_{DD} = 3.3 V + 5%, T_A = –20°C to 75°C)**
- **Phase-Frequency Detector (PFD) Includes a High-Speed Edge-Triggered Detector With Internal Charge Pump**
- **Independent VCO, PFD Power-Down Mode**
- **Thin Small-Outline Package (14 Terminal)**
- **Compatible Pin Assignment to TLC2932, TLC2933**

PW PACKAGE
(TOP VIEW)



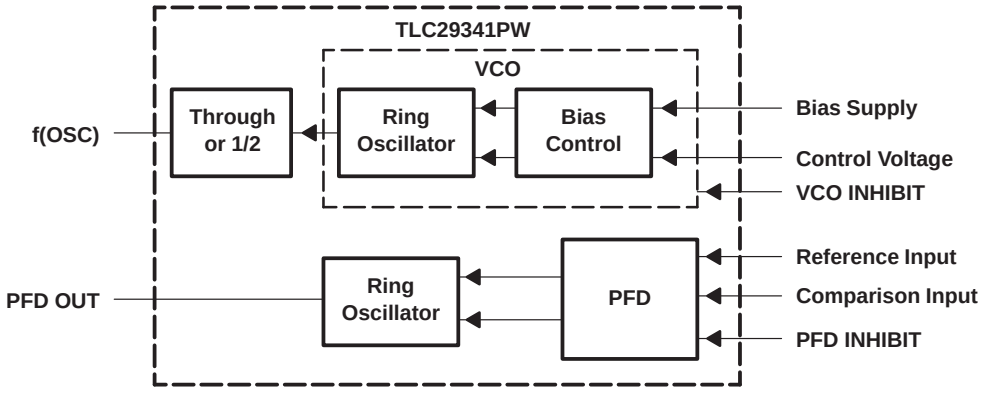
description

The TLC2934, a mixed signal IC designed for phase-locked-loop (PLL) systems, is composed of a voltage-controlled oscillator (VCO) and an edge-triggered-type phase frequency detector (PFD).

The internal VCO is based on the TLC2932 and TLC2933s ring oscillator. It oscillates in wider frequency with lower supply voltage, and it has stable oscillating performance. The oscillation function, provided by only one external resistor connection, supplies bias to the VCI internal circuit. Oscillator range is covered from 10 MHz to 130 MHz with a 3.3-V supply voltage. The VCO has an inhibit function to stop oscillation and for the power-down mode.

The internal PFD, a high-speed rising edge triggered type, has an internal charge pump with a high-impedance output buffer. The PFD detects phase difference between the reference frequency input and the signal frequency input from the VCO output through an external counter device. This functions the same as TLC2932 and TLC2933. The PFD also has the inhibit function for stop phase comparison and for power-down mode.

block diagram



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
FIN-A, FIN-B	4 5	I	Frequency signal inputs for PFD. The reference frequency signal (f_{REF-IN}) and the VCO output signal through the external counter device are applied to these terminals. When the LPF design is the lag-lead filter (passive filter and noninverting), $f_{(REF-IN)}$ is input to FIN-A, and the VCO output signal is to FIN-B.
LOGIC GND	7		GND terminal for the internal logic circuit
LOGIC V_{DD}	1		Power supply terminal for the internal logic circuit. This power supply terminal separates from VCO V_{DD} to reduce cross-coupling between supplies.
PFD INHIBIT	9	I	PFD INHIBIT (power-down) control signal input terminal
PFD OUT	6	O	PFD output terminal. When PFD INHIBIT is high, PFD OUT is in the high-impedance state.
R_{BIAS}	13	I	Bias resistor (R_{BIAS}) terminal. Connect a resistor between VCO GND and this terminal to supply bias to internal VCO circuit. TLC2934 bias resistor connection is different from TLC2932 and TLC2933, where bias resistor R_{BIAS} is connected to VCO V_{DD}.
SELECT	2	I	1/2 divider select terminal. L=through output, H=1/2 output.
TEST	8		Test terminal. Use for production test. Tie to GND when in normal use.
VCO GND	11		GND terminal for internal VCO
VCO OUT	3	O	VCO output terminal. When VCO INHIBIT = high, VCO OUT is low.
VCO INHIBIT	10	I	VCO INHIBIT (power-down) control signal input terminal
$V_{CO\ IN}$	12	I	VCO control voltage input terminal. Normally, The external LPF is connected to this terminal.
VCO V_{DD}	14		Power supply terminal for the internal VCO circuit. This power supply terminal should be separate from LOGIC V_{DD} to reduce cross-coupling between supplies.

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage (each supply), V_{DD} (see Note 1) . . . . . –0.5 V to 4 V
Input voltage range (each input), V_I (see Note 1) . . . . . –0.5 V to V_{DD} + 0.5 V
Input current (each input), I_I . . . . . ±20 mA
Output current (each output), I_O . . . . . ±20 mA
Continuous total power dissipation at (or below) T_A = 25°C (see Note 2), P_D . . . . . 700 mW
Operating free-air temperature range. T_A . . . . . –20°C to 75°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to network ground terminal.
2. For operation above 25°C free–air temperature, derate linearly at the rate of 5.6 mW/°C

recommended operating conditions

		MIN	TYP	MAX	UNIT
Supply voltage (each supply, V_{DD} (see Notes 3 and 4)		3.15	3.3	3.45	V
Input voltage (each input except for $V_{CO\ IN}$, V_I		0		V_{DD}	V
Output current (each output), I_O		0		±2	mA
VCO control voltage, $V_{CO\ IN}$		0.5		V_{DD}	V
Lock frequency (through output)	R_{BIAS} = 1 kΩ	36		130	MHz
	R_{BIAS} = 1.8 kΩ	28		90	
	R_{BIAS} = 2.4 kΩ	26		80	
	R_{BIAS} = 3.3 kΩ	20		60	
Lock frequency (1/2 output)	R_{BIAS} = 1 kΩ	18		65	MHz
	R_{BIAS} = 1.8 kΩ	14		45	
	R_{BIAS} = 2.4 kΩ	13		40	
	R_{BIAS} = 3.3 kΩ	10		30	
Bias resistor, R_{BIAS}		1.0		3.3	KΩ
Operating temperature range, T_A		–20		75	°C
$V_{CO\ IN}$ voltage at VCO INHIBIT↓, $V_{(CINH)}$ (see Note 5)			0	0.5	V

NOTES: 3. It is recommended that the logic supply terminal (LOGIC V_{DD}) and the VCO supply terminal (VCO V_{DD}) be at the same voltage and separated from each other.
4. A bypass capacitor is placed as close as possible to each supply terminal.
5. For stable restart of VCO, V_{COIN} is 0 V when VCO INHIBIT is pulled down to GND level to disable the VCO INHIBIT function. And also, $V_{CO\ IN}$ should be 0 V when the operation will be started by supplying the power.

electrical characteristics over recommended operating free-air temperature range, V_{DD}=3.3 V (unless otherwise noted)

VCO

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –2 mA	3.1			V
V_{OL}	Low-level output voltage	I_{OL}= 2 mA			0.2	V
V_{IH}	High-level input voltage	Logic signal input	2.3			V
V_{IL}	Low-level input voltage	Logic signal input			1.0	V
I_I	Input current at TEST, VCO INHIBIT	V_I = V_{DD} or GND			±1	µA
$Z_{V(CO\ IN)}$	Input impedance at V_{COIN}	V_{COIN} = 1/2 V_{DD}		10		MΩ
$I_{DD(INH)}$	VCO supply current (inhibit)	See Note 6		0.01	1	µA
$I_{DD(VCO)}$	VCO supply current	See Note 7		10	15	mA

NOTES: 6. Current into VCO V_{DD}, when VCO INHIBIT = V_{DD}, PFD is inhibited.
7. Current into VCO V_{DD}, when V_{COIN} = 1/2 V_{DD}, R_{BIAS} = 1 kΩ, VCO INHIBIT = GND, PFD is inhibited.

electrical characteristics over recommended operating free-air temperature range, V_{DD}=3.3 V (unless otherwise noted) (continued)

VCO

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –2 mA	3.1			V
V_{OL}	Low-level output voltage	I_{OL} = 2 mA			0.2	V
I_{OZ}	High-impedance state output current	PFD INHIBIT = high, $V_O = V_{DD}$ or GND			±1	µA
V_{IH}	High-level input voltage at FIN–A,B		2.3			V
V_{IL}	Low-level input voltage at FIN–A,B				1.0	V
$V_{(TO)}$	Positive input threshold voltage at PFD INHIBIT		1.0	1.65	2.3	V
C_I	Input capacitance at FIN-A,B			5		pF
$Z_{(IN)}$	Input impedance at FIN-A,B			10		MΩ
$I_{DD(PFD)}$	PFD supply current	See Note 8		1.5	6.0	mA

NOTE 8: Current into LOGIC V_{DD}, when FIN-A, FIN-B=50 MHz ($V_{I(pp)}$ = 3.3V, rectangular wave), Test=GND, no load, and VCO OUT is inhibited.

VCO

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$f_{(OSC)}$	Operating oscillation frequency	R_{BIAS} = 1 kΩ	67	90	113	MHz
$t_{(STB)}$	Time to stable oscillation	See Note 9		0.7	10	µs
t_r	Rise time	C_L = 15 pF, See Figure 3		1.7	5	ns
t_f	Fall time	C_L = 15 pF, See Figure 3		1.1	4	ns
$f_{(duty)}$	Duty cycle at VCO OUT	R_{BIAS} = 1.0 kΩ, $V_{CO\ IN}$ = 1/2 V_{DD}	45%	50%	55%	
	Temperature coefficient of oscillation frequency	R_{BIAS}=1.0kΩ, $V_{CO\ IN}$ = 1/2 V_{DD}, T_A = –20°C to 75°C		0.03		%/°C
	Supply voltage coefficient of oscillation frequency	R_{BIAS} = 1 kΩ, $V_{CO\ IN}$ = 1.65 V, V_{DD} = 3.15 V to 3.45 V		0.02		%/mV
	Jitter absolute	R_{BIAS} = 1 kΩ, $V_{CO\ IN}$ = 1/2 V_{DD}		50		ps

NOTE 9: Current into VCO V_{DD}, when VCO INHIBIT = V_{DD}, PFD is inhibited.

PFD AC

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{MAX}	Maximum operating frequency		50			MHz
t_{PLZ}	PFD output disable time from low level	See Figures 4 and 5 and Table 6		15.3	40	ns
t_{PHZ}	PFD output disable time from high level			15.5	40	ns
t_{PZL}	PFD output enable time from low level			2.4	10	ns
t_{PZH}	PFD output enable time from high level			2.5	10	ns
t_r	Rise time	C_L=15 pF (see Figure 3)		1.2	5	ns
t_f	Fall time	C_L=15 pF (see Figure 3)		0.7	5	ns

PARAMETER MEASUREMENT INFORMATION

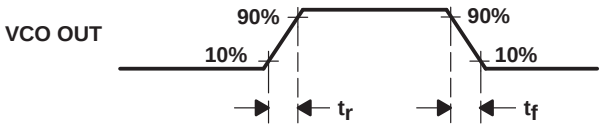
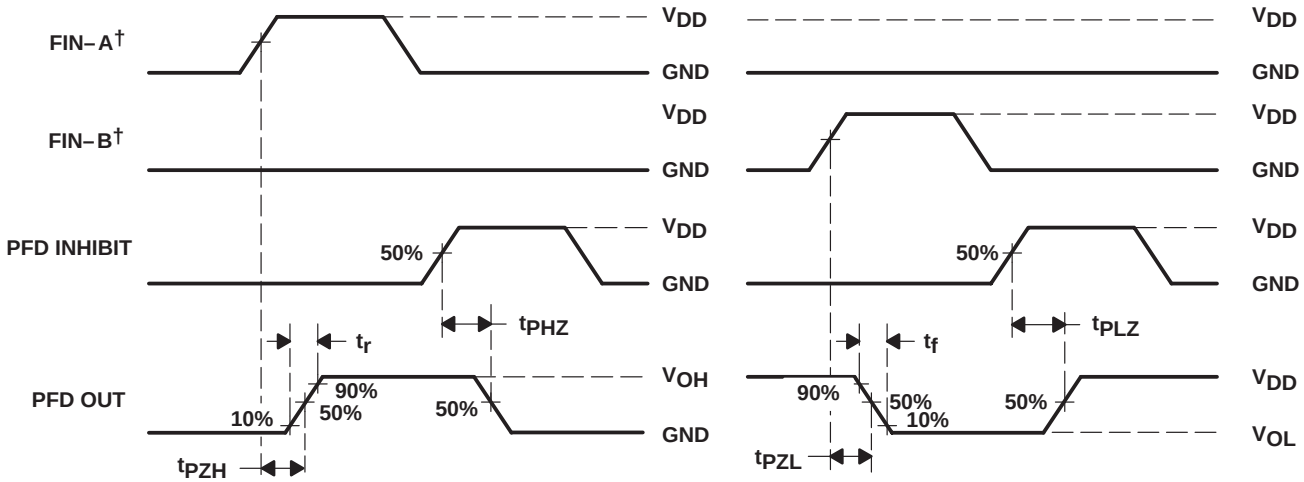


Figure 1. VCO Output Voltage Waveform



(see Figure 3 and PFD Output Test Conditions Table)

† FIN-A and FIN-B are for reference phase only, not for timing.

Figure 2. PFD Output Voltage Waveform

PFD Output Test Conditions

PARAMETER	R_L	C_L	S_L	S_2
t_{PZH}	1 kΩ	15 pF	Open	Close
t_{PHZ}				
t_r				
t_{PZL}			Close	Open
t_{PLZ}				
t_f				

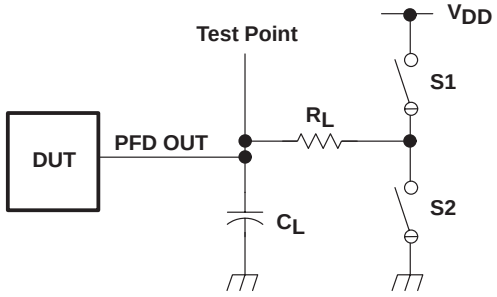


Figure 3. PFD Output Test Condition

TYPICAL CHARACTERISTICS

VCO OSCILLATION FREQUENCY
vs
VCO CONTROL VOLTAGE

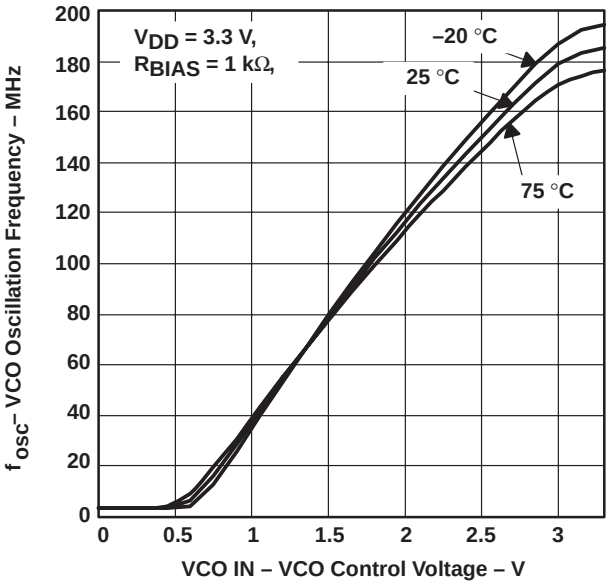


Figure 4

VCO OSCILLATION FREQUENCY
vs
VCO CONTROL VOLTAGE

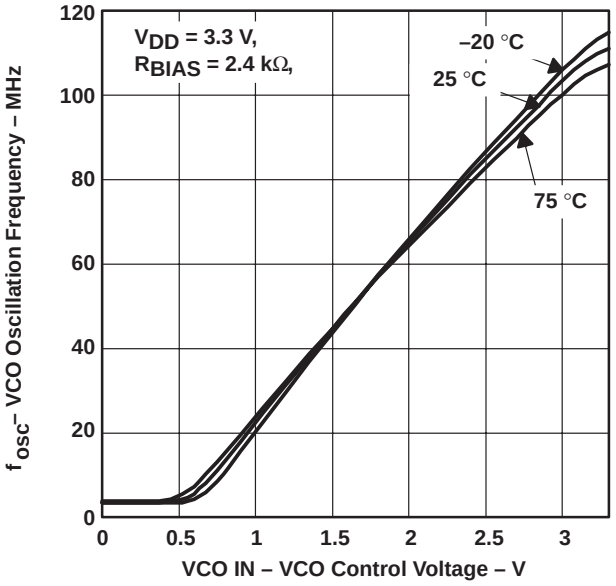


Figure 5

VCO OSCILLATION FREQUENCY
vs
VCO CONTROL VOLTAGE

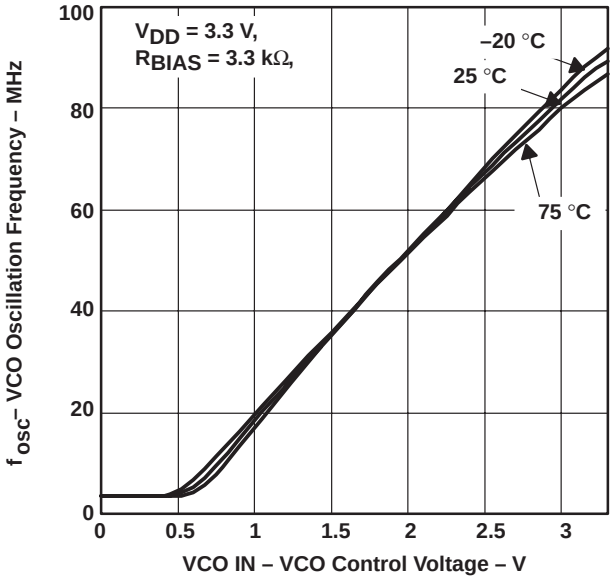


Figure 6

VCO OSCILLATION FREQUENCY
vs
VCO SUPPLY VOLTAGE

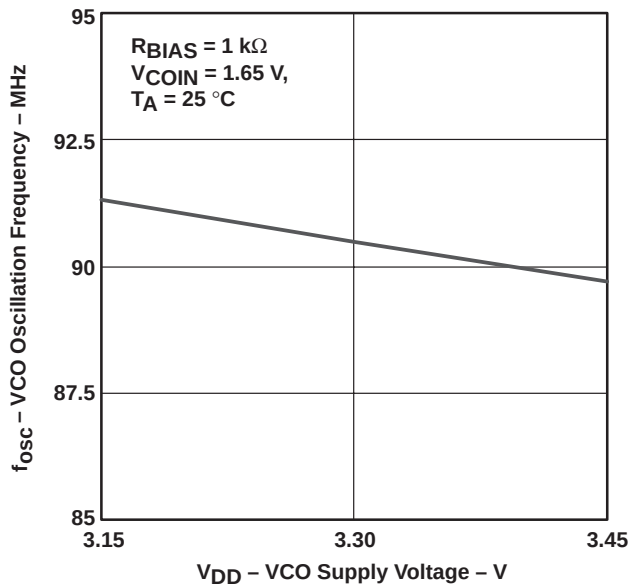


Figure 7

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLC2934IPW	NRND	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-20 to 75	Y2934	
TLC2934IPWG4	NRND	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-20 to 75	Y2934	
TLC2934IPWR	NRND	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-20 to 75	Y2934	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

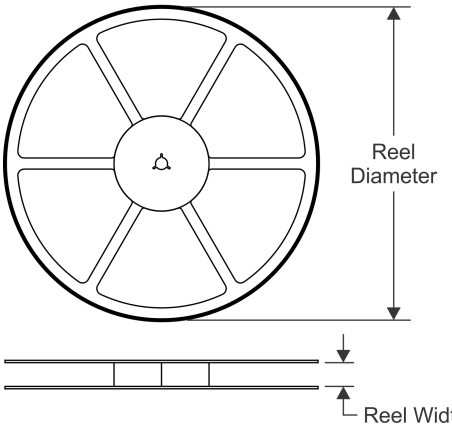
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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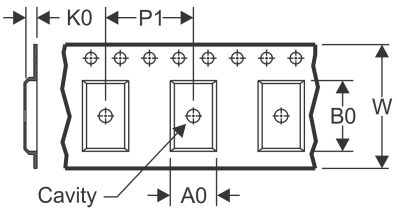
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

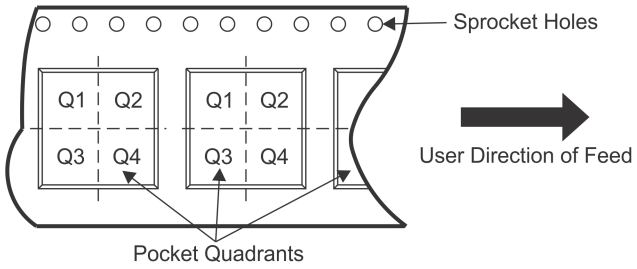


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

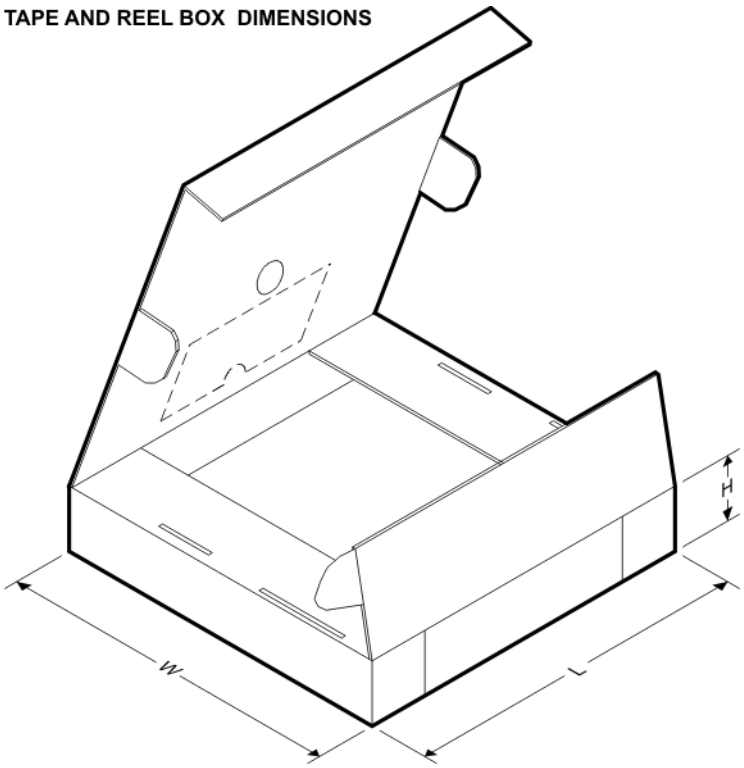
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLC2934IPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLC2934IPWR	TSSOP	PW	14	2000	367.0	367.0	35.0

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