

RELIABILITY REPORT
FOR
MAX2981GCB+
PLASTIC ENCAPSULATED DEVICES

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MAXIM INTEGRATED

160 RIO ROBLES
SAN JOSE, CA 95134

Approved by
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Conclusion

The MAX2981GCB/V+ successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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I. Device Description**A. General**

The MAX2981 powerline communication analog front-end (AFE) and line-driver IC is a state-of-the-art CMOS device that delivers high performance at low cost. This highly integrated design combines an analog-to-digital converter (ADC), digital-to-analog converter (DAC), adaptive gain control (AGC), filters, and line driver on a single chip. The MAX2981 substantially reduces previously required system components and complies with the HomePlug® 1.0 standard. Combined with Maxim's integrated PHY/MAC digital baseband, the device delivers the most flexible and cost-effective solution. The advanced design of the MAX2981 allows operation without external control, enabling simplified connection to a variety of HomePlug 1.0 digital PHY ICs. The MAX2981 is specified over the -40°C to +105°C automotive temperature range and is offered in a 64-pin lead-free LQFP package. The device is qualified to the AEC-Q100 Rev F automotive standard.

II. Manufacturing Information

A. Description/Function:	Integrated Powerline Communication Analog Front-End Transceiver and Line Driver
B. Process:	TS25EF
C. Number of Device Transistors:	128598
D. Fabrication Location:	Taiwan
E. Assembly Location:	Korea
F. Date of Initial Production:	July 21, 2009

III. Packaging Information

A. Package Type:	64-pin LQFP
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Die Attach:	Conductive
E. Bondwire:	Au (1 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-9000-3276
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 3
J. Single Layer Theta Ja:	N/A
K. Single Layer Theta Jc:	N/A
L. Multi Layer Theta Ja:	40°C/W
M. Multi Layer Theta Jc:	8°C/W

IV. Die Information

A. Dimensions:	216 X 142 mils
B. Passivation:	HDP Oxide, Nitride
C. Interconnect:	Ti/TiN/Al/Ti/TiN
D. Backside Metallization:	None
E. Minimum Metal Width:	
F. Minimum Metal Spacing:	
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO ₂
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:	Richard Aburano (Manager, Reliability Engineering) Don Lipps (Manager, Reliability Engineering) Bryan Preeshl (Vice President of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% For all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. Sampling Plan:	Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 110C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{1000 \times 986 \times 236 \times 2} \quad (\text{Chi square value for MTTF upper limit})$$

(where 986 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$$\lambda = 3.9 \times 10^{-9}$$

$$\lambda = 3.9 \text{ F.I.T. (60\% confidence level @ 25°C)}$$

The following failure rate represents data collected from Maxim's reliability monitor program. Maxim performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at <http://www.maxim-ic.com/qa/reliability/monitor>. Cumulative monitor data for the TS25EF Process results in a FIT Rate of 1.0 @ 25C and 17.5 @ 55C (0.8 eV, 60% UCL).

B. Moisture Resistance Tests

The industry standard 85°C/85%RH or HAST testing is monitored per device process once a quarter.

C. E.S.D. and Latch-Up Testing

The WV13 die type has been found to have all pins able to withstand a transient pulse of:

ESD-HBM:	+/- 2500V per JEDEC JESD22-A114
ESD-CDM:	+/- 750V per JEDEC JESD22-C101

Latch-Up testing has shown that this device withstands a current of +/- 250mA and overvoltage per JEDEC JESD78.

Table 1
 Reliability Evaluation Test Results

MAX2981GCB+

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)				
	Ta = 110°C Biased Time = 1000 hrs.	DC Parameters & functionality	236	0
Moisture Testing (Note 2)				
HAST	Ta = 130°C RH = 85% Biased Time = 96hrs.	DC Parameters & functionality	238	0
Mechanical Stress (Note 2)				
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters & functionality	314	0

Note 1: Life Test Data may represent plastic DIP qualification lots.

Note 2: Generic Package/Process data