MP6004

Primary-Side Regulated Flyback/Buck 80V DCDC Converter

The Future of Analog IC Technology

DESCRIPTION

The MP6004 is a monolithic flyback dc-dc converter with a 180 V power switch that targets isolated or non-isolated 13 W PoE applications. It supports both primary-side regulated flyback and high-voltage buck applications.

MP6004 uses fixed peak current and variable frequency discontinuous conduction mode (DCM) to regulate constant output voltage. The primary-side regulation without opto-coupler feedback in flyback mode simplifies the design and saves BOM cost while buck mode minimizes the solution size for non-isolated applications. A 180 V integrated power MOSFET optimizes the device for various wide voltage applications.

The MP6004 protection features include over-load protection, over-voltage protection, open-circuit protection, and thermal shutdown.

The MP6004 is available in a QFN-14 3mm x 3mm package.

FEATURES

- Supports Primary-Side Regulated Flyback without Opto-Coupler Feedback
- Supports Buck from Up to 80 V Input
- Integrated 180 V Switching Power MOSFET
- Internal 80 V Start-Up Circuit
- Up to 3 A Programmable Current Limit
- Discontinuous Conduction Mode
- OLP, OVP, Open-Circuit, and Thermal Protection
- Flexible Self-Power or External V_{CC} Power
- Minimal External Component Count
- Available in a QFN-14 3mm x 3mm Package

APPLICATIONS

- Security Cameras
- VoIP Phones
- WLAN Access Points
- General Flyback and Buck Converters

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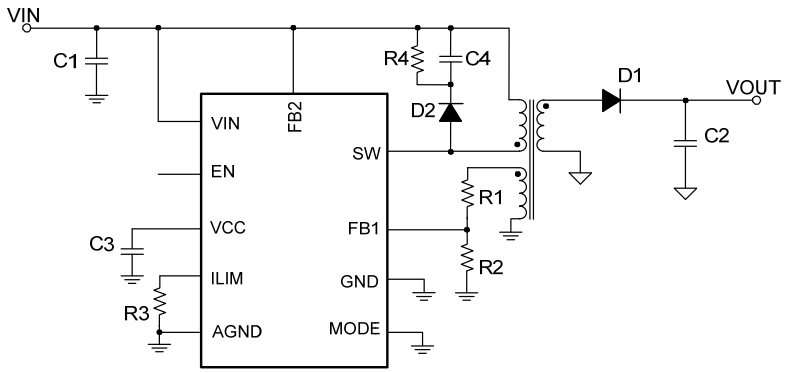
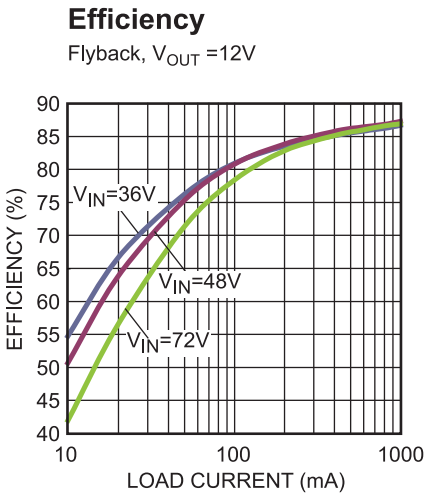
TYPICAL APPLICATION





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ORDERING INFORMATION

Part Number*	Package	Top Marking
MP6004GQ	QFN-14 (3mm x 3mm)	*See Below*

* For Tape & Reel, add suffix –Z (e.g. MP6004GQ–Z)

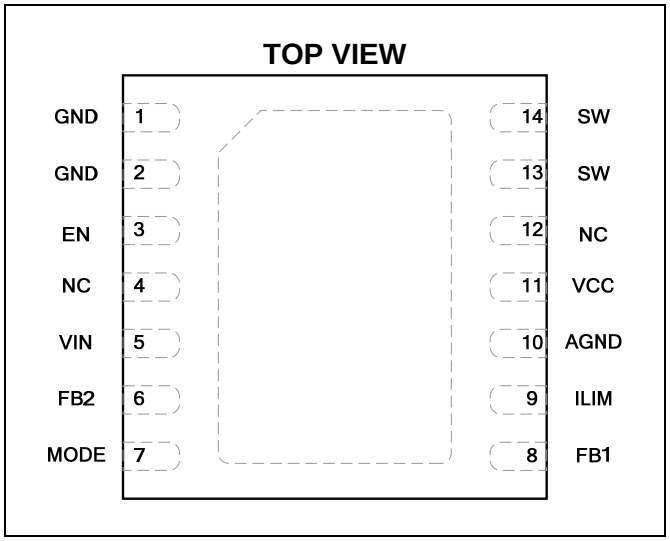
TOP MARKING

AMNY

LLL

AMN: Product code of MP6004GQ
Y: Year code
LLL: Lot number

PACKAGE REFERENCE



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ABSOLUTE MAXIMUM RATINGS (1)

VIN .....-0.3 V to +100 V
SW .....-0.7 V to +180 V
FB1 .....-0.7 V to +6.5 V(2)
FB2 to VIN .....-6.5 V to +0.3 V
All other pins .....-0.3 V to +6.5 V(3)
VCC sinking current ..... 1.5 mA(4)
FB1 sinking current ..... ±1 mA(2)
EN sinking current ..... 1 mA(5)
Continuous power dissipation (T_A = +25°C) (6) ..... 2.5 W
Junction temperature .....150°C
Lead temperature .....260°C
Storage temperature ..... -65°C to +150°C

Recommended Operating Conditions (7)

Supply voltage (V_{IN}) .....14 V to 80 V
Switching voltage (V_{SW}) .....-0.5 V to +150 V
Maximum VCC sinking current ..... 1.2 mA(4)
Maximum FB1 sinking current ..... ±0.5 mA(2)
Maximum EN sinking current ..... 0.5 mA(5)
Maximum switching frequency..... 200 kHz
Maximum current limit..... 3 A
Switching junction temp. (T_J). .. -40°C to +125°C

Thermal Resistance (8)

	θ_{JA}	θ_{JC}	
QFN-14 (3mm x 3mm).....	50.....	12	°C/W

NOTES:

1) Exceeding these ratings may damage the device.
2) Refer to the “Output Voltage Setting” section on page 18.
3) VCC and EN voltage can be pulled higher than this rating, but the external pull-up current should be limited. Refer to “VCC sinking current” and “EN sinking current” ratings to the left.
4) Refer to the “V_{CC} Power Supply Setting” section on page 17..
5) Refer to the “EN Control Setting” section on page 17.
6) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
7) The device is not guaranteed to function outside of its operating conditions.
8) Measured on JESD51-7, 4-layer PCB.

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ELECTRICAL CHARACTERISTICS

V_{IN} = 48 V, V_{EN} = 5 V, V_{OUT} = 12 V, T_J = -40°C to 125°C, typical value is tested at 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Power supply and UVLO						
VIN UVLO rising threshold	V_{IN-R}	V_{IN} rising	10.5	11.6	12.8	V
VIN UVLO falling threshold	V_{IN-F}	V_{IN} falling	7.4	8.2	9	V
VCC regulation(9)	V_{CC}	Load = 0 mA to 10 mA	4.8	5.4	5.9	V
VCC UVLO rising threshold(9)	V_{CC-R}	V_{IN} is higher than UVLO, Vcc rising	4.3	4.7	5.1	V
VCC UVLO falling threshold(9)	V_{CC-F}	V_{IN} is higher than UVLO, Vcc falling	4	4.5	4.8	V
Quiescent current	I_Q	V_{FB1} = 2.2 V, V_{FB2} = V_{IN}		380		µA
EN high-level voltage			3.9			V
EN low-level voltage					1.3	V
EN input current				5.5	7.5	µA
Voltage feedback						
FB1 reference voltage	V_{REF1}	Respect to GND, T_J = 25°C	1.94	1.99	2.04	V
		Respect to GND, T_J = -40°C to +125°C	1.93	1.99	2.05	V
FB1 leakage current	I_{FB1}	Respect to GND, V_{FB1} = 2 V		10	50	nA
Flyback mode DCM detect threshold on FB1	V_{DCM1}	Respect to GND	25	50	75	mV
FB1 open-circuit threshold	$V_{FB1OPEN}$		-90	-60	-20	mV
FB1 OVP threshold	V_{FB1OVP}		120%	125%	130%	V_{REF1}
Minimum diode conduction time for FB1 sample	T_{SAMPLE}		1.4	2.2	3	µs
FB2 reference voltage	V_{REF2}	Respect to V_{IN}, T_J = 25°C	-1.955	-1.88	-1.805	V
		Respect to V_{IN}, T_J = -40°C to +125°C	-1.96	-1.88	-1.8	V
FB2 leakage current	I_{FB2}	Respect to V_{IN}, V_{FB2} = -2 V		10	50	nA
Buck mode DCM detect threshold on SW	V_{DCM2}	Respect to V_{IN}	0		0.14	V
Switching power device						
On resistance	R_{ON-SW}	V_{CC} = 5.4 V		0.8		Ω
Current sense						
Current limit	I_{LIMIT}	R_{ILIM} = 53.6 kΩ, L = 47 µH	1.85	2.05	2.25	A
Current leading-edge Blanking time	T_{LEB}			450		ns

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ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 48 V, V_{EN} = 5 V, V_{OUT} = 12 V, T_J = -40°C to 125°C, typical value is tested at 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
DCDC converter thermal shutdown						
Thermal shutdown temperature(10)	T_{SD}			150		ºC
Thermal shutdown hysteresis(10)	T_{HYS}			20		ºC

NOTES:

9) The maximum VCC UVLO rising threshold is higher than the minimum VCC regulation in the EC table due to production distribution. However, for one unit, VCC regulation is higher than the VCC UVLO rising threshold. The VCC UVLO rising threshold is about 87 percent of the VCC regulation voltage, and the VCC UVLO falling threshold is about 83 percent of the VCC regulation voltage in one unit.

10) Guaranteed by characterization, not tested in production.

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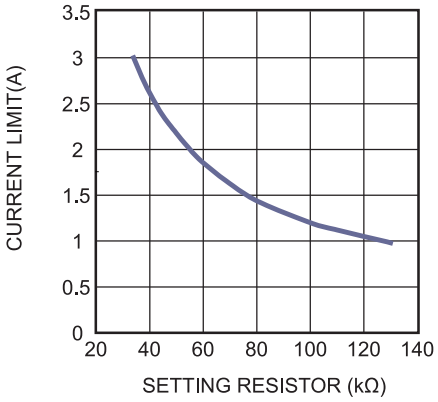
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 48 V, V_{OUT} = 12 V, I_{OUT} = 1 A, T_A = 25°C, unless otherwise noted.

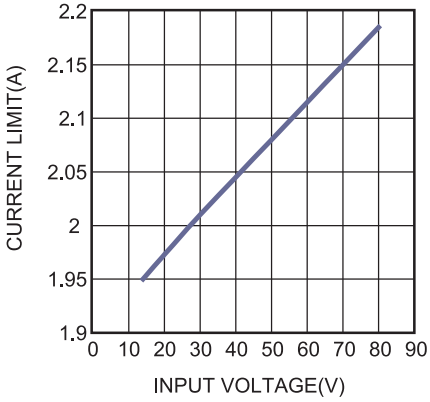
Current Limit vs. Setting Resistor

L =47µH



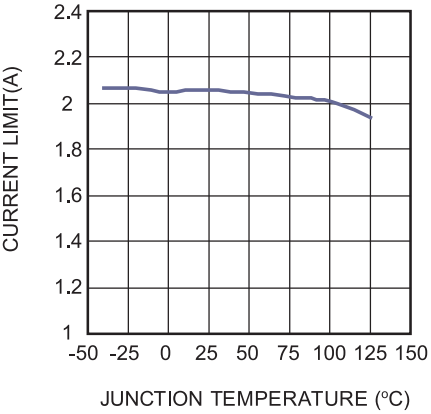
Current Limit vs. Input Voltage

R_{LIMIT} =53.6kΩ, L =47µH

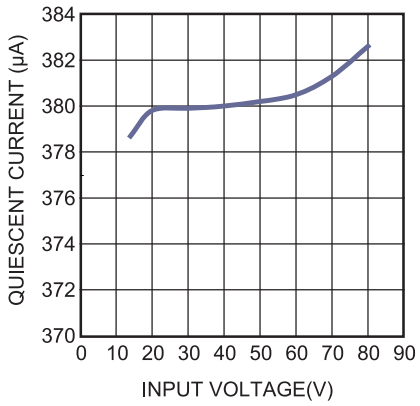


Current Limit vs. Junction Temperature

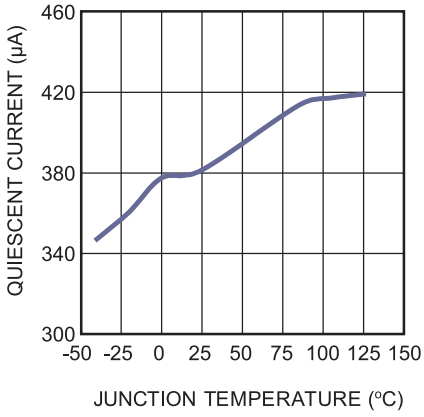
R_{LIMIT} =53.6kΩ, L =47µH



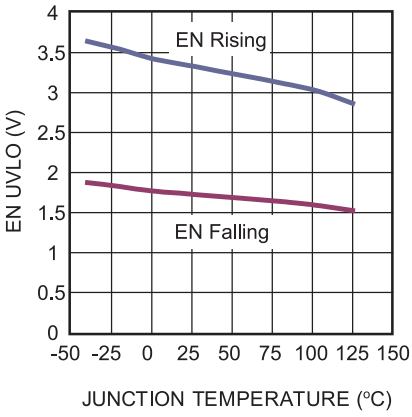
Quiescent Current vs. Input Voltage



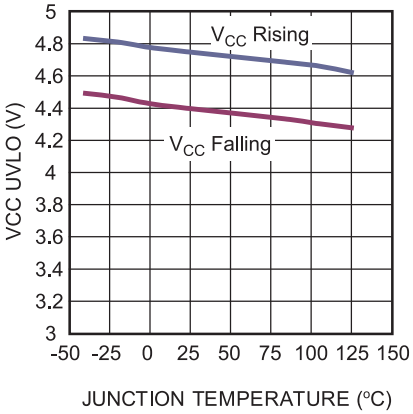
Quiescent Current vs. Junction Temperature



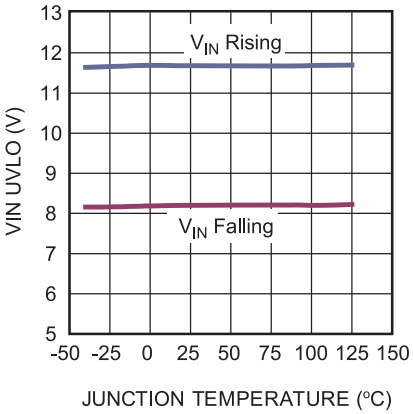
EN UVLO vs. Junction Temperature



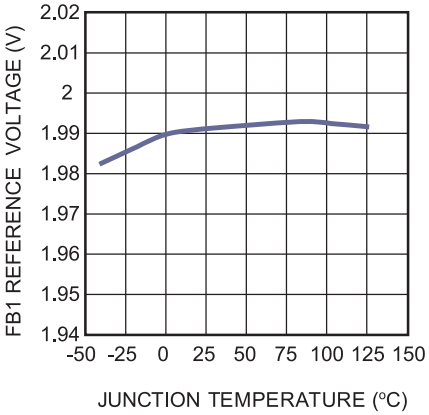
V_{CC} UVLO vs. Junction Temperature



V_{IN} UVLO vs. Junction Temperature



FB1 Reference Voltage vs. Junction Temperature



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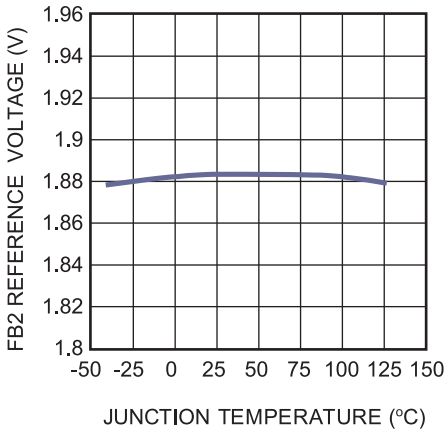
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 48 V, V_{OUT} = 12 V, I_{OUT} = 1 A, T_A = 25°C, unless otherwise noted.

FB2 Reference Voltage vs. Junction Temperature



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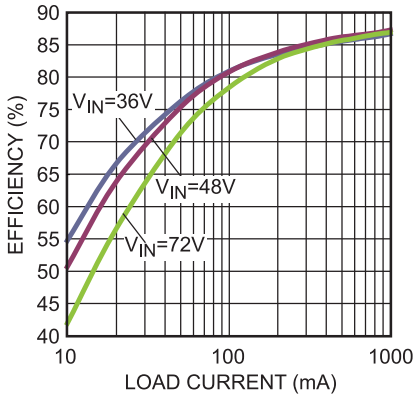
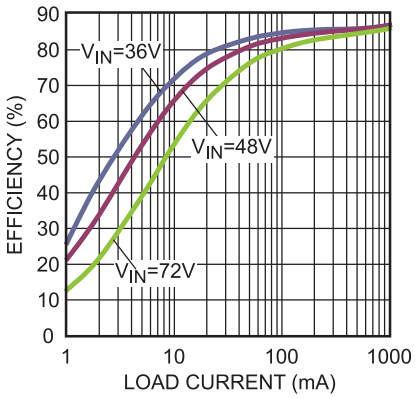
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 48 V, V_{OUT} = 12 V, I_{OUT} = 1 A, Flyback mode, T_A = 25°C, unless otherwise noted.

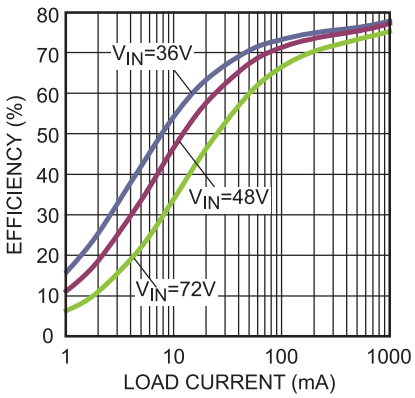
Efficiency
Flyback, V_{OUT} =12V



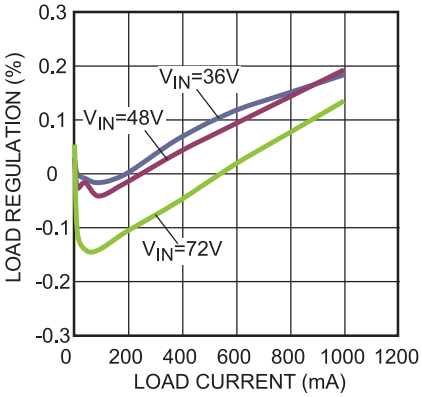
Efficiency
Buck, V_{OUT} =12V



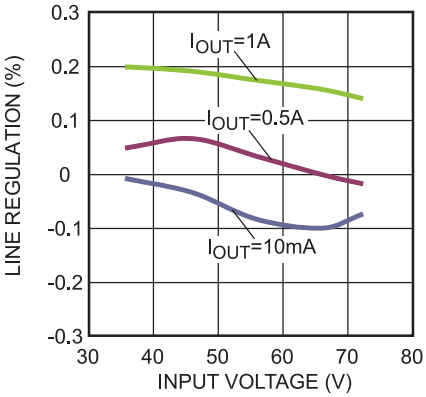
Efficiency
Buck, V_{OUT} =5V



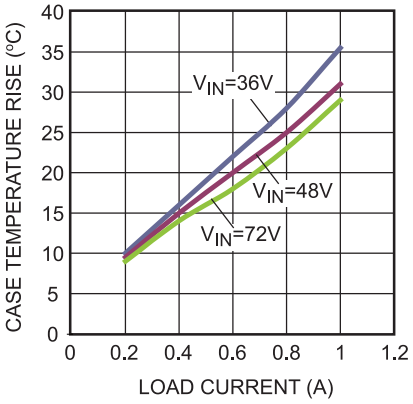
Load Regulation
Flyback, V_{OUT} =12V



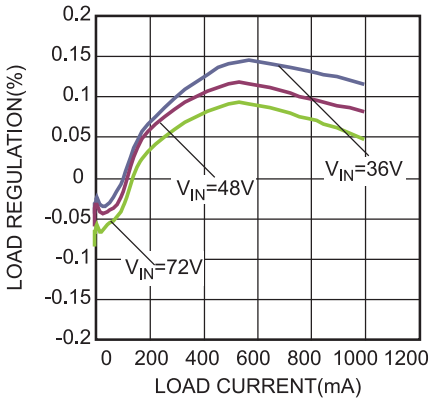
Line Regulation
Flyback, V_{OUT} =12V



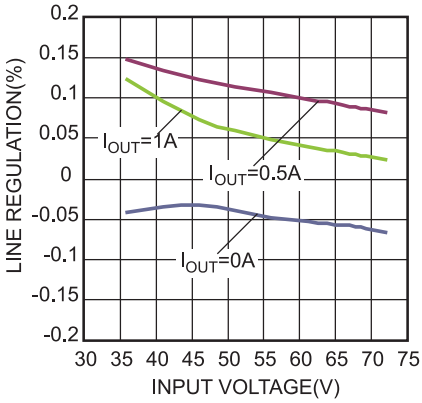
Case Temperature Rise
Flyback, V_{OUT} =12V



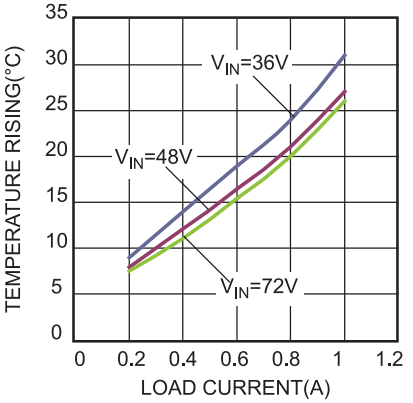
Load Regulation
Buck, V_{OUT}=12V



Line Regulation
Buck, V_{OUT}=12V



Case Temperature Rising
Buck, V_{OUT}=12V



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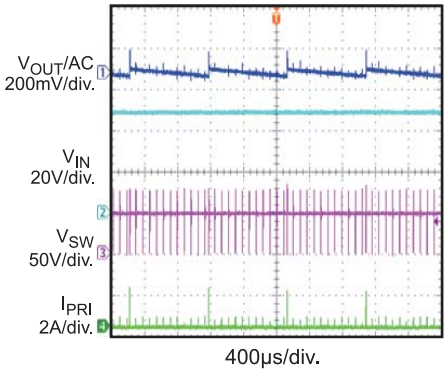
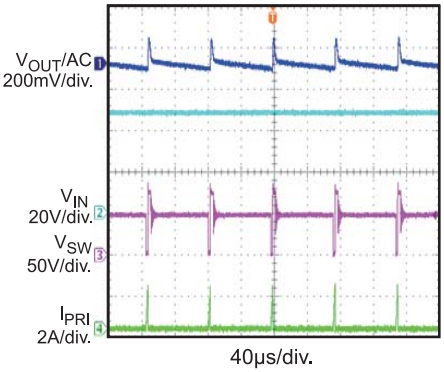
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 48 V, V_{OUT} = 12 V, I_{OUT} = 1 A, Flyback mode, T_A = 25°C, unless otherwise noted.

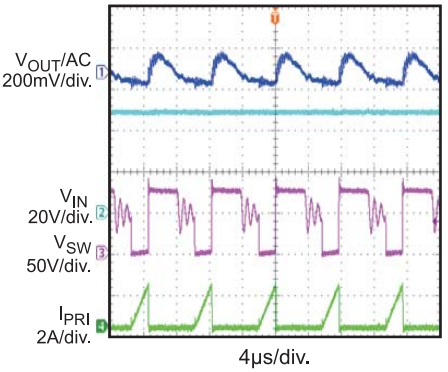
Steady State
I_{OUT} = 10mA



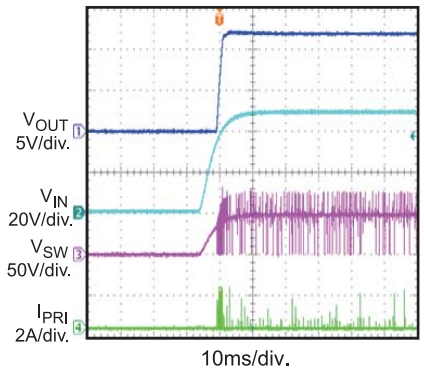
Steady State
I_{OUT} = 100mA



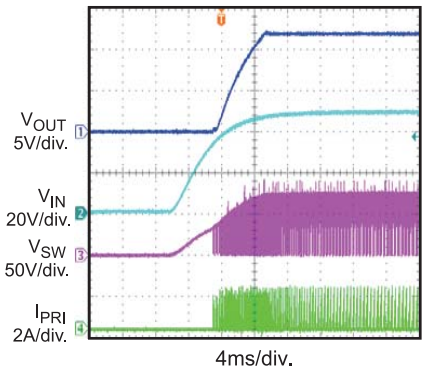
Steady State
I_{OUT} = 1A



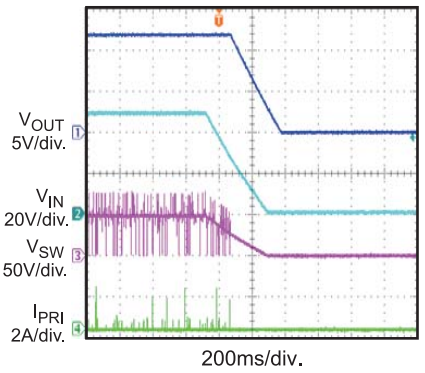
V_{IN} Start-Up
I_{OUT} = 10mA



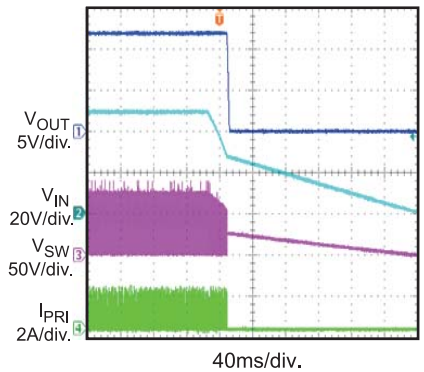
V_{IN} Start-Up
I_{OUT} = 1A



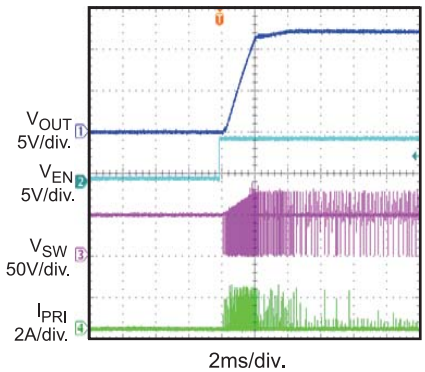
V_{IN} Shutdown
I_{OUT} = 10mA



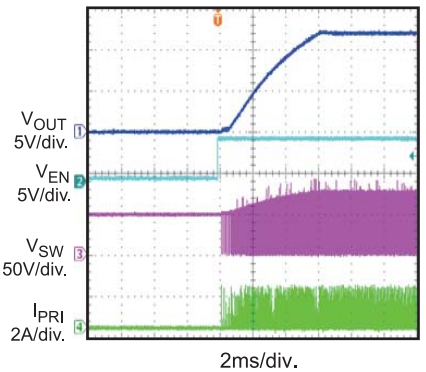
V_{IN} Shutdown
I_{OUT} = 1A



EN Start-Up
I_{OUT} = 10mA



EN Start-Up
I_{OUT} = 1A



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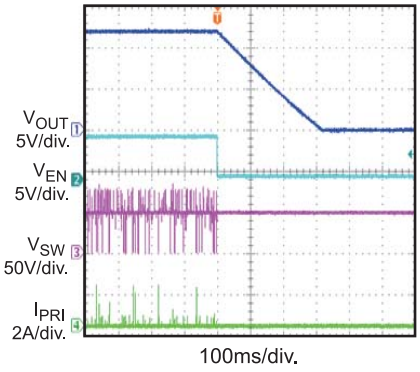
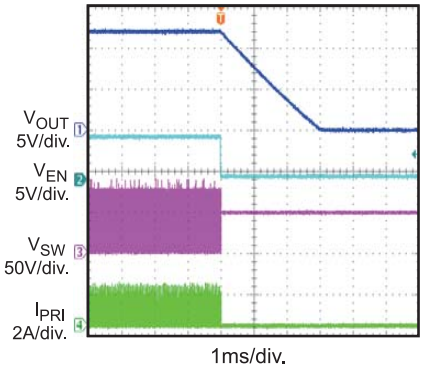
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 48 V, V_{OUT} = 12 V, I_{OUT} = 1 A, Flyback mode, T_A = 25°C, unless otherwise noted.

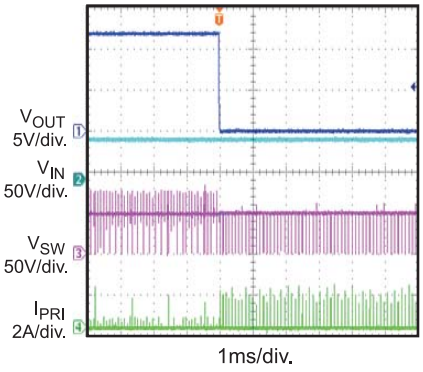
EN Shutdown
I_{OUT} = 10mA



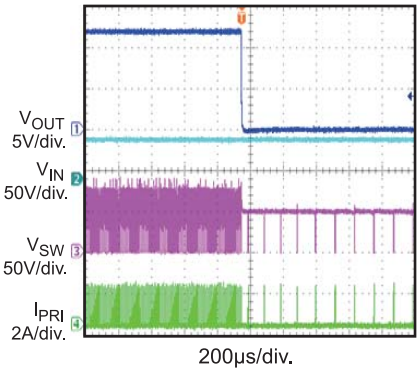
EN Shutdown
I_{OUT} = 1A



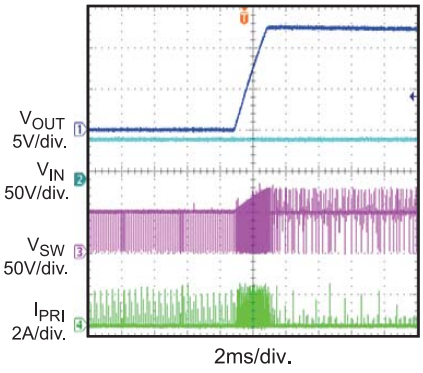
SCP Entry
I_{OUT} = 10mA



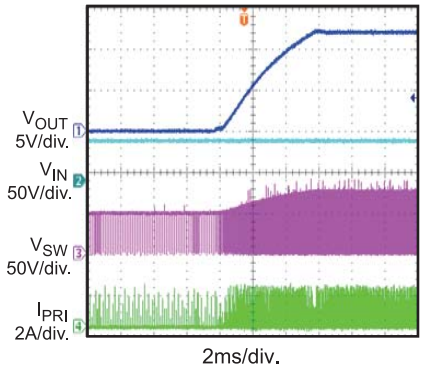
SCP Entry
I_{OUT} = 1A



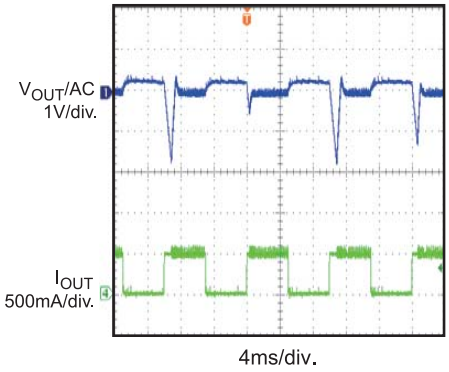
SCP Recovery
I_{OUT} = 10mA



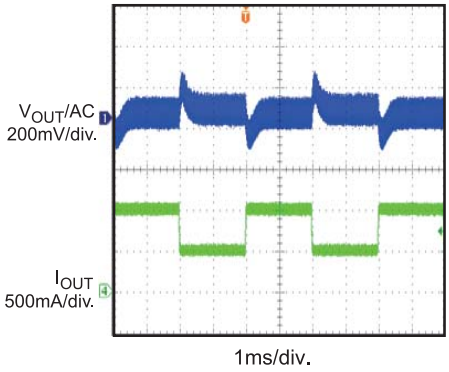
SCP Recovery
I_{OUT} = 1A



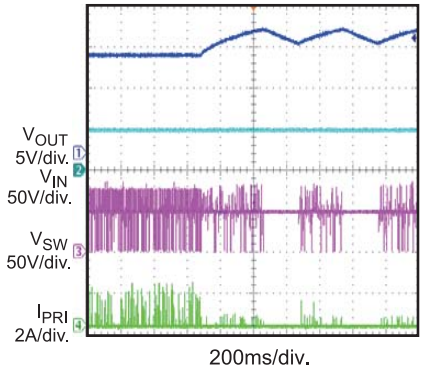
Load Transient
I_{OUT} =10mA to 0.5A,
I_{RAMP}=25mA/µs



Load Transient
I_{OUT} =0.5A to 1A,
I_{RAMP}=25mA/µs



OVP
I_{OUT} = 100mA to 2mA



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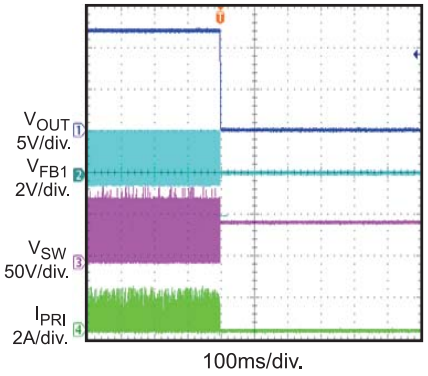
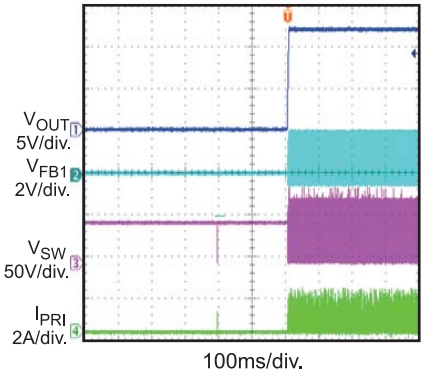
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 48 V, V_{OUT} = 12 V, I_{OUT} = 1 A, Flyback mode, T_A = 25°C, unless otherwise noted.

FB1 Open-Circuit Entry
I_{OUT} = 1A



FB1 Open-Circuit Recovery
I_{OUT} = 1A



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PIN FUNCTIONS

PIN#	Name	Description
1, 2	GND	**Switching converter power return**.
3	EN	**Regulator on/off control input.** EN can program VIN UVLO start-up through a Zener diode and a resistor divider.
4,12	NC	**No connection.** NC is not connected internally. Float NC or connect to GND in layout.
5	VIN	**Positive power supply terminal.**
6	FB2	**Feedback for non-isolated buck solution.** Connect FB2 to VIN in flyback application.
7	MODE	**Buck mode or flyback mode select pin.** MODE is pulled up internally to VCC through a 1.5 μA current source. Float MODE for buck application mode; connect MODE to GND for flyback application mode.
8	FB1	**Feedback for flyback solution.** Connect FB1 to GND in buck application.
9	ILIM	**IC switching current limit program pin.** Connect ILIM to GND through a resistor to program the peak current limit.
10	AGND	**Analog power return for switching converter control circuit.**
11	VCC	**Supply bias voltage pin, powered through internal LDO from VIN**. It is recommended to connect a capacitor (no less than 1 μF) between VCC and GND.
13,14	SW	**Drain of converter switching MOSFET.**

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FUNCTION DIAGRAM

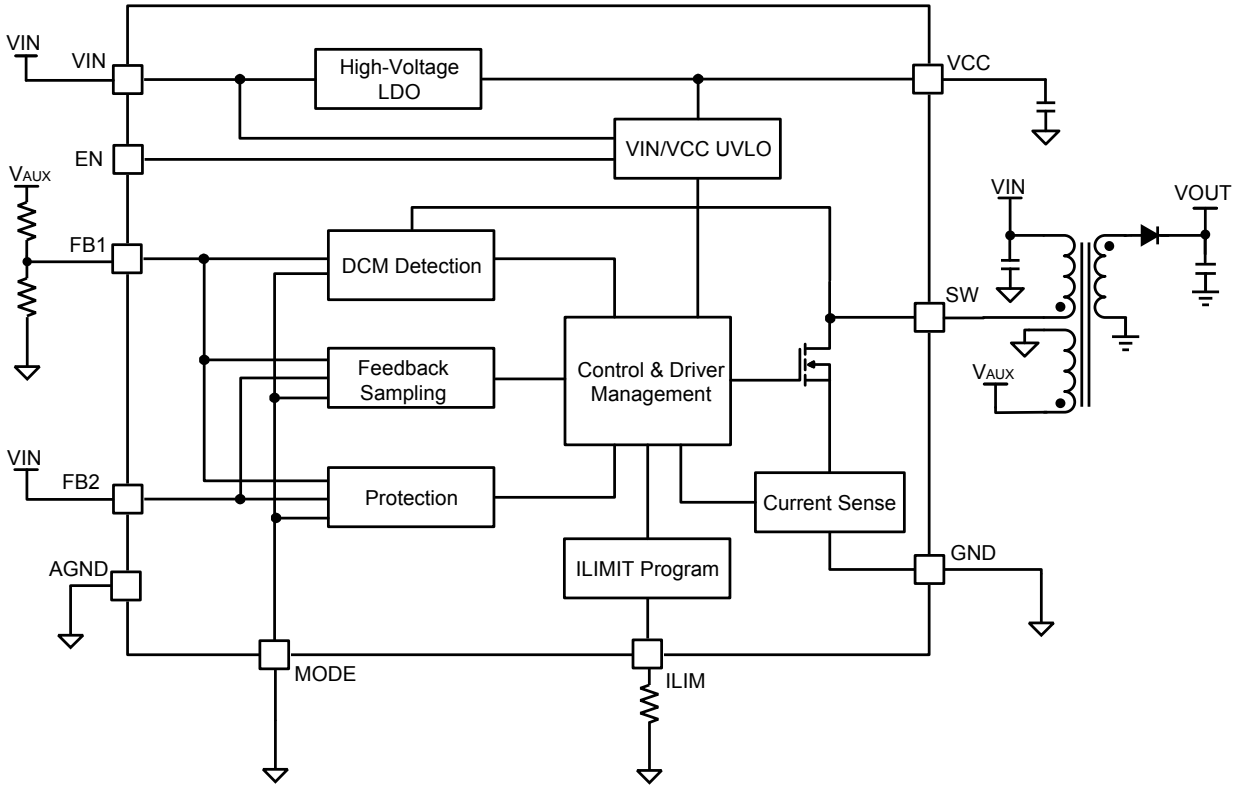

Figure 1—Functional block diagram

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OPERATION

Start-Up and Power Supply

MP6004 features an 80 V start-up circuit. When V_{IN} is higher than 4.3 V, the capacitor at VCC is charged through the internal LDO. Normally V_{CC} is regulated at 5.4 V (if VIN is high enough), and the V_{CC} UVLO is 4.7 V, typically. With the exception of V_{CC} UVLO, the MP6004 has an additional 11.6 V V_{IN} UVLO. When V_{IN} is higher than the 11.6 V UVLO, V_{CC} is charged higher than the 4.7 V UVLO, and EN pin is high, MP6004 starts switching.

V_{CC} can be powered from the transformer auxiliary winding to save IC power loss. Refer to the "Vcc Power Supply Setting" section on page 18 for more details.

Flyback and Buck Mode

MP6004 supports both flyback and buck topology applications. Connect MODE to GND to set the MP6004 in flyback mode, and float MODE to set the MP6004 in buck mode. MODE is pulled up internally to V_{CC} through a 1.5 μA current source. Do not connect MODE to V_{IN} in buck mode, and do not place a resistor between MODE and GND in flyback mode.

Switching Work Principle

After start-up, MP6004 works in discontinuous conduction mode (DCM). The second switching cycle will not start until the inductor current drops to 0 A. In each cycle, the internal MOSFET is turned on, and the current-sense circuit senses the current $I_{P(t)}$ internally.

Use Equation (1) to calculate the rate at which the current rises linearly in flyback mode:

$$\frac{dI_{p(t)}}{dt} = \frac{V_{IN}}{L_M} \quad (1)$$

When $I_{P(t)}$ rises up to I_{PK}, the internal MOSFET turns off (see Figure 2). The energy stored in the primary-side inductance transfers to the secondary-side through the transformer.

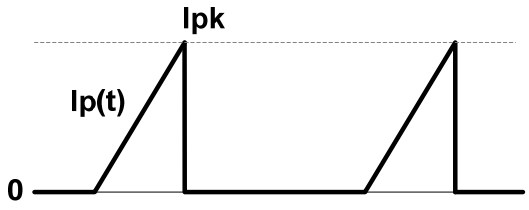

Figure 2—Primary-side current waveform

The primary-side inductance (L_M) stores energy in each cycle as a function of Equation (2):

$$E = \frac{1}{2} L_M I_{PK}^2 \quad (2)$$

Calculate the power transferred from the input to the output with Equation (3):

$$P = \frac{1}{2} L_M I_{PK}^2 F_S \quad (3)$$

Where F_S is the switching frequency. When I_{PK} is constant, the output power depends on F_S and L_M.

Use Equation (4) to calculate the rate at which the current rises linearly in buck mode:

$$\frac{dI_{p(t)}}{dt} = \frac{V_{IN} - V_{OUT}}{L_M} \quad (4)$$

The internal MOSFET turns off when $I_{P(t)}$ rises to I_{PK} (see Figure 3). The output current is calculated with Equation (5):

$$I_{OUT} = \frac{1}{2} D I_{PK} \quad (5)$$

Where, D is the inductor current conducting duty cycle.

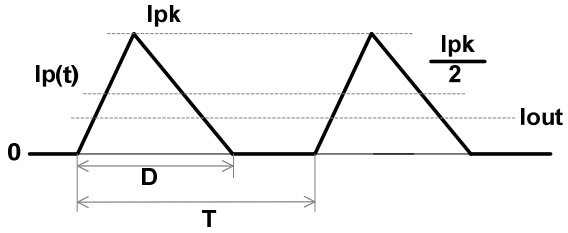

Figure 3—Inductor current waveform

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Light-Load Control

In flyback mode (if the load decreases), MP6004 stretches down the frequency automatically to reduce the power transferring while keeping the same I_{PK} in each cycle. An approximate 10 kHz minimum frequency is applied to detect the output voltage even at a very light load. During this condition, the switching I_{PK} jumps between 20 percent of the normal I_{PK} and 100 percent of the normal I_{PK} to reduce the power transferring. The MP6004 still transfers some energy to the output even if there is no load on the output due to the 10 kHz minimum frequency. This means that some load is required to maintain the output voltage, or else V_{OUT} will rise and trigger an OVP.

In buck mode, the MP6004 has no minimum frequency limit, so it stretches down to a very low frequency and regulates the output automatically even there is no load on the output.

Frequency Control

By monitoring the auxiliary winding voltage in flyback mode or monitoring the SW voltage in buck mode, the MP6004 detects and regulates the inductor current in DCM. The frequency is controlled by the peak current, the current ramp slew rate, and the load current. The maximum frequency occurs when the MP6004 runs in critical conduction mode, providing the maximum load power. The MP6004 switching frequency should be lower than 200 kHz in the design.

Voltage Control

In flyback application, the MP6004 detects the auxiliary winding voltage from FB1 during the secondary-side diode conduction period.

Assume the secondary winding is the master, and the auxiliary winding is the slave. When the secondary-side diode conducts, the FB1 voltage is calculated with Equation (6):

$$V_{FB1} = \frac{N_A}{N_S} \times (V_{OUT} + V_{D1F}) \times \frac{R_2}{R_1 + R_2} \quad (6)$$

Where:

V_{D1F} is the output diode forward-drop voltage.

V_{OUT} is the output voltage.

N_A and N_S are the turns of the auxiliary winding and the secondary-side winding, respectively.

R1 and R2 are the resistor dividers for sampling.

The output voltage differs from the secondary-winding voltage due to the current-dependant diode forward voltage drop. If the secondary-winding voltage is always detected at a fixed secondary current, the difference between the output voltage and the secondary-winding voltage is a fixed V_{D1F}. MP6004 starts sampling the auxiliary-winding voltage after the internal power MOSFET turns off for 0.7 µs and finishes the sampling after the secondary-side diode conducts for 3 µs. This provides good regulation when the load changes. However, the secondary diode conducting period must be longer than 3 µs in each cycle, and the FB1 signal must be smooth 0.7 µs after the switch turns off.

With a buck solution, there is one FB2 pin referenced to VIN. It can be used as the reference voltage for the buck application. The output voltage is referenced to VIN and does not have the same GND as the input power.

Programming the Current Limit

The MP6004 current limit is set by an external resistor (R3) from ILIM to ground. The value of R3 can be estimated with Equation (7):

$$I_{LIM} = \frac{100}{R3} + \frac{V_L \times 0.18}{L} \quad (7)$$

Where I_{LIM} is the current limit in A, V_L is the voltage applied on the inductor when the MOSFET turns on, R3 is the setting resistor in kΩ, and L is the inductor in µH.

The current limit cannot be programmed higher than 3 A.

Leading-Edge Blanking

Transformer parasitic capacitance induces a current spike on the sense resistor when the power switch turns on. The MP6004 includes a 450 ns leading-edge blanking period to avoid falsely terminating the switching pulse. During this blanking period, the current sense comparator is disabled, and the gate driver cannot switch off.

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DCM Detection

The MP6004 regulator operates in discontinuous conduction mode in both flyback and buck modes.

In flyback mode, the MP6004 detects the falling edge of the FB1 voltage in each cycle. The second cycle switching will not start unless the chip detects a 50 mV falling edge on FB1.

In buck mode, the MP6004 detects the falling edge of the SW voltage in each cycle. The second cycle switching will not start unless the chip detects 0.14 V falling edge between V_{SW}-V_{IN}.

Over-Voltage & Open-Circuit Protection

In flyback mode, the MP6004 includes over-voltage protection (OVP) and open-circuit protection. If the voltage at FB1 exceeds 125 percent of V_{REF1} (or FB1's -60 mV falling edge cannot be detected because the feedback resistor is removed), immediately the MP6004 shuts off the driving signal and enters hiccup mode by re-charging the internal capacitor. The MP6004 resumes normal operation when the fault is removed.

In buck mode, if the voltage at FB2 is higher than the reference voltage, the MP6004 stops switching immediately.

Over-Load Protection

MP6004 will always work in DCM mode for any condition.

In flyback mode, the secondary-side diode conduction duty cycle is limited to about 80 percent. In an over-load condition, the output energy is limited by I_{PK} and F_S. With a heavier load, the output drops and the diode conduction period becomes longer. This causes the switching frequency to drop so that the output energy can be limited. The MP6004 has same protection logic for an over-load/output-short condition.

In buck mode, the duty cycle limitation does not apply, but the output current is limited to half of I_{PK}.

Thermal Shutdown

When the junction temperature exceeds 150°C, the MP6004 shuts down. Once the temperature drops below 130°C, the part re-starts automatically.

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APPLICATION INFORMATION

EN Control Setting

MP6004 turns on when EN goes high, and it turns off when EN goes low. EN is pulled low internally by an approximate 0.9 MΩ resistor.

In flyback mode, the maximum on time is limited at about 8 μs. The secondary-side rectifier diode conduction time should be longer than 3 μs for FB1 feedback sampling. If V_{IN} decreases and the inductor current cannot ramp the I_{PK} to setting value within the maximum on time, the diode conduction time decreases to less than 3 μs, causing FB1 feedback sample failure. The MP6004 treats this failure as a V_{OUT} drop and generates more pulses, causing V_{OUT} to overshoot. In this condition, EN can be used to program V_{IN} UVLO and shuts down the part before V_{IN} drops (triggering the maximum on time). Since the EN high-level voltage is 3.9 V and the low-level voltage is 1.3 V, it is hard to program the V_{IN} UVLO with a small hysteresis. In this condition, one resistor divider and one Zener diode is recommended (see Figure 4).

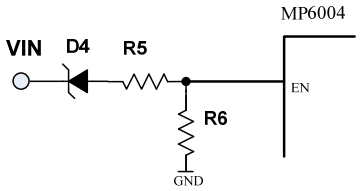

Figure 4—VIN UVLO setting with EN control

For example, the MP6004 should be turned on before V_{IN} rises to 36 V and shut down before V_{IN} drops to 20 V. One 20 V Zener diode (D4) and a resistor divider (R5 = 100 kΩ/R6 = 49.9 kΩ) can be selected to program the V_{IN} UVLO. The programmed V_{IN} rising threshold can be calculated with Equation (8):

$$V_{IN_R} < 20V + \frac{100k\Omega + 49.9k\Omega}{49.9k\Omega} \times 3.9V = 31.7V \quad (8)$$

The programmed V_{IN} falling threshold is calculated with Equation (9):

$$V_{IN_F} > 20V + \frac{100k\Omega + 49.9k\Omega}{49.9k\Omega} \times 1.3V = 23.9V \quad (9)$$

In buck mode, FB2 feedback is not affected by the rectifier diode conduction time, but the Zener diode and resistor divider are recommended to set the appropriate V_{IN} UVLO.

There is an internal Zener diode on EN, which clamps the EN voltage to prevent runaway. The maximum pull-up current for the internal Zener clamp (assuming 6.5 V) should be less than 0.5 mA. If EN is driven with an external signal, use a signal voltage less than 6.5 V or connect EN to the signal through a pull-up resistor that ensures the maximum pull-up current is less than 0.5 mA. If using a resistor divider (see Figure 4) and V_{IN}-V_{ZENER} is higher than 6.5 V, the minimum resistance for the pull-up resistor R5 should be calculated with Equation (10):

$$\frac{V_{IN} - V_{ZENER} - 6.5V}{R5} - \frac{6.5V}{R6} < 0.5mA \quad (10)$$

V_{CC} Power Supply Setting

The V_{CC} voltage is charged through the internal LDO by VIN. Normally, V_{CC} is regulated at 5.4 V, typically. A capacitor no less than 1 μF is recommended for decoupling between V_{CC} and GND.

In flyback mode, V_{CC} can be powered from the transformer auxiliary winding to save the high-voltage LDO power loss.

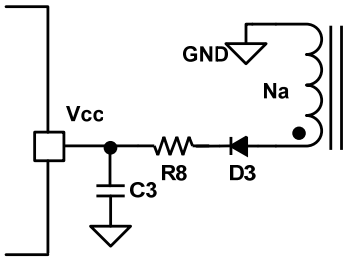

Figure 5—Supply V_{CC} from auxiliary winding

The auxiliary winding supply voltage can be calculated with Equation (11):

$$V_{CC} = \frac{N_A}{N_S} \times (V_{OUT} + V_{D1F}) - V_{D3F} \quad (11)$$

Where N_A and N_S are the turns of the auxiliary winding and the output winding, V_{D1F} is the output rectifier diode voltage drop, and V_{D3F} is the D3 voltage drop in Figure 5.

V_{CC} voltage is clamped at about 6.2 V by one internal Zener diode. The clamp current

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capability is about 1.2 mA. If the auxiliary winding power voltage is higher than 6.2 V (especially in a heavy-load condition), a series resistor (R8) is necessary to limit the current to VCC. For simple application, supply the V_{CC} power through the internal LDO directly.

Output Voltage Setting

In MP6004, there are two feedback pins for different application modes.

In flyback mode, the converter detects the auxiliary winding voltage from FB1. R1 and R2 are the resistor dividers for the feedback sampling (see Figure 6).

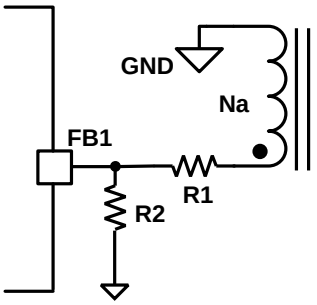

Figure 6—Feedback in isolation application

When the primary-side power MOSFET turns off, the auxiliary-winding voltage is sampled. The output voltage is estimated with Equation (12):

$$V_{OUT} = \frac{V_{REF1} \times (R_1 + R_2)}{R_2} \times \frac{N_S}{N_A} - V_{D1F} \quad (12)$$

Where,
N_S is the transformer secondary-side winding turns.
N_A is the transformer auxiliary winding turns.
V_{D1F} is the rectifier diode forward drop.
V_{REF1} is the reference voltage of FB1 (1.99 V, typically).

When the primary-side power MOSFET turns on, the auxiliary winding forces a negative voltage to FB1. The FB1 voltage is clamped to less than -0.7 V internally, but the clamp current should be limited to less than -0.5 mA by R1. For example, if the auxiliary winding forces -11 V to R1 (to make the current flowing from FB1 to R1 lower than -0.5 mA), R1 resistance must be higher than 22 kΩ (if ignoring R2 current).

Generally, select R2 with a 10 kΩ to 50 kΩ resistor to limit noise and provide an appropriate R1 for the -0.5 mA negative current limit.

In buck application, the feedback pin is FB2. The output voltage can be estimated with Equation (13):

$$V_{OUT} = -\frac{R_1 + R_2}{R_2} \times V_{REF2} \quad (13)$$

Where, V_{REF2} is the reference voltage of FB2 -1.88 V, typically.

Maximum Switching Frequency

When MP6004 works in DCM, the frequency reaches its maximum value during a full-load condition. The maximum frequency is affected by the peak current limit, the inductance, and the input/output voltage. Generally, design the maximum frequency lower than 200 kHz.

In buck mode, the maximum frequency occurs when the buck runs in critical conduction mode. The frequency can be calculated with Equation (14):

$$F_{SW_MAX} = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{I_{LIM} \times L \times V_{IN}} \quad (14)$$

Where, I_{LIM} is the I_{PK} set by the current limit resistor.

With a lighter load, the frequency is lower than the maximum frequency above.

In flyback mode, design the maximum frequency with the minimum input voltage and the maximum load condition. Calculate the frequency with Equation (15):

$$F_{SW} \le \frac{1}{T_{ON} + T_{CON} + T_{DELAY}} \quad (15)$$

Where:

T_{ON} is the MOSFET one pulse turn-on time determined with Equation (16):

$$T_{ON} = \frac{I_{LIM} \times L_M}{V_{IN}} \quad (16)$$

L_M is the transformer primary-winding inductance.

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T_{CON} is the rectifier diode current conducting time and can be calculated with Equation (17):

$$T_{CON} = \frac{N_S \times I_{LIM} \times L_M}{N_P \times (V_{OUT} + V_{D1F})} \quad (17)$$

Where, N_S is the transformer secondary-side winding turns.N_P is the transformer primary-side winding turns.
T_{DELAY} is the resonant delay time from the rectifier diode current drop to 0 A to the auxiliary-winding voltage drop to 0 V. The resonant time can be tested on the board (estimate around 0.5 μs).

In flyback mode, the MP6004 samples the feedback signal within 3 μs after the primary-side MOSFET turns off. The secondary-side diode conduction time in Equation (17) should be higher than 3 μs. This time period, combined with the duty cycle, determines the maximum frequency.

Input Capacitor Selection

An input capacitor is required to supply the AC ripple current to the inductor while limiting noise at the input source. A low ESR capacitor is required to keep the noise to the IC at a minimum. Ceramic capacitors are preferred, but tantalum or low ESR electrolytic capacitors will suffice. For ceramic capacitors, the capacitance dominates the impedance at the switching frequency. The ripple will be the worst at light load. The required input capacitance can be estimated with Equation (18):

$$C_1 = \frac{0.5 \times I_{LIM} \times T_{ON}}{V_{INP_P}} \quad (18)$$

Where C_1 is the input capacitor value, V_{INP-P} is the expected input ripple, and T_{ON} is the MOSFET turn-on time.
In an isolated application, T_{ON} is calculated with Equation (19):

$$T_{ON} = \frac{I_{LIM} \times L_M}{V_{IN}} \quad (19)$$

In a non-isolation application, T_{ON} is calculated with Equation (20):

$$T_{ON} = \frac{I_{LIM} \times L}{V_{IN} - V_{OUT}} \quad (20)$$

Where L is the buck`s inductor value.

Output Capacitor Selection

The output capacitor maintains the DC output voltage. For best results, use ceramic capacitors or low ESR capacitors to minimize the output voltage ripple. For ceramic capacitors, the capacitance dominates the impedance at the switching frequency.

In flyback application, the worst output ripple occurs under a light-load condition; the worst output ripple can be estimated by Equation (21):

$$V_{OUTP_P} = \frac{0.5 \times N_P \times I_{LIM} \times T_{CON}}{N_S \times C2} \quad (21)$$

Where,
C2 is the output capacitor value.
V_{OUTP-P} is the output ripple.

Normally, a 44 μF or higher ceramic capacitor is recommended as the output capacitor. This allows a small Vo ripple and stable operation.

In buck application, the worst Vout ripple can be estimated with Equation (22):

$$V_{OUTP_P} = \frac{0.5 \times I_{LIM}^2 \times L \times (V_{IN} + V_{D1F})}{C2 \times (V_{IN} - V_{OUT}) \times (V_{OUT} + V_{D1F})} \quad (22)$$

Leakage Inductance

The transformer's leakage inductance decreases system efficiency and affects the output current and voltage precision. Optimize the transformer structure to minimize the leakage inductance. Aim for a leakage inductance less than 3 percent of the primary-winding inductance.

RCD Snubber for Flyback

The transformer leakage inductance causes spikes and excessive ringing on the MOSFET drain voltage waveform, affecting the output voltage sampling 0.7 μs after the MOSFET turns off. The RCD snubber circuit limits the SW voltage spike (see Figure 7).

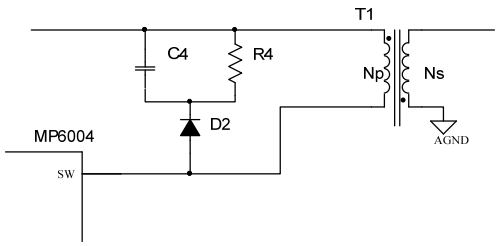

Figure 7—RCD snubber

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The power dissipation in the snubber circuit is estimated with Equation (23):

$$P_{SN} = \frac{1}{2} \times L_K \times I_{LIM}^2 \times F_S \quad (23)$$

Where, L_K is the leakage inductance.

Since R4 consumes the majority of the power, R4 is estimated with Equation (24):

$$R4 = \frac{V_{SN}^2}{P_{SN}} \quad (24)$$

Where, V_{SN} is the expected snubber voltage on C4.

The snubber capacitor C4 can be designed to get appropriate voltage ripple on the snubber using Equation (25):

$$\Delta V_{SN} = \frac{V_{SN}}{R4 \times C4 \times F_S} \quad (25)$$

Generally, a 15 percent ripple is acceptable.

Buck Inductor Selection

The inductor is required to transfer the energy between the input source and the output capacitors. Unlike normal application where inductors determine the inductor ripple, the MP6004 always works in DCM while V_{IN}, V_{OUT}, and I_{LIM} are constant. The inductor only determines the speed of the current rising and falling, which determines the switching period. The expected maximum frequency can determine the inductor value using Equation (26):

$$L \approx \frac{(V_{IN} - V_{OUT}) \times (V_{OUT} + V_{D1F})}{(V_{IN} + V_{D1F}) \times I_{PEAK}} \times \frac{1}{F_{SW}} \quad (26)$$

F_{SW} is the expected maximum switching frequency, which should be lower than 200 kHz in general setting.

Output Diode Selection

The output rectifier diode supplies current to the output capacitor when the internal MOSFET is off. Use a Schottky diode to reduce loss due to the diode forward voltage and recovery time.

In isolation application, the diode should be rated for a reverse voltage greater than Equation (27):

$$V_{D1} = V_{OUT} + \frac{V_{IN} \times N_S}{N_P} + V_{PD1} \quad (27)$$

V_{PD1} can be selected at 40 percent ~100 percent of V_{OUT} + V_{IN} x N_S/N_P. An RC or RCD snubber circuit for the output diode D1 is recommended.

In buck mode, the diode reverse voltage equates to the input voltage. A 20 percent ~ 40 percent margin is recommended.

In both applications, the current rating should be higher than the maximum output current.

Dummy Load

When the system operates without a load in flyback mode, the output voltage rises above the normal operation voltage because of the minimum switching frequency limitation. Use a dummy load for good load regulation. A large dummy load decreases efficiency, so the dummy load is a tradeoff between efficiency and load regulation. For applications using Figure 10, a minimum load of around 10 mA is recommended.

PCB Layout Guidelines

Efficient PCB layout for high-frequency switching power supplies is critical. Poor layout may result in reduced performance, excessive EMI, resistive loss, and system instability. For best results, refer to Figure 8 and Figure 9 and follow the guidelines below:

For flyback application:

1. Keep the input loop as short as possible between the input capacitor, transformer, SW, and GND plane for minimal noise and ringing.
2. Keep the output loop between the rectifier diode, the output capacitor, and the transformer as short as possible.
3. Keep the clamp loop circuit between D2, C4, and the transformer as small as possible.
4. Place the VCC capacitor close to VCC for the best decoupling. The current setting resistor R3 should be placed as close to ILIM and AGND as possible.
5. Keep the feedback trace far away from noise sources (such as SW). The trace connecting FB1 should be short.

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6. Use a single point connection between power GND and signal GND. Vias around GND and the thermal pad are recommended to lower the die temperature.

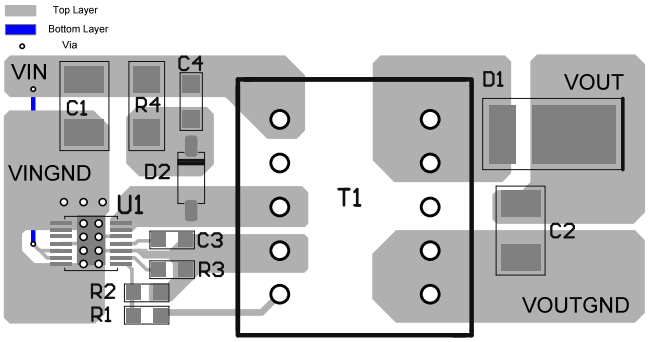

Figure 8—Recommended flyback layout

For buck application:

1. Keep the input loop as short as possible between the input capacitor, rectifier diode, SW, and GND plane for minimal noise and ringing.
2. Keep the output loop between the rectifier diode, the output capacitor, and the inductor as short as possible.
3. Place the VCC capacitor close to VCC for the best decoupling. The current setting resistor R3 should be placed as close to ILIM and AGND as possible.
4. Connect the output voltage sense and VIN power supply from the output capacitor with parallel traces. The feedback trace should be far away from noise sources (such as SW). The trace connected to FB2 should be short.
5. Use a single point connection between power GND and signal GND. Vias around GND and the thermal pad are recommended to lower the die temperature.

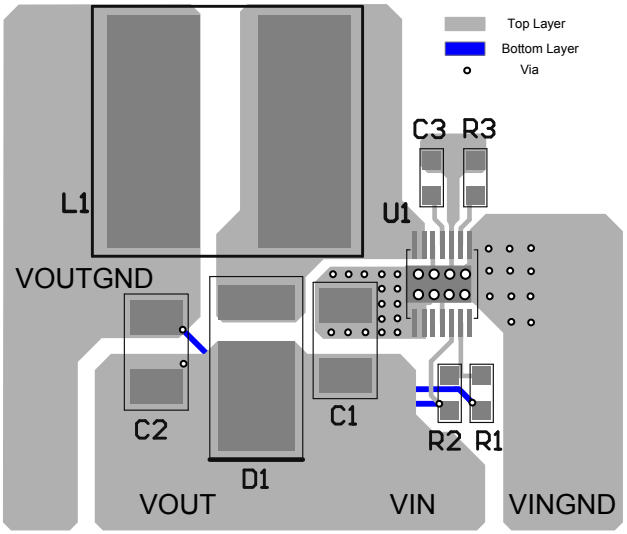

Figure 9—Recommended buck layout

Design Example

Table 1 shows a design example following the application guidelines for the following specifications in flyback applications:

Table 1—Flyback design example

V_{IN}	36 V-72 V
V_{OUT}	12 V
I_{OUT}	0 A-1 A

The typical application circuit for V_{OUT} = 12 V in Figure 10 shows the detailed application schematic and is the basis for the typical performance waveforms. For more detailed device applications, please refer to the related evaluation board datasheet.

Table 2 shows a design example following the application guidelines for the following specifications in buck applications:

Table 2—Buck design example

V_{IN}	36 V-72 V
V_{OUT}	12 V
I_{OUT}	0 A-1 A

The typical application circuit is shown in Figure 11. For more detailed device applications, please refer to the related evaluation board datasheet.

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TYPICAL APPLICATION CIRCUITS

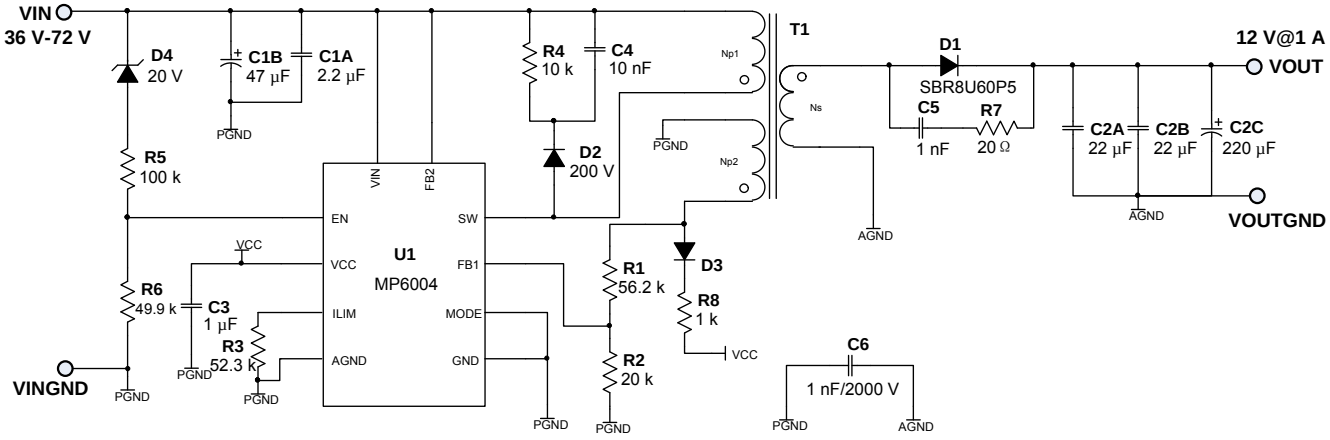

Figure 10—Flyback application circuit, V_{IN} = 36 V-72 V, V_{OUT} = 12 V, I_{OUT} =1 A

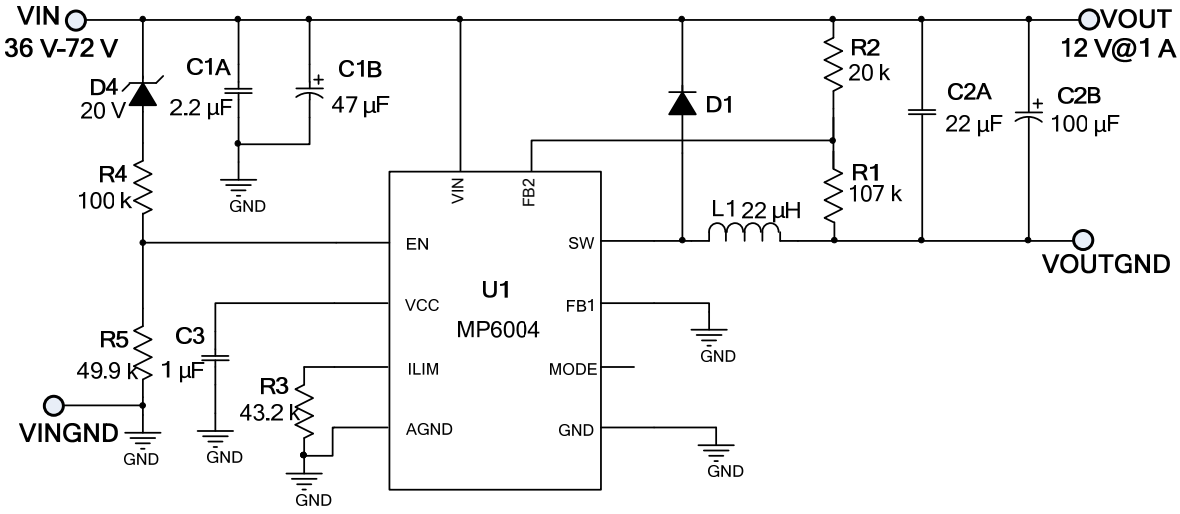

Figure 11—Buck application circuit, V_{IN} = 36 V-72 V, V_{OUT} = 12 V, I_{OUT} = 1 A

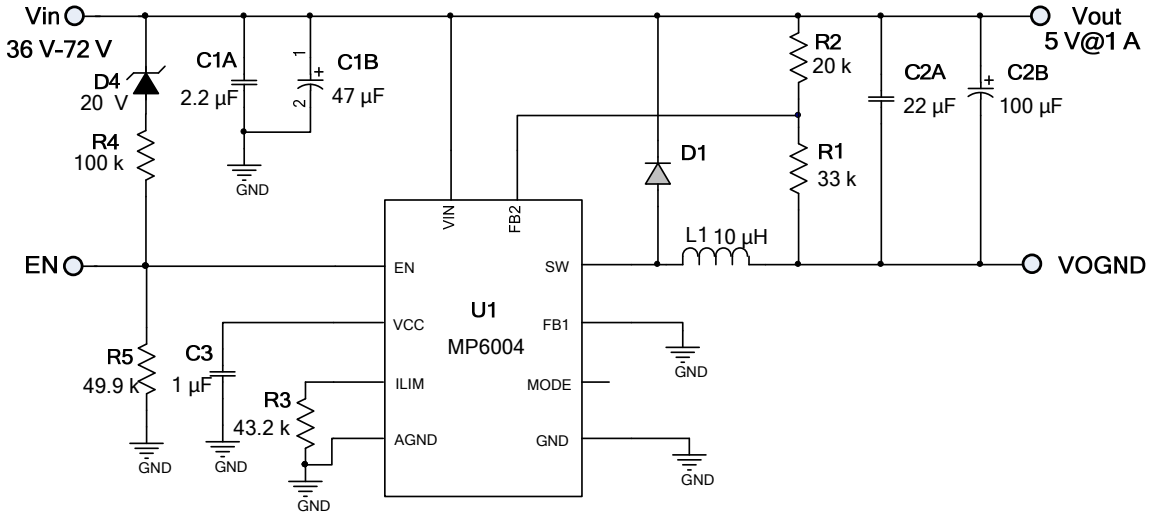

Figure 12—Buck application circuit, V_{IN} = 36 V-72 V, V_{OUT} = 5 V, I_{OUT} = 1 A

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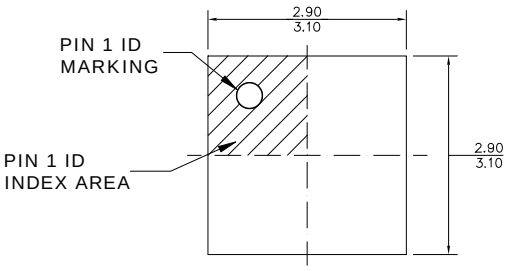
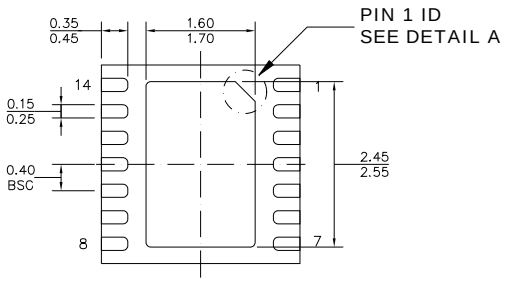
PACKAGE INFORMATION

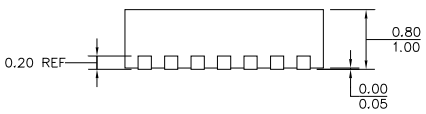
QFN-14 (3mm X 3mm)



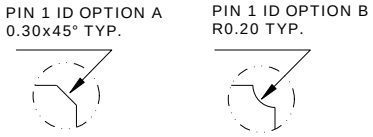
TOP VIEW



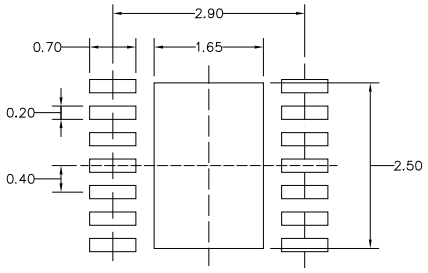
BOTTOM VIEW



SIDE VIEW



DETAIL A



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-229.
5) DRAWING IS NOT TO SCALE.

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