PIC16(L)F18854 Family
Silicon Errata and Data Sheet Clarification

The PIC16(L)F18854 family devices that you have received conform functionally to the current Device Data Sheet (DS40001826**D**), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in Table 1. The silicon issues are summarized in Table 2.

The errata described in this document will be addressed in future revisions of the PIC16(L)F18854 silicon.

Note:	This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of Table 2 apply to the current silicon revision **(A1)**.

Data Sheet clarifications and corrections start on page 5, following the discussion of silicon issues.

The silicon revision level can be identified using the current version of MPLAB® IDE and Microchip's programmers, debuggers, and emulation tools, which are available at the Microchip corporate website (www.microchip.com).

For example, to identify the silicon revision level using MPLAB IDE in conjunction with a hardware debugger:

1. Using the appropriate interface, connect the device to the hardware debugger.
2. Open an MPLAB IDE project.
3. Configure the MPLAB IDE project for the appropriate device and hardware debugger.
4. For MPLAB X IDE, select *Window > Dashboard* and click the **Refresh Debug Tool Status** icon ( ).
5. Depending on the development tool used, the part number *and* Device Revision ID value appear in the **Output** window.

Note:	If you are unable to extract the silicon revision level, please contact your local Microchip sales office for assistance.

The DEVREV values for the various PIC16(L)F18854 silicon revisions are shown in Table 1.

TABLE 1: SILICON DEVREV VALUES

Part Number	Device ID(1)	Revision ID (Silicon Revision)(2)	
		A1	A2
PIC16F18854	306Ah	2001h	2002h
PIC16LF18854	306Bh	2001h	2002h

Note 1: The Revision ID and Device ID are located in the Configuration memory at addresses 8005h and 8006h, respectively.

2: Refer to the *"PIC16(L)F188XX Memory Programming Specification"* (DS40001753) for detailed information on Device and Revision IDs for your specific device.

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TABLE 2: SILICON ISSUE SUMMARY

Module	Feature	Item No.	Issue Summary	Affected Revision(1)	
				A1	A2
Analog-to-Digital Converter with Computation (ADC2)	Computation Overflow Bit	1.1	The Computation Overflow bit will be erroneously set by the ADFLTR.	X	
Analog-to-Digital Converter with Computation (ADC2)	ADC Conversion	1.2	When using ADCRC as the ADCC clock source, there is a delay of one instruction cycle to set the ADGO bit.	X	
Analog-to-Digital Converter with Computation (ADC2)	Positive Voltage Reference	1.3	Using the FVR as the ADC positive voltage reference can cause missing codes.	X	X
Nonvolatile Memory Control	NVMREG Access	2.1	Self-writes on LF devices below 2.2V at -40°C may not work.	X	
EEPROM	Indirect Read	3.1	Indirect read of EEPROM with FSR returns unexpected value.	X	
ECCP	Compare Mode	4.1	Toggle mode may output multiple pulses when source clock has a prescaler other than 1:1.	X	
MSSP	I^2C Communication	5.1	Acknowledge failure on LF Devices Only.	X	
Electrical Specifications	Fixed Voltage Reference (FVR) Accuracy	6.1	Fixed Voltage Reference (FVR) output tolerance may be higher than specified at temperatures below -20°C.	X	
Secondary Oscillator (Sosc)	Low-Power Mode	7.1	SOSC does not properly run in Low-Power mode at low temperatures.	X	
Comparators	Offset Voltage	8.1	Comparator Input Offset value is higher than specified.	X	X

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

Silicon Errata Issues

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the shaded column in the following tables apply to the current silicon revision **(A1)**.

1. Module: Analog-to-Digital Converter with Computation (ADC2)

1.1 Computation Overflow Bit

If the sign bit of ADFLTR (bit 7 of ADFLTRH) is set, the Computation Overflow bit will also be set, even though this is not a legitimate case of an overflow event.

Work around

None.

Affected Silicon Revisions

A1	A2						
X							

1.2 ADC Conversion

When using ADCRC as the clock source for ADCC, there is a delay of one instruction cycle between the user setting the ADGO bit and being able to read it set. This can lead to a false conversion complete scenario (i.e., ADGO being cleared), depending if the user code has a bit clear test (BTFSC) instruction on the ADGO bit, immediately after setting the ADGO bit. See code example below.

e.g.

```
BSF ADCON0, ADGO      ; Start conversion
BTFSC ADCON0, ADGO    ; Is conversion done?
GOTO $-1              ; No, test again
```

The BTFSC will pass the very first time in this situation.

Work around

Add a `NOP` instruction after setting the ADGO bit and before testing the bit for completion of conversion. See code example below.

e.g.

```
BSF ADCON0, ADGO      ; Start conversion
NOP
BTFSC ADCON0, ADGO    ; Is conversion done?
GOTO $-1              ; No, test again
```

Affected Silicon Revisions

A1	A2						
X							

1.3 Positive Voltage Reference

Using the FVR as the positive voltage reference for the ADC can cause an increase in missing codes.

Work around

Increase the bit conversion time (TAD) to 8 us or higher.

Affected Silicon Revisions

A1	A2						
X	X						

2. Module: Nonvolatile Memory Control

2.1 NVMREG Access

When performing self-writes through NVMREG access on PIC16LF18854 devices with V_{DD} below 2.2V and temperature of -40°C, the writes may not work. This applies to both PFM and EEPROM writes.

Work around

None.

Affected Silicon Revisions

A1	A2						
X							

3. Module: EEPROM

3.1 Indirect Read

Performing FSR reads of Data EEPROM addresses other than the lowest address (FSR=7000h) will return unexpected values.

Work around

Set NVMADRH:L to the desired address (F000h through F0FFh) and retrieve the EEPROM value from the NVMDATL register by setting the NVMREGS and RD bits in the NVMCON1 register.

Affected Silicon Revisions

A1	A2						
X							

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4. Module: ECCP

4.1 Compare Mode

The ECCP Compare Toggle modes (CCPxCON<3:0> bits = 0010 or 0001) output multiple pulses instead of a single toggle pulse when its source clock has a prescaler other than 1:1.

Work around

Use CCP Compare mode with pulse output (CCPxCON<3:0> bits = 1011) to clock a CLC configured as a J-K flip-flop in Toggle mode.

Affected Silicon Revisions

A1	A2						
X							

5. Module: MSSP

5.1 I^2C Communication

When using the MSSP to perform I^2C communication on LF devices and the voltage for VDD is above 3V, the Acknowledge signal (ACK) does not always occur after the second address byte is received, as expected. This issue exhibits itself when the MSSP is configured either for 7-bit or 10-bit addressing and in either Master or Slave mode.

The issue occurs more frequently when using 10-bit addressing in Slave mode and the lower address bits (A7-A0) are transmitted by the Master on the SDA line.

Work around

Do not exceed 3V on VDD when using an LF device in this manner.

Affected Silicon Revisions

A1	A2						
X							

6. Module: Electrical Specifications

6.1 Fixed Voltage Reference (FVR) Accuracy

At temperatures below -20°C, the output voltage for the FVR may be greater than the levels specified in the data sheet. This will apply to all three gain amplifier settings (1X, 2X, 4X). The affected parameter numbers found in the data sheet are: FVR01, (1X gain setting), FVR02 (2X gain setting), and FVR03 (4X gain setting).

Work around

At temperatures above -20°C, the stated tolerances in the data sheet remain in effect. Operate the FVR only at temperatures above -20°C.

Affected Silicon Revisions

A1	A2						
X							

7. Module: Secondary Oscillator (SOSC)

7.1 Low-Power Mode

While operating the device at low temperatures and using the SOSC in Low-Power mode (OSCCON3<6> = 0), the SOSC might fail to operate as expected.

Work around

If SOSC functionality is required at low temperatures, configure the SOSC for high-power operation (OSCCON3<6> = 1).

Affected Silicon Revisions

A1	A2						
X							

8. Module: Comparators

8.1 Offset Voltage

The maximum value of the input offset voltage for the comparators is increasing from ±30 mV to ±60 mV.

The parameter in the data sheet is CM01, also known as VIOFF.

Work around

None.

Affected Silicon Revisions

A1	A2						
X	X						

Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS40001826**D**):

Note:	Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

None.

APPENDIX A: DOCUMENT REVISION HISTORY

Rev E Document (3/2020)

Added Module 8 (Comparators).

Rev D Document (3/2018)

Added Module 7 (Secondary Oscillator) and a row in Table 2;

Added silicon revision A2 and associated issues.

Rev C Document (6/2017)

Added Module 1.3 (PVR), Module 5 (MSSP) and Module 6 (Electrical Specifications).

Data Sheet Clarifications:
Removed all modules, data sheet updated.

Rev B Document (9/2016)

Modifications brought to Table 2.

Silicon Errata Issues:
Added ADC Conversion feature to Analog-to-Digital Converter with Computation (ADC2);
Added EEPROM and ECCP modules.

Data Sheet Clarifications:
Added modules 4 to 15.

Rev A Document (5/2016)

Initial release of this document.

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