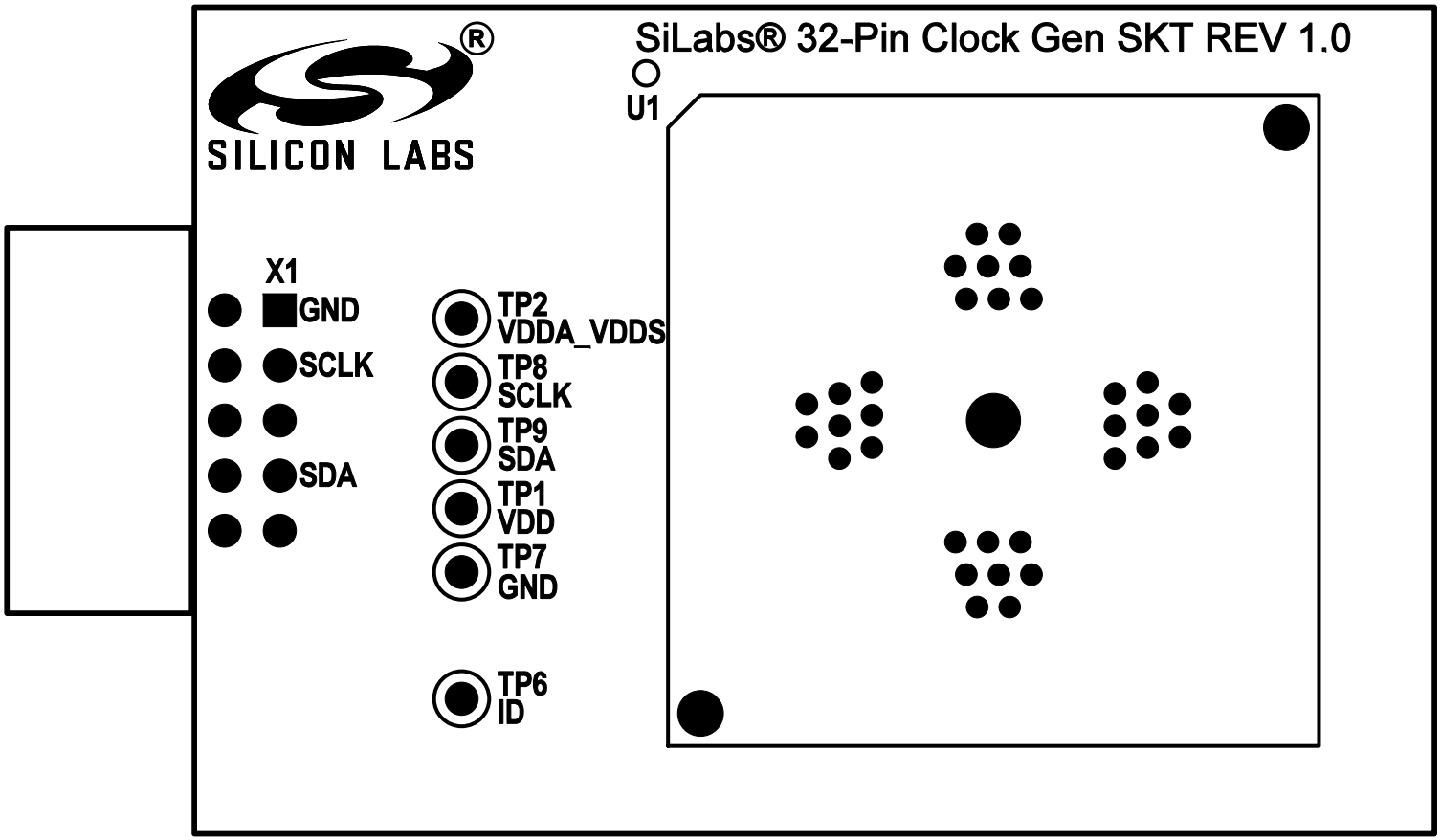
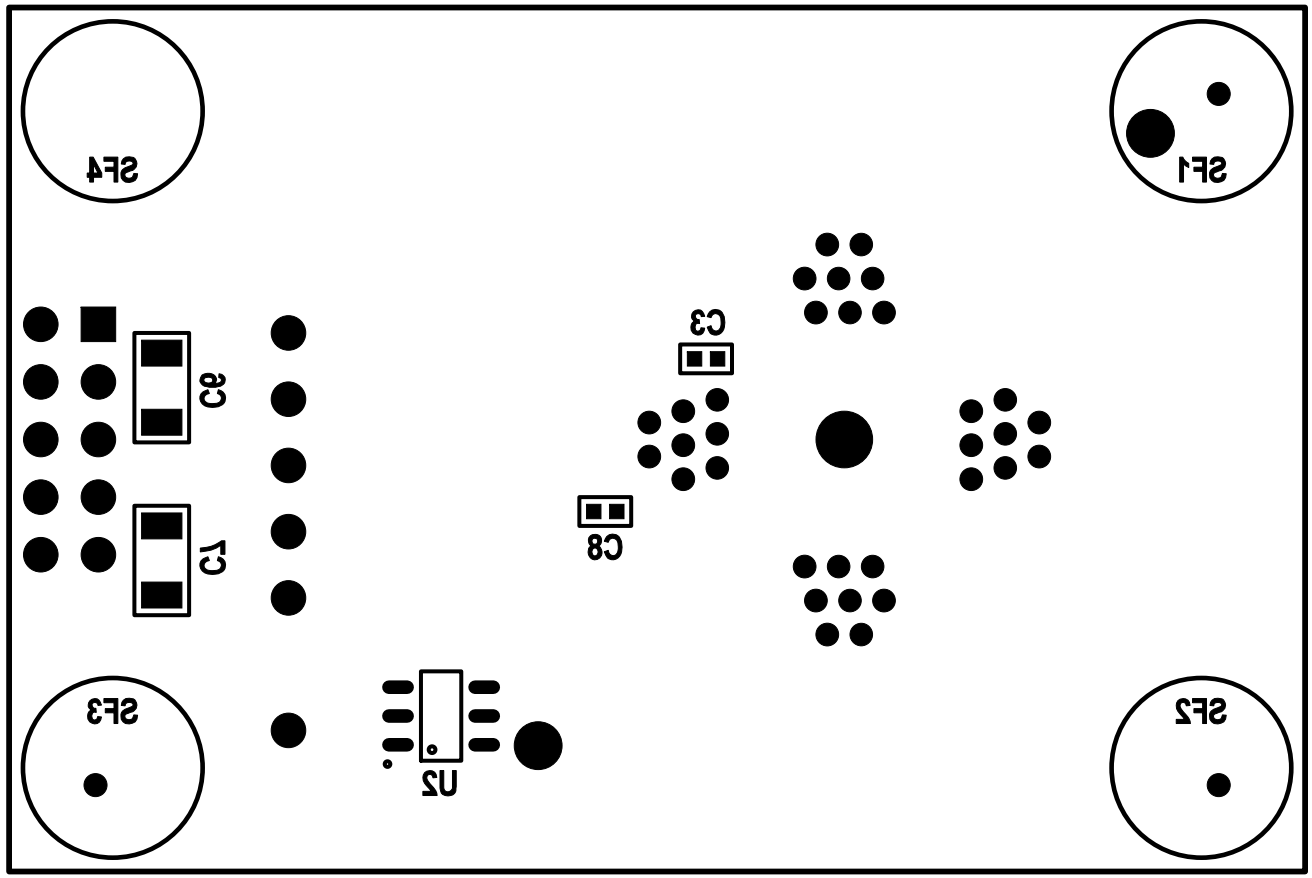
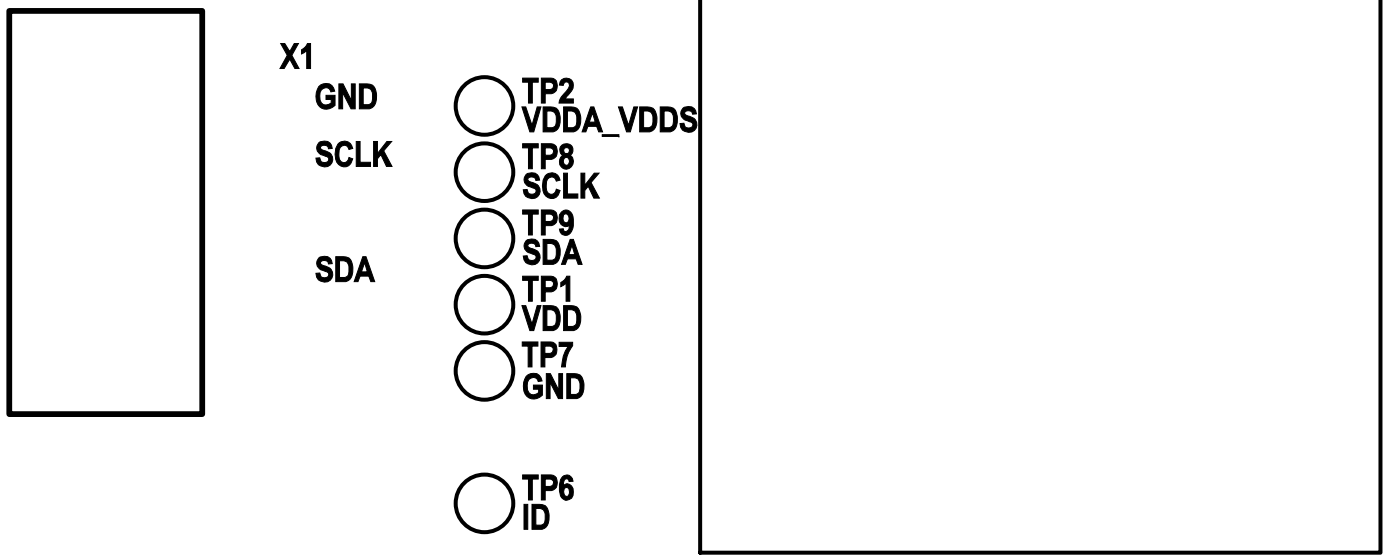


PRIMARY SILKSCREEN

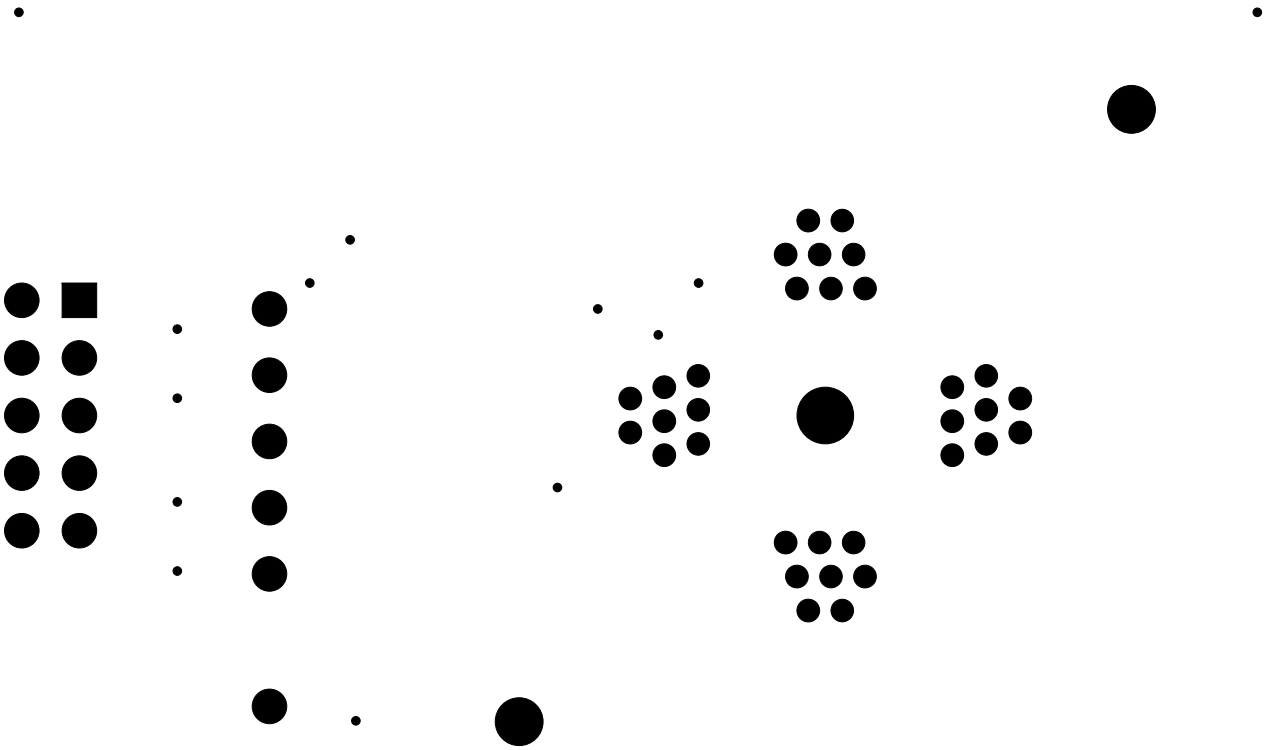


SECONDARY SILKSCREEN

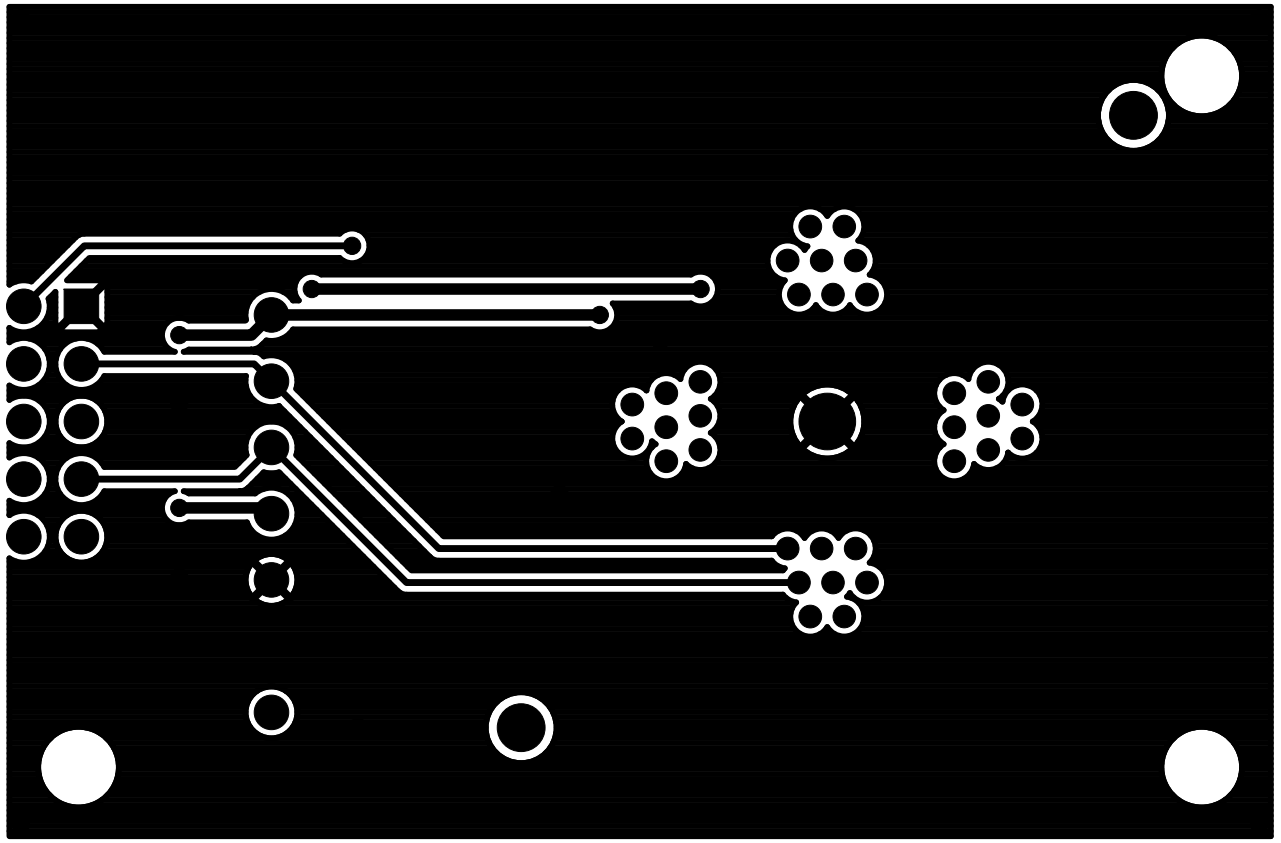
SiLabs® 32-Pin Clock Gen SKT REV 1.0



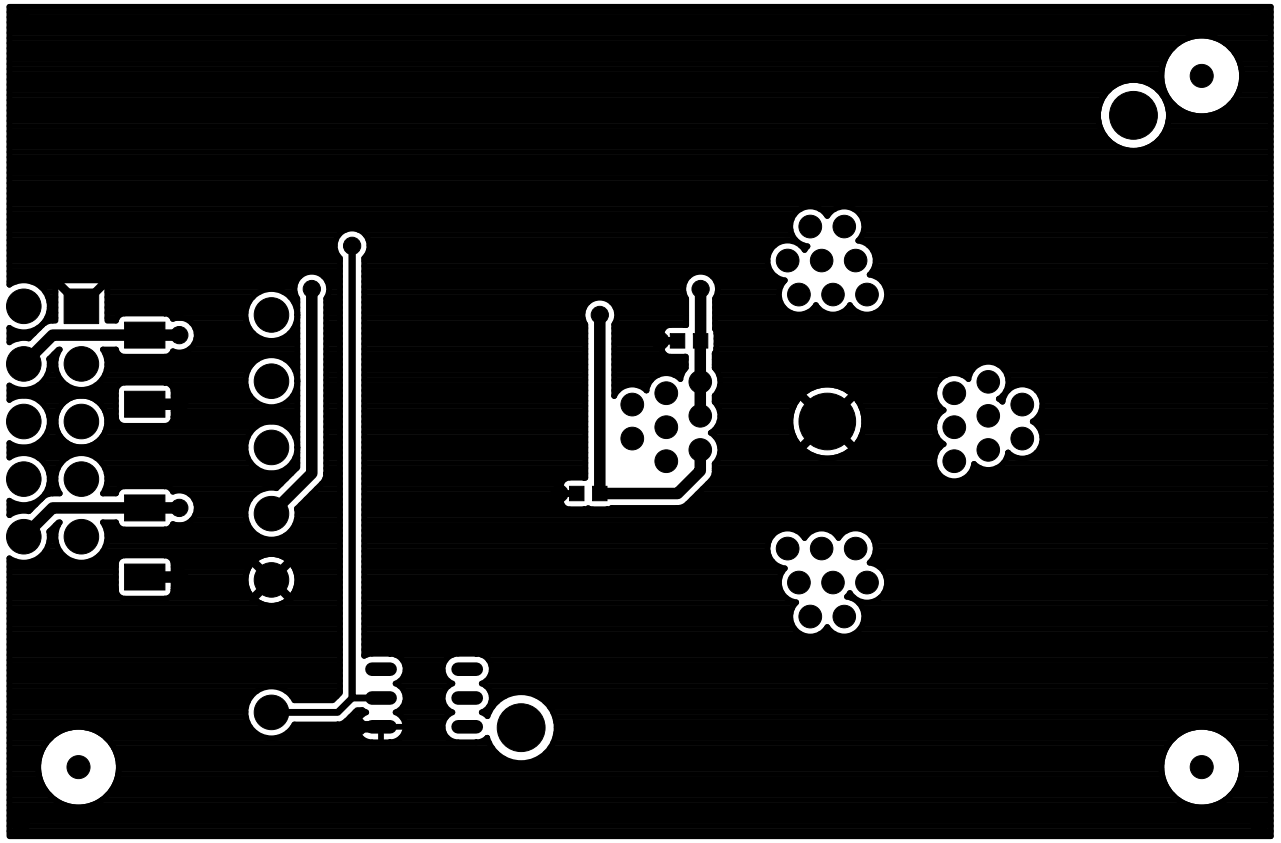
PRIMARY SILKSCREEN



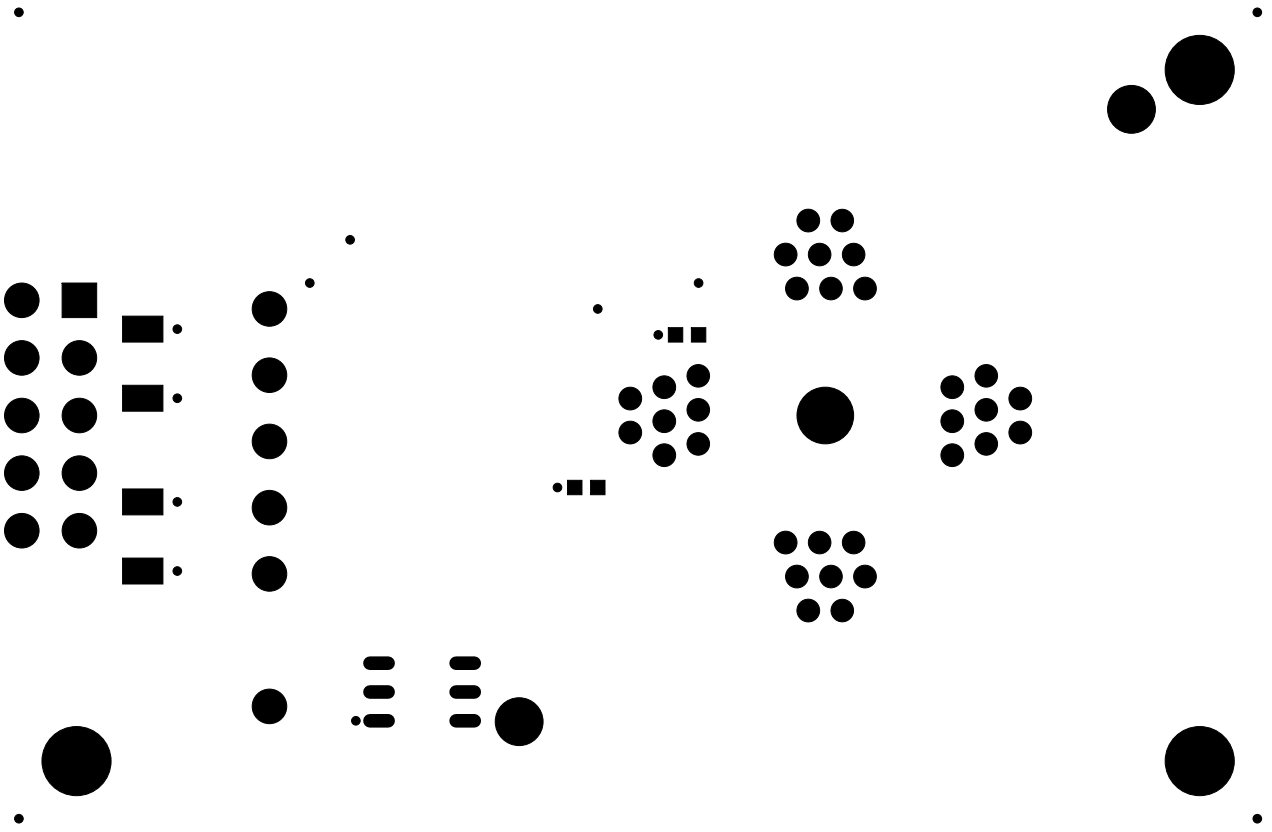
PRIMARY SOLDER MASK



PRIMARY SIDE

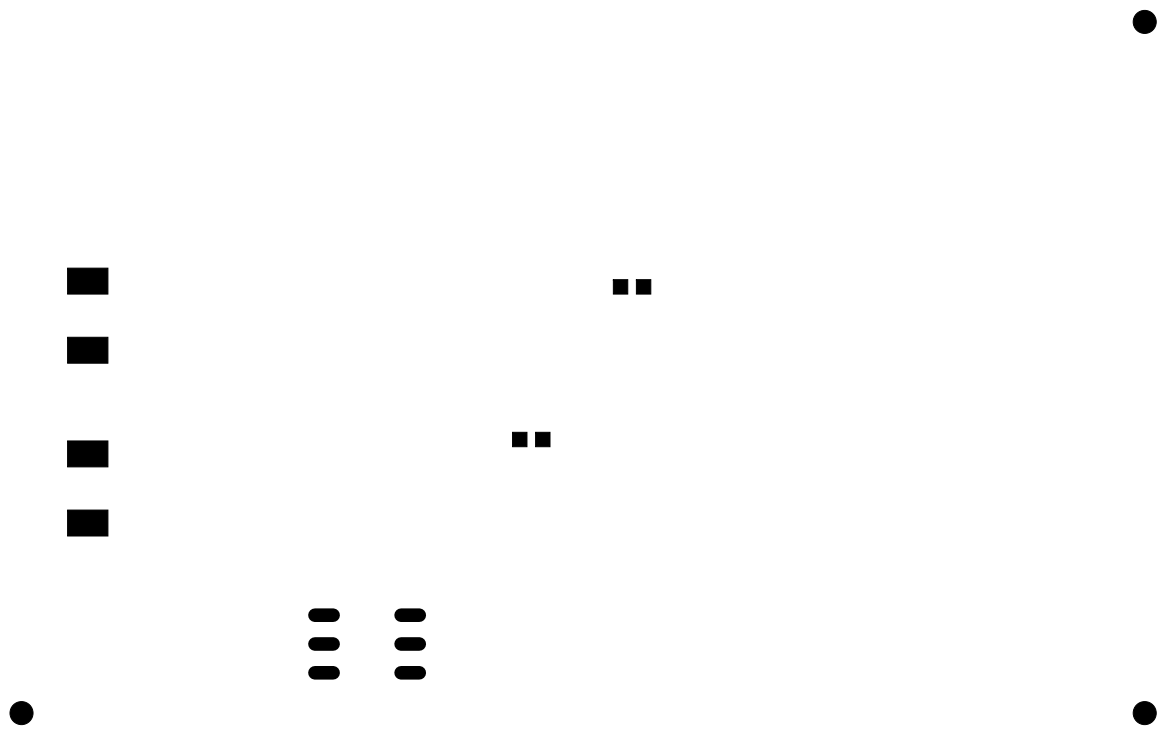


BOTTOM SIDE

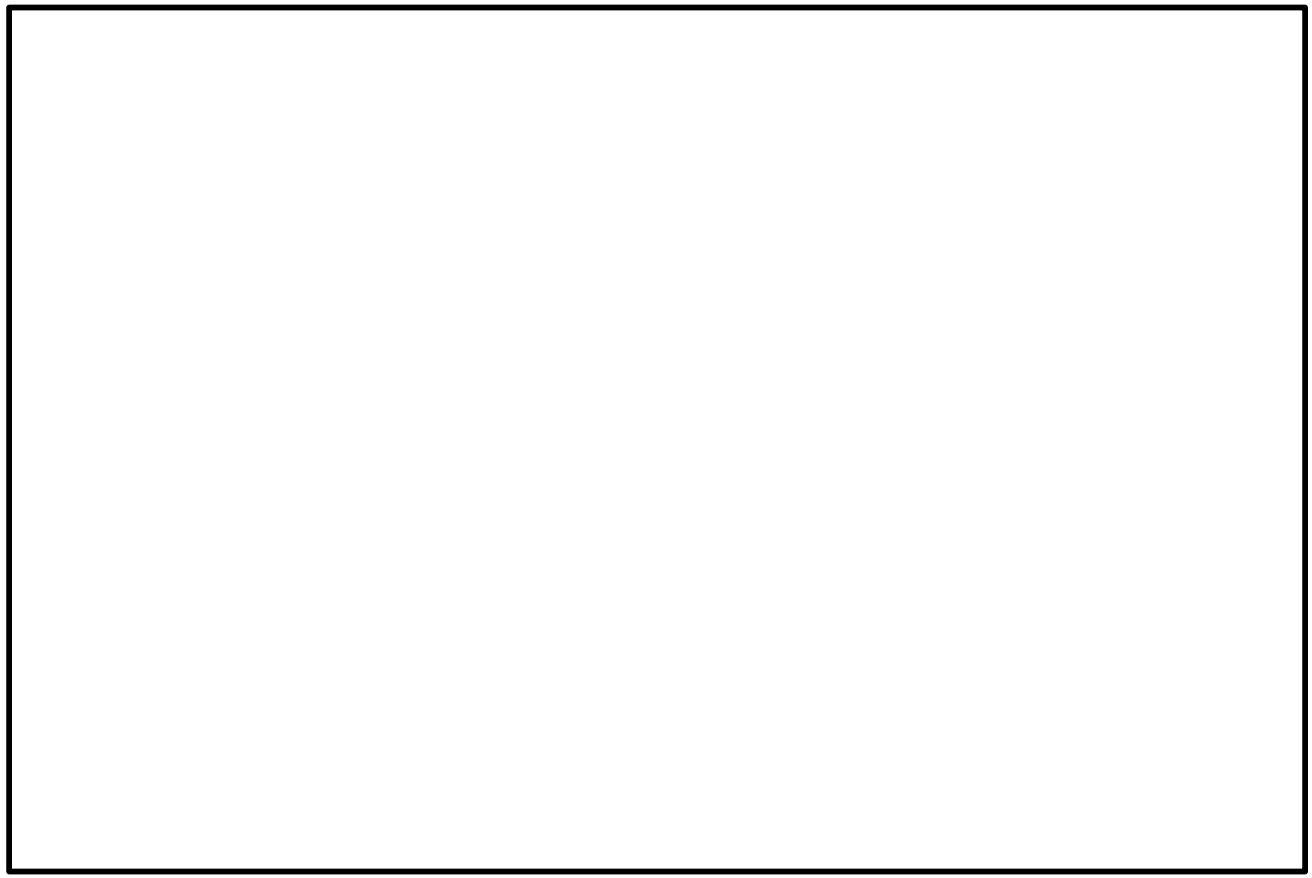


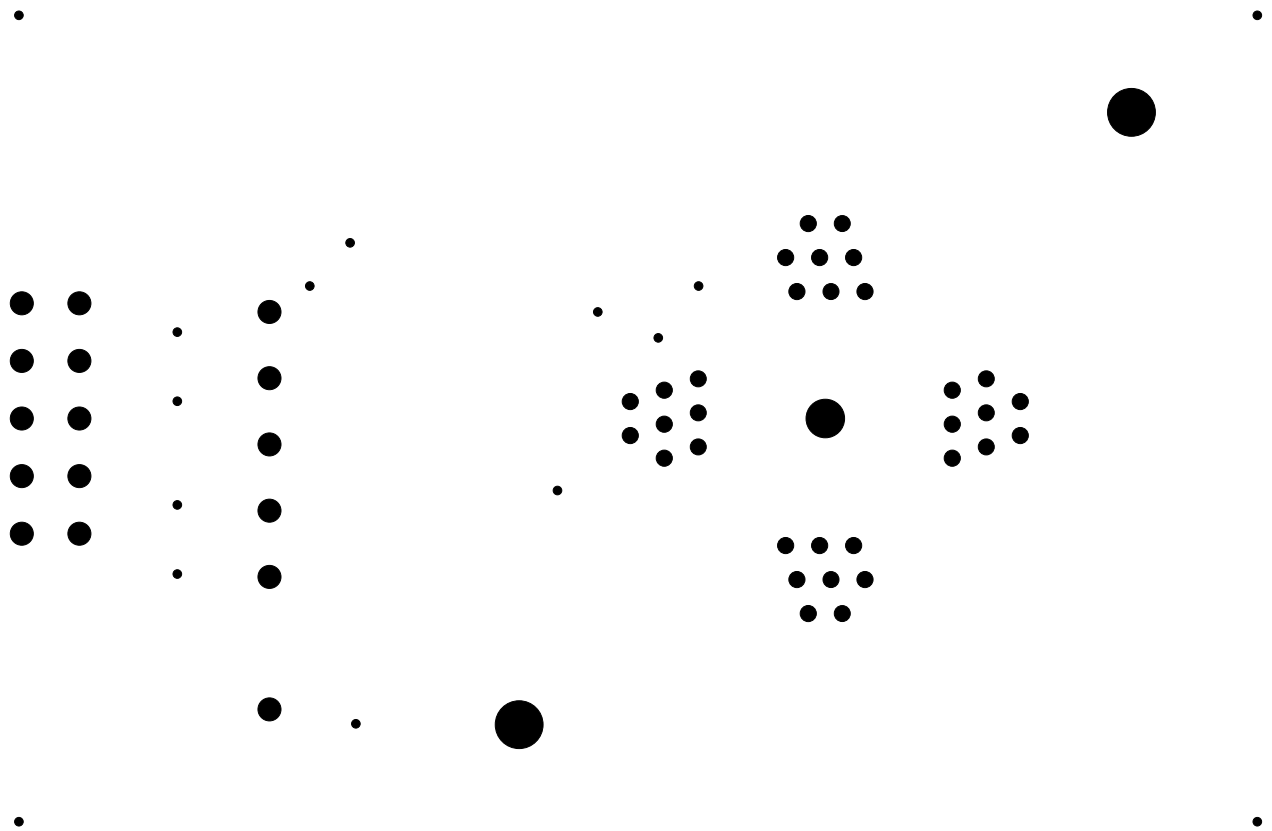
SECONDARY SOLDER MASK

SECONDARY SILKSCREEN



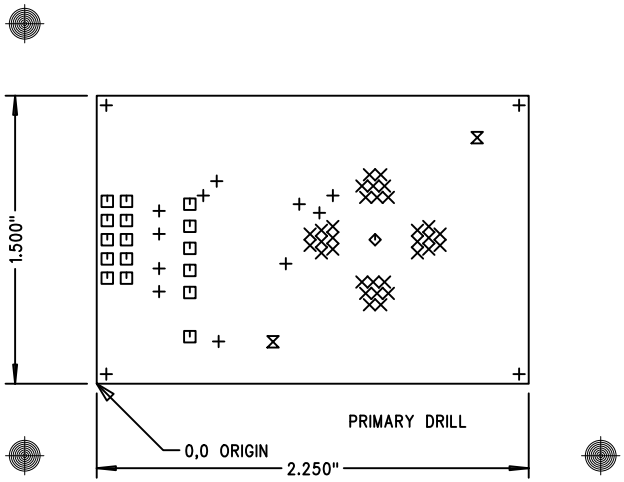
SECONDARY SOLDER PASTE





NOTES : UNLESS OTHERWISE SPECIFIED

1. MANUFACTURE IN ACCORDANCE WITH IPC-6012, TYPE 3, CLASS 2.
2. END PRODUCT FEATURES SHALL NOT VARY MORE THAN 20% FROM ARTWORK ORIGINALS.
3. LAMINATE AND PREPREG SHALL BE AS PER IPC-4101/26,83,98 WITH A DECOMPOSITION TEMPERATURE >= 345°C, COLOR, NATURAL.
4. COPPER WEIGHT SHALL BE 1.0 OZ./SQ. FT. BEFORE PLATING.
5. ALL PLATED THROUGH HOLES SHALL HAVE A MINIMUM OF 0.001" COPPER.
6. DRILL HOLE TOLERANCE AFTER PLATING SHALL BE ±0.003".
7. MINIMUM ANNULAR RING SHALL BE 0.001".
8. MINIMUM ANNULAR RING AT EMERGENT CONDUCTORS SHALL BE 0.003".
9. FINAL PCB THICKNESS SHALL BE 0.062" ±10%.
10. WARP/TWIST SHALL NOT EXCEED 1.0%
11. FINISH SHALL BE LPI, BLUE S.M.O.B.C., BALANCE ENIG.
12. SILKSCREEN WITH NONCONDUCTIVE WHITE EPOXY INK.
13. REFERENCE ADDITIONAL FAB NOTES IN FILE README.TXT



LAYER STACKUP	FILE NAMES
PRIMARY SILKSCREEN	5332-32SKT_PSS.PHO
PRIMARY SOLDERMASK	5332-32SKT_PSM.PHO
PRIMARY SIDE	5332-32SKT_PRI.PHO
SECONDARY SIDE	5332-32SKT_SEC.PHO
SECONDARY SOLDERMASK	5332-32SKT_SSM.PHO
SECONDARY SILKSCREEN	5332-32SKT_SSS.PHO

SCALE: NONE

SIZE	QTY	SYM	PLT	TOOL	TOL
0.015	15	+	P	1	+0/-0.015
0.028	32	X	P	2	+/-0.003
0.040	16	⊡	P	3	+/-0.003
0.067	1	◇	P	4	+/-0.003
0.083	2	⧖	N	5	+/-0.003

UNLESS OTHERWISE SPECIFIED

DIMENSIONS ARE IN INCHES AND APPLY AFTER FINISH
DIMENSIONS IN BRACKETS [ ] ARE IN MILLIMETERS
INTERPRET DRAWING PER MIL-D-1000

TOLERANCES

HOLE TOLERANCES PER 78027

DECIMALS	ANGLES	SURFACES
.XX +/- .XXX +/-	+/-	MICROINCHES

PART TO BE FREE OF BURRS

BREAK EDGES	BEND RADIUS	BEND RELIEF
MAX	MAX	MAX

DESIGN	TT	08JUNE2017
LAYOUT	AA	08JUNE2017

DO NOT SCALE DRAWING

COMPANY: SILICON LABS
400 W Cesar Chavez
AUSTIN, TX 78701
(512)416-8500
www.silabs.com

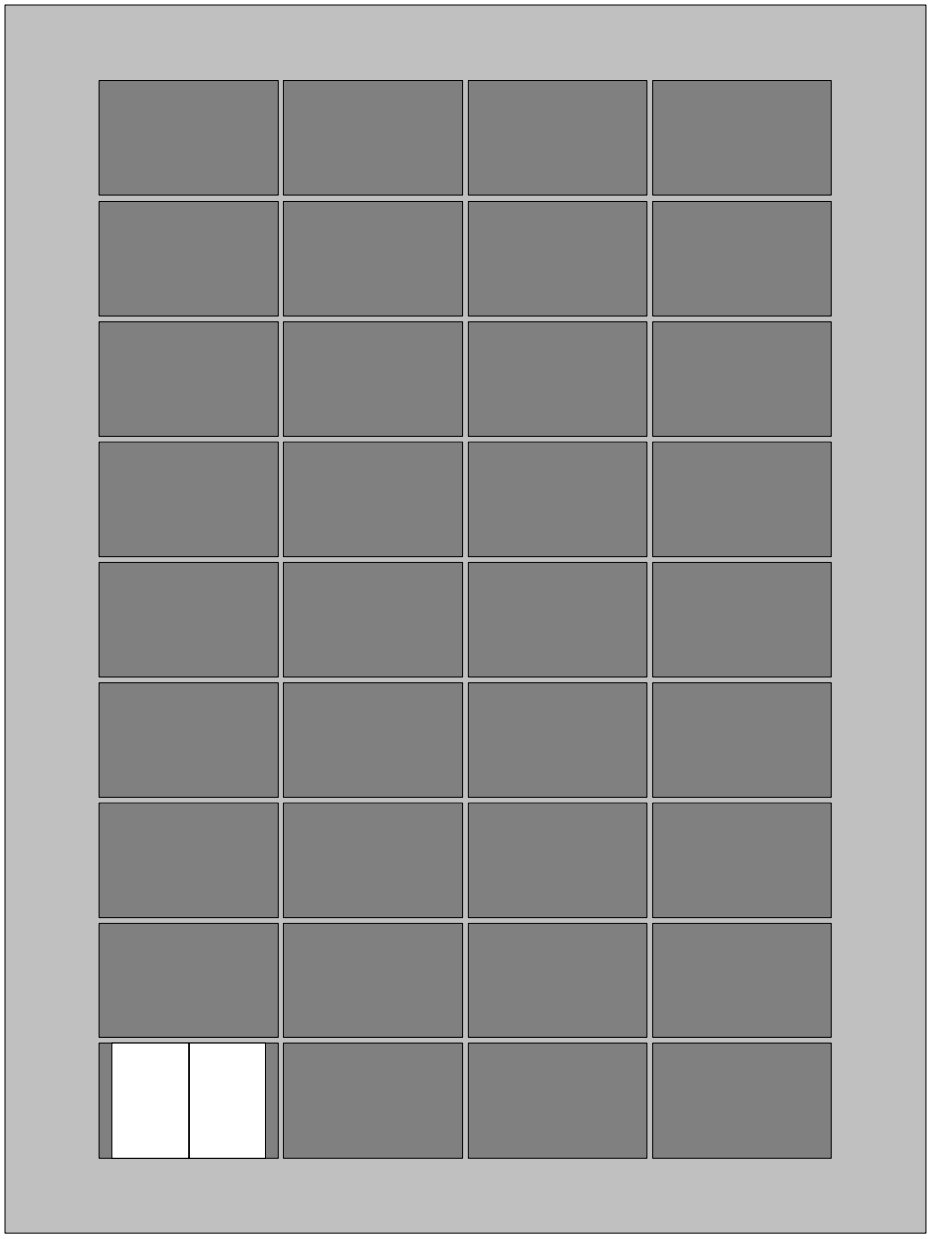
NAME: Si5332-32SKT

REV : 1.0

SIZE A

PART NUMBER:

SCALE 1:1 | FABRICATION DRAWING | SHEET 1 OF 1



Si5332-32SKT Rev1.0

Size:
Panel: 18.0 x 24.0
Array: 3.5 x 2.25
Part: 1.5 x 2.25

Panel Yield:
36 Arrays of 2 Parts
72 Parts Total
65.6% Material Utilization

Matrix:
On Panel: 4 x 9, Origin: X1.85 Y1.475
On Array: 2 x 1

Spacing:
On Panel: 0.1 x 0.1
On Array: 0.0 x 0.0

Panel Borders:
Left: 1.85 Right: 1.85
Top: 1.475 Bottom: 1.475

Array Borders:
Left: 0.25 Right: 0.25
Top: 0.0 Bottom: 0.0

Notes:

Please add 4, 0.125" NP tooling holes located 0.125" from tab corners and 3, 40/120 fiduials to each side of array located 0.25" from tooling holes.