NTJD4158C, NVJD4158C

MOSFET – Small Signal, Complementary, SC-88
30 V/-20 V, +0.25/-0.88 A

ON Semiconductor®

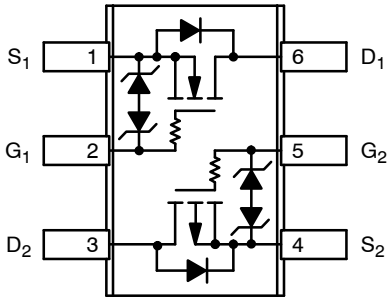
www.onsemi.com

$V_{(BR)DSS}$	$R_{DS(on)}$ Typ	I_D Max
N–Ch 30 V	1.0 Ω @ 4.5 V	0.25 A
	1.5 Ω @ 2.5 V	
P–Ch –20 V	215 mΩ @ –4.5 V	–0.88 A
	345 mΩ @ –2.5 V	

Features
- Leading 20 V Trench for Low $R_{DS(on)}$ Performance
- ESD Protected Gate
- SC–88 Package for Small Footprint (2 x 2 mm)
- NV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC–Q101 Qualified and PPAP Capable
- These Devices are Pb–Free, Halogen Free/BFR Free and are RoHS Compliant

Applications
- DC–DC Conversion
- Load/Power Management
- Load Switch
- Cell Phones, MP3s, Digital Cameras, PDAs

SC–88 (SOT–363)
(6–Leads)



(Top View)

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Parameter			Symbol	Value	Unit
Drain–to–Source Voltage		N–Ch	V_{DSS}	30	V
		P–Ch		–20	
Gate–to–Source Voltage		N–Ch	V_{GS}	±20	V
		P–Ch		±12	
N–Channel Continuous Drain Current (Note 1)	Steady State	T_A = 25°C	I_D	0.25	A
		T_A = 85°C		0.18	
P–Channel Continuous Drain Current (Note 1)	Steady State	T_A = 25°C		–0.88	
		T_A = 85°C		–0.63	
Power Dissipation (Note 1)	Steady State	T_A = 25°C	P_D	0.27	W
Pulsed Drain Current	N–Ch	tp = 10 μs	I_{DM}	0.5	A
	P–Ch			–3.0	
Operating Junction and Storage Temperature			T_J, T_{stg}	–55 to 150	°C
Source Current (Body Diode)		N–Ch	I_S	0.25	A
		P–Ch		–0.48	
Lead Temperature for Soldering Purposes (1/8″ from case for 10 s)			T_L	260	°C

THERMAL RESISTANCE RATINGS

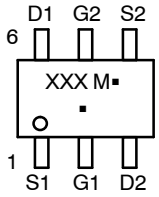
Parameter	Symbol	Max	Unit
Junction–to–Ambient – Steady State (Note 1)	$R_{\theta JA}$	460	°C/W

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

MARKING DIAGRAM & PIN ASSIGNMENT



SC–88 (SOT–363)
CASE 419B
STYLE 26



XXX = Specific Device Code
M = Date Code
▪ = Pb–Free Package
(Note: Microdot may be in either location)

ORDERING INFORMATION
See detailed ordering and shipping information in the package dimensions section on page 7 of this data sheet.

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1. Surface mounted on FR4 board using 1 in sq pad size
   (Cu area = 1.127 in sq [1 oz] including traces).

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Parameter	Symbol	N/P	Test Condition		Min	Typ	Max	Unit
OFF CHARACTERISTICS (Note 3)								
Drain−to−Source Breakdown Voltage	$V_{(BR)DSS}$	N	V_{GS} = 0 V	I_D = 250 μA	30			V
		P		I_D = −250 μA	−20			
Drain−to−Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$	N				33		mV/°C
		P				−9.0		
Zero Gate Voltage Drain Current	I_{DSS}	N	V_{GS} = 0 V, V_{DS} = 30 V	T_J = 25°C			1.0	μA
		P	V_{GS} = 0 V, V_{DS} = −16 V				1.0	
		N	V_{GS} = 0 V, V_{DS} = 30 V	T_J = 125°C		0.5		
		P	V_{GS} = 0 V, V_{DS} = −16 V			0.5		
Gate−to−Source Leakage Current	I_{GSS}	N	V_{DS} = 0 V, V_{GS} = 10 V				1.0	μA
		P	V_{DS} = 0 V, V_{GS} = −4.5 V				1.0	
ON CHARACTERISTICS (Note 2)								
Gate Threshold Voltage	$V_{GS(TH)}$	N	V_{GS} = V_{DS}	I_D = 100 μA	0.8	1.2	1.5	V
		P		I_D = −250 μA	−0.45	−0.61	−1.5	
Negative Gate Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$	N				3.2		mV/°C
		P				−2.7		
Drain−to−Source On Resistance	$R_{DS(on)}$	N	V_{GS} = 4.5 V, I_D = 10 mA			1.0	1.5	Ω
		P	V_{GS} = −4.5 V, I_D = −0.88 A			0.215	0.260	
		N	V_{GS} = 2.5 V, I_D = 10 mA			1.5	2.5	
		P	V_{GS} = −2.5 V, I_D = −0.71 A			0.345	0.500	
Forward Transconductance	g_{FS}	N	V_{DS} = 3.0 V, I_D = 10 mA			0.08		S
		P	V_{DS} = −10 V, I_D = −0.88 A			3.0		
CHARGES, CAPACITANCES AND GATE RESISTANCE								
Input Capacitance	C_{ISS}	N	f = 1 MHz, V_{GS} = 0 V	V_{DS} = 5.0 V		20	33	pF
		P		V_{DS} = −20 V		155	225	
Output Capacitance	C_{OSS}	N		V_{DS} = 5.0 V		19	32	
		P		V_{DS} = −20 V		25	40	
Reverse Transfer Capacitance	C_{RSS}	N		V_{DS} = 5.0 V		7.25	12	
		P		V_{DS} = −20 V		18	30	
Total Gate Charge	$Q_{G(TOT)}$	N	V_{GS} = 5.0 V, V_{DS} = 24 V, I_D = 0.1 A			0.9	1.5	nC
		P	V_{GS} = −4.5 V, V_{DS} = −10 V, I_D = −0.88 A			2.2	3.5	
Threshold Gate Charge	$Q_{G(TH)}$	N	V_{GS} = 5.0 V, V_{DS} = 24 V, I_D = 0.1 A			0.2		
		P	V_{GS} = −4.5 V, V_{DS} = −10 V, I_D = −0.88 A			0.2		
Gate−to−Source Charge	Q_{GS}	N	V_{GS} = 5.0 V, V_{DS} = 24 V, I_D = 0.1 A			0.3		
		P	V_{GS} = −4.5 V, V_{DS} = −10 V, I_D = −0.88 A			0.5		
Gate−to−Drain Charge	Q_{GD}	N	V_{GS} = 5.0 V, V_{DS} = 24 V, I_D = 0.1 A			0.2		
		P	V_{GS} = −4.5 V, V_{DS} = −10 V, I_D = −0.88 A			0.65		
SWITCHING CHARACTERISTICS (Note 3)								
Turn−On Delay Time	$t_{d(ON)}$	N	V_{GS} = 4.5 V, V_{DD} = 5.0 V, I_D = 250 mA, R_G = 50 Ω			15		ns
Rise Time	t_r					66		
Turn−Off Delay Time	$t_{d(OFF)}$					56		
Fall Time	t_f					78		
Turn−On Delay Time	$t_{d(ON)}$	P	V_{GS} = −4.5 V, V_{DD} = −10 V, I_D = −0.5 A, R_G = 20 Ω			5.8		
Rise Time	t_r					6.5		
Turn−Off Delay Time	$t_{d(OFF)}$					13.5		
Fall Time	t_f					3.5		
DRAIN−SOURCE DIODE CHARACTERISTICS								
Forward Diode Voltage	V_{SD}	N	V_{GS} = 0 V, T_J = 25°C	I_S = 10 mA		0.65	0.7	V
		P		I_S = −0.48 A		−0.8	−1.2	
		N	V_{GS} = 0 V, T_J = 125°C	I_S = 10 mA		0.45		
		P		I_S = −0.48 A		−0.66		
Reverse Recovery Time	t_{RR}	N	V_{GS} = 0 V, d_{IS}/d_t = 8.0 A/μs	I_S = 10 mA		12.4		ns
		P	V_{GS} = 0 V, d_{IS}/d_t = 100 A/μs	I_S = −0.48 mA		10.6		

2. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.
3. Switching characteristics are independent of operating junction temperatures.

TYPICAL N−CHANNEL PERFORMANCE CURVES (T_J = 25°C unless otherwise noted)

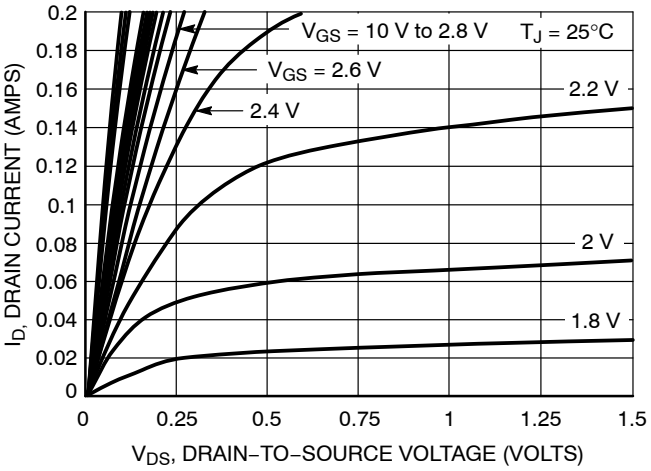


Figure 1. On−Region Characteristics

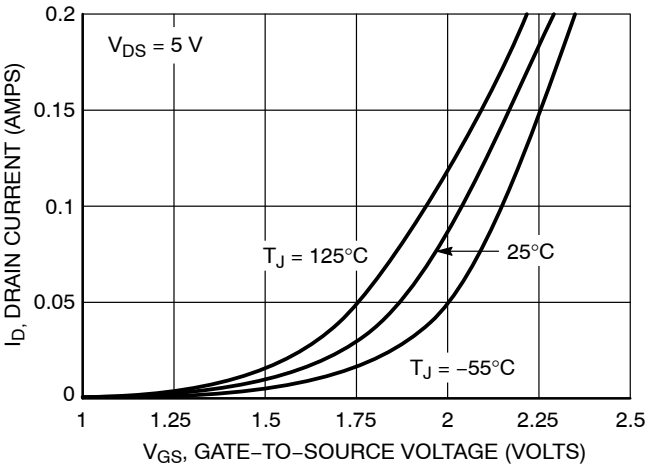


Figure 2. Transfer Characteristics

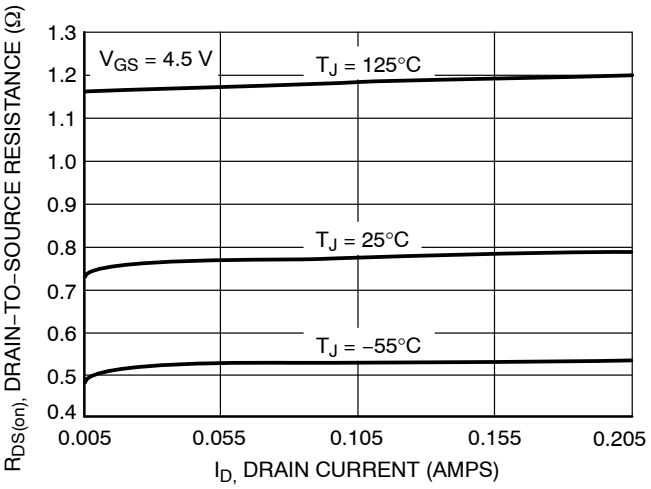


Figure 3. On−Resistance vs. Drain Current and Temperature

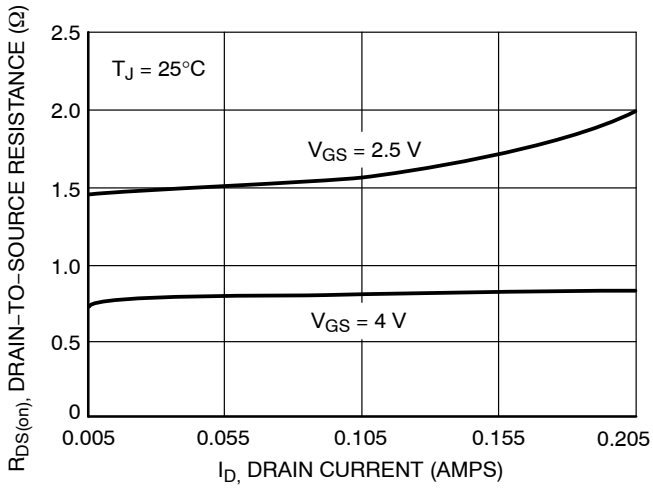


Figure 4. On−Resistance vs. Drain Current and Gate Voltage

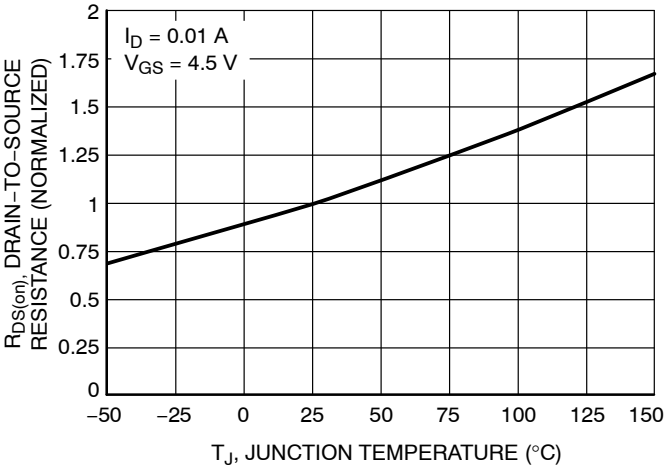


Figure 5. On−Resistance Variation with Temperature

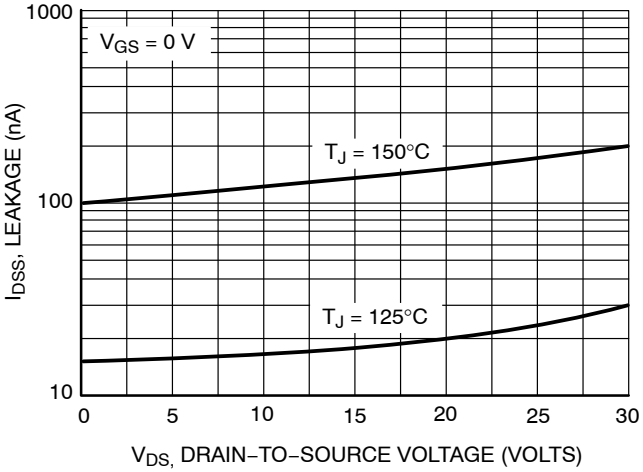


Figure 6. Drain−to−Source Leakage Current vs. Voltage

TYPICAL N−CHANNEL PERFORMANCE CURVES (T_J = 25°C unless otherwise noted)

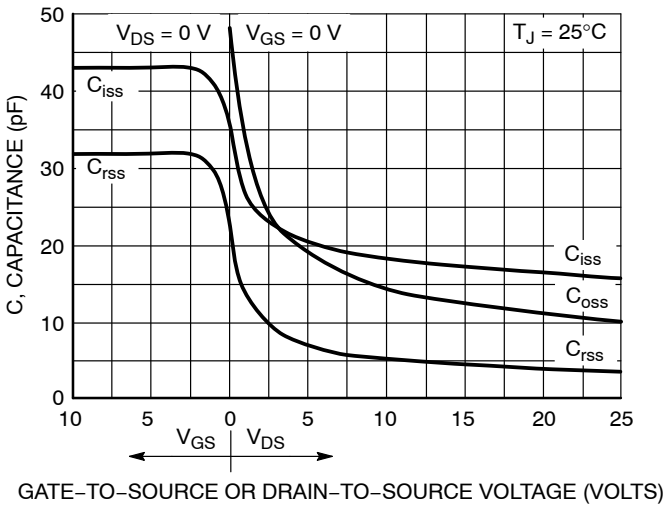


Figure 7. Capacitance Variation

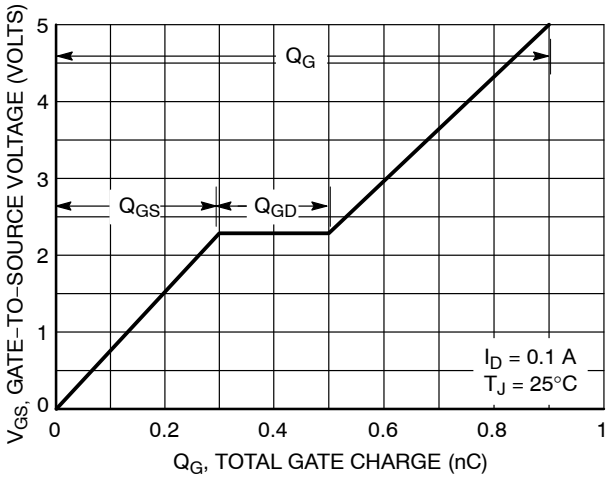


Figure 8. Gate−to−Source Voltage vs. Total Gate Charge

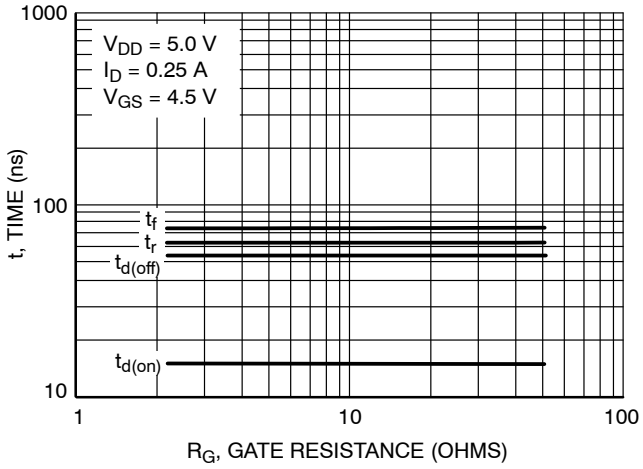


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

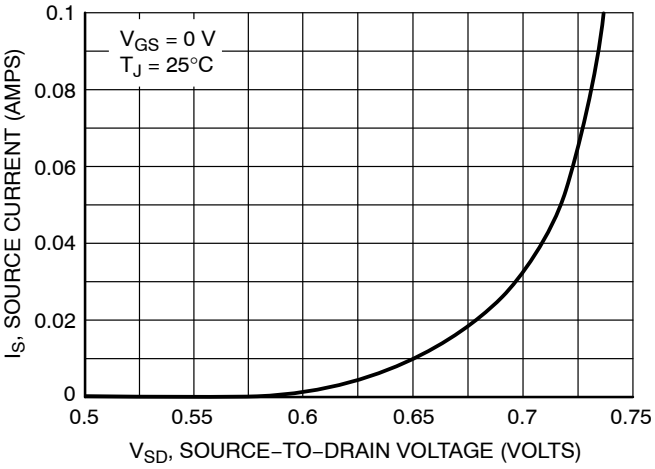


Figure 10. Diode Forward Voltage vs. Current

TYPICAL P−CHANNEL PERFORMANCE CURVES (T_J = 25°C unless otherwise noted)

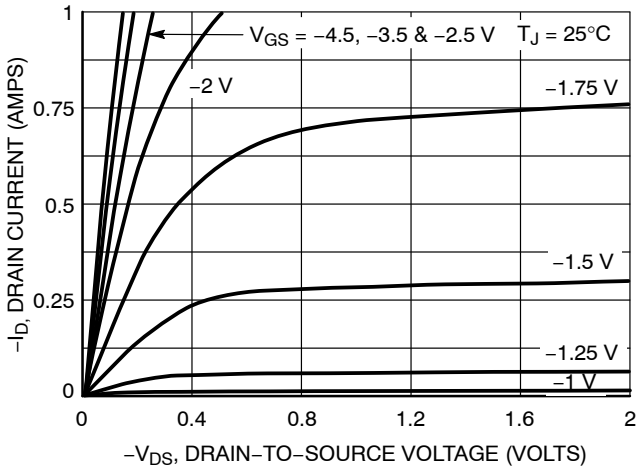


Figure 1. On−Region Characteristics

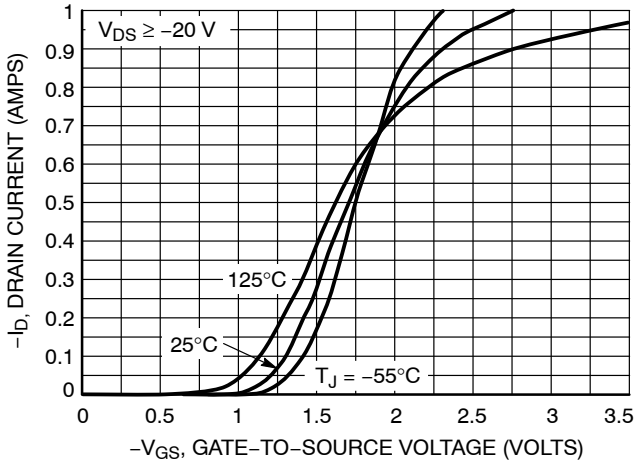


Figure 2. Transfer Characteristics

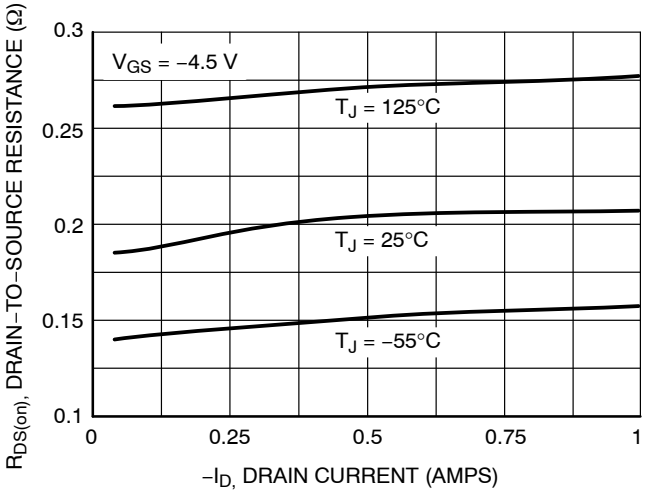


Figure 3. On−Resistance vs. Drain Current and Temperature

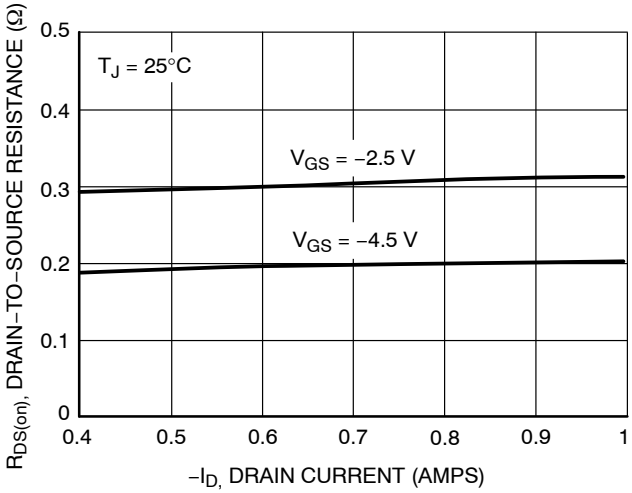


Figure 4. On−Resistance vs. Drain Current and Gate Voltage

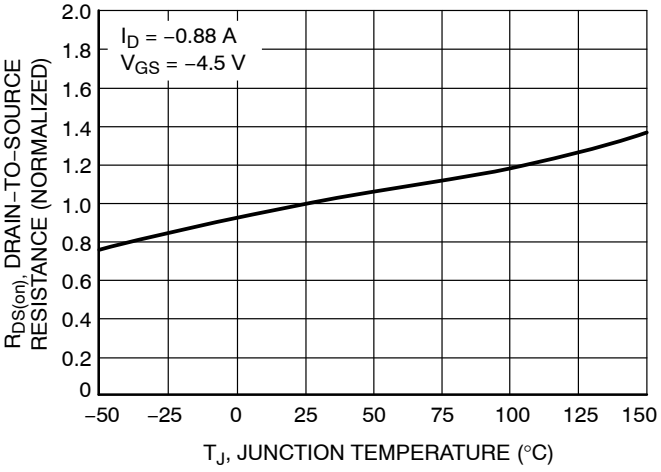


Figure 5. On−Resistance Variation with Temperature

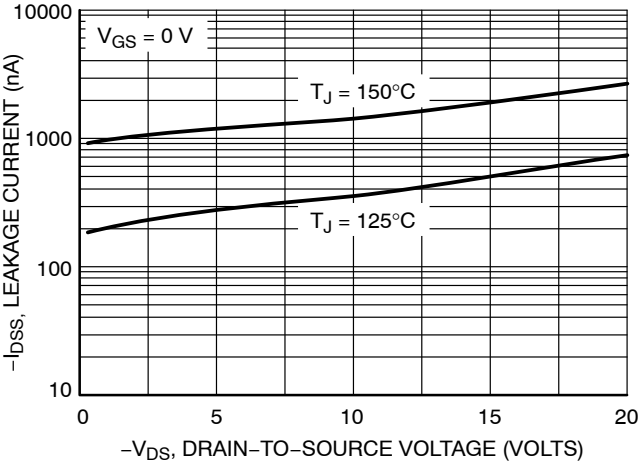


Figure 6. Drain−to−Source Leakage Current vs. Voltage

TYPICAL P−CHANNEL PERFORMANCE CURVES (T_J = 25°C unless otherwise noted)

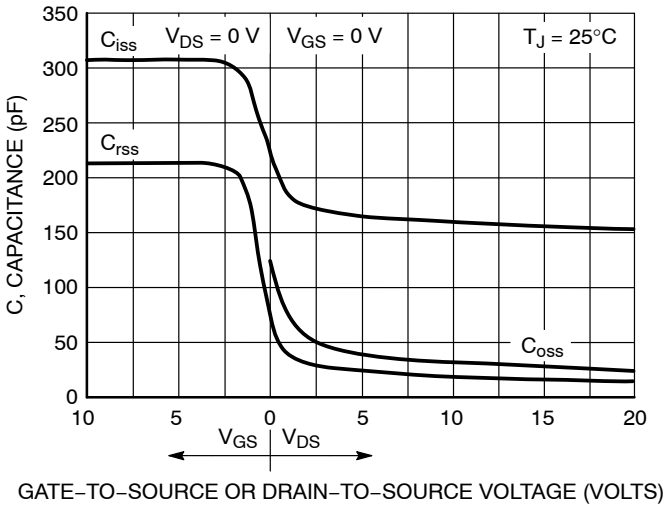


Figure 7. Capacitance Variation

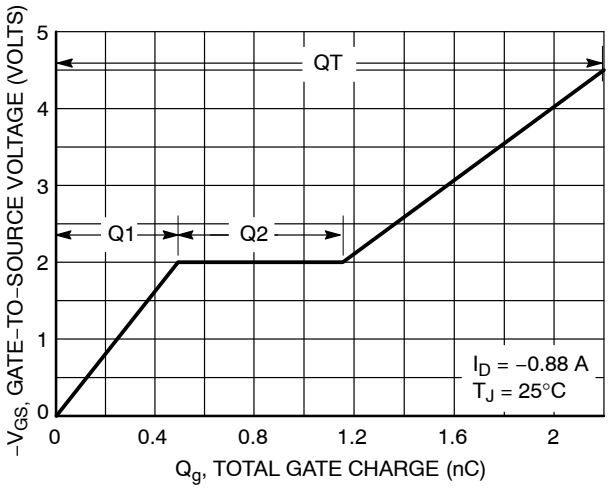


Figure 8. Gate−to−Source Voltage vs. Total Gate Charge

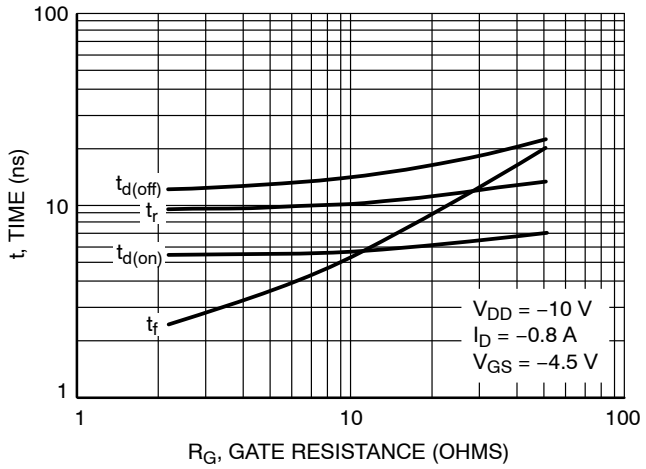


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

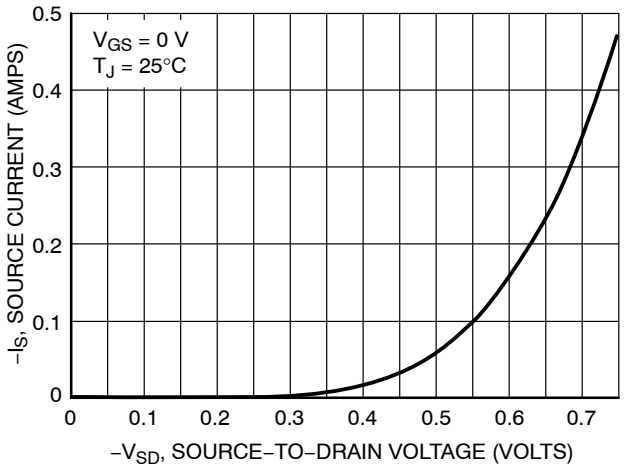


Figure 10. Diode Forward Voltage vs. Current

ORDERING INFORMATION

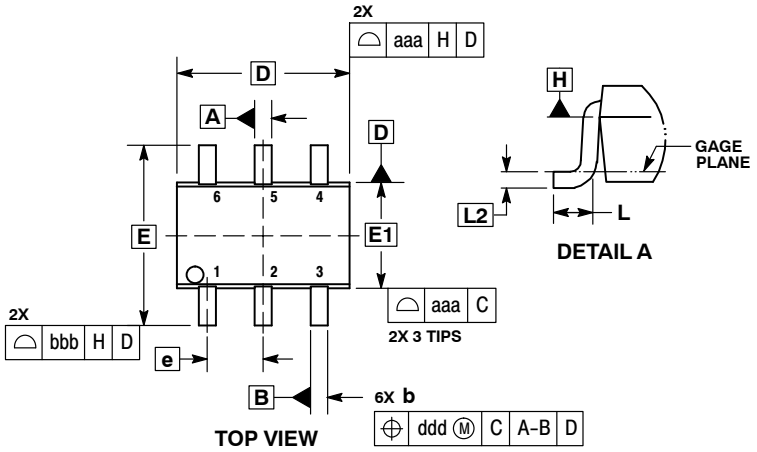
Device	Marking	Package	Shipping†
NTJD4158CT1G	TCD	SC−88 (Pb−Free)	3000 / Tape & Reel
NTJD4158CT2G	TCD		
NVJD4158CT1G*	VCD		

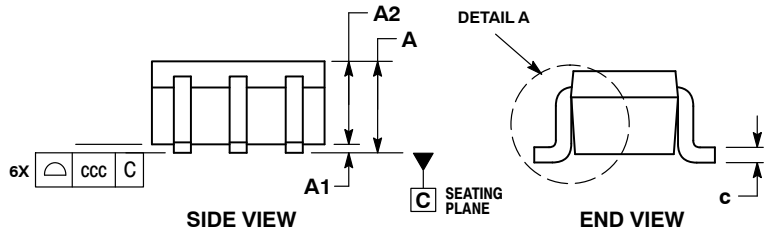
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*NV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q101 Qualified and PPAP Capable.

PACKAGE DIMENSIONS

SC−88/SC70−6/SOT−363
CASE 419B−02
ISSUE Y



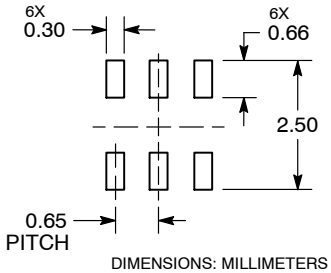


NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.20 PER END.
4. DIMENSIONS D AND E1 AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY AND DATUM H.
5. DATUMS A AND B ARE DETERMINED AT DATUM H.
6. DIMENSIONS b AND c APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.08 AND 0.15 FROM THE TIP.
7. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 TOTAL IN EXCESS OF DIMENSION b AT MAXIMUM MATERIAL CONDITION. THE DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT.

	MILLIMETERS			INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
A	---	---	1.10	---	---	0.043
A1	0.00	---	0.10	0.000	---	0.004
A2	0.70	0.90	1.00	0.027	0.035	0.039
b	0.15	0.20	0.25	0.006	0.008	0.010
C	0.08	0.15	0.22	0.003	0.006	0.009
D	1.80	2.00	2.20	0.070	0.078	0.086
E	2.00	2.10	2.20	0.078	0.082	0.086
E1	1.15	1.25	1.35	0.045	0.049	0.053
e	0.65 BSC			0.026 BSC		
L	0.26	0.36	0.46	0.010	0.014	0.018
L2	0.15 BSC			0.006 BSC		
aaa	0.15			0.006		
bbb	0.30			0.012		
ccc	0.10			0.004		
ddd	0.10			0.004		

STYLE 26:
PIN 1. SOURCE 1
2. GATE 1
3. DRAIN 2
4. SOURCE 2
5. GATE 2
6. DRAIN 1

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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