# UCC23511 1.5-A Source, 2-A Sink, 5.7-kV$_{RMS}$ Opto-Compatible Single-Channel Isolated Gate Driver

## 1 Features

- 5.7-kV$_{RMS}$ single channel isolated gate driver with opto-compatible input
- Pin-to-pin, drop in upgrade for opto isolated gate drivers
- 1.5-A source / 2-A sink, peak output current
- 14-V to 33-V output driver supply voltage
- Rail-to-rail output
- 105-ns (maximum) propagation delay
- 25-ns (maximum) part-to-part delay matching
- 35-ns (maximum) pulse width distortion
- 150-kV/μs (minimum) common-mode transient immunity (CMTI)
- Isolation barrier life >50 Years
- 13-V reverse polarity voltage handling capability on input stage
- Stretched SO-6 package with >8.5-mm creepage and clearance
- Operating junction temperature, $T_J$: –40°C to +150°C
- Safety-related certifications:
  - 5.7-kV$_{RMS}$ isolation for 1 minute per UL 1577
  - 8000-V$_{PK}$reinforced isolation per DIN V VDE V0884-11: 2017-01 (planned)
  - CQC certification per GB4943.1-2011 (planned)

## 2 Applications

- Industrial motor-control drives
- Industrial power supplies, UPS
- Solar inverters
- Induction heating

## 3 Description

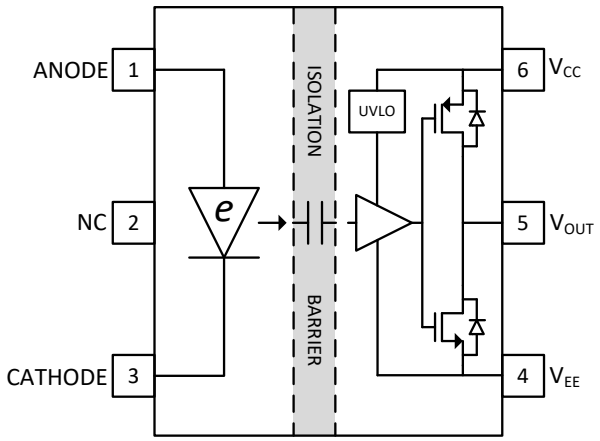
The UCC23511 is an Opto-compatible, single-channel, isolated gate driver for IGBTs, MOSFETs and SiC MOSFETs, with 1.5-A source and 2-A sink peak output current and 5.7-kV$_{RMS}$ reinforced isolation rating. The high supply voltage range of 33-V allows the use of bipolar supplies to effectively drive IGBTs and SiC power FETs. UCC23511 can drive both low side and high side power FETs. Key features and characteristics bring significant performance and reliability upgrades over standard opto-coupler based gate drivers while maintaining pin-to-pin compatibility in both schematic and layout design. Performance highlights include high common mode transient immunity (CMTI), low propagation delay, and small pulse width distortion. Tight process control results in small part-to-part skew. The input stage is an emulated diode (ediode) which means long term reliability and excellent aging characteristics compared to traditional LEDs. It is offered in a stretched SO6 package with >8.5mm creepage and clearance, and a mold compound from material group I which has a comparative tracking index (CTI) >600V. UCC23511's high performance and reliability makes it ideal for use in all types of motor drives, solar inverters, industrial power supplies, and appliances. The higher operating temperature opens up opportunities for applications not previously able to be supported by traditional optocouplers.

**Device Information**(1)

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|---|---|---|
| UCC23511 | Stretched SO-6 | 7.5 mm x 4.68 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.

**Functional Block Diagram of UCC23511 (SO6)**




An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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## 4 Revision History

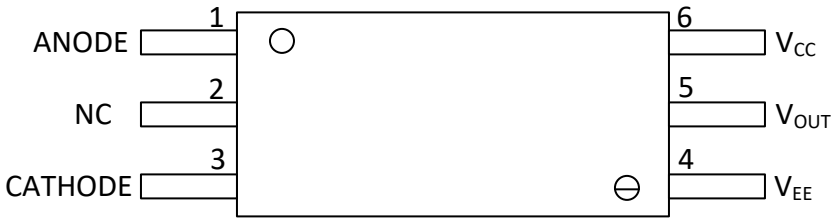
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Original (September 2019) to Revision A | Page |
|---|---|
| • Changed marketing status from Advance Information to Initial Release | 1 |


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# 5 Pin Configuration and Function

**UCC23511 Package**
**SO-6**
**Top View**




**Pin Functions**

| PIN | | TYPE(1) | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| | UCC23511 | | |
| ANODE | 1 | I | Anode |
| CATHODE | 3 | I | Cathode |
| NC | 2 | - | No Connection |
| $V_{CC}$ | 6 | P | Positive output supply rail |
| $V_{EE}$ | 4 | P | Negative output supply rail |
| $V_{OUT}$ | 5 | O | Gate-drive output |

(1) P = Power, G = Ground, I = Input, O = Output

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# 6 Specifications

## 6.1 Absolute Maximum Ratings

Over operating free air temperature range (unless otherwise noted)(1)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| Average Input Current | $I_{F(AVG)}$ | - | 25 | mA |
| Peak Transient Input Current | $I_{F(TRAN)}$ <1us pulse, 300pps | | 1 | A |
| Reverse Input Voltage | $V_{R(MAX)}$ | | 14 | V |
| Output supply voltage | $V_{CC} – V_{EE}$ | -0.3 | 35 | V |
| Output signal voltage | $V_{OUT} – V_{CC}$ | | 0.3 | V |
| Output signal voltage | $V_{OUT} – V_{EE}$ | -0.3 | | V |
| Junction temperature | $T_J$(2) | -40 | 150 | °C |
| Storage temperature | $T_{stg}$ | -65 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) To maintain the recommended operating conditions for $T_J$, see the *Thermal Information* section.

## 6.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS–001(1) | ±4000 | V |
| | | Charged device model (CDM), per JEDEC specification JESD22-C101(2) | ±1000 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 6.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Output Supply Voltage($V_{CC} – V_{EE}$) | 14 | | 33 | V |
| $I_F$ (ON) | Input Diode Forward Current (Diode "ON") | 7 | | 16 | mA |
| $V_F$ (OFF) | Anode voltage - Cathode voltage (Diode "OFF") | -13 | | 0.9 | V |
| $T_J$ | Junction temperature | -40 | | 150 | °C |
| $T_A$ | Ambient temperature | -40 | | 125 | °C |

## 6.4 Thermal Information

| THERMAL METRIC(1) | | UCC23511 SO6 6 Pins | UNIT |
|---|---|---|---|
| $R_{qJA}$ | Junction-to-ambient thermal resistance | 126 | °C/W |
| $R_{qJC(top)}$ | Junction-to-case (top) thermal resistance | 66.1 | °C/W |
| $R_{qJB}$ | Junction-to-board thermal resistance | 62.8 | °C/W |
| $Y_{JT}$ | Junction-to-top characterization parameter | 29.6 | °C/W |
| $Y_{JB}$ | Junction-to-board characterization parameter | 60.8 | °C/W |

(1) For more information about traditional and new thermal metrics, see the http://www.ti.com/lit/SPRA953 application report.


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## 6.5 Power Ratings

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $P_D$ | Maximum power dissipation on input and output | $V_{CC}$ = 20 V, $I_F$= 10mA 10-kHz, 50% duty cycle, square wave,180-nF load, $T_A$=25°C | | | 750 | mW |
| $P_{D1}$ | Maximum input power dissipation(1) | | | | 10 | mW |
| $P_{D2}$ | Maximum output power dissipation | | | | 740 | mW |

(1) Recommended maximum PD1 = 40mW. Absolute maximum PD1 = 55mW

## 6.6 Insulation Specifications

| PARAMETER | | TEST CONDITIONS | SPECIFICATION | UNIT |
|---|---|---|---|---|
| CLR | External clearance(1) | Shortest terminal-to-terminal distance through air | >8.5 | mm |
| CPG | External Creepage(1) | Shortest terminal-to-terminal distance across the package surface | >8.5 | mm |
| DTI | Distance through the insulation | Minimum internal gap (internal clearance) | >17 | µm |
| CTI | Comparative tracking index | DIN EN 60112 (VDE 0303-11); IEC 60112 | >600 | V |
| | Material Group | According to IEC 60664-1 | I | |
| | Overvoltage category per IEC 60664-1 | Rated mains voltage ≤ 600 $V_{RMS}$ | I-IV | |
| | | Rated mains voltage ≤ 1000 $V_{RMS}$ | I-III | |
| **DIN V VDE 0884-11 (VDE V 0884-11)** | | | | |
| $V_{IORM}$ | Maximum repetitive peak isolation voltage | AC voltage (bipolar) | 1500 | $V_{PK}$ |
| $V_{IOWM}$ | Maximum isolation working voltage | AC voltage (sine wave); time-dependent dielectric breakdown (TDDB) test; see Figure 1 | 1060 | $V_{RMS}$ |
| | | DC voltage | 1500 | $V_{DC}$ |
| $V_{IOTM}$ | Maximum transient isolation voltage | $V_{TEST} = V_{IOTM}$, t = 60 sec (qualification)<br>$V_{TEST} = 1.2 \times V_{IOTM}$, t = 1 s (100% production) | 8000 | $V_{PK}$ |
| $V_{IOSM}$ | Maximum surge isolation voltage(2) | Test method per IEC 62368, 1.2/50 ms waveform,<br>$V_{TEST} = 1.6 \times V_{IOSM} = 12800\ V_{PK}$ (qualification) | 8000 | $V_{PK}$ |
| $q_{pd}$ | Apparent charge(3) | Method a: After I/O safety test subgroup 2/3, $V_{ini} = V_{IOTM}$, $t_{ini}$ = 60 s; $V_{pd(m)} = 1.2 \times V_{IORM} = 1800\ V_{PK}$, $t_m$ = 10 s | ≤5 | pC |
| | | Method a: After environmental tests subgroup 1, $V_{ini} = V_{IOTM}$, $t_{ini}$ = 60 s; $V_{pd(m)} = 1.6 \times V_{IORM} = 2400\ V_{PK}$, $t_m$ = 10 s | ≤5 | |
| | | Method b1: At routine test (100% production) and preconditioning (type test), $V_{ini} = V_{IOTM}$, $t_{ini}$ = 1 s; $V_{pd(m)} = 1.875 \times V_{IORM} = 2813\ V_{PK}$, $t_m$ = 1 s | ≤5 | |
| $C_{IO}$ | Barrier capacitance, input to output(4) | $V_{IO}$ = 0.4 x sin (2πft), f = 1 MHz | 0.5 | pF |
| $R_{IO}$ | Insulation resistance, input to output(4) | $V_{IO}$ = 500 V, $T_A$ = 25°C | $>10^{12}$ | Ω |
| | | $V_{IO}$ = 500 V, 100°C ≤ $T_A$ ≤ 125°C | $>10^{11}$ | |
| | | $V_{IO}$ = 500 V at $T_S$ = 150°C | $>10^{9}$ | |
| | Pollution degree | | 2 | |
| | Climatic category | | 40/125/21 | |
| **UL 1577** | | | | |
| $V_{ISO}$ | Withstand isolation voltage | $V_{TEST} = V_{ISO} = 5700\ V_{RMS}$, t = 60 s (qualification),<br>$V_{TEST} = 1.2 \times V_{ISO} = 6840\ V_{RMS}$, t = 1 s (100% production) | 5700 | $V_{RMS}$ |

(1) Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance. Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves, ribs, or both on a printed-circuit board are used to help increase these specifications.
(2) Testing is carried out in air or oil to determine the intrinsic surge immunity of the isolation barrier.
(3) Apparent charge is electrical discharge caused by a partial discharge (pd).
(4) All pins on each side of the barrier tied together creating a two-pin device.


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## 6.7 Safety-Related Certifications

| VDE | UL | CQC |
|---|---|---|
| Plan to certify according to DIN V VDE V 0884-11: 2017-01 | Plan to certify according to UL 1577 Component Recognition Program | Plan to certify according to GB4943.1-2011 |
| Reinforced insulation Maximum transient isolation voltage, 8000 $V_{PK}$; Maximum repetitive peak isolation voltage, 1500 $V_{PK}$; Maximum surge isolation voltage, 8000 $V_{PK}$ | Single protection, 5700 $V_{RMS}$ | Reinforced insulation, Altitude ≤ 5000 m, Tropical Climate |
| Certificate planned | File number: E181974 | Certificate planned |

## 6.8 Safety Limiting Values

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $I_S$ | Safety input, output, or supply current | $R_{qJA}$ = 126°C/W, $V_I$ = 15 V, $T_J$ = 150°C, $T_A$ = 25°C | | | 50 | mA |
| | | $R_{qJA}$ = 126°C/W, $V_I$ = 30 V, $T_J$ = 150°C, $T_A$ = 25°C | | | 25 | |
| $P_S$ | Safety input, output, or total power | $R_{qJA}$ = 126°C/W, $T_J$ = 150°C, $T_A$ = 25°C | | | 750 | mW |
| $T_S$ | Maximum safety temperature(1) | | | | 150 | °C |

(1) The maximum safety temperature, $T_S$, has the same value as the maximum junction temperature, $T_J$ , specified for the device. The $I_S$ and $P_S$ parameters represent the safety current and safety power respectively. The maximum limits of $I_S$ and $P_S$ should not be exceeded. These limits vary with the ambient temperature, $T_A$. The junction-to-air thermal resistance, $R_{qJA}$, in the Thermal Information table is that of a device installed on a high-K test board for leaded surface-mount packages. Use these equations to calculate the value for each parameter: $T_J = T_A + R_{qJA} \times P$, where P is the power dissipated in the device. $T_{J(max)} = T_S = T_A + R_{qJA} \times P_S$, where $T_{J(max)}$ is the maximum allowed junction temperature. $P_S = I_S \times V_I$ , where VI is the maximum supply voltage.

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## 6.9 Electrical Characteristics

Unless otherwise noted, all typical values are at $T_A$ = 25°C, $V_{CC}$–$V_{EE}$= 15V, $V_{EE}$= GND. All min and max specifications are at recommended operating conditions ($T_J$ = -40C to 150°C, $I_{F(on)}$= 7 mA to 16 mA, $V_{EE}$= GND, $V_{CC}$= 15 V to 30 V, $V_{F(off)}$= –5V to 0.8V)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **INPUT** | | | | | | |
| $I_{FLH}$ | Input Forward Threshold Current Low to High | $V_{OUT}$ > 5 V, Cg = 1 nF | 1.5 | 2.8 | 4 | mA |
| $V_F$ | Input Forward Voltage | $I_F$ =10 mA | 1.8 | 2.1 | 2.4 | V |
| $V_{F_HL}$ | Threshold Input Voltage High to Low | V < 5 V, Cg = 1 nF | 0.9 | | | V |
| $\Delta V_F/\Delta T$ | Temp Coefficient of Input Forward Voltage | $I_F$ =10 mA | | 1 | 1.35 | mV/ºC |
| $V_R$ | Input Reverse Breakdown Voltage | $I_R$= 10 uA | 15 | | | V |
| $C_{IN}$ | Input Capacitance | F = 0.5 MHz | | 15 | | pF |
| **OUTPUT** | | | | | | |
| $I_{OH}$ | High Level Peak Output Current | $I_F$ = 10 mA, $V_{CC}$ =15V, $C_{LOAD}$=0.18uF, $R_{G_total}$=6Ω(1), $C_{VDD}$=10uF, Pulse width <10us | 1 | 1.5 | | A |
| $I_{OL}$ | Low Level Peak Output Current | $V_F$= 0 V, $V_{CC}$ =15V, $C_{LOAD}$=0.18uF, $R_{G_total}$=6Ω(1), $C_{VDD}$=10uF, Pulse width <10us | 1 | 2.0 | | A |
| $V_{OH}$ | High Level Output Voltage | $I_F$ = 10 mA, $I_O$= -20mA (with respect to VCC) | 0.07 | 0.18 | 0.36 | V |
| | | $I_F$ = 10 mA, $I_O$= 0 mA | | VCC | | V |
| $V_{OL}$ | Low Level Output Voltage | $V_F$ = 0 V, $I_O$= 20 mA | | | 25 | mV |
| $I_{CC_H}$ | Output Supply Current (Diode On) | $I_F$ = 10 mA, $I_O$= 0 mA | | | 2.2 | mA |
| $I_{CC_L}$ | Output Supply Current (Diode Off) | $V_F$ = 0 V, $I_O$= 0 mA | | | 2 | mA |
| **UNDER VOLTAGE LOCKOUT** | | | | | | |
| $UVLO_R$ | Under Voltage Lockout VCC rising | $V_{CC_Rising}$, $I_F$=10 mA | 11 | 12.5 | 13.5 | V |
| $UVLO_F$ | Under Voltage Lockout VCC falling | $V_{CC_Falling}$, $I_F$=10 mA | 10 | 11.5 | 12.5 | V |
| $UVLO_{HYS}$ | UVLO Hysteresis | | | 1.0 | | V |

(1) $R_{G_total}$ is the total gate resistance. It includes the external gate resistor on the PCB + the internal gate resistance of the power switch. Min $R_{G_total}$ of 4Ω is recommended (for $V_{CC}$-$V_{EE}$ =15V). For more details, refer to section 9 (Application and Implementation) of this datasheet.

## 6.10 Switching Characteristics

Unless otherwise noted, all typical values are at $T_A$ = 25°C, $V_{CC}$-$V_{EE}$= 30 V, $V_{EE}$= GND. All min and max specifications are at recommended operating conditions ($T_J$ = -40 to 150°C, $I_{F(ON)}$= 7 mA to 16 mA, $V_{EE}$= GND, $V_{CC}$= 15 V to 30 V, $V_{F(OFF)}$= –5V to 0.8V)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_r$ | Output-signal Rise Time | Cg = 1nF<br>$F_{SW}$ = 20 kHz, (50% Duty Cycle)<br>VCC=15V | | | 28 | ns |
| $t_f$ | Output-signal Fall Time | | | | 25 | ns |
| $t_{PLH}$ | Propagation Delay, Low to High | | | 70 | 105 | ns |
| $t_{PHL}$ | Propagation Delay, High to Low | | | 70 | 105 | ns |
| $t_{PWD}$ | Pulse Width Distortion $\lvert t_{PHL} - t_{PLH} \rvert$ | | | | 35 | ns |
| $t_{sk(pp)}$ | Part-to-Part Skew in Propagation Delay Between any Two Parts(1) | Cg = 1nF<br>$F_{SW}$ = 20 kHz, (50% Duty Cycle)<br>VCC=15V, $I_F$=10mA | | | 25 | ns |
| $t_{UVLO_rec}$ | UVLO Recovery Delay | $V_{CC}$ Rising from 0V to 15V | | 20 | 30 | µs |

(1) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between the output of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads ensured by characterization.


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## Switching Characteristics (continued)

Unless otherwise noted, all typical values are at $T_A$ = 25°C, $V_{CC}$-$V_{EE}$= 30 V, $V_{EE}$= GND. All min and max specifications are at recommended operating conditions ($T_J$ = -40 to 150°C, $I_{F(ON)}$= 7 mA to 16 mA, $V_{EE}$= GND, $V_{CC}$= 15 V to 30 V, $V_{F(OFF)}$= –5V to 0.8V)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $CMTI_H$ | Common-mode Transient Immunity (Output High) | $I_F$ = 10 mA, $V_{CM}$ = 1500 V, $V_{CC}$= 30 V, $T_A$= 25ºC | 150 | | | kV/µs |
| $CMTI_L$ | Common-mode Transient Immunity (Output Low) | $V_F$ = 0 V, $V_{CM}$ = 1500 V, $V_{CC}$= 30 V, $T_A$= 25ºC | 150 | | | kV/µs |

## 6.11 Insulation Characteristics Curves

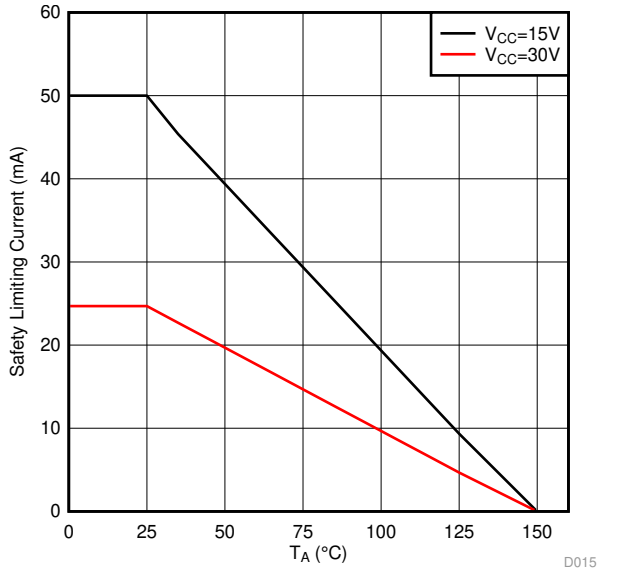



**Figure 1. Thermal Derating Curve for Limiting Current per VDE**

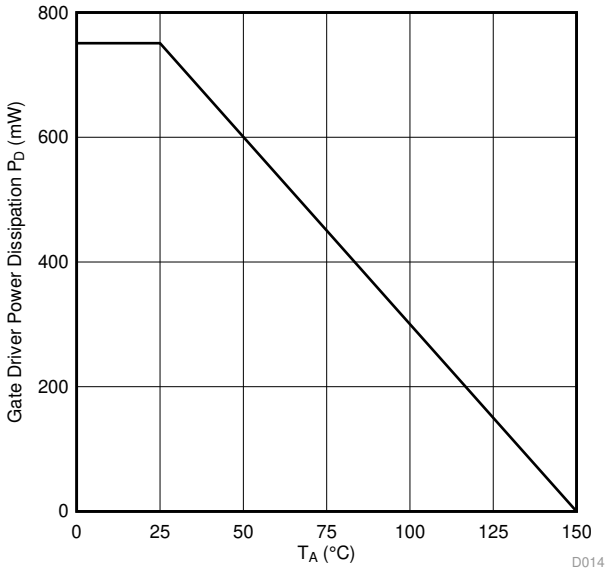



**Figure 2. Thermal Derating Curve for Limiting Power per VDE**

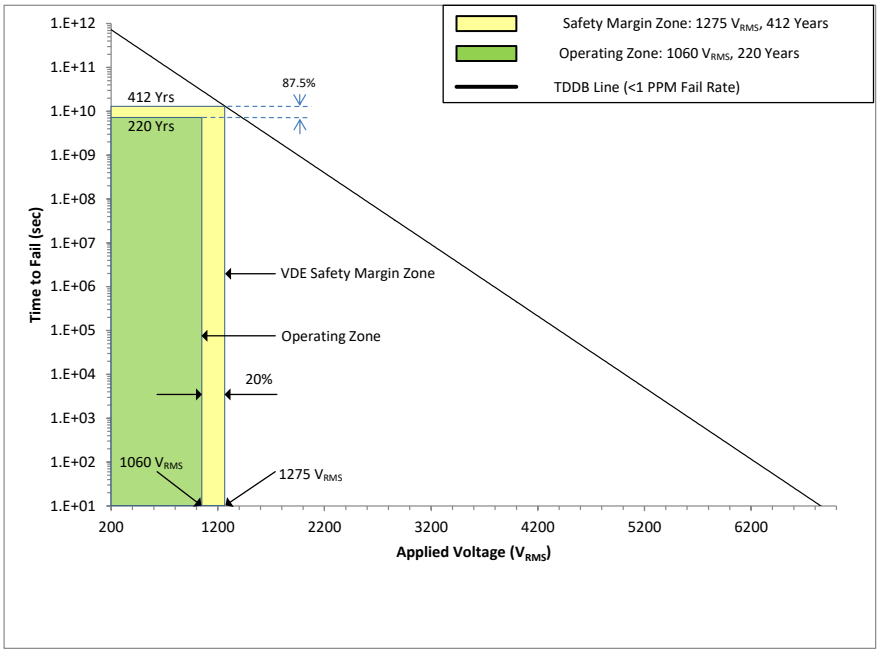



**Figure 3. Reinforced Isolation Capacitor Life Time Projection**

## 6.12 Typical Characteristics

$V_{CC}$= 15 V, 1-µF capacitor from $V_{CC}$ to $V_{EE}$, $C_{LOAD}$ = 1 nF for timing tests and 180nF for $I_{OH}$ and $I_{OL}$ tests, $T_J$ = –40°C to +150°C, (unless otherwise noted)

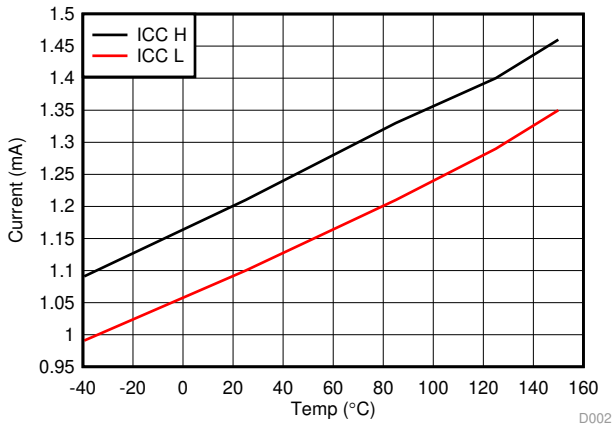



**Figure 4. Supply currents versus Temperature**

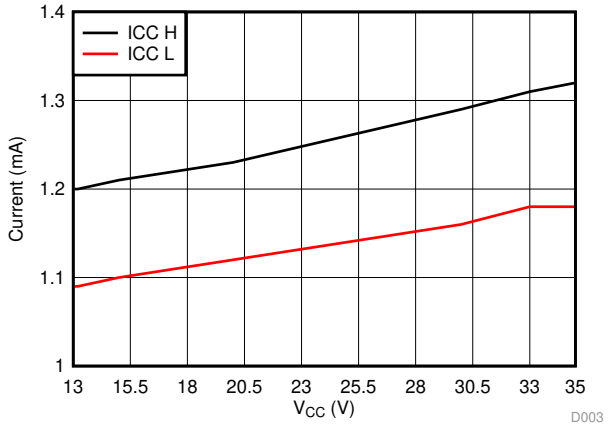



**Figure 5. Supply current versus Supply Voltage**

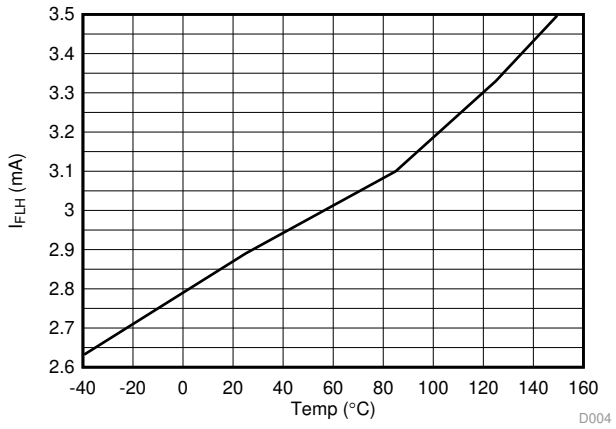



**Figure 6. Forward threshold current versus Temperature**

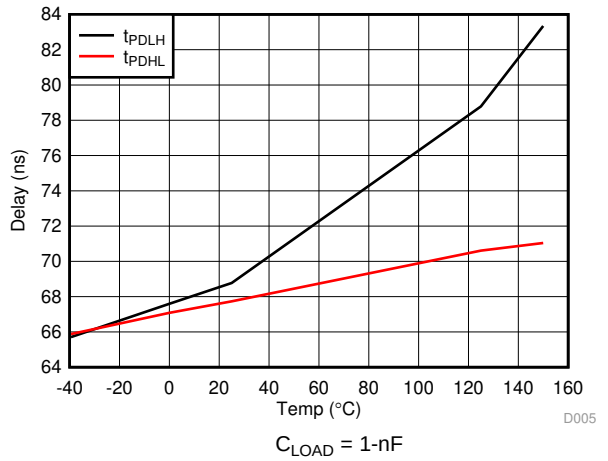



**Figure 7. Propagation delay versus Temperature**

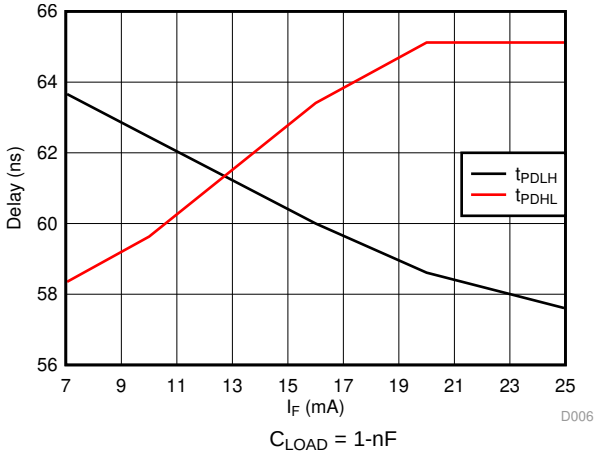



**Figure 8. Propagation delay versus Forward current**

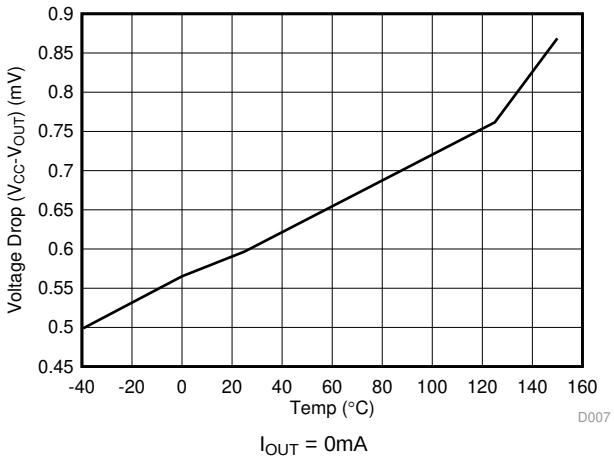
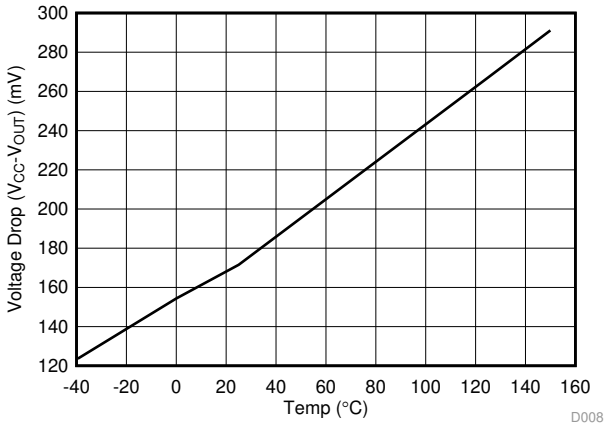



**Figure 9. $V_{OH}$ (No Load) versus Temperature**


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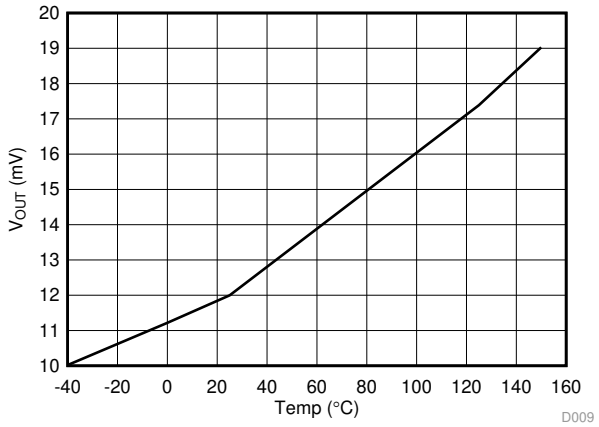
## Typical Characteristics (continued)

$V_{CC}$= 15 V, 1-µF capacitor from $V_{CC}$ to $V_{EE}$, $C_{LOAD}$ = 1 nF for timing tests and 180nF for $I_{OH}$ and $I_{OL}$ tests, $T_J$ = –40°C to +150°C, (unless otherwise noted)




$I_{OUT}$ = 20mA (sourcing)

**Figure 10. $V_{OH}$ (20mA Load) versus Temperature**




$I_{OUT}$ = 20mA (sinking)

**Figure 11. $V_{OL}$ versus Temperature**

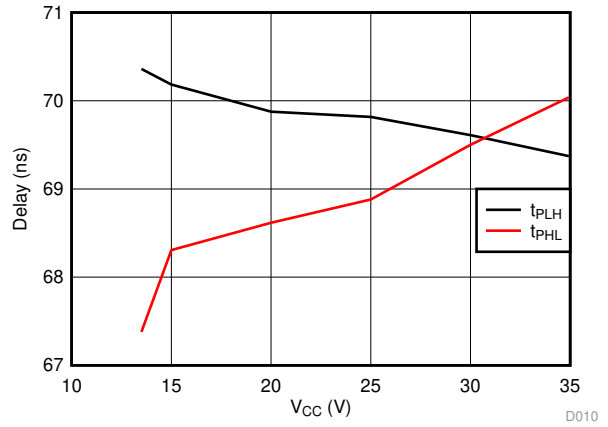



**Figure 12. Propagation delay versus Supply voltage**

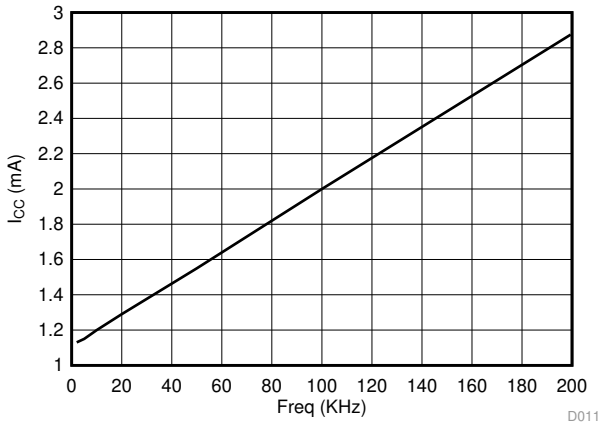
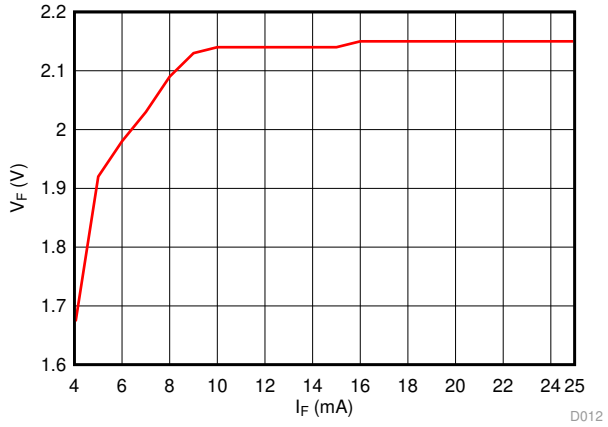
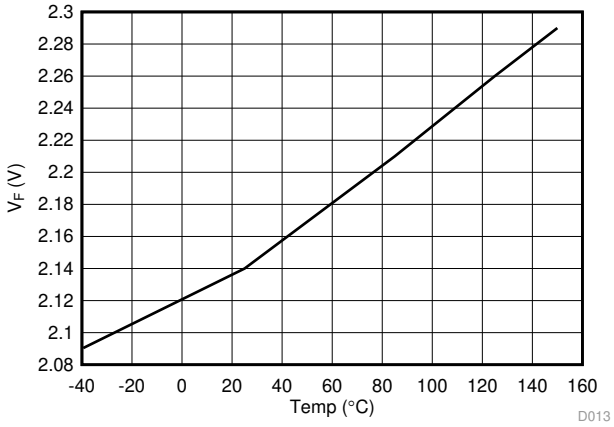



**Figure 13. Supply current versus Frequency**




$T_A$ = 25°C

**Figure 14. Forward current versus Forward voltage drop**




$I_F$ = 10mA

**Figure 15. Forward voltage drop versus Temperature**

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# 7 Parameter Measurement Information

## 7.1 Propagation Delay, rise time and fall time

Figure 16 shows the propagation delay from the input forward current $I_F$, to $V_{OUT}$. This figures also shows the circuit used to measure the rise ($t_r$) and fall ($t_f$) times and the propagation delays $t_{PDLH}$ and $t_{PDHL}$.

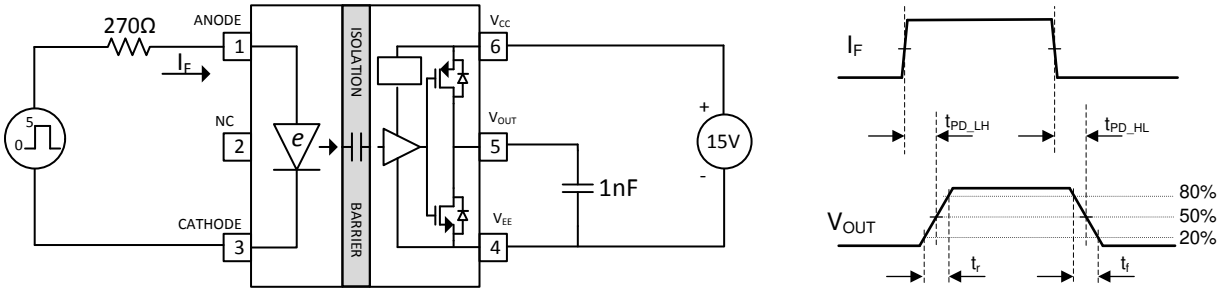



**Figure 16. $I_F$ to $V_{OUT}$ Propagation Delay, Rise Time and Fall Time**

## 7.2 $I_{OH}$ and $I_{OL}$ testing

Figure 17 shows the circuit used to measure the output drive currents $I_{OH}$ and $I_{OL}$. A series resistor of 6 Ω and a load capacitance of 180 nF are used at the output. The peak dv/dt of the capacitor voltage is measured in order to determine the peak source and sink currents of the gate driver.

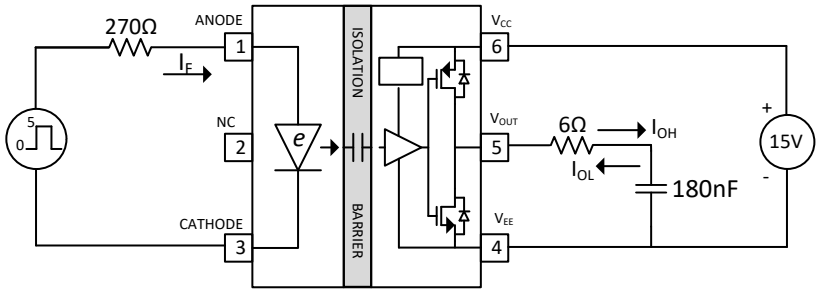



**Figure 17. $I_{OH}$ and $I_{OL}$**

## 7.3 CMTI Testing

Figure 18 is the simplified diagram of the CMTI testing. Common mode voltage is set to 1500V. The test is performed with $I_F$ = 6mA (VOUT= High) and $I_F$ = 0mA ($V_{OUT}$ = LOW). The diagram also shows the fail criteria for both cases. During the application on the CMTI pulse with $I_F$ = 6mA, if $V_{OUT}$ drops from VCC to ½VCC it is considered as a failure. With $I_F$= 0mA, if $V_{OUT}$ rises above 1V, it is considered as a failure.

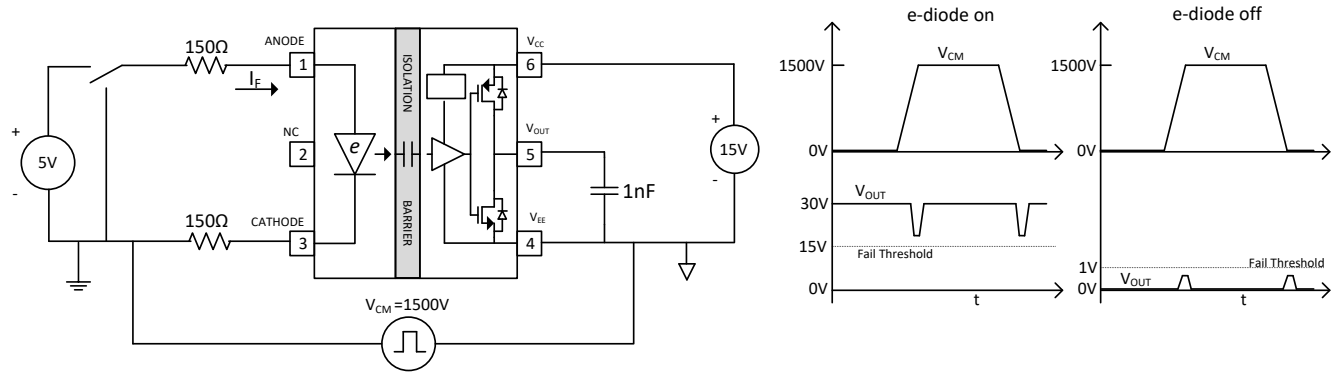



**Figure 18. CMTI Test Circuit for UCC23511**


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# 8 Detailed Description

## 8.1 Overview

UCC23511 is a single channel isolated gate driver, with an opto-compatible input stage, that can drive IGBTs, MOSFETs and SiC FETs. It has 1.5-A source and 2-A sink peak output current capability with max output driver supply voltage of 33V. The inputs and the outputs are galvanically isolated. UCC23511 is offered in an industry standard 6 pin (SO6) package with >8.5mm creepage and clearance. It has a working voltage of 1060-$V_{RMS}$, reinforced isolation rating of 5.7-$kV_{RMS}$ for 60s and a surge rating of 8-$kV_{PK}$. It is pin-to-pin compatible with standard opto isolated gate drivers. While standard opto isolated gate drivers use an LED as the input stage, UCC23511 uses an emulated diode (or "e-diode") as the input stage which does not use light emission to transmit signals across the isolation barrier. The input stage is isolated from the driver stage by dual, series HV $SiO_2$ capacitors in full differential configuration that not only provides reinforced isolation but also offers best-in-class common mode transient immunity of >150kV/us. The e-diode input stage along with capacitive isolation technology gives UCC23511 several performance advantages over standard opto isolated gate drivers. They are as follows:

1. Since the e-diode does not use light emission for its operation, the reliability and aging characteristics of UCC23511 are naturally superior to those of standard opto isolated gate drivers.
2. Higher ambient operating temperature range of 125°C, compared to only 105°C for most opto isolated gate drivers
3. The e-diode forward voltage drop has less part-to-part variation and smaller variation across temperature. Hence, the operating point of the input stage is more stable and predictable across different parts and operating temperature.
4. Higher common mode transient immunity than opto isolated gate drivers
5. Smaller propagation delay than opto isolated gate drivers
6. Due to superior process controls achievable in capacitive isolation compared to opto isolation, there is less part-to-part skew in the prop delay, making the system design simpler and more robust
7. Smaller pulse width distortion than opto isolated gate drivers

The signal across the isolation has an on-off keying (OOK) modulation scheme to transmit the digital data across a silicon dioxide based isolation barrier (see Figure 19). The transmitter sends a high-frequency carrier across the barrier to represent one digital state and sends no signal to represent the other digital state. The receiver demodulates the signal after advanced signal conditioning and produces the output through a buffer stage. The UCC23511 also incorporates advanced circuit techniques to maximize the CMTI performance and minimize the radiated emissions from the high frequency carrier and IO buffer switching. Figure 20 shows conceptual detail of how the OOK scheme works.

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## 8.2 Functional Block Diagram

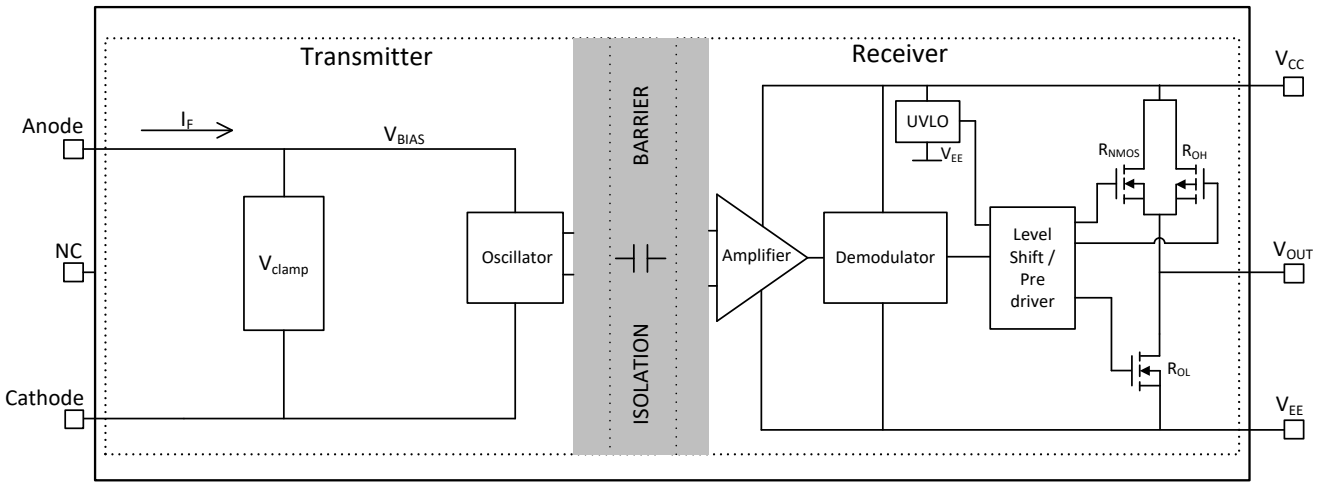



**Figure 19. Conceptual Block Diagram of a Isolated Gate Driver with an Opto Emulated Input Stage (SO6 pkg)**

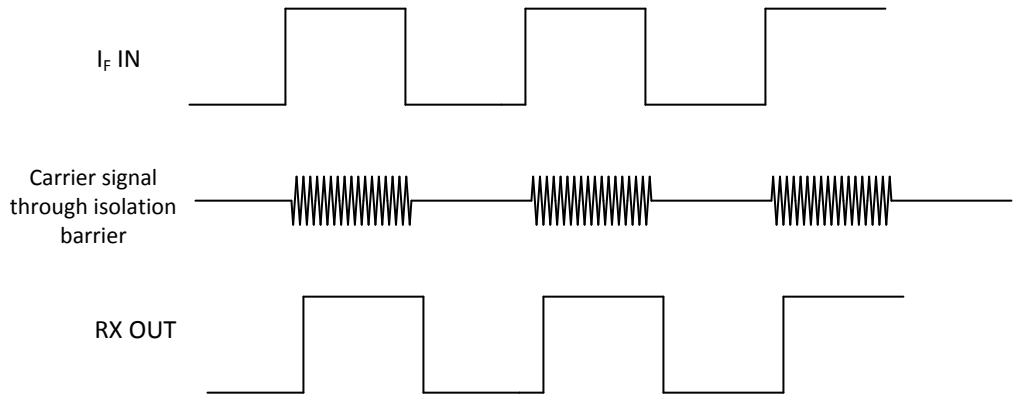



**Figure 20. On-Off Keying (OOK) Based Modulation Scheme**

## 8.3 Feature Description

### 8.3.1 Power Supply

Since the input stage is an emulated diode, no power supply is needed at the input.

The output supply, $V_{CC}$, supports a voltage range from 14V to 33V. For operation with bipolar supplies, the power device is turned off with a negative voltage on the gate with respect to the emitter or source. This configuration prevents the power device from unintentionally turning on because of current induced from the Miller effect. The typical values of the $V_{CC}$ and $V_{EE}$ output supplies for bipolar operation are 15V and -8V with respect to GND for IGBTs, and 20V and -5V for SiC MOSFETs.

For operation with unipolar supply, the $V_{CC}$ supply is connected to 15V with respect to GND for IGBTs, and 20V for SiC MOSFETs. The $V_{EE}$ supply is connected to 0V.


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## Feature Description (continued)

### 8.3.2 Input Stage

The input stage of UCC23511 is simply the e-diode and therefore has an Anode (Pin 1) and a Cathode (Pin 3). Pin 2 has no internal connection and can be left open or connected to ground. The input stage does not have a power and ground pin. When the e-diode is forward biased by applying a positive voltage to the Anode with respect to the Cathode, a forward current $I_F$ flows into the e-diode. The forward voltage drop across the e-diode is 2.1V (typ). An external resistor should be used to limit the forward current. The recommended range for the forward current is 7mA to 16mA. When $I_F$ exceeds the threshold current $I_{FLH}$(2.8mA typ.) a high frequency signal is transmitted across the isolation barrier through the high voltage $SiO_2$ capacitors. The HF signal is detected by the receiver and $V_{OUT}$ is driven high. See Selecting the Input Resistor for information on selecting the input resistor. The dynamic impedance of the e-diode is very small(<1.0Ω) and the temperature coefficient of the e-diode forward voltage drop is <1.35mV/°C. This leads to excellent stability of the forward current $I_F$ across all operating conditions. If the Anode voltage drops below $V_{F_HL}$ (0.9V), or reverse biased, the gate driver output is driven low. The reverse breakdown voltage of the e-diode is >15V. So for normal operation, a reverse bias of up to 13V is allowed. The large reverse breakdown voltage of the e-diode enables UCC23511 to be operated in interlock architecture (see example in Figure 21) where $V_{SUP}$ can be as high as 12V. The system designer has the flexibility to choose a 3.3V, 5.0V or up to 12V PWM signal source to drive the input stage of UCC23511 using an appropriate input resistor. The example shows two gate drivers driving a set of IGBTs. The inputs of the gate drivers are connected as shown and driven by two buffers that are controlled by the MCU. Interlock architecture prevents both the e-diodes from being "ON" at the same time, preventing shoot through in the IGBTs. It also ensures that if both PWM signals are erroneously stuck high (or low) simultaneously, both gate driver outputs will be driven low.

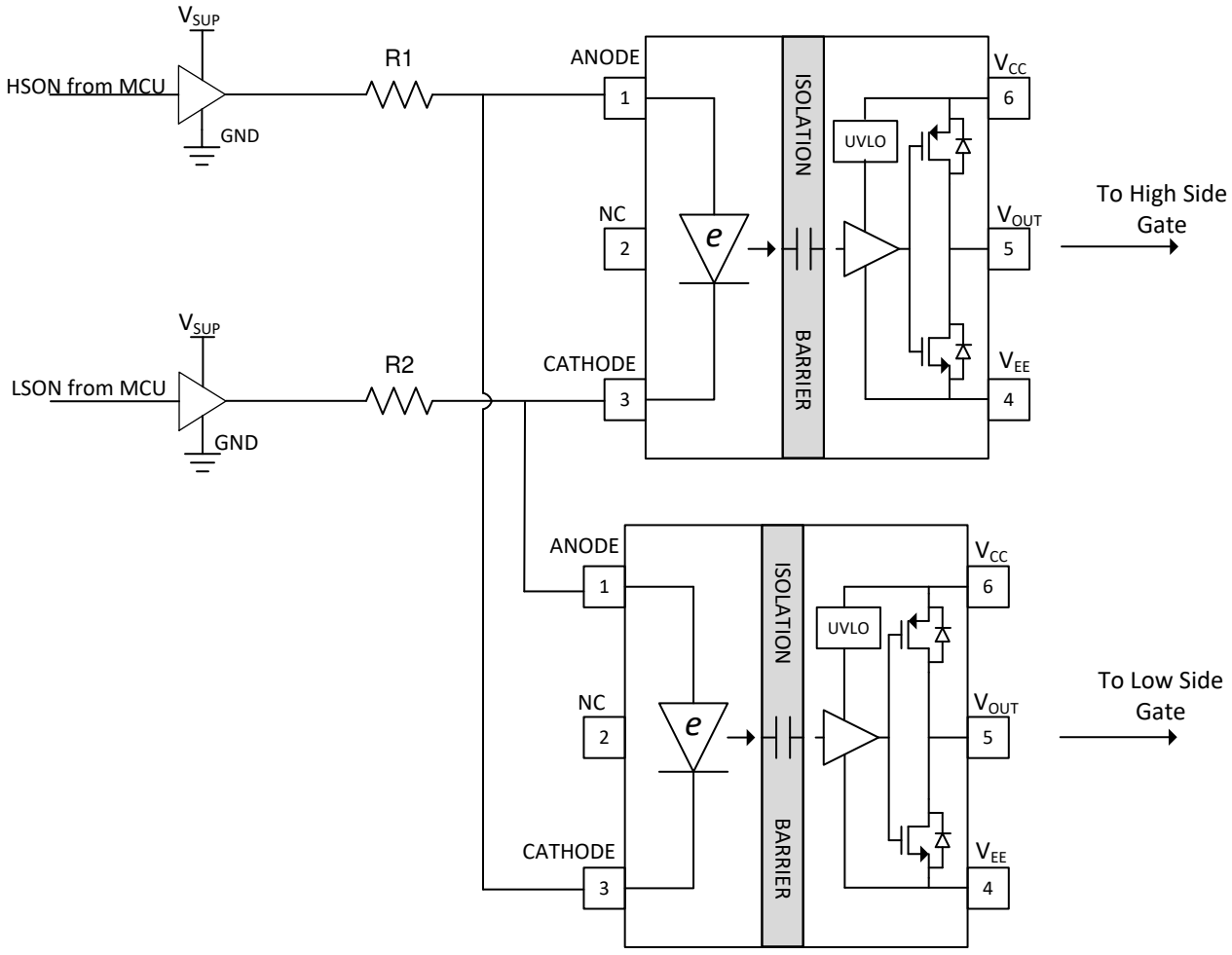



**Figure 21. Interlock**

## Feature Description (continued)

### 8.3.3 Output Stage

The output stages of the UCC23511 family feature a pullup structure that delivers the highest peak-source current when it is most needed which is during the Miller plateau region of the power-switch turnon transition (when the power-switch drain or collector voltage experiences dV/dt). The output stage pullup structure features a P-channel MOSFET and an additional pull-up N-channel MOSFET in parallel. The function of the N-channel MOSFET is to provide a brief boost in the peak-sourcing current, enabling fast turnon. Fast turnon is accomplished by briefly turning on the N-channel MOSFET during a narrow instant when the output is changing states from low to high. The on-resistance of this N-channel MOSFET ($R_{NMOS}$) is approximately 5.1 Ω when activated.

**Table 1. UCC23511 On-Resistance**

| $R_{NMOS}$ | $R_{OH}$ | $R_{OL}$ | UNIT |
|---|---|---|---|
| 5.1 | 9.5 | 0.40 | Ω |

The $R_{OH}$ parameter is a DC measurement and is representative of the on-resistance of the P-channel device only. This parameter is only for the P-channel device because the pullup N-channel device is held in the OFF state in DC condition and is turned on only for a brief instant when the output is changing states from low to high. Therefore, the effective resistance of the UCC23511 pullup stage during this brief turnon phase is much lower than what is represented by the $R_{OH}$ parameter, yielding a faster turn on. The turnon-phase output resistance is the parallel combination $R_{OH}$ || $R_{NMOS}$.

The pulldown structure in the UCC23511 is simply composed of an N-channel MOSFET. The output voltage swing between $V_{CC}$ and $V_{EE}$ provides rail-to-rail operation because of the MOS-out stage which delivers very low dropout.

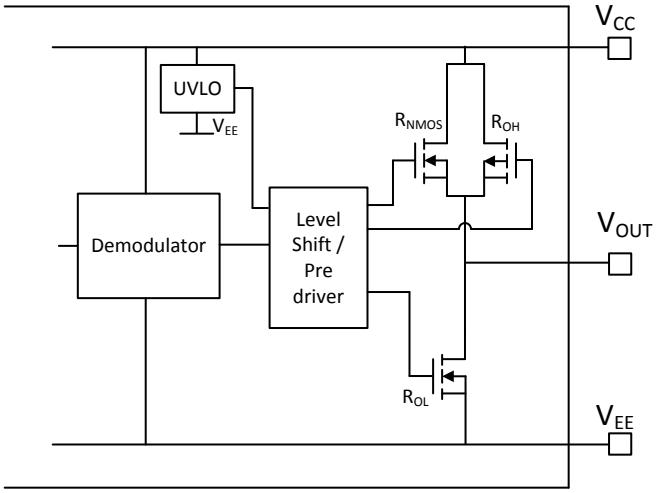



**Figure 22. Output Stage**

### 8.3.4 Protection Features

#### *8.3.4.1 Undervoltage Lockout (UVLO)*

UVLO function is implemented for $V_{CC}$ and $V_{EE}$ pins to prevent an under-driven condition on IGBTs and MOSFETs. When $V_{CC}$ is lower than $UVLO_R$ at device start-up or lower than $UVLO_F$ after start-up, the voltage-supply UVLO feature holds the effected output low, regardless of the input forward current as shown in Table 2. The $V_{CC}$ UVLO protection has a hysteresis feature ($UVLO_{hys}$). This hysteresis prevents chatter when the power supply produces ground noise which allows the device to permit small drops in bias voltage, which occurs when the device starts switching and operating current consumption increases suddenly.

When $V_{CC}$ drops below $UVLO_F$, a delay, $t_{UVLO_rec}$ occurs on the output when the supply voltage rises above $UVLO_R$ again.


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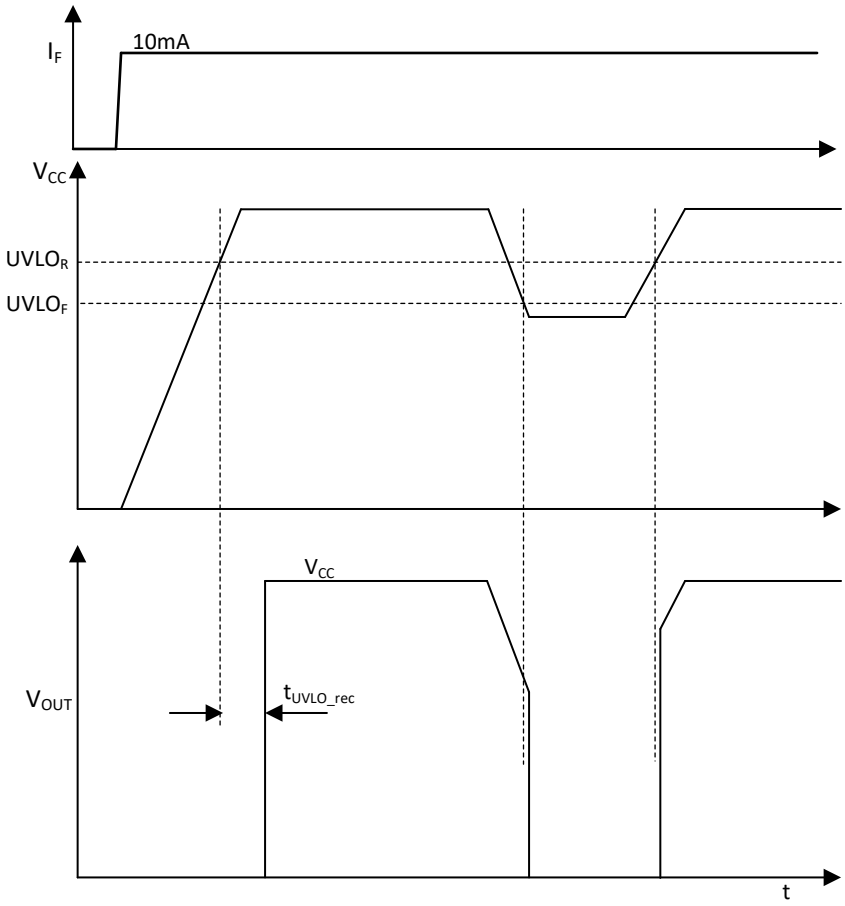



**Figure 23. UVLO functionality**

### *8.3.4.2 Active Pulldown*

The active pull-down function is used to pull the IGBT or MOSFET gate to the low state when no power is connected to the $V_{CC}$ supply. This feature prevents false IGBT and MOSFET turn-on by clamping $V_{OUT}$ pin to approximately 2V.

When the output stage of the driver is in an unbiased condition ($V_{CC}$ floating), the driver outputs (see Figure 22) are held low by an active clamp circuit that limits the voltage rise on the driver outputs. In this condition, the upper PMOS & NMOS are held off while the lower NMOS gate is tied to the driver output through an internal 500-kΩ resistor. In this configuration, the lower NMOS device effectively clamps the output ($V_{OUT}$) to less than 2V.

### *8.3.4.3 Short-Circuit Clamping*

The short-circuit clamping function is used to clamp voltages at the driver output and pull the output pin $V_{OUT}$ slightly higher than the $V_{CC}$ voltage during short-circuit conditions. The short-circuit clamping function helps protect the IGBT or MOSFET gate from overvoltage breakdown or degradation. The short-circuit clamping function is implemented by adding a diode connection between the dedicated pins and the $V_{CC}$ pin inside the driver. The internal diodes can conduct up to 500-mA current for a duration of 10 µs and a continuous current of 20 mA. Use external Schottky diodes to improve current conduction capability as needed.

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## 8.4 Device Functional Modes

Table 2 lists the functional modes for UCC23511

**Table 2. Function Table for UCC23511 with VCC Rising**

| e-diode | VCC | $V_{OUT}$ |
|---|---|---|
| OFF ($I_F$< $I_{FLH}$) | 0V - 33V | Low |
| ON ($I_F$> $I_{FLH}$) | 0V - $UVLO_R$ | Low |
| ON ( ($I_F$> $I_{FLH}$) | $UVLO_R$ - 33V | High |

**Table 3. Function Table for UCC23511 with VCC Falling**

| e-diode | VCC | $V_{OUT}$ |
|---|---|---|
| OFF ($I_F$< $I_{FLH}$) | 0V - 33V | Low |
| ON ($I_F$> $I_{FLH}$) | $UVLO_F$- 0V | Low |
| ON ( ($I_F$> $I_{FLH}$) | 33V - $UVLO_F$ | High |

### 8.4.1 ESD Structure

Figure 24 shows the multiple diodes involved in the ESD protection components of the UCC23511 device . This provides pictorial representation of the absolute maximum rating for the device.

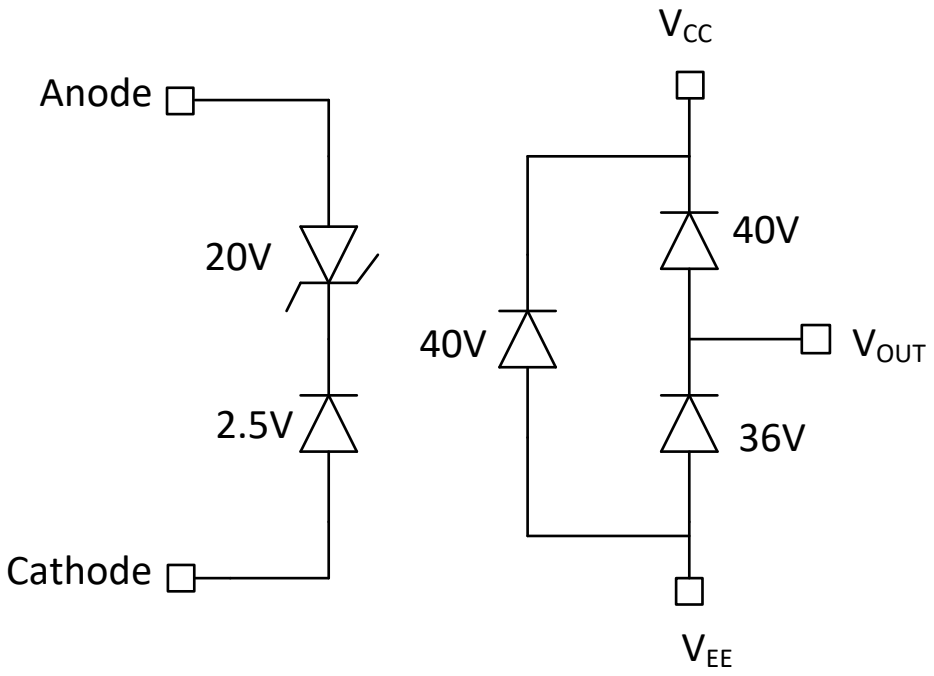



**Figure 24. ESD Structure**


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# 9 Application and Implementation

**NOTE**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 9.1 Application Information

UCC23511 is a single channel, isolated gate driver with opto-compatible input for power semiconductor devices, such as MOSFETs, IGBTs, or SiC MOSFETs. It is intended for use in applications such as motor control, industrial inverters, and switched-mode power supplies. It differs from standard opto isolated gate drivers as it does not have an LED input stage. Instead of an LED, it has an emulated diode (e-diode). To turn the e-diode "ON", a forward current in the range of 7mA to 16mA should be driven into the Anode. This will drive the gate driver output High and turn on the power FET. Typically, MCU's are not capable of providing the required forward current. Hence a buffer has to be used between the MCU and the input stage of UCC23511. Typical buffer power supplies are either 5V or 3.3V. A resistor is needed between the buffer and the input stage of UCC23511 to limit the current. It is simple, but important to choose the right value of resistance. The resistor tolerance, buffer supply voltage tolerance and output impedance of the buffer, have to be considered in the resistor selection. This will ensure that the e-diode forward current stays within the recommended range of 7mA to 16mA. Detailed design recommendations are given in the Application Information. The current driven input stage offers excellent noise immunity that is need in high power motor drive systems, especially in cases where the MCU cannot be located close to the isolated gate driver. UCC23511 offers best in class CMTI performance of >150kV/us at 1500V common mode voltages.

The e-diode is capable of 25mA continuous in the forward direction. The forward voltage drop of the e-diode has a very tight part to part variation (1.8V min to 2.4V max). The temperature coefficient of the forward drop is <1.35mV/°C. The dynamic impedance of the e-diode in the forward biased region is ~1Ω. All of these factors contribute in excellent stability of the e-diode forward current. To turn the e-diode "OFF", the Anode - Cathode voltage should be <0.8V, or $I_F$ should be $<I_{FLH}$. The e-diode can also be reverse biased up to 13V (14V abs max) in order to turn it off and bring the gate driver output low. The large reverse breakdown voltage of the input stage provides system designers the flexibility to drive the input stage with 12V PWM signals without the need for an additional clamping circuit on the Anode and Cathode pin.

The output power supply for UCC23511 can be as high as 33V (35V abs max). The output power supply can be configured externally as a single isolated supply up to 33V or isolated bipolar supply such that $V_{CC}$-$V_{EE}$ does not exceed 33V, or it can be bootstrapped (with external diode & capacitor) if the system uses a single power supply with respect to the power ground. Typical quiescent power supply current from $V_{CC}$ is 1.2mA (max 2.2mA).

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## 9.2 Typical Application

The circuit in Figure 25, shows a typical application for driving IGBTs.

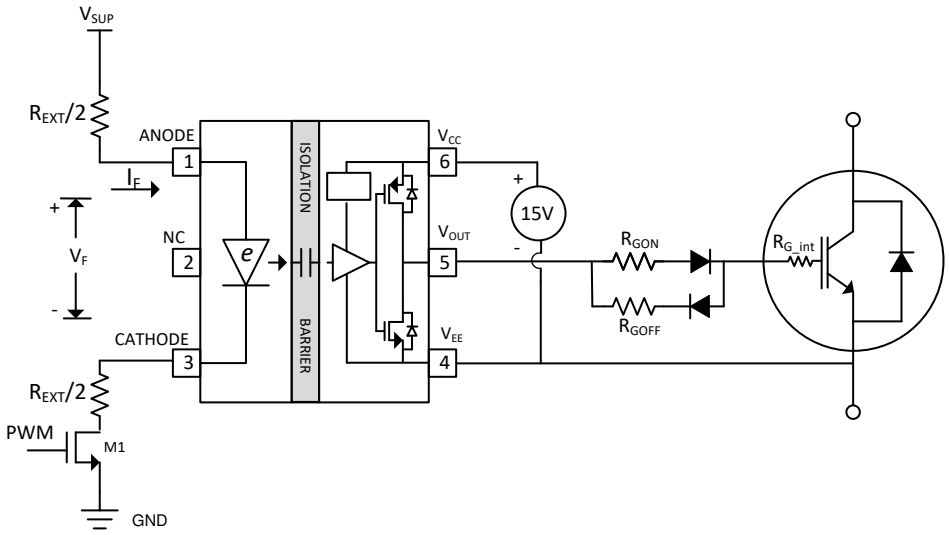



**Figure 25. Typical Application Circuit for UCC23511 to Drive IGBT**

### 9.2.1 Design Requirements

Table 4 lists the recommended conditions to observe the input and output of the UCC23511 gate driver.

**Table 4. UCC23511 Design Requirements**

| PARAMETER | VALUE | UNIT |
|---|---|---|
| $V_{CC}$ | 15 | V |
| $I_F$ | 10 | mA |
| Switching frequency | 8 | kHz |


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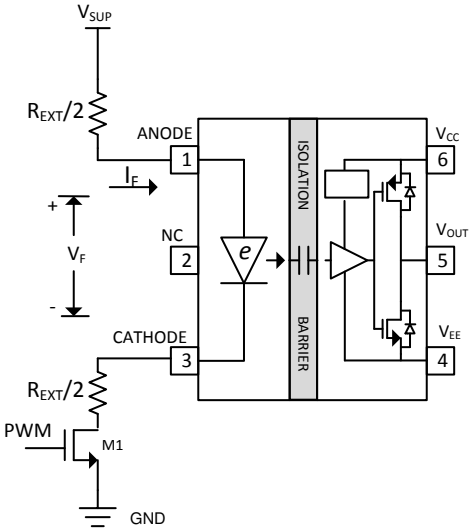
### 9.2.2 Detailed Design Procedure

#### *9.2.2.1 Selecting the Input Resistor*

The input resistor limits the current that flows into the e-diode when it is forward biased. The threshold current $I_{FLH}$ is 2.5mA typ. The recommended operating range for the forward current is 7mA to 16mA (e-diode ON). All the electrical specifications are guaranteed in this range. The resistor should be selected such that for typical operating conditions, $I_F$ is 10mA. Following are the list of factors that will affect the exact value of this current:

1. Supply Voltage $V_{SUP}$ variation
2. Manufacturer's tolerance for the resistor and variation due to temperature
3. e-diode forward voltage drop variation (at $I_F$=10mA, $V_F$= typ 2.1V, min 1.8V, max 2.4V, with a temperature coefficient <1.35mV/°C and dynamic impedance <1Ω)

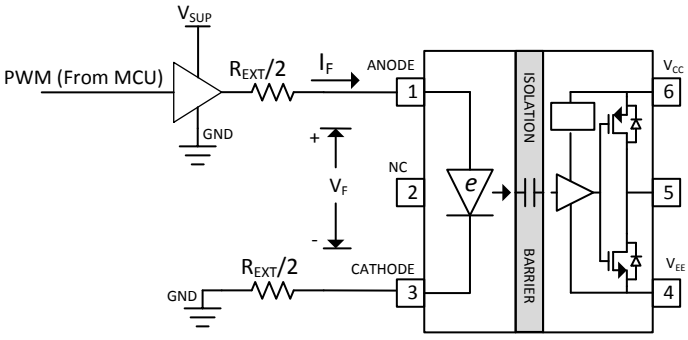
See Figure 26 for the schematic using a single NMOS and split resistor combination to drive the input stage of UCC23511. The input resistor can be selected using the equation shown.




$$R_{EXT} = \frac{V_{SUP} - V_F}{I_F} - R_{M1}$$

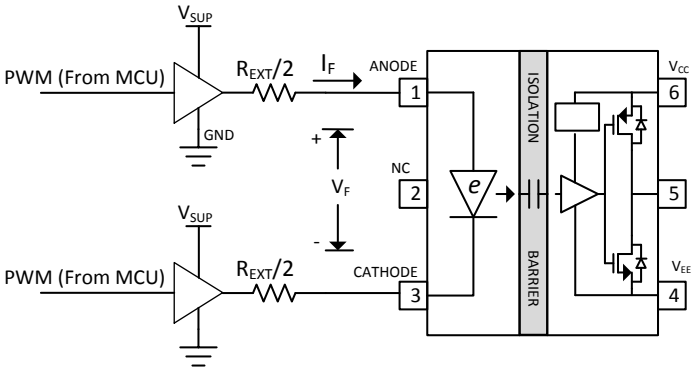
**Figure 26. Configuration 1: Driving the input stage of UCC23511 with a single NMOS and split resistors**

Driving the input stage of UCC23511 using a single buffer is shown in Figure 27 and using 2 buffers is shown in Figure 28




$$R_{EXT} = \frac{V_{SUP} - V_F}{I_F} - R_{OH_buf}$$

**Figure 27. Configuration 2: Driving the input stage of UCC23511 with one Buffer and split resistors**




$$R_{EXT} = \frac{V_{SUP} - V_F}{I_F} - (R_{OH_buf} + R_{OL_buf})$$

**Figure 28. Configuration 3: Driving the input stage of UCC23511 with 2 buffers and split resistors**

Table 5 shows the range of values for $R_{EXT}$ for the 3 different configurations shown in Figure 26, Figure 27 and Figure 28.The assumptions used in deriving the range for $R_{EXT}$ are as follows:

1. Target forward current $I_F$ is 7mA min, 10mA typ and 16mA max
2. e-diode forward voltage drop is 1.8V to 2.4V
3. $V_{SUP}$ (Buffer supply voltage) is 5V with ±5% tolerance
4. Manufacturer's tolerance for $R_{EXT}$ is 1%
5. NMOS resistance is 0.25Ω to 1.0Ω (for configuration 1)
6. $R_{OH}$(buffer output impedance in output "High" state) is 13Ω min, 18Ω typ and 22Ω max
7. $R_{OL}$(buffer output impedance in "Low" state) is 10Ω min, 14Ω typ and 17Ω max

**Table 5. $R_{EXT}$ Values to Drive The Input Stage**

| | $R_{EXT}$ Ω | | |
|---|---|---|---|
| **Configuration** | Min | Typ | Max |
| Single NMOS and $R_{EXT}$ | 218 | 290 | 331 |
| Single Buffer and $R_{EXT}$ | 204 | 272 | 311 |
| Two Buffers and $R_{EXT}$ | 194 | 259 | 294 |

#### *9.2.2.2 Gate-Driver Output Resistor*

The external gate-driver resistors, $R_{G(ON)}$ and $R_{G(OFF)}$ are used to:

1. Limit ringing caused by parasitic inductances and capacitances
2. Limit ringing caused by high voltage or high current switching dv/dt, di/dt, and body-diode reverse recovery
3. Fine-tune gate drive strength, specifically peak sink and source current to optimize the switching loss
4. Reduce electromagnetic interference (EMI)

The output stage of UCC23511 has a pull up structure consisting of a P-channel MOSFET and an N-channel MOSFET in parallel, as shown in Figure 22. The N-channel MOSFET provides the peak current that charges the gate of the IGBT (or power switch) while the P-channel MOSFET ensures that $V_{OUT}$ will go all the way upto $V_{CC}$. Figure 25 shows the internal gate resistance, $R_{G_int}$ of the power switch. $R_{G_int}$is usually specified in the datasheet of the power switch. When turning the power switch "on", the gate driver sees a total gate resistance $R_{G_total} = R_{GON} + R_{G_int}$ and when turning the power switch "off", the gate driver sees a total gate resistance $R_{G_total} = R_{GOFF} + R_{G_int}$ in series with the gate capacitance where,

- $R_{GON}$ is the external resistance on the pcb for turn "on"
- $R_{GOFF}$ is the external resistance on the pcb for turn "off"


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- $R_{G_int}$ is the internal gate resistance of the power switch that can be found in the data sheet of the power switch
- Ideal diodes — zero resistance and zero voltage drop — are assumed on both the turn-on and turn-off paths, for simplicity. Adjust accordingly based on design component selections.

To illustrate the procedure to select $R_{GON}$ and $R_{GOFF}$ , let us consider the following example with the assumptions listed below:

1. Power switch internal gate resistance is 2 ohms
2. Desired charging current is 1.5A
3. Desired discharging current is 1.7A
4. Gate driver supply is 15V

For this example, since $V_{CC}$=15V, use the typical curves shown in Figure 29. It can be seen that we need a total turn on resistance of 7 ohms (peak charging current of 1.5A) and a total turn off resistance of 8 ohms (peak discharging current of 1.7A). Subtracting the internal gate resistance of the power switch, we get $R_{GON}$= 7 ohms - 2 ohms = 5 ohms, and $R_{GOFF}$= 8 ohms- 2 ohms = 6 ohms.

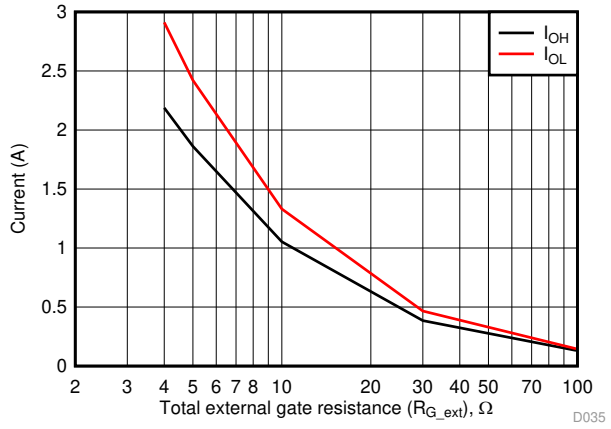



**Figure 29. Peak drive current vs Total gate resistance, $R_{G_total}$ (Gate driver supply =15V)**

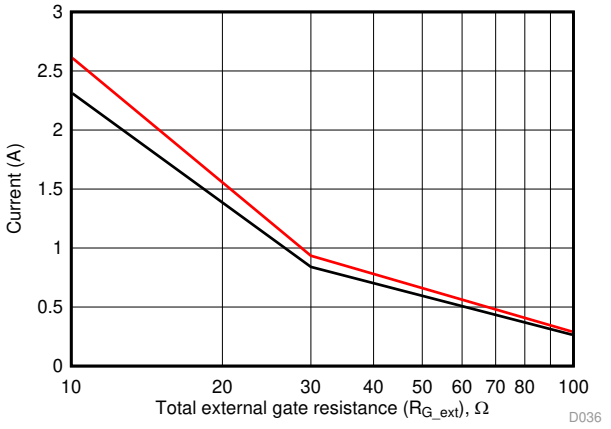



**Figure 30. Peak drive current vs Total gate resistance, $R_{G_total}$ (Gate driver supply = 30V)**

Use Table 6 to find the minimum gate resistance to be used with UCC23511 when driving a power switch. The values shown includes the power switch internal gate resistance $R_{G_int}$. Hence, $R_{G_int}$ must be subtracted from the values shown to determine the value of the resistor to populate on the printed circuit board.

The diodes shown in series with each, $R_{GON}$ and $R_{GOFF}$, in Figure 25 ensure the gate drive current flows through the intended path, respectively, during turn-on and turn-off. Note that the diode forward drop will reduce the voltage level at the gate of the power switch. To achieve rail-to-rail gate voltage levels, add a resistor from the $V_{OUT}$ pin to the power switch gate, with a resistance value approximately 20 times higher than $R_{GON}$ and $R_{GOFF}$. For the examples described in this section, a good choice would be 100 Ω to 200 Ω.

**Table 6. Minimum gate resistor (Ω)**

| Gate driver supply $V_{CC}$-$V_{EE}$ (V) | Minimum total gate resistance (Ω) = ($R_{GON}$+ $R_{G_int}$) or ($R_{GOFF}$+ $R_{G_int}$) |
|---|---|
| 15 | 4 |
| 23 | 7 |
| 30 | 10 |

**NOTE**

The estimated peak current is also influenced by PCB layout and load capacitance. Parasitic inductance in the gate-driver loop can slow down the peak gate-drive current and introduce overshoot and undershoot. Therefore, TI strongly recommends that the gate-driver loop should be minimized. Conversely, the peak source and sink current is dominated by loop parasitics when the load capacitance ($C_{ISS}$) of the power transistor is very small (typically less than 1 nF) because the rising and falling time is too small and close to the parasitic ringing period.

#### 9.2.2.3 Estimate Gate-Driver Power Loss

The total loss, $P_G$, in the gate-driver subsystem includes the power losses ($P_{GD}$) of the UCC23511 device and the power losses in the peripheral circuitry, such as the external gate-drive resistor.

The $P_{GD}$ value is the key power loss which determines the thermal safety-related limits of the UCC23511 device, and it can be estimated by calculating losses from several components.

The first component is the static power loss, $P_{GDQ}$, which includes power dissipated in the input stage ($P_{GDQ_IN}$) as well as the quiescent power dissipated in the output stage ($P_{GDQ_OUT}$) when operating with a certain switching frequency under no load. $P_{GDQ_IN}$ is determined by $I_F$ and $V_F$ and is given by Equation 1. The $P_{GDQ_OUT}$ parameter is measured on the bench with no load connected to $V_{OUT}$ pin at a given $V_{CC}$, switching frequency, and ambient temperature. In this example, $V_{CC}$ is 15 V. The current on the power supply, with PWM switching at 10 kHz, is measured to be $I_{CC}$ = 1.33 mA . Therefore, use Equation 2 to calculate $P_{GDQ_OUT}$.

$$P_{GDQ_IN} = \frac{1}{2} * V_F * I_F \quad (1)$$

$$P_{GDQ_OUT} = V_{CC} * I_{CC} \quad (2)$$

The total quiescent power (without any load capacitance) dissipated in the gate driver is given by the sum of Equation 1 and Equation 2 as shown in Equation 3

$$P_{GDQ} = P_{GDQ_IN} + P_{GDQ_OUT} = 10\ mW + 20mW = 30mW \quad (3)$$

The second component is the switching operation loss, $P_{GDSW}$, with a given load capacitance which the driver charges and discharges the load during each switching cycle. Use Equation 4 to calculate the total dynamic loss from load switching, $P_{GSW}$.

$$P_{GSW} = V_{CC2} \times Q_G \times f_{SW} \quad (4)$$

where

- $Q_G$ is the gate charge of the power transistor at $V_{CC}$.

So, for this example application the total dynamic loss from load switching is approximately 18 mW as calculated in Equation 5.

$$P_{GSW} = 15\ V \times 120\ nC \times 10\ kHz = 18\ mW \quad (5)$$

$Q_G$ represents the total gate charge of the power transistor switching 520 V at 50 A, and is subject to change with different testing conditions. The UCC23511 gate-driver loss on the output stage, $P_{GDO}$, is part of $P_{GSW}$. $P_{GDO}$ is equal to $P_{GSW}$ if the external gate-driver resistance and power-transistor internal resistance are 0 Ω, and all the gate driver-loss will be dissipated inside the UCC23511. If an external turn-on and turn-off resistance exists, the total loss is distributed between the gate driver pull-up/down resistance, external gate resistance, and power-transistor internal resistance. Importantly, the pull-up/down resistance is a linear and fixed resistance if the source/sink current is not saturated to 4.6A/5.7A, however, it will be non-linear if the source/sink current is saturated. Therefore, $P_{GDO}$ is different in these two scenarios.

**Case 1 - Linear Pull-Up/Down Resistor:**


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$$P_{GDO} = \frac{P_{GSW}}{2}\left[\frac{R_{OH}||R_{NMOS}}{R_{OH}||R_{NMOS} + R_{GON} + R_{GFET_int}} + \frac{R_{OL}}{R_{OL} + R_{GOFF} + R_{GFET_int}}\right] \quad (6)$$

In this design example, all the predicted source and sink currents are less than 4.6 A and 5.7 A, therefore, use Equation 6 to estimate the UCC23511 gate-driver loss.

$$P_{GDO} = \frac{18\ mW}{2}\left[\frac{9.5\Omega||5.1\Omega}{9.5\Omega||5.1\Omega + 5.1\Omega + 0\Omega} + \frac{0.4\Omega}{0.4\Omega + 10\Omega + 0\Omega}\right] = 3.9\ mW \quad (7)$$

**Case 2 - Nonlinear Pull-Up/Down Resistor:**

$$P_{GDO} = f_{sw}\ x\left[4.5A\ x \int_0^{T_{R_Sys}} (V_{CC} - V_{OUT}(t))dt + 5.3A\ x \int_0^{T_{F_Sys}} V_{OUT}(t)\,dt\right] \quad (8)$$

where

- $V_{OUT(t)}$ is the gate-driver OUT pin voltage during the turnon and turnoff period. In cases where the output is saturated for some time, this value can be simplified as a constant-current source (4.6 A at turnon and 5.7 A at turnoff) charging or discharging a load capacitor. Then, the $V_{OUT(t)}$ waveform will be linear and the $T_{R_Sys}$ and $T_{F_Sys}$ can be easily predicted.

For some scenarios, if only one of the pullup or pulldown circuits is saturated and another one is not, the $P_{GDO}$ is a combination of case 1 and case 2, and the equations can be easily identified for the pullup and pulldown based on this discussion.

Use Equation 9 to calculate the total gate-driver loss dissipated in the UCC23511 gate driver, $P_{GD}$.

$$P_{GD} = P_{GDQ} + P_{GDO} = 30mW + 3.9mW = 33.9mW \quad (9)$$

#### 9.2.2.4 Estimating Junction Temperature

Use Equation 10 to estimate the junction temperature ($T_J$) of UCC23511.

$$T_J = T_C + \Psi_{JT} \times P_{GD} \quad (10)$$

where

- $T_C$ is the UCC23511 case-top temperature measured with a thermocouple or some other instrument.
- $\Psi_{JT}$ is the junction-to-top characterization parameter from the table.

Using the junction-to-top characterization parameter ($\Psi_{JT}$) instead of the junction-to-case thermal resistance ($R_{\theta JC}$) can greatly improve the accuracy of the junction temperature estimation. The majority of the thermal energy of most ICs is released into the PCB through the package leads, whereas only a small percentage of the total energy is released through the top of the case (where thermocouple measurements are usually conducted). The $R_{\theta JC}$ resistance can only be used effectively when most of the thermal energy is released through the case, such as with metal packages or when a heat sink is applied to an IC package. In all other cases, use of $R_{\theta JC}$ will inaccurately estimate the true junction temperature. The $\Psi_{JT}$ parameter is experimentally derived by assuming that the dominant energy leaving through the top of the IC will be similar in both the testing environment and the application environment. As long as the recommended layout guidelines are observed, junction temperature estimations can be made accurately to within a few degrees Celsius.

#### 9.2.2.5 Selecting $V_{CC}$ Capacitor

Bypass capacitors for $V_{CC}$ is essential for achieving reliable performance. TI recommends choosing low-ESR and low-ESL, surface-mount, multi-layer ceramic capacitors (MLCC) with sufficient voltage ratings, temperature coefficients, and capacitance tolerances. A 50-V, 10-µF MLCC and a 50-V, 0.22-µF MLCC are selected for the $C_{VCC}$ capacitor. If the bias power supply output is located a relatively long distance from the $V_{CC}$ pin, a tantalum or electrolytic capacitor with a value greater than 10 µF should be used in parallel with $C_{VCC}$.

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**NOTE**

DC bias on some MLCCs will impact the actual capacitance value. For example, a 25-V, 1-μF X7R capacitor is measured to be only 500 nF when a DC bias of 15-$V_{DC}$ is applied.

## 10 Power Supply Recommendations

The recommended input supply voltage ($V_{CC}$) for the UCC23511 device is from 14V to 33V. The lower limit of the range of output bias-supply voltage ($V_{CC}$) is determined by the internal UVLO protection feature of the device. $V_{CC}$ voltage should not fall below the UVLO threshold for normal operation, or else the gate-driver outputs can become clamped low for more than 20 μs by the UVLO protection feature. The higher limit of the $V_{CC}$ range depends on the maximum gate voltage of the power device that is driven by the UCC23511 device, and should not exceed the recommended maximum $V_{CC}$ of 33 V. A local bypass capacitor should be placed between the $V_{CC}$ and $V_{EE}$ pins, with a value of 220-nF to 10-μF for device biasing. TI recommends placing an additional 100-nF capacitor in parallel with the device biasing capacitor for high frequency filtering. Both capacitors should be positioned as close to the device as possible. Low-ESR, ceramic surface-mount capacitors are recommended.

If only a single, primary-side power supply is available in an application, isolated power can be generated for the secondary side with the help of a transformer driver such as Texas Instruments' SN6501 or SN6505A. For such applications, detailed power supply design and transformer selection recommendations are available in *SN6501 Transformer Driver for Isolated Power Supplies* data sheet and *SN6505A Low-Noise 1-A Transformer Drivers for Isolated Power Supplies* data sheet.


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# 11 Layout

## 11.1 Layout Guidelines

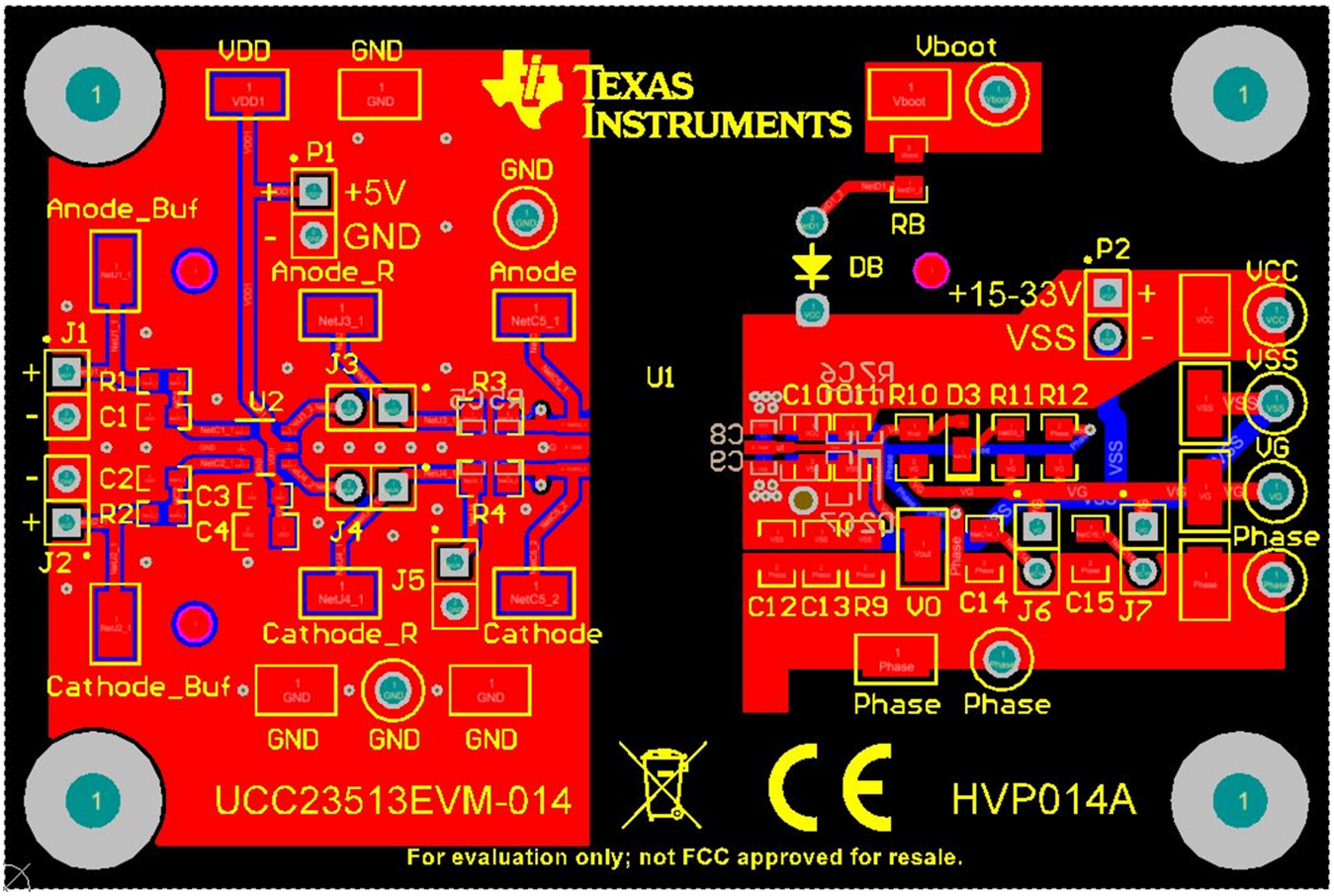
Designers must pay close attention to PCB layout to achieve optimum performance for the UCC23511. Some key guidelines are:

- Component placement:
  - Low-ESR and low-ESL capacitors must be connected close to the device between the $V_{CC}$ and $V_{EE}$ pins to bypass noise and to support high peak currents when turning on the external power transistor.
  - To avoid large negative transients on the $V_{EE}$ pins connected to the switch node, the parasitic inductances between the source of the top transistor and the source of the bottom transistor must be minimized.
- Grounding considerations:
  - Limiting the high peak currents that charge and discharge the transistor gates to a minimal physical area is essential. This limitation decreases the loop inductance and minimizes noise on the gate terminals of the transistors. The gate driver must be placed as close as possible to the transistors.
- High-voltage considerations:
  - To ensure isolation performance between the primary and secondary side, avoid placing any PCB traces or copper below the driver device. A PCB cutout or groove is recommended in order to prevent contamination that may compromise the isolation performance.
- Thermal considerations:
  - A large amount of power may be dissipated by the UCC23511 if the driving voltage is high, the load is heavy, or the switching frequency is high. Proper PCB layout can help dissipate heat from the device to the PCB and minimize junction-to-board thermal impedance ($\theta_{JB}$).
  - Increasing the PCB copper connecting to the $V_{CC}$ and $V_{EE}$ pins is recommended, with priority on maximizing the connection to $V_{EE}$. However, the previously mentioned high-voltage PCB considerations must be maintained.
  - If the system has multiple layers, TI also recommends connecting the $V_{CC}$ and $V_{EE}$ pins to internal ground or power planes through multiple vias of adequate size. These vias should be located close to the IC pins to maximize thermal conductivity. However, keep in mind that no traces or coppers from different high voltage planes are overlapping.

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## 11.2 Layout Example

Figure 31 shows a PCB layout example with the signals and key components labeled.




(1) No PCB traces or copper are located between the primary and secondary side, which ensures isolation performance.

**Figure 31. Layout Example**


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## Layout Example (continued)

Figure 32 and Figure 33 show the top and bottom layer traces and copper.

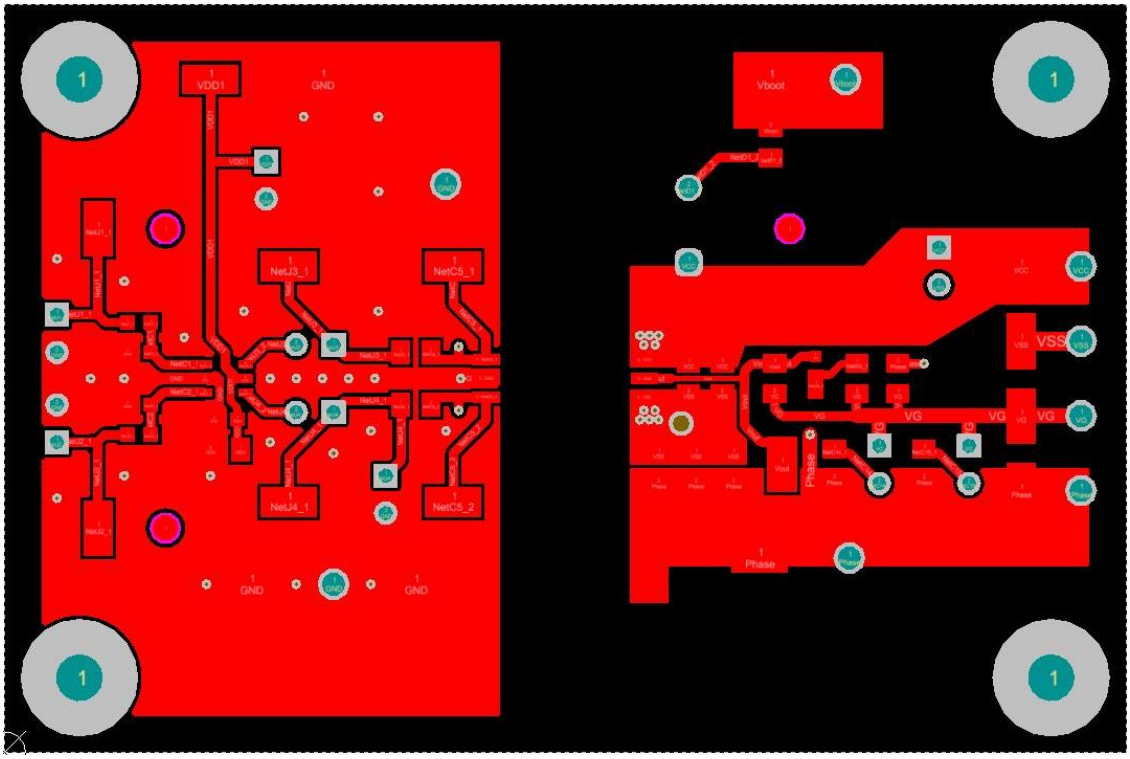



**Figure 32. Top-Layer Traces and Copper**

## Layout Example (continued)

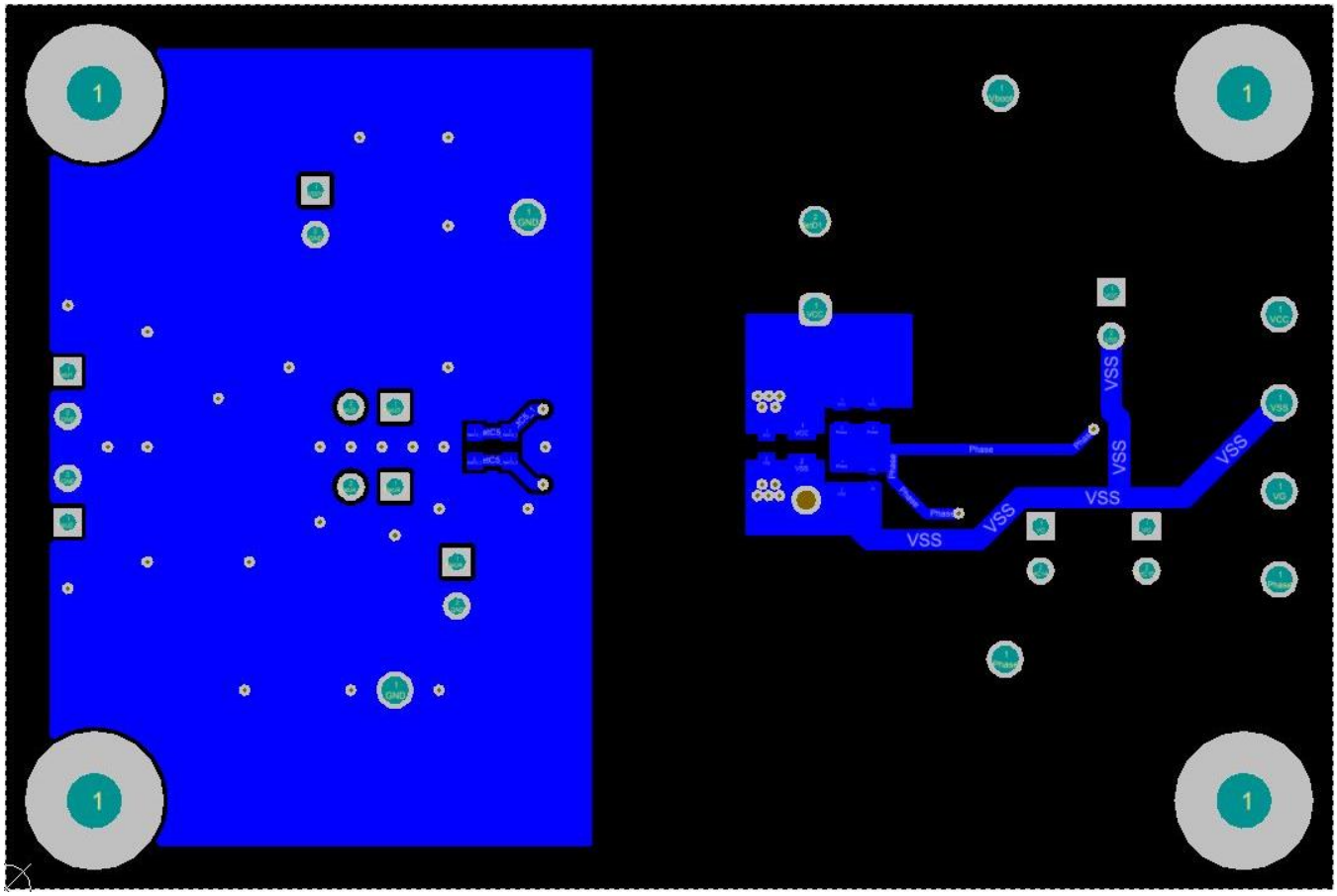
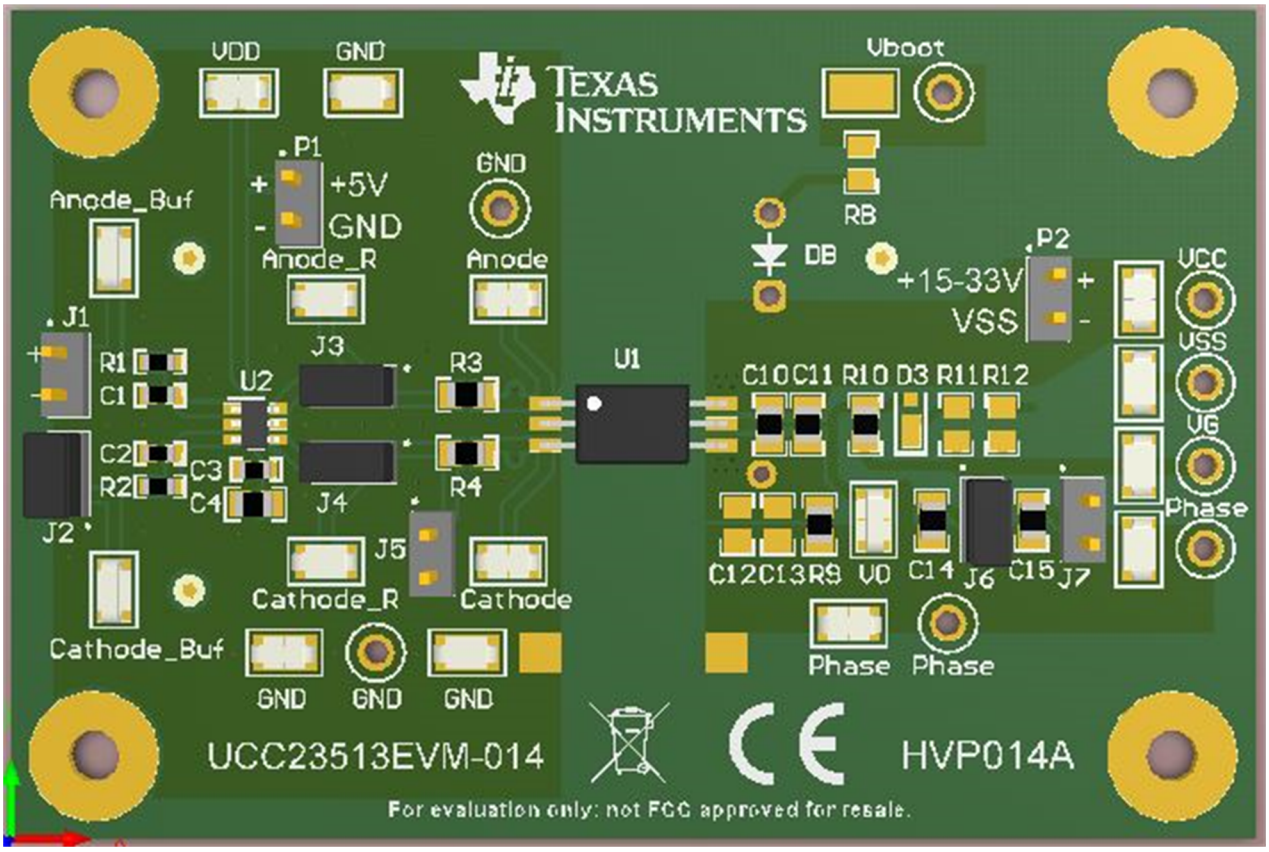



**Figure 33. Bottom-Layer Traces and Copper (Flipped)**


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## Layout Example (continued)

Figure 34 shows the 3D layout of the top view of the PCB.




(1) The location of the PCB cutout between primary side and secondary sides ensures isolation performance.

**Figure 34. 3-D PCB View**

### 11.3 PCB Material

Use standard FR-4 UL94V-0 printed circuit board. This PCB is preferred over cheaper alternatives because of lower dielectric losses at high frequencies, less moisture absorption, greater strength and stiffness, and the self-extinguishing flammability-characteristics.

### 11.4 Custom Design With WEBENCH® Tools

Click here to create a custom design using the UCC3511 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage ($V_{IN}$), output voltage ($V_{OUT}$), and output current ($I_{OUT}$) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

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## 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.


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## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| UCC23511DWY | ACTIVE | SOIC | DWY | 6 | 100 | Green (RoHS & no Sb/Br) | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | UCC23511 | Samples |
| UCC23511DWYR | ACTIVE | SOIC | DWY | 6 | 850 | Green (RoHS & no Sb/Br) | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | UCC23511 | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

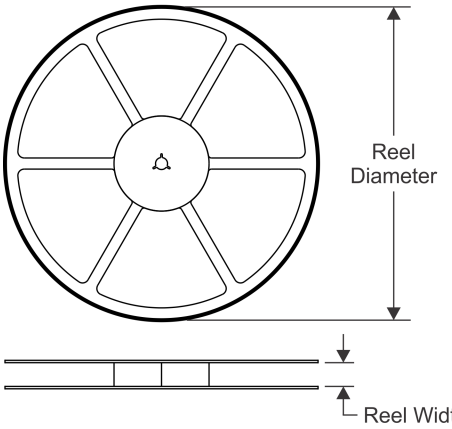
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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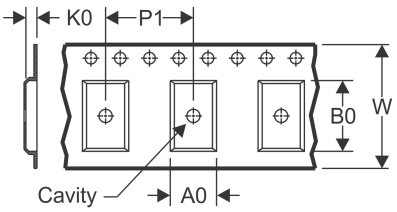
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## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

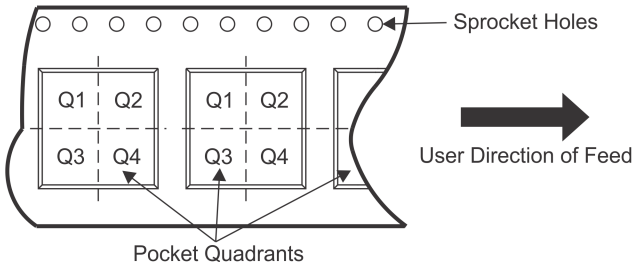



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

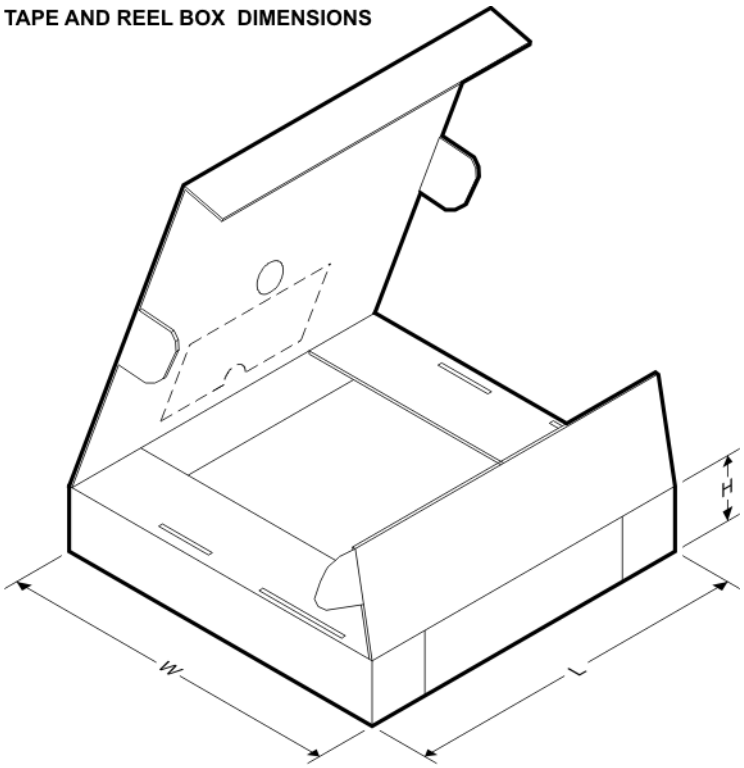
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| UCC23511DWYR | SOIC | DWY | 6 | 850 | 330.0 | 16.4 | 12.05 | 5.08 | 4.0 | 16.0 | 16.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

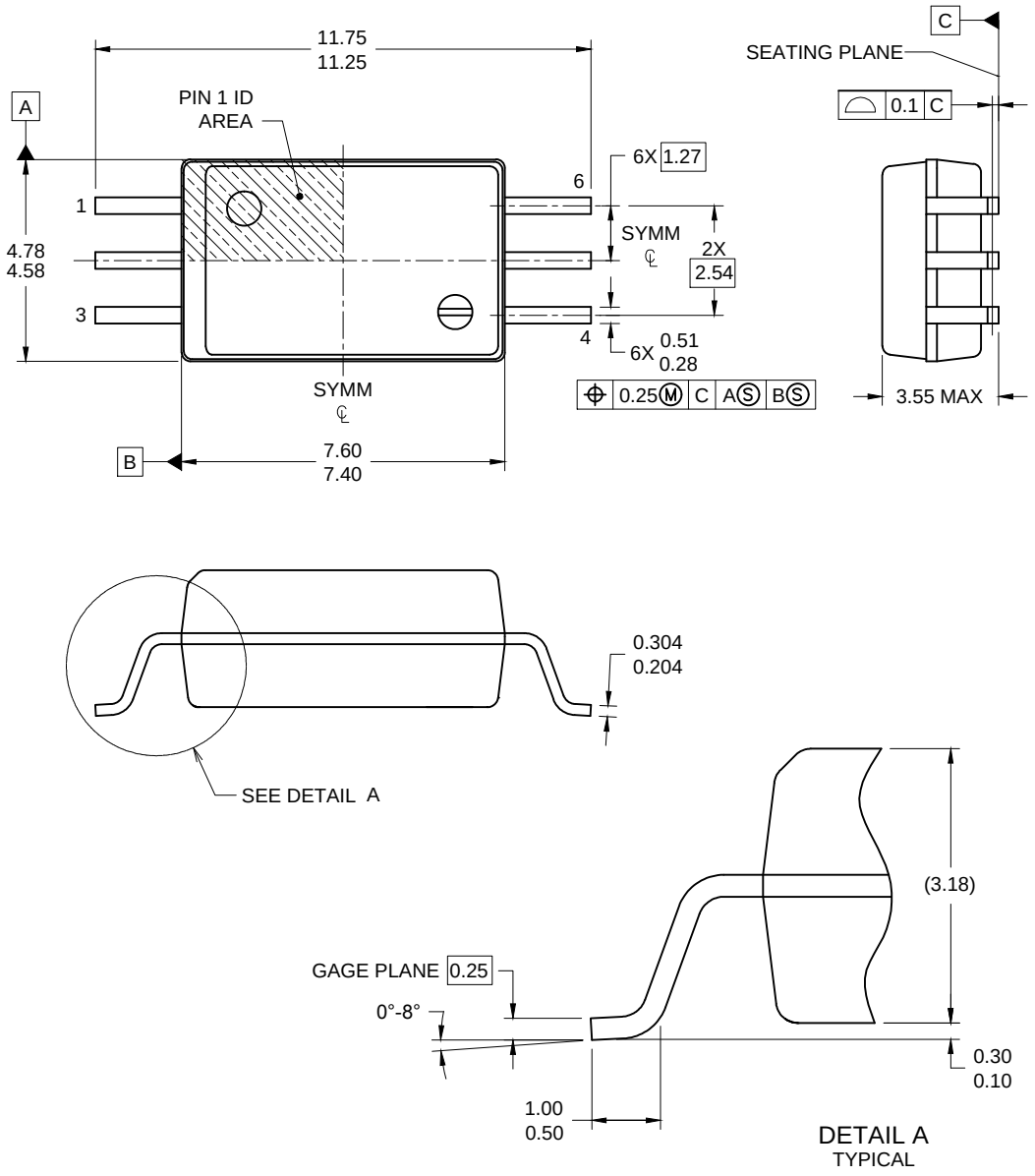
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| UCC23511DWYR | SOIC | DWY | 6 | 850 | 350.0 | 350.0 | 43.0 |

# PACKAGE OUTLINE

## DWY0006A

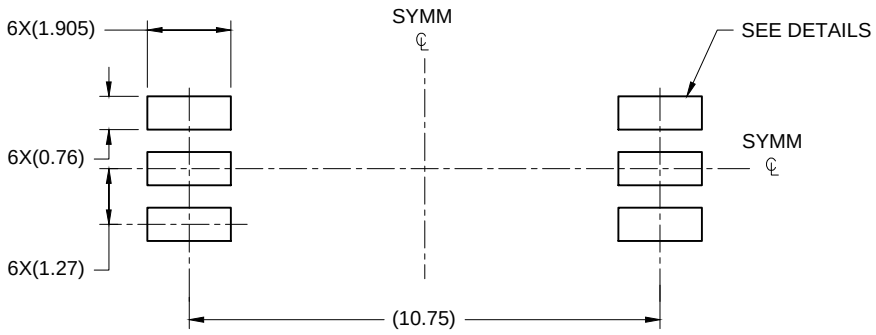
## SOIC -3.55 mm max height

SOIC

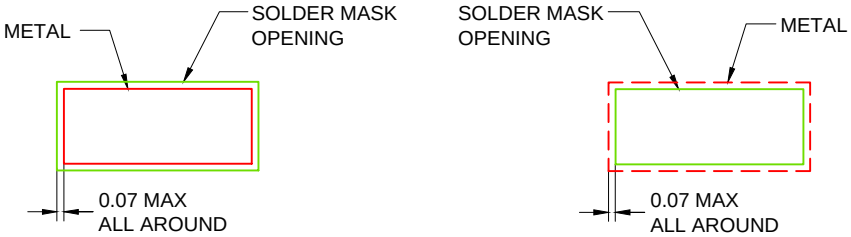



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.70 per side.




LAND PATTERN EXAMPLE
SCALE:6X

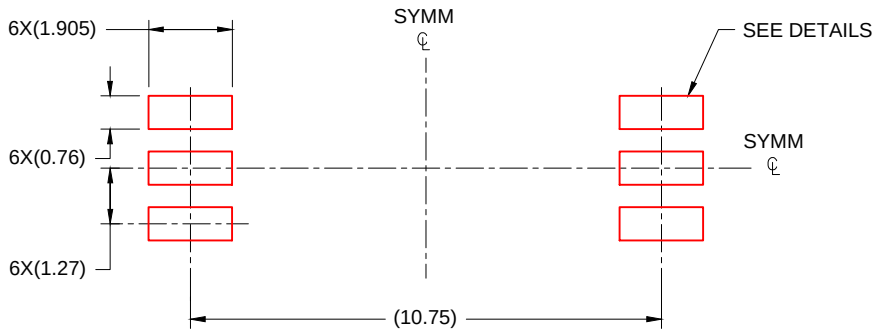



SOLDER MASK DETAAILS

4223977/A 01/2018

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 6X

4223977/A 01/2018

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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