NUP4106

ESD Protection Diode

Low Capacitance Surface Mount ESD Protection for High−Speed Data Interfaces

The NUP4106 surge protection is designed to protect equipment attached to high speed communication lines from ESD and lightning.

Features

- SO−8 Package
- Peak Power − 500 W 8 x 20 μS
- ESD Rating:
  IEC 61000−4−2 (ESD) 15 kV (air) 8 kV (contact)
- UL Flammability Rating of 94 V−0
- This is a Pb−Free Device

Typical Applications

- High Speed Communication Line Protection
- T1/E1 Secondary Protection
- T3/E3 Secondary Protection
- Analog Video Protection
- Base Stations
- I^2C Bus Protection

MAXIMUM RATINGS

Rating		Symbol	Value	Unit
Peak Power Dissipation 8 x 20 μS @ T_A = 25°C (Note 1)		P_{pk}	500	W
Junction and Storage Temperature Range		T_J, T_{stg}	−55 to +150	°C
Lead Solder Temperature − Maximum 10 Seconds Duration		T_L	260	°C
IEC 61000−4−2	Contact Air	ESD	±8 ±15	kV

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

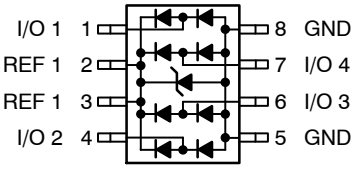
1. Non−repetitive current pulse 8 x 20 μS exponential decay waveform
   Pin 2/3 to Pin 5/8

ON Semiconductor®

www.onsemi.com

SO−8 LOW CAPACITANCE VOLTAGE SUPPRESSOR 500 WATTS PEAK POWER 3.3 VOLTS

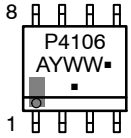
PIN CONFIGURATION AND SCHEMATIC





SOIC−8
CASE 751
PLASTIC

MARKING DIAGRAM



A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping†
NUP4106DR2G	SO−8 (Pb−Free)	2500/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

© Semiconductor Components Industries, LLC, 2009

ELECTRICAL CHARACTERISTICS

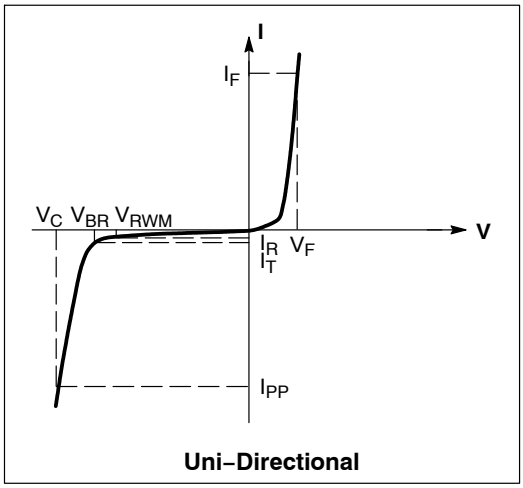
Characteristic	Symbol	Min	Typ	Max	Unit
Reverse Breakdown Voltage @ I_t = 1.0 mA	V_{BR}	5.0	–	–	V
Reverse Leakage Current @ V_{RWN} = 3.3 V	I_R	N/A	–	5.0	μA
Maximum Clamping Voltage @ I_{PP} = 1.0 A, 8 x 20 μS	V_C	N/A	–	7.0	V
Maximum Clamping Voltage @ I_{PP} = 10 A, 8 x 20 μS	V_C	N/A	–	10	V
Maximum Clamping Voltage @ I_{PP} = 25 A, 8 x 20 μS	V_C	N/A	–	15	V
Between I/O Pins and Ground @ V_R = 0 V, 1.0 MHz	Capacitance	–	8.0	15	pF
Between I/O Pins @ V_R = 0 Volts, 1.0 MHz	Capacitance	–	4.0	–	pF

ELECTRICAL CHARACTERISTICS

(T_A = 25°C unless otherwise noted)

Symbol	Parameter
I_{PP}	Maximum Reverse Peak Pulse Current
V_C	Clamping Voltage @ I_{PP}
V_{RWM}	Working Peak Reverse Voltage
I_R	Maximum Reverse Leakage Current @ V_{RWM}
V_{BR}	Breakdown Voltage @ I_T
I_T	Test Current
I_F	Forward Current
V_F	Forward Voltage @ I_F
P_{pk}	Peak Power Dissipation
C	Capacitance @ V_R = 0 and f = 1.0 MHz

*See Application Note AND8308/D for detailed explanations of datasheet parameters.



TYPICAL CHARACTERISTICS

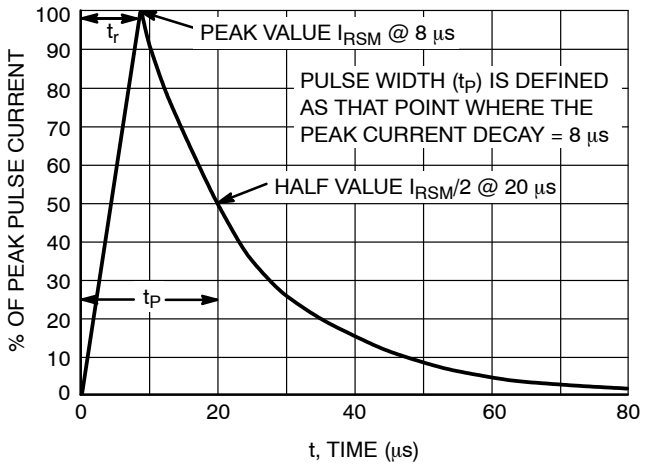


Figure 1. 8 x 20 μs Pulse Waveform

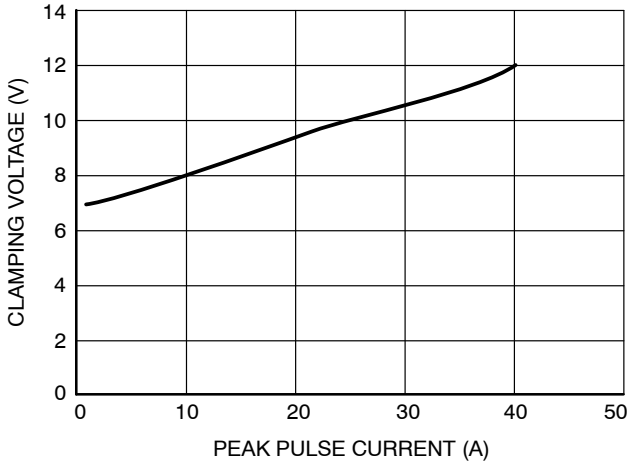


Figure 2. Clamping Voltage vs. Peak Pulse Current (8 x 20 μs Waveform)

APPLICATIONS INFORMATION

The NUP4106 is a low capacitance surge protection diode array designed to protect sensitive electronics such as communications systems, computers, and computer peripherals against damage due to ESD events or transient overvoltage conditions. Because of its low capacitance, it can be used in high speed I/O data lines. The integrated design of the NUP4106 offers surge rated, low capacitance steering diodes and a surge protection diode integrated in a single package (SO−8). If a transient condition occurs, the steering diodes will drive the transient to the positive rail of the power supply or to ground. The surge protection device protects the power line against overvoltage conditions avoiding damage to the power supply and other downstream components.

NUP4106 Configuration Options

The NUP4106 is able to protect up to four data lines against transient overvoltage conditions by driving them to a fixed reference point for clamping purposes. The steering diodes will be forward biased whenever the voltage on the protected line exceeds the reference voltage (Vf or V_{CC} + Vf). The diodes will force the transient current to bypass the sensitive circuit.

Data lines are connected at pins 1, 4, 6 and 7. The negative reference is connected at pins 5 and 8. These pins must be connected directly to ground using a ground plane to minimize the PCB's ground inductance. It is very important to reduce the PCB trace lengths as much as possible to minimize parasitic inductances.

Option 1

Protection of four data lines and the power supply using V_{CC} as reference.

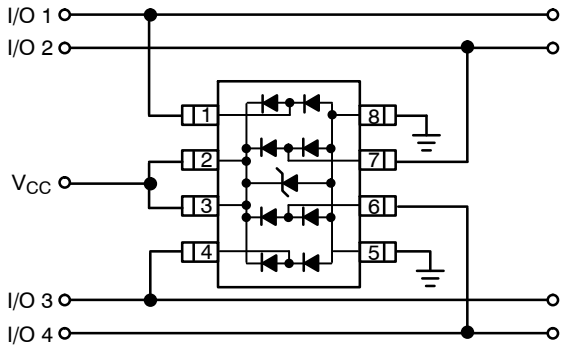


Figure 3.

For this configuration, connect pins 2 and 3 directly to the positive supply rail (V_{CC}). The data lines are referenced to the supply voltage. The internal surge protection diode prevents overvoltage on the supply rail. Biasing of the steering diodes reduces their capacitance.

Option 2

Protection of four data lines with bias and power supply isolation resistor.

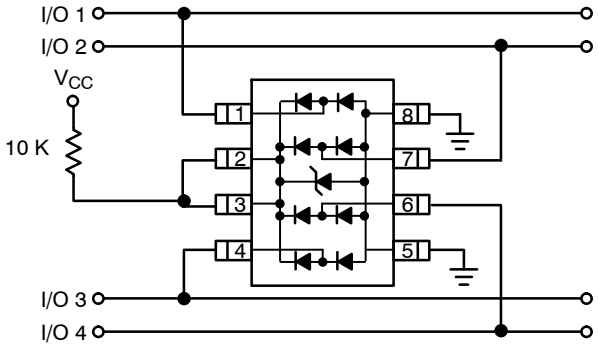


Figure 4.

The NUP4106 can be isolated from the power supply by connecting a series resistor between pins 2 and 3 and V_{CC}. A 10 kΩ resistor is recommended for this application. This will maintain a bias on the internal surge protection and steering diodes, reducing their capacitance.

Option 3

Protection of four data lines using the internal surge protection diode as reference.

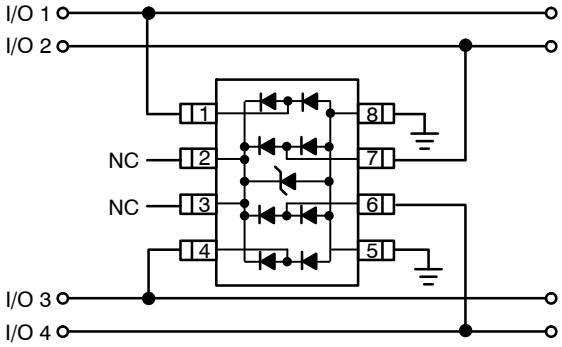


Figure 5.

In applications lacking a positive supply reference or those cases in which a fully isolated power supply is required, the internal surge protection can be used as the reference. For these applications, pins 2 and 3 are not connected. In this configuration, the steering diodes will conduct whenever the voltage on the protected line exceeds the working voltage of the surge protection plus one diode drop (Vc=Vf + V_{RWM}).

ESD Protection of Power Supply Lines

When using diodes for data line protection, referencing to a supply rail provides advantages. Biasing the diodes reduces their capacitance and minimizes signal distortion. Implementing this topology with discrete devices does have disadvantages. This configuration is shown below:

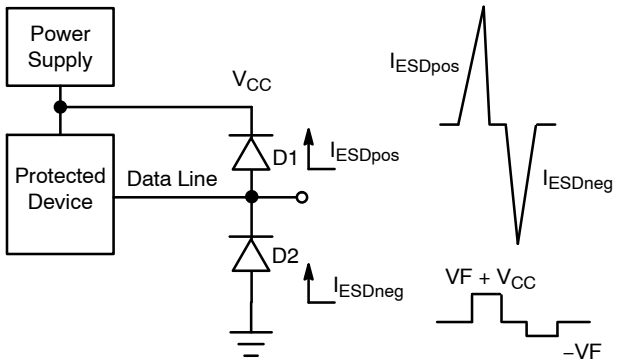


Figure 6.

Looking at the figure above, it can be seen that when a positive ESD condition occurs, diode D1 will be forward biased while diode D2 will be forward biased when a negative ESD condition occurs. For slower transient conditions, this system may be approximated as follows:

For positive pulse conditions:

$Vc = V_{CC} + Vf_{D1}$

For negative pulse conditions:

$Vc = -Vf_{D2}$

ESD events can have rise times on the order of some number of nanoseconds. Under these conditions, the effect of parasitic inductance must be considered. A pictorial representation of this is shown below.

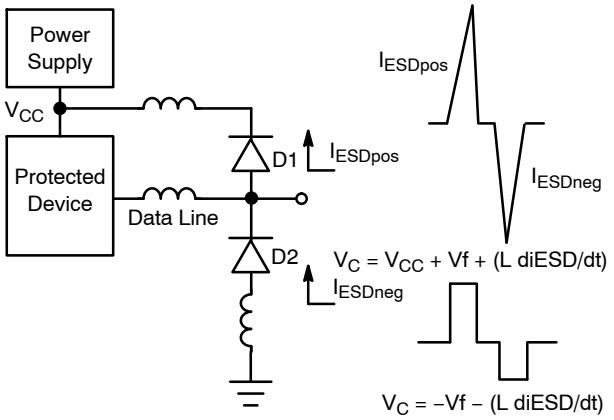


Figure 7.

An approximation of the clamping voltage for these fast transients would be:

For positive pulse conditions:

$Vc = V_{CC} + Vf + (L\ di_{ESD}/dt)$

For negative pulse conditions:

$Vc = -Vf - (L\ di_{ESD}/dt)$

As shown in the formulas, the clamping voltage (Vc) not only depends on the Vf of the steering diodes but also on the L di_{ESD}/dt factor. A relatively small trace inductance can result in hundreds of volts appearing on the supply rail. This endangers both the power supply and anything attached to that rail. This highlights the importance of good board layout. Taking care to minimize the effects of parasitic inductance will provide significant benefits in transient immunity.

Even with good board layout, some disadvantages are still present when discrete diodes are used to suppress ESD events across datalines and the supply rail. Discrete diodes with good transient power capability will have larger die and therefore higher capacitance. This capacitance becomes problematic as transmission frequencies increase. Reducing capacitance generally requires reducing die size. These small die will have higher forward voltage characteristics at typical ESD transient current levels. This voltage combined with the smaller die can result in device failure.

The ON Semiconductor NUP4106 was developed to overcome the disadvantages encountered when using discrete diodes for ESD protection. This device integrates a surge protection diode within a network of steering diodes.

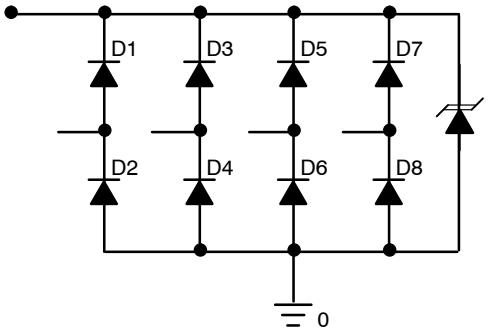


Figure 8. NUP4106 Equivalent Circuit

During an ESD condition, the ESD current will be driven to ground through the surge protection diode as shown below.

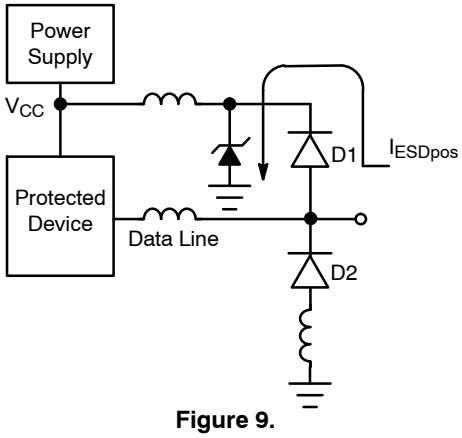


Figure 9.

The resulting clamping voltage on the protected IC will be: $Vc = V_{FD1} + V_{RWM}$.

The clamping voltage of the surge protection diode is provided in Figure 2 and depends on the magnitude of the ESD current. The steering diodes are fast switching devices with unique forward voltage and low capacitance characteristics.

TYPICAL APPLICATIONS

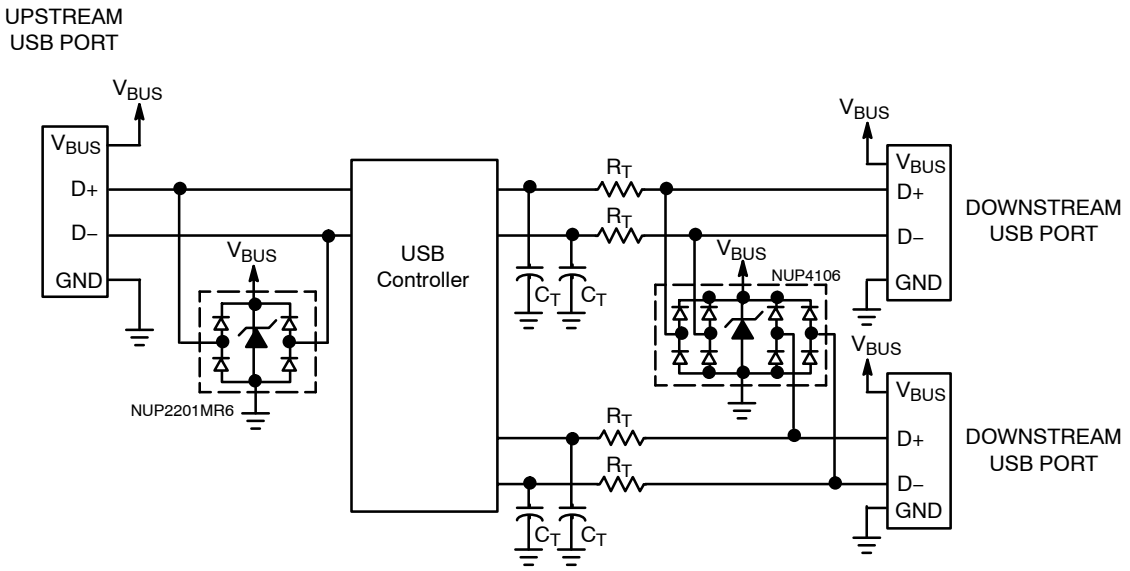


Figure 10. ESD Protection for USB Port

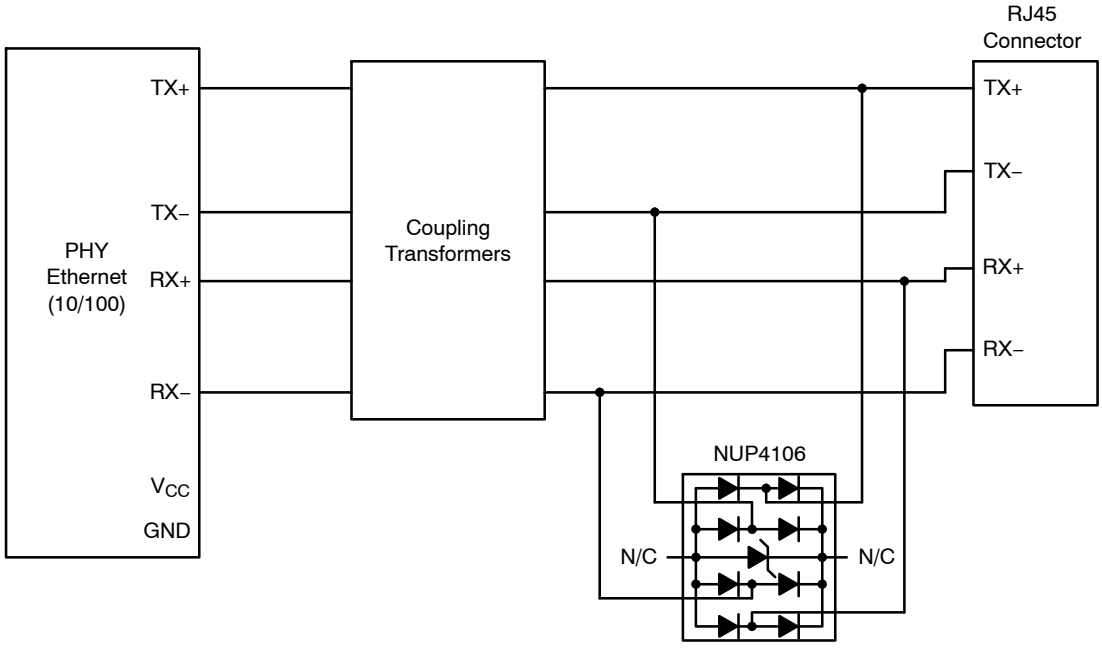


Figure 11. Protection for Ethernet 10/100 (Differential Mode)

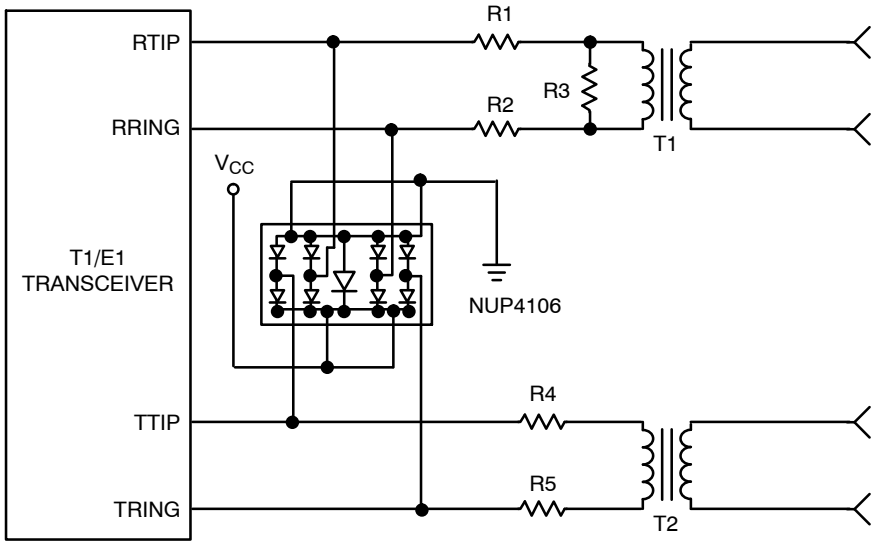
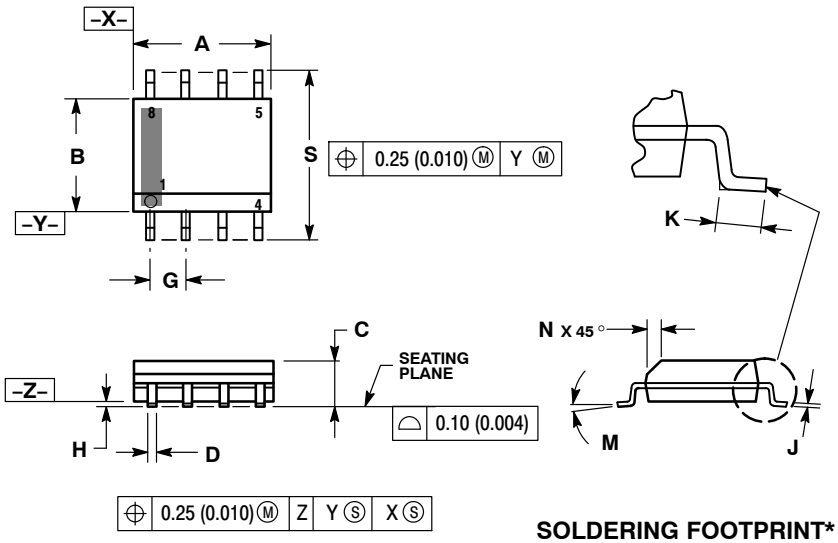


Figure 12. TI/E1 Interface Protection

PACKAGE DIMENSIONS

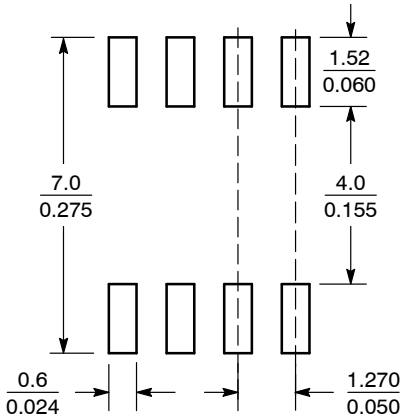
SOIC−8 NB
CASE 751−07
ISSUE AK



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0 °	8 °	0 °	8 °
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

SOLDERING FOOTPRINT*



SCALE 6:1 $\left(\frac{\text{mm}}{\text{inches}}\right)$

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ON Semiconductor and ON are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of ON Semiconductor's product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent−Marking.pdf. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using ON Semiconductor products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by ON Semiconductor. "Typical" parameters which may be provided in ON Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. ON Semiconductor does not convey any license under its patent rights nor the rights of others. ON Semiconductor products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use ON Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold ON Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that ON Semiconductor was negligent regarding the design or manufacture of the part. ON Semiconductor is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
19521 E. 32nd Pkwy, Aurora, Colorado 80011 USA
Phone: 303−675−2175 or 800−344−3860 Toll Free USA/Canada
Fax: 303−675−2176 or 800−344−3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800−282−9855 Toll Free USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81−3−5817−1050

ON Semiconductor Website: **www.onsemi.com**

Order Literature: http://www.onsemi.com/orderlit

For additional information, please contact your local Sales Representative