TEXAS INSTRUMENTS

TPS54010EVM-067 14-Amp

SWIFT™ Regulator Evaluation Module

User's Guide

August 2004

PMP Systems Power

SLVU114

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EVM WARNINGS AND RESTRICTIONS

It is important to operate this EVM within the input voltage ranges of 2.2 V to 4 V (PVIN) and 3 V to 4 V (VIN), and output voltage ranges of 0.9 V (Vout min) to 2.5 V (Vout max, with PVIN >3.3 V).

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 55°C. The EVM is designed to operate properly with certain components above 60°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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Chapter 1

Introduction

This chapter contains introductory information for the TPS54010 and support documentation for the TPS54010EVM-067 evaluation module (HPA067). Included in this user's guide are the performance specifications, the schematic, and the bill of materials for the TPS54010EVM-067.

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1.1 Background

The TPS54010 dc/dc converter is designed to provide up to a 14-A output from an input voltage source of 2.2 V to 4 V. Rated input voltage and output current range are given in Table 1−1. This evaluation module is designed to demonstrate the small PCB areas that may be achieved when designing with the TPS54010 regulator and does not reflect the high efficiencies that may be achieved when designing with this part. The switching frequency is set at a nominal 700 kHz, allowing the use of a small footprint 0.68-µH output inductor. The high- and low-side MOSFETs are incorporated inside the TPS54010 package along with the gate drive circuitry. The low drain-to-source on resistance of the MOSFETs allows the TPS54010 to achieve high efficiencies and helps to keep the junction temperature low at high output currents. The compensation components are provided external to the IC and allow for an adjustable output voltage and a customizable loop response. The TPS54010 is a full-featured device including programmable undervoltage lockout, synchronization, adjustable switching frequency, enable, and power-good functions.

Table 1−1. Input Voltage and Output Current Summary

EVM	INPUT VOLTAGE RANGE	OUTPUT CURRENT RANGE
TPS54010EVM−067	VIN = 3 V to 4 V PVIN = 2.2 V to 3.5 V	0 to 14 A

Note: Maximum PVIN for the TPS54010 is 4 V. To operate the TPS54010EVM-067 at PVIN greater than 3.5 V may require that the compensation network be adjusted.

1.2 Performance Specification Summary

A summary of the TPS54010EVM-067 performance specifications is provided in Table 1−2. Specifications are given for an input voltage of PVIN = VIN = 3.3 V and an output voltage of 1.5 V, unless otherwise specified. The TPS54010EVM-067 is designed and tested for PVIN = 2.2 V to 3.5 V. Above 3.5 V, the EVM still operates; however, the phase margin is less than 45 degrees. The ambient temperature is 25°C for all measurements, unless otherwise noted. The maximum input voltage for the TPS54010 is 4 V.

Table 1−2. TPS54010EVM-067 Performance Specification Summary

Specification		Test Conditions	Min	Typ	Max	Units
PVIN Voltage range			2.2	3.3	4.0	V
VIN Voltage range			3	3.3	4.0	V
Output voltage set point				1.5		V
Output current range		PVIN = 2.2 V to 3.5 V, VIN = 3 V to 4 V	0		14	A
Line regulation		I_O = 0 − 14 A, PVIN = 2.2 V to 4 V VIN = 3.3 V		±0.2%		
Load regulation		VIN = PVIN = 3.3 V, I_O = 0 to 3 A		±0.2%		
Load transient response	Voltage change	I_O =3.5 A to 10.5 A		−50		mV_{PK}
	Recovery time			80		µs
	Voltage change	I_O = 10.5 A to 3.5 A		+50		mV_{PK}
	Recovery time			80		µs
Loop bandwidth		PVIN = 2.2 V, VIN = 3.3 V		57		kHz
Phase margin		PVIN = 2.2 V, VIN = 3.3 V		54		°
Loop bandwidth		PVIN = 3.5 V, VIN = 3.3 V		73		kHz
Phase margin		PVIN = 3.5 V, VIN = 3.3 V		45		°
Input ripple voltage				250	300	mV_{PP}
Output ripple voltage				5	10	mV_{PP}
Output rise time				N/A		ms
Operating frequency				500		kHz
Maximum efficiency		VIN = 3.3 V, VOUT = 1.5 V, I_O = 2 A PVIN = 2.2 V		94%		–

1.3 Modifications

Whereas the TPS54010EVM−067 is designed to demonstrate the small size that can be attained when designing with the TPS54010, many of the features, which allow for extensive modifications, have been included in this EVM.

1.3.1 Output Voltage Set Point

To change the output voltage of the EVM, it is necessary to change the value of resistor R2. Changing the value of R2 can change the output voltage in the range of 0.9 V to 2.5 V. The value of R2 for a specific output voltage can be calculated by using Equation 1−1.

Equation 1−1.

$$R_2 = 10\ k\Omega \times \frac{0.891\ V}{V_O - 0.891\ V}$$

Table 1−3 lists the R2 values for some common output voltages. Note that PVIN must be greater than 3 V to generate a 2.5-V output.

Table 1−3. Output Voltages Available

Output Voltage (V)	R2 Value (Ω)
1.2	28.5 k
1.5	14.7 k
1.8	9.76 k
2.5	5.49 k

The minimum output voltage is limited by the minimum controllable on time of the device, 200 ns, and depends on the duty cycle and operating frequency. The approximate minimum output voltage can be calculated using Equation 1−2.

Equation 1−2.

$$V_{OUTMIN} = 200\ nsec \times f_s \times V_{INMAX}$$

1.3.2 Switching Frequency

The switching frequency of the EVM is set to 700 kHz by setting R4 to 71.5 kΩ. The switching frequency can be trimmed to any value between 250 kHz and 700 kHz by changing the value of R4 using Equation 1−1. The EVM also can be set to one of the two internally programmed frequencies. Remove R4 and use a jumper on the J4 pin 3 header to select 350−kHz or 550−kHz operation. The jumper settings are conveniently silk-screened on the EVM printed-circuit board. Note that decreasing the switching frequency results in increased output ripple unless the value of L1 is increased.

Equation 1−3.

$$f_{SW} = \frac{100\ k\Omega}{R_4} \times 500(kHz)$$

1.3.3 Input Filter

An onboard electrolytic input capacitor is included at C1. Depending on the application, this capacitor can be removed.

1.3.4 Split Input Voltage Rails

The TPS54010 is provided with two input voltage rails, PVIN and VIN. In normal operation, the two input voltages would be applied per Table 1−1 at the J1 and J2 connectors. It is possible to operate the EVM from a single 3−V to 3.5−V source by applying the voltage at the J1 connector and installing a jumper on JP1.

1.3.5 Synchronization

The TPS54010EVM-067 is synchronized to an external clock frequency. The synchronization frequency range is 330 kHz to 700 kHz. Drive a synchronization signal into the SYNC pin by connecting to pin 2 of J4 and use R4 to set the free-running frequency to 80% of the synchronization signal.

1.3.6 Extending Slow−Start Time

The slow−start time (T_{SS})can be extended by changing the value of C5. The value for C5 for a desired slow−start time is given by Equation 1−4.

Equation 1−4.

$$C5(\mu F) = T_{SS}(ms) \times \frac{5\ \mu A}{1.2\ V}$$

1.3.7 Output Filter

A location is provided to add an additional output filter capacitor (C12). The pads are sized for a 1210 component.

1.4 Trademarks

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Chapter 2

Test Setup and Results

This chapter describes how to properly connect, set up, and use the TPS54010EVM-067 evaluation module. The chapter also includes typical test results for the TPS54010EVM-067 and covers efficiency, output voltage regulation, load transients, loop response, output ripple, input ripple, and start-up.

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2.1 Input/Output Connections

The TPS54010EVM-067 is provided with input/output connectors and test points as shown in Table 2−1. Connect a power supply capable of supplying 12 A to J1 through a pair of 14 AWG wires. Connect a power supply capable of supplying 25 mA to J2 through a pair of 22 AWG wires. Connect the load to J3 through a pair of 14 AWG wires. The maximum load current capability is 14 A. Minimize wire lengths to reduce losses in the wires. Test points TP1 and TP2 provide a place to monitor the the PVIN and VIN input voltages wth TPS providing a convenient ground reference. Use TP7 to monitor the output voltage with TP8 as the ground reference.

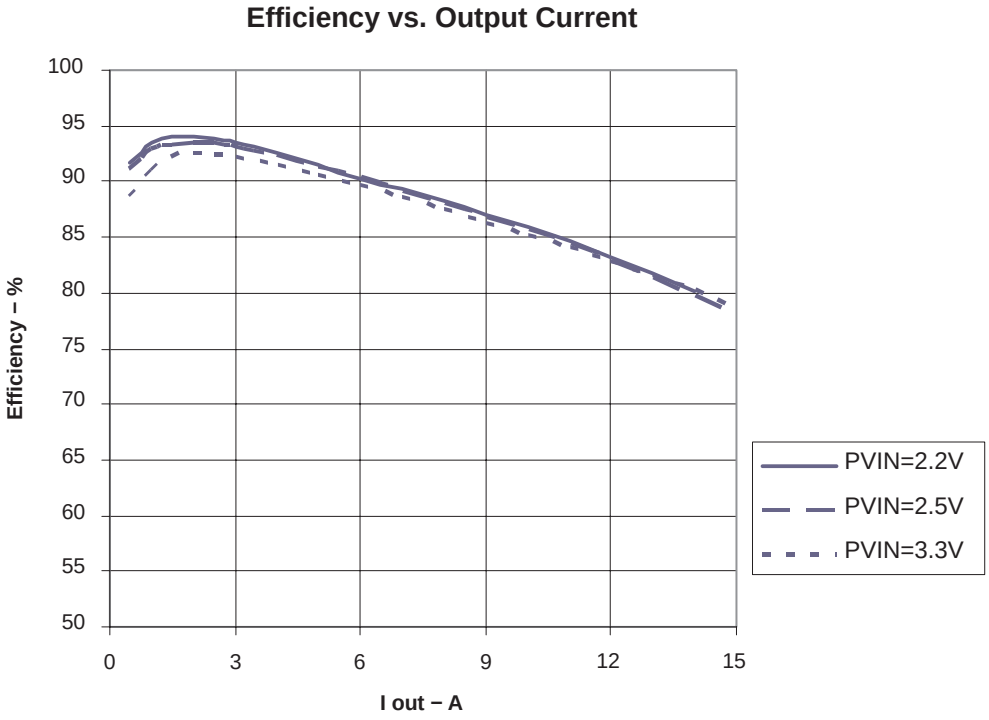
Table 2−1. EVM Connectors and Test Points

Reference Designator	Function
J1	PVIN, 2.2 V to 3.5 V nominal
J2	VIN, 3.3 V nominal, 3 V to 4 V
J3	VOUT, 1.5 V at 14 A maximum
J4	3-pin header for VIN, SYNC and GND. With R4 open, jumper SYNC to VIN for 550−kHz operation or SYNC to GND for 350−kHz operation,
J5	2-pin header for ENA, ground to disable , open to enable
JP1	Jumper to connect VIN to PVIN
TP1	VIN test point at VIN connector
TP2	PVIN test point at PVIN connector
TP3	GND test point at VIN and PVIN connectors
TP4	PWRGD signal monitor test point
TP5	Test point used for loop response measurements
TP6	PH test point
TP7	Output voltage test point at VOUT connector
TP8	GND test point at VOUT connector

2.2 Efficiency

The TPS54010EVM-067 efficiency peaks at load current of about 2 A and then decreases as the load current increases towards full load. Figure 2−1 shows the efficiency for the TPS54010 at an ambient temperature of 25°C. The efficiency is lower at higher ambient temperatures, due to temperature variation in the drain-to-source resistance of the MOSFETs. The efficiency is slightly lower at 700 kHz than at lower switching frequencies due to the gate and switching losses in the MOSFETs.

Figure 2−1. Measured Efficiency, TPS54010



2.3 Output Voltage Regulation

The output voltage load regulation of the TPS54010EVM-067 is shown in Figure 2−2, whereas, the output voltage line regulation is shown in Figure 2−3. Measurements are given for an ambient temperature of 25°C.

Figure 2−2. Load Regulation

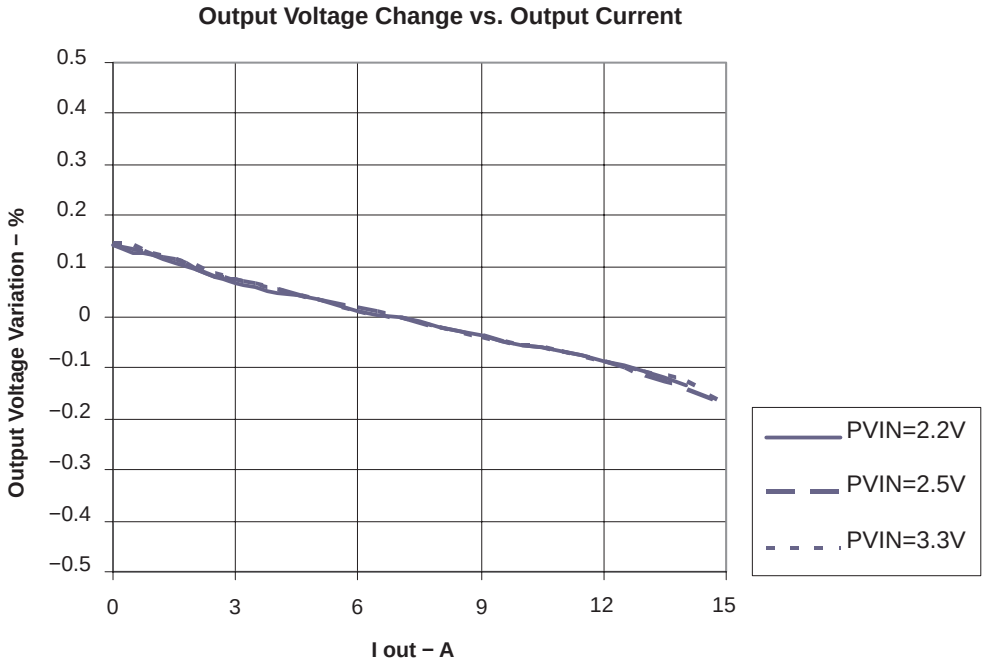
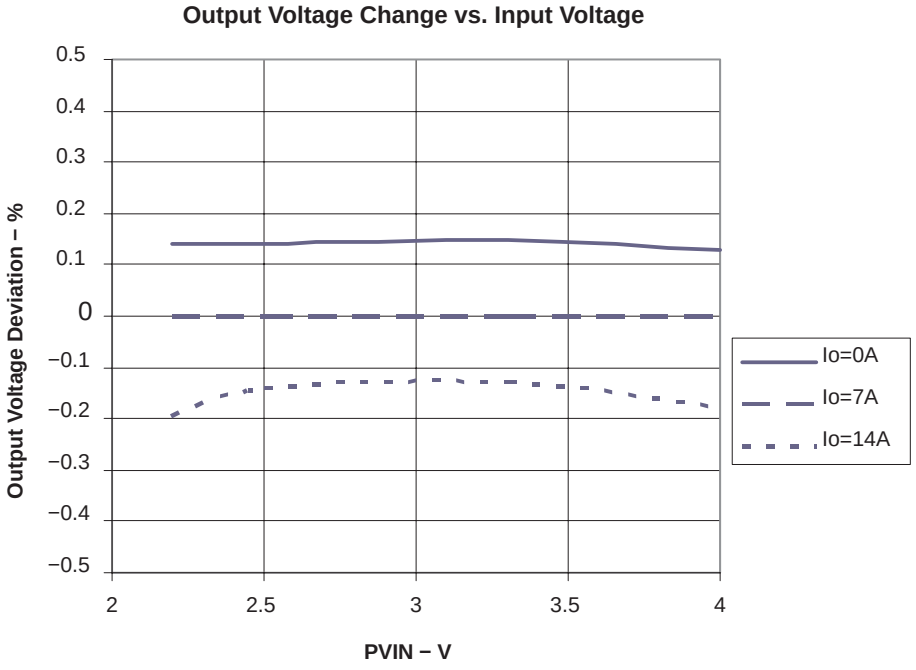


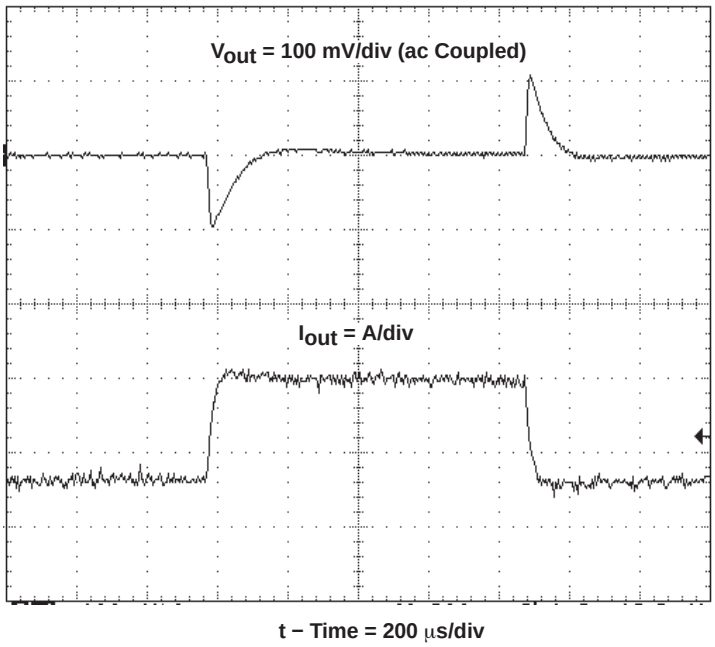
Figure 2−3. Line Regulation



2.4 Load Transients

The TPS54010EVM-067 response to load transients is shown in Figure 2−4. The current step is from 25 to 75 percent of maximum rated load. Total peak-to-peak voltage variation is as shown, including ripple and noise on the output.

Figure 2−4. Load Transient Response, TPS54010



2.5 Loop Characteristics

The TPS54010EVM-067 loop response characteristics are shown in Figure 2−5 and Figure 2−6. Gain and phase plots are shown for each device at PVIN voltages of 2.2 V and 3.5 V.

Figure 2−5. Measured Loop Response, TPS54010, PVIN = 2.2 V

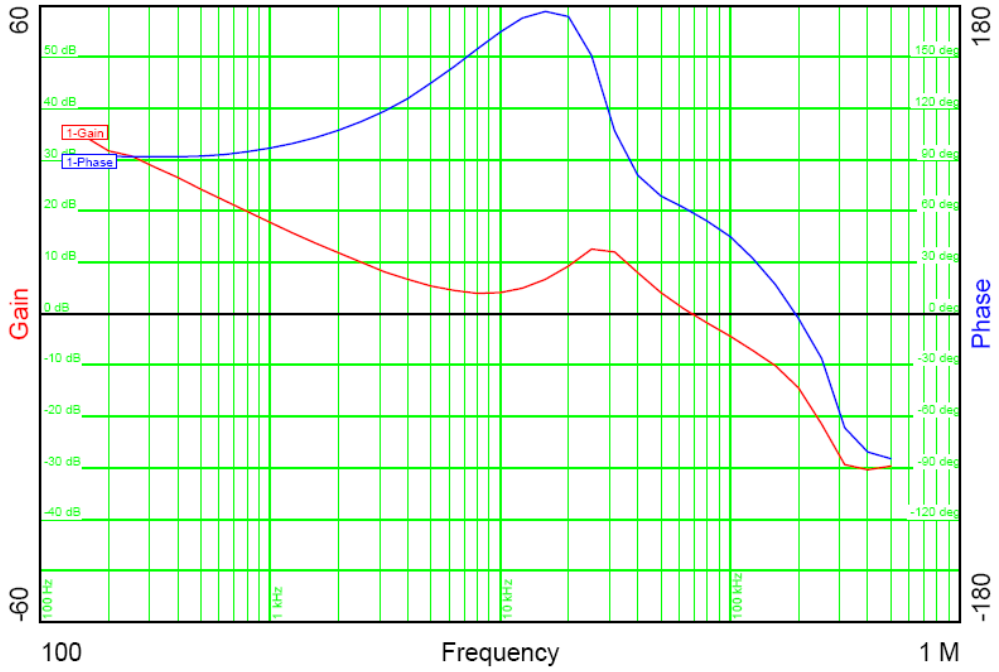
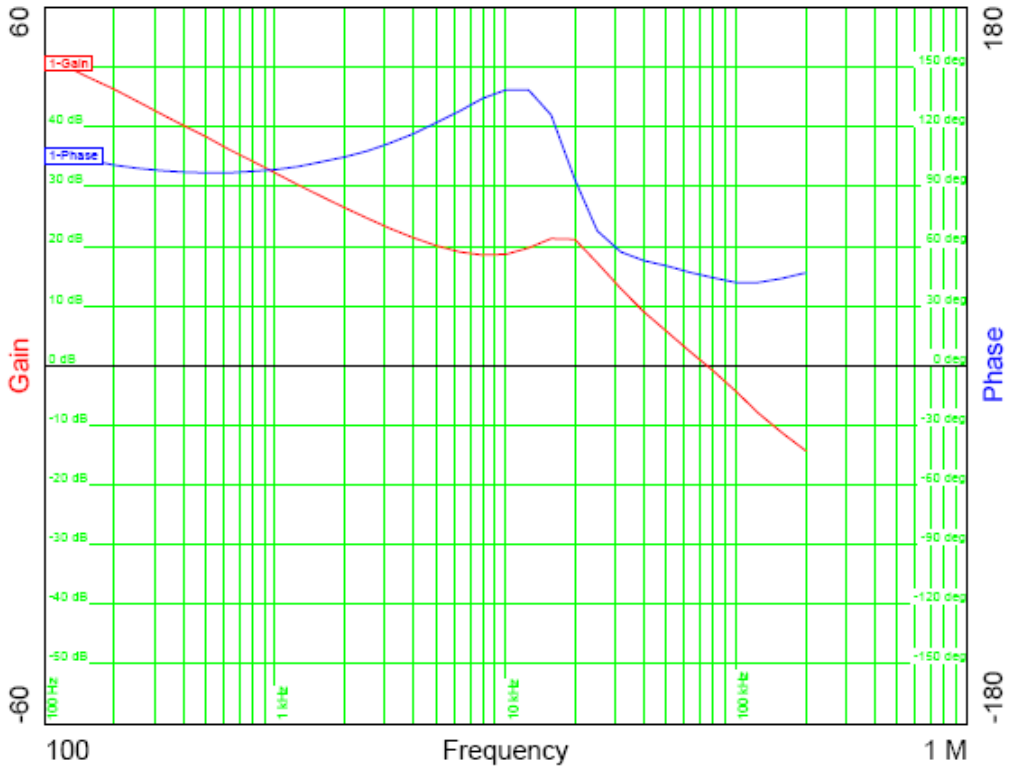


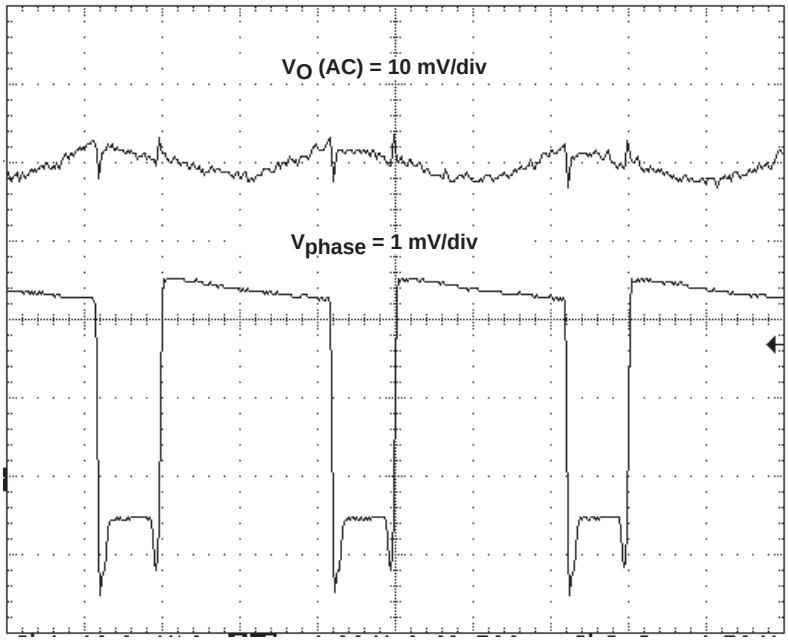
Figure 2−6. Measured Loop Response, TPS54010, VIN = 3.5 V



2.6 Output Voltage Ripple

The TPS54010EVM−067 output voltage ripple is shown in Figure 2−7. The input voltages are PVIN = 2.5 V and VIN = 3.3 V for the TPS54010. Output current is the rated full load of 14 A. Voltage is measured directly across output capacitors.

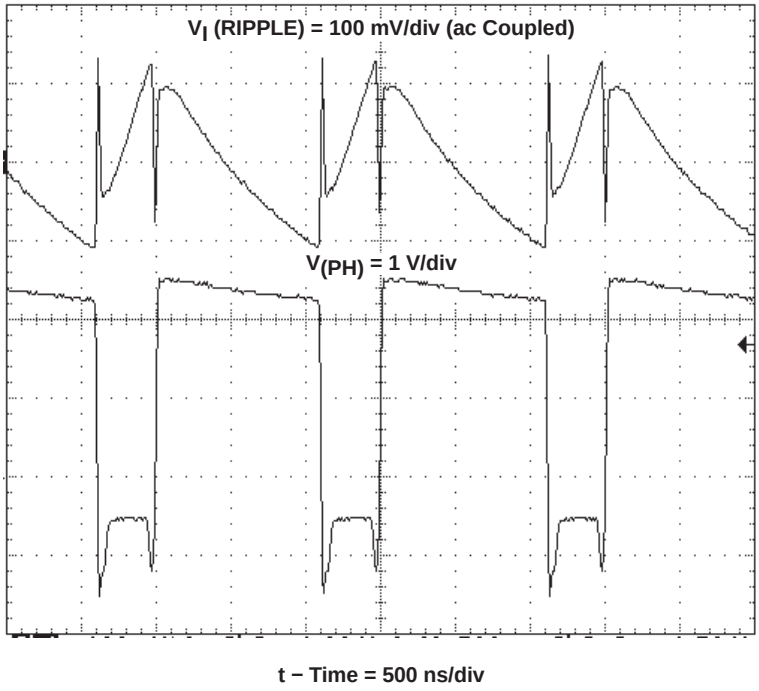
Figure 2−7. Measured Output Voltage Ripple, TPS54010



2.7 Input Voltage Ripple

The TPS54010EVM−067 output voltage ripple is shown in Figure 2−8. The input voltages PVIN = 2.5 V and VIN = 3.3 V for the TPS54010. Output current for each device is rated full load of 14 A.

Figure 2−8. Input Voltage Ripple, TPS54010



2.8 Powering Up and Down

The TPS54010EVM-067 start-up waveforms are shown in Figure 2−9 and Figure 2−10. In Figure 2−9, the top trace shows VIN charging up from 0 V to 3.3 V. When the input voltage reaches the internally set UVLO threshold voltage, the slow−start sequence begins. After a delay, Vo begins to ramp up linearly at the externally set slow−start rate toward 1.5 V. In this case, the PVIN voltage rail is already present at VIN power up. In Figure 2−10, the output voltage is shown relative to SS/ENA. PVIN and VIN are applied to the EVM while SS/ENA is held low, disabling the device. When SS/ENA is released, the slow−start voltage begins to ramp up at the externally set rate. When the SS/ENA voltage reaches the enable threshold voltage of 1.2 V, the output voltage begins to ramp up toward its final value of 1.5 V.

Figure 2−9. Power Up, VOUT Relative to VIN

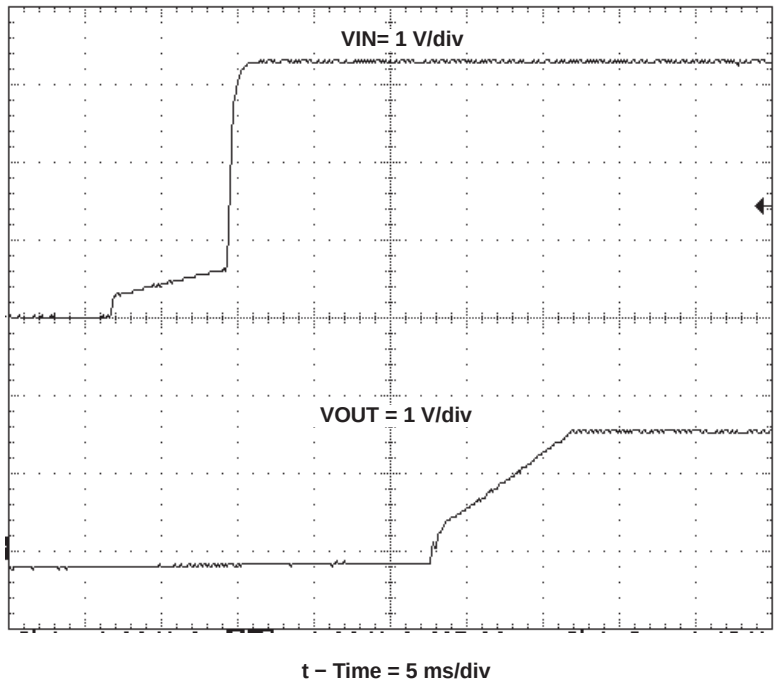
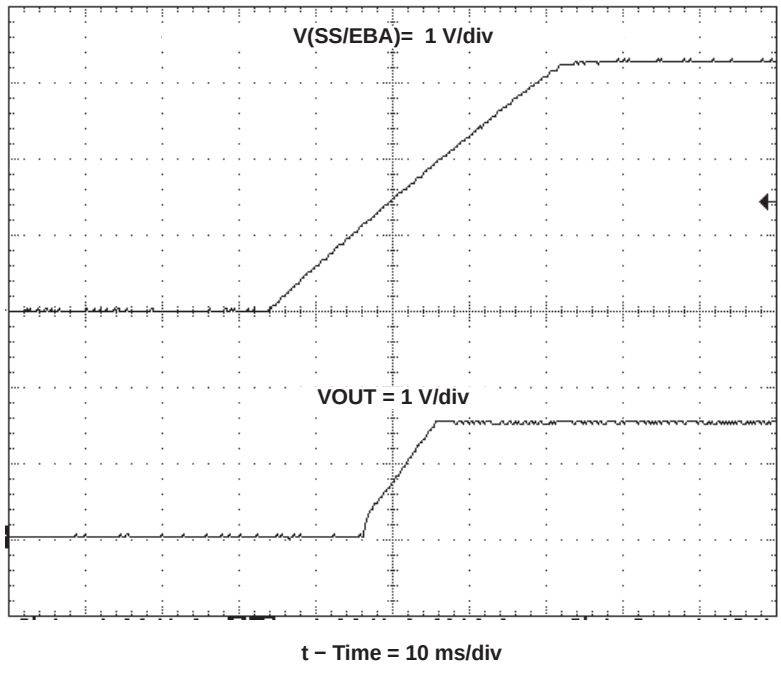


Figure 2−10. Power Up, VOUT Relative to SS/ENA



Chapter 3

Board Layout

This chapter provides a description of the TPS54010EVM−067 board layout and layer illustrations.

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3.1 Layout

The board layout for the TPS54010EVM-067 is shown in Figure 3−1 through NO TAG. The top−side layer of the TPS54010EVM-067 is laid out in a manner typical of a user application. The top, bottom, and internal ground layers are 2.0-oz. copper.

The top layer contains the main power traces for Vin, Vout, and Vphase. Also on the top layer are connections for the remaining pins of the TPS54010 and a large area filled with ground. The bottom layer contains ground and Vout copper areas, and some signal routing. The two internal layers are dedicated ground layers. The top and bottom and internal ground traces are connected with multiple vias placed around the board including 10 directly under the TPS54010 device to provide a thermal path from the PowerPAD™ land to ground.

The input decoupling capacitors (C1, C9, C10, and C11), bias decoupling capacitor (C4), and bootstrap capacitor (C3) are all located as close to the IC as possible. In addition, the compensation components are also located close to the IC. The compensation circuit ties to the output voltage at the point of regulation, adjacent to the high-frequency bypass output capacitor.

Figure 3−1. Top−Side Layout

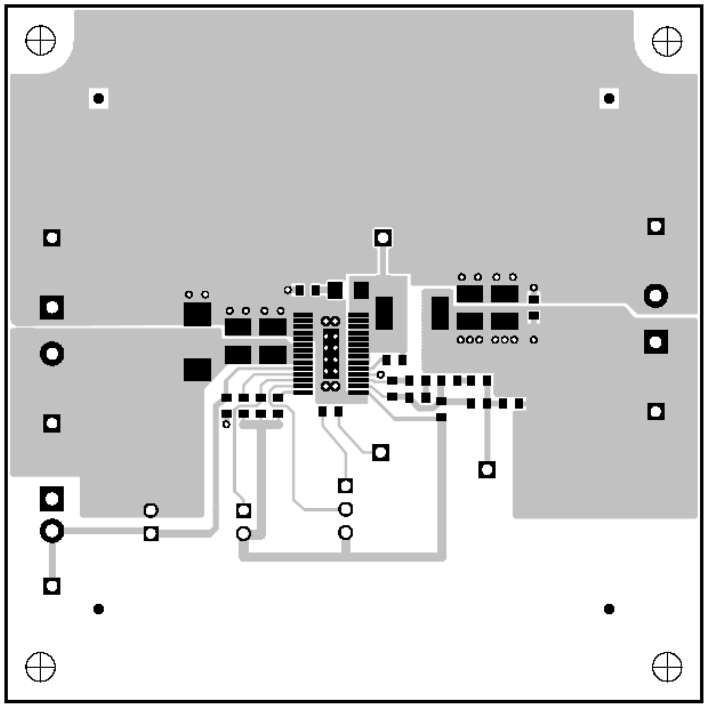


Figure 3−2. Internal Ground Layer 2

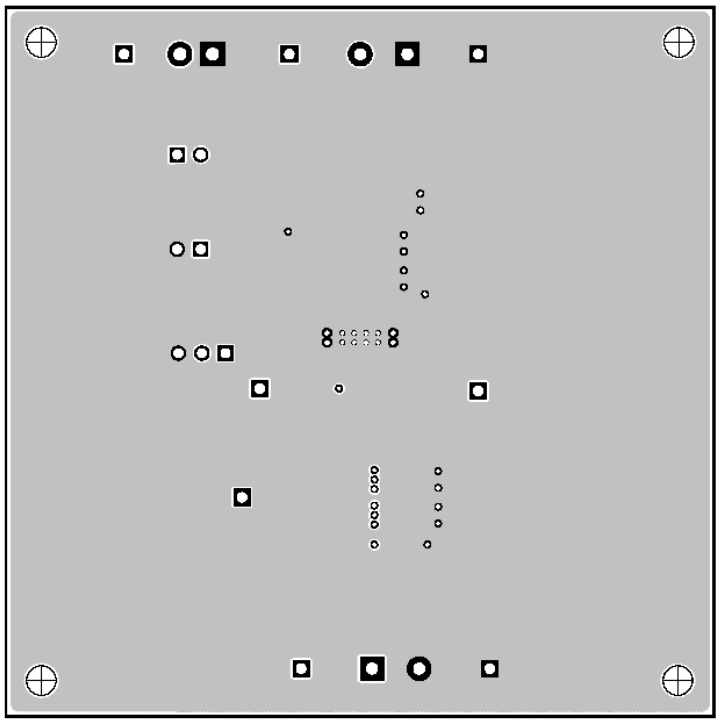


Figure 3−3. Internal Ground Layer 3

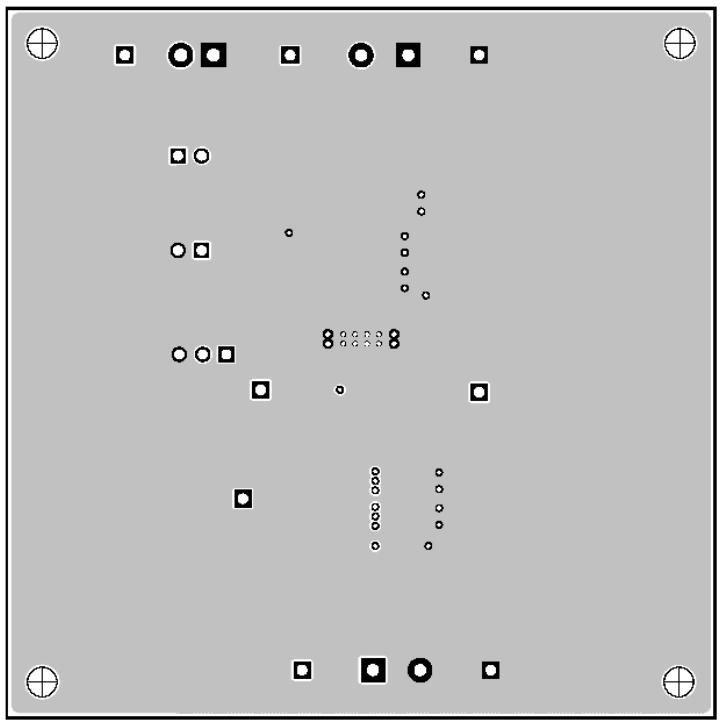


Figure 3−4. Bottom−Side Layout (Looking From Top Side)

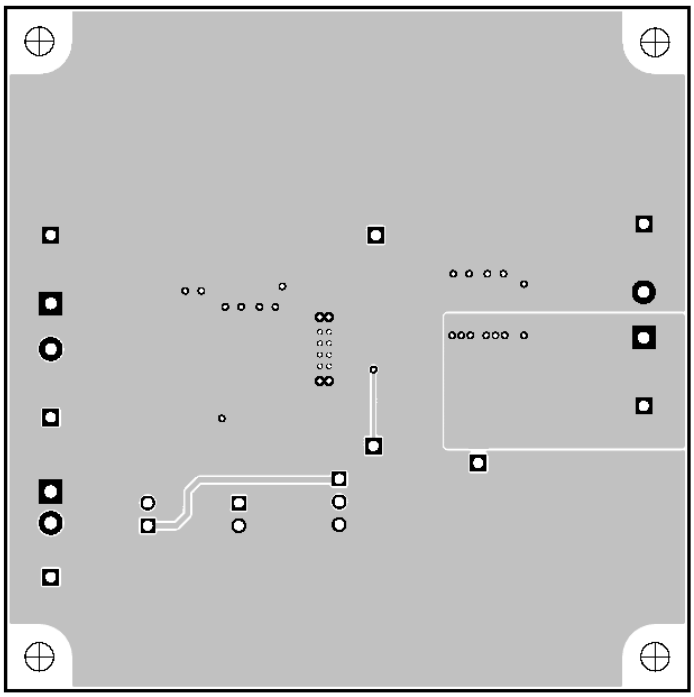
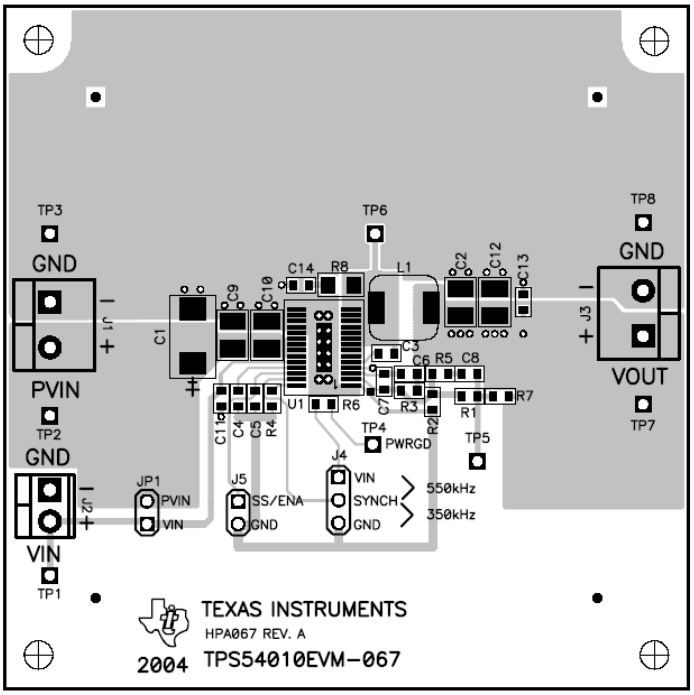


Figure 3−5. Top−SIde Assembly



Chapter 4

Schematic and Bill of Materials

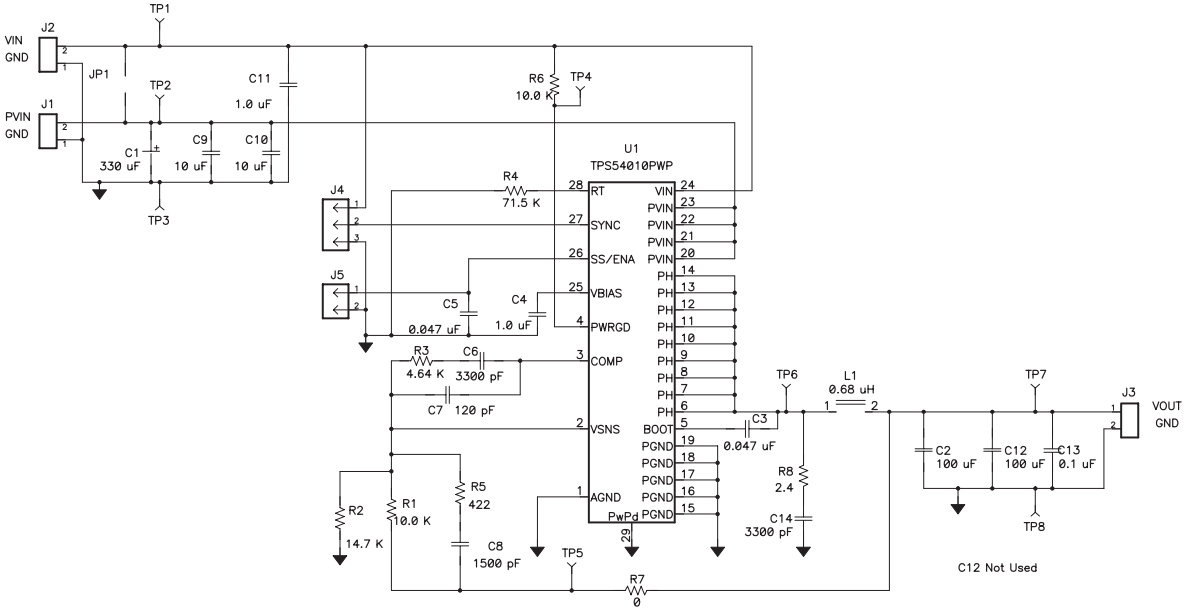
This chapter presents the TPS54010EVM−067 schematic and bill of materials.

Topic **Page**

4.1 Schematic

The schematic for the TPS54010EVM−067 is shown in Figure 4−1.

Figure 4−1. TPS54010EVM-067 Schematic



4.2 Bill of Materials

Table 4−1 contains the bill of materials for the TPS54010EVM−067.

Table 4−1. TPS54010EVM-067 Bill of Materials

Count	RefDes	Description	Size	MFR	Part Number
1	C1	Capacitor, POSCAP, 330-µF, 6.3−V, 10 µW, 20%	E	Sanyo	6TPD330M
1	C13	Capacitor, ceramic, 0.1-µF, 16−V, X7R, 10%	603	std	std
1	C2	Capacitor, ceramic, 100-µF 6.3−V, X5R, 20%	1210	TDK	C3225X5R0J107M
−	C12	Capacitor, ceramic, 100-µF, 6.3−V, X5R, 20%	1210	TDK	C3225X5R0J107M
2	C3, C5	Capacitor, ceramic, 0.047-µF, 25−V, X7R, 10%	603	std	std
2	C4, C11	Capacitor, ceramic, 1.0-µF, 10−V, X5R, 10%	603	std	std
2	C6, C14	Capacitor, ceramic, 3300-pF, 50−V, X7R, 10%	603	std	std
1	C7	Capacitor, ceramic, 120-pF, 50−V, NPO, 10%	603	std	std
1	C8	Capacitor, ceramic, 1500-pF, 50−V, X7R, 10%	603	std	std
2	C9, C10	Capacitor, ceramic, 10-µF 16−V, X5R, 20%	1210	TDK	C3225X5R1C106M
2	J1, J3	Terminal block, 2−pin, 15−A, 5,1 mm	148830	OST	ED1609
1	J2	Terminal block, 2−pin, 6−A, 3,5 mm	75525	OST	ED1514
1	J4	Header, 3−pin, 100 mil spacing, (36−pin strip)	0.100 x 3	Sullins	PTC36SAAN
2	J5, JP1	Header, 2−pin, 100 mil spacing, (36−pin strip)	0.100 x 2	Sullins	PTC36SAAN
3	—	Shunt, 100−mil, black	0.1	3M	929950−00
1	L1	Inductor, SMT, 0.68-µH, 25A, 6 mΩ	0.270 sq	Vishay	IHLP−2525CZ−01
2	R1, R6	Resistor, chip, 10.0 kΩ, 1/16−W, 1%	603	Std	Std
1	R2	Resistor, chip, 14.7 kΩ, 1/16−W, 1%	603	Std	Std
1	R3	Resistor, chip, 4.64 kΩ,, 1/16−W, 1%	603	Std	Std
1	R4	Resistor, chip, 71.5 kΩ, 1/16−W, 1%	603	Std	Std
1	R5	Resistor, chip, 422 Ω,, 1/16−W, 1%	603	std	std
1	R7	Resistor, chip, 0−Ω, 1/16−W, 1%	603	Std	Std
1	R8	Resistor, chip, 2.4−Ω, 1/8−W, 1%	1206	std	std
6	TP1, TP2, TP4, TP5, TP6, TP7	Test point, red, 1 mm	0.038”, 6400”	Farnell	240−345
2	TP3, TP8	Test point, black, 1 mm	0.038”, 6400”	Farnell	240−333
1	U1	IC, IFET power controller, 2.2 to 4−V, 14−A	PWP28	TI	TPS54010PWP
1	—	PCB, 3 In x 3 In x 0.062 In		Any	HPA067