LM5121/-Q1 Wide Input Synchronous Boost Controller with Disconnection Switch Control

1 Features

- AEC-Q100 Qualified with the following results:
  - Device Temperature Grade 1: -40°C to +125°C Ambient Operating Temperature Range
  - Device HBM ESD Classification Level 2
  - Device CDM ESD Classification Level C6
- Maximum Input Voltage: 65 V
- Min Input Voltage: 3.0 V (4.5 V for startup)
- Output Voltage Up to 100 V
- Bypass ($V_{OUT} = V_{IN}$) Operation
- 1.2-V Reference with ±1.0% Accuracy
- Free-Run/Synchronizable up to 1 MHz
- Peak Current Mode Control
- Robust Integrated 3-A Gate Drivers
- Adaptive Dead-Time Control
- Optional Diode Emulation Mode
- Programmable Cycle-by-Cycle Current Limit
- Programmable Line UVLO
- Programmable Soft-Start
- Thermal Shutdown Protection
- Low Shutdown Quiescent Current: 9 µA
- Programmable Slope Compensation
- Programmable Skip Cycle Mode Reduces Standby Power
- Supports External VCC Bias Supply Option
- Load Disconnection in Shutdown Mode (True Shutdown)
- Inrush Current Limiting
- Hiccup Mode Short Circuit/Overload Protection
- Circuit Breaker Function
- Capable of Input Transient Suppression
- Capable of Reverse Battery Protection
- Thermally Enhanced 20-Pin HTSSOP

2 Applications

- 12-V, 24-V, and 48-V Power Systems
- Automotive Start-Stop
- High Current Boost Power Supply
- Battery Powered System

3 Description

The LM5121 is a synchronous boost controller intended for high-efficiency, high-power boost regulator applications. The control method is based upon peak current mode control. Current mode control provides inherent line feed-forward, cycle-by-cycle current limiting and ease of loop compensation.

The switching frequency is programmable up to 1 MHz. Higher efficiency is achieved using two robust N-channel MOSFET gate drivers with adaptive dead-time control. A user-selectable diode emulation mode enables discontinuous mode operation for improved efficiency at light load conditions.

The LM5121 provides disconnection switch control which completely disconnects the output from the input during an output short or a shutdown condition. During start-up sequence, inrush current is limited by the disconnection switch control.

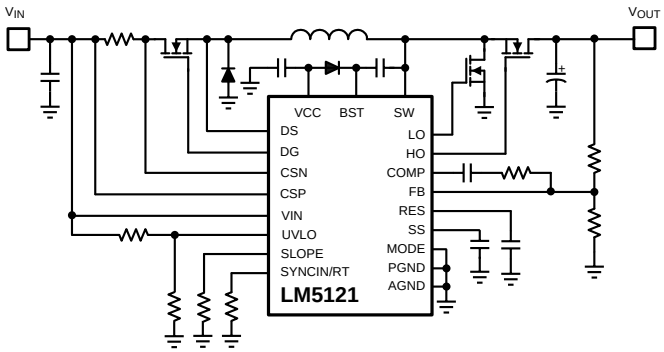
An internal charge pump allows 100% duty cycle operation of the high-side synchronous switch (Bypass operation). Additional features include thermal shutdown, frequency synchronization, hiccup mode current limit and adjustable line undervoltage lockout.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LM5121	HTSSOP (20)	6.50 mm x 4.40 mm
LM5121-Q1		

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Simplified Application Diagram



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4 Revision History

Changes from Revision B (December 2014) to Revision C	Page
• Added Automotive ESD Features	1
• Changed equation	20

Changes from Revision A (September 2013) to Revision B	Page
• Added *Pin Configuration and Functions* section, *Handling Rating* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1

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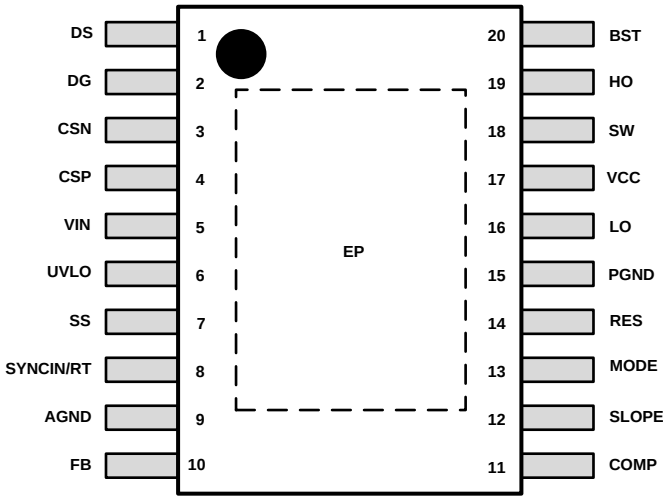
5 Pin Configuration and Functions

HTSSOP
PWP Package
TOP VIEW



Pin Functions

PIN		I/O(1)	DESCRIPTION
NAME	NO.		
AGND	9	G	Analog ground connection. Return for the internal voltage reference and analog circuits.
BST	20	P/I	High-side driver supply for bootstrap gate drive. Connect to the cathode of the external bootstrap diode and to the bootstrap capacitor. The bootstrap capacitor supplies current to charge the high-side N-channel MOSFET gate and should be placed as close to controller as possible. An internal BST charge pump will supply 200 µA current into bootstrap capacitor for bypass operation.
COMP	11	O	Output of the internal error amplifier. The loop compensation network should be connected between this pin and the FB pin.
CSN	3	I	Inverting input of current sense amplifier. Connect to the negative-side of the current sense resistor.
CSP	4	I	Non-inverting input of current sense amplifier. Connect to the positive-side of the current sense resistor.
DG	2	O	Disconnection switch control pin. Connect to the gate terminal of the N-channel MOSFET disconnection switch.
DS	1	I/O	Source connection of N-channel MOSFET disconnection switch. Connect to the source terminal of the disconnection switch, the cathode terminal of the freewheeling diode and the supply input of boost inductor.
EP	EP	N/A	Exposed pad of the package. No internal electrical connections. Should be soldered to the large ground plane to reduce thermal resistance.
FB	10	I	Feedback. Inverting input of the internal error amplifier. A resistor divider from the output to this pin sets the output voltage level. The regulation threshold at the FB pin is 1.2 V.
HO	19	O	High-side N-channel MOSFET gate drive output. Connect to the gate of the high-side synchronous N-channel MOSFET switch through a short, low inductance path.
LO	16	O	Low-side N-channel MOSFET gate drive output. Connect to the gate of the low-side N-channel MOSFET switch through a short, low inductance path.
MODE	13	I	Switching mode selection pin. Internal 700 kΩ pull-up and 100 kΩ pull-down resistor hold MODE pin to 0.15 V as a default. By adding external pull-up or pull-down resistor, MODE pin voltage can be programmed. When MODE pin voltage is greater than 1.2 V, diode emulation mode threshold, forced PWM mode is enabled, allowing current to flow in either direction through the high-side N-channel MOSFET switch. When MODE pin voltage is less than 1.2 V, the controller works in diode emulation mode. Skip cycle comparator is activated as a default condition when the MODE pin is left floating. If the MODE pin is grounded, the controller still operates in diode emulation mode, but the skip cycle comparator will not be triggered in normal operation, this enables pulse skipping operation at light load.

(1) G = Ground, I = Input, O = Output, P = Power

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Pin Functions (continued)

PIN		I/O[1]	DESCRIPTION
NAME	NO.		
PGND	15	G	Power ground connection pin for low-side N-channel MOSFET gate driver. Connect directly to the source terminal of the low-side N-channel MOSFET switch.
RES	14	O	The restart timer pin for an external capacitor that configures hiccup mode off-time and restart delay during over load conditions and hiccup mode short circuit protection. Connect directly to the AGND when hiccup mode operation is not required.
SLOPE	12	I	Slope compensation is programmed by an external resistor between SLOPE and the AGND.
SS	7	I	Soft-start programming pin. An external capacitor and an internal 10 µA current source set the ramp rate of the internal error amplifier reference during soft-start.
SW	18	I/O	Switching node of the boost regulator. Connect to the bootstrap capacitor, the source terminal of the high-side N-channel MOSFET switch and the drain terminal of the low-side N-channel MOSFET switch through short, low inductance paths.
SYNCIN/RT	8	I	The internal oscillator frequency is programmed by an external resistor between RT and the AGND. The internal oscillator can be synchronized to an external clock by applying a positive pulse signal into this pin. The recommended maximum internal oscillator frequency is 2 MHz which leads to 1 MHz maximum switching frequency.
UVLO	6	I	Undervoltage lockout programming pin. If the UVLO pin is below 0.4 V, the regulator is in the shutdown mode with all functions disabled. If the UVLO pin voltage is greater than 0.4 V and below 1.2 V, the regulator is in standby mode with the VCC regulator operational and no switching at the HO and LO outputs. If the UVLO pin voltage is above 1.2 V, the startup sequence begins. A 10 µA current source at UVLO pin is enabled when UVLO exceeds 1.2 V and flows through the external UVLO resistors to provide hysteresis. The UVLO pin should not be left floating.
VCC	17	P/O/I	VCC bias supply pin. Locally decouple to PGND using a low ESR/ESL capacitor located as close to controller as possible.
VIN	5	P/I	Supply voltage input source for the VCC regulator. Connect to the input capacitor and source power supply connection with short, low impedance paths.

6 Specifications

6.1 Absolute Maximum Ratings[1]

Over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Input	VIN, CSP, CSN	–0.3	75	V
	BST to SW, FB, MODE, UVLO, VCC[2]	–0.3	15	
	SW	–5.0	105	
	BST	–0.3	115	
	SS, SLOPE, SYNCIN/RT	–0.3	7	
	CSP to CSN, PGND	–0.3	0.3	
Output[3]	DG to DS	–3.0	18	
	DG to VIN	–75	15	
	DS	–3.0	75	
	HO to SW	–0.3	BST to SW+0.3	
	LO	–0.3	VCC+0.3	
	COMP, RES	–0.3	7	
Thermal	Junction Temperature	–40	150	ºC
T_{stg}	Storage temperature range	–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* are not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. Unless otherwise specified, all voltages are referenced to AGND pin.
(2) See Application Information when input supply voltage is less than the VCC voltage.
(3) All output pins are not specified to have an external voltage applied.

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6.2 ESD Ratings: LM5121

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2	kV
		Charged device model (CDM), per JEDED specification JESD22-C101 (2)	±1	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 ESD Ratings: LM5121-Q1

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002 (1)		±2	kV
		Charged device model (CDM), per AEC Q100-011	Corner pins	±1	
			Other pins		

(1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.4 Recommended Operating Conditions (1)

Over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Input supply voltage (2)	VIN	4.5		65	V
Disconnection switch voltage (2)	DG, DS	3.0		65	
Low-side driver bias voltage	VCC			14	
High-side driver bias voltage	BST to SW	3.8		14	
Current sense common mode range (2)	CSP, CSN	3.0		65	
Switch node voltage	SW			100	
Junction temperature	T_J	–40		125	ºC

(1) *Recommended Operating Conditions* are conditions under which operation of the device is intended to be functional, but does not guarantee specific performance limits.
(2) Minimum VIN operating voltage is always 4.5 V. The minimum input power supply voltage can be 3.0 V after start-up, assuming VIN voltage is supplied from an available external source.

6.5 Thermal Information

THERMAL METRIC (1)		LM5121, LM5121-Q1 PWP (HTSSOP) 20 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance (Typ.)	40	ºC/W
$R_{\theta JC(bot)}$	Junction-to-case (bot) thermal resistance (Typ.)	4	ºC/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.6 Electrical Characteristics

Unless otherwise specified, these specifications apply for –40°C ≤ T_J ≤ +125°C, V_{VIN} = 12 V, V_{VCC} = 8.3 V, R_T = 20 kΩ, no load on LO and HO. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VIN SUPPLY						
$I_{SHUTDOWN}$	VIN shutdown current	V_{UVLO} = 0 V		9	17	µA
I_{BIAS}	VIN operating current (exclude the current into RT resistor)	V_{UVLO} = 2 V, non-switching		4	5	mA
VCC REGULATOR						
$V_{CC(REG)}$	VCC regulation	No load	6.9	7.6	8.3	V
	VCC dropout (VIN to VCC)	V_{VIN} = 4.5 V, no external load			0.25	V
		V_{VIN} = 4.5 V, I_{VCC} = 25 mA		0.28	0.5	V
	VCC sourcing current limit	V_{VCC} = 0 V	50	62		mA
I_{VCC}	VCC operating current (exclude the current into RT resistor)	V_{VCC} = 8.3 V		3.5	5	mA
		V_{VCC} = 12 V		4.5	8	mA
	VCC undervoltage threshold	VCC rising, V_{VIN} = 4.5 V	3.9	4.0	4.1	V
		VCC falling, V_{VIN} = 4.5 V			3.7	V
	VCC undervoltage hysteresis			0.385		V
UNDERVOLTAGE LOCKOUT						
	UVLO threshold	UVLO rising	1.17	1.20	1.23	V
	UVLO hysteresis current	V_{UVLO} = 1.4 V	7	10	13	µA
	UVLO standby threshold	UVLO rising	0.3	0.4	0.5	V
	UVLO standby hysteresis			0.1	0.125	V
MODE						
	Diode emulation mode threshold	MODE rising	1.20	1.24	1.28	V
	Diode emulation mode hysteresis			0.1		V
	Default MODE voltage		145	155	170	mV
	Default skip cycle threshold	COMP rising, measured at COMP		1.290		V
		COMP falling, measured at COMP		1.245		V
	Skip cycle hysteresis	Measured at COMP		40		mV
ERROR AMPLIFIER						
V_{REF}	FB reference voltage	Measured at FB, V_{FB}= V_{COMP}	1.188	1.200	1.212	V
	FB input bias current	V_{FB}= V_{REF}		5		nA
V_{OH}	COMP output high voltage	I_{SOURCE} = 2 mA, V_{VCC} = 4.5 V	2.75			V
		I_{SOURCE} = 2 mA, V_{VCC} = 12 V	3.40			V
V_{OL}	COMP output low voltage	I_{SINK} = 2 mA			0.25	V
A_{OL}	DC gain			80		dB
f_{BW}	Unity gain bandwidth			3		MHz
OSCILLATOR						
f_{SW1}	Switching frequency 1	R_T = 20 kΩ	400	450	500	kHz
f_{SW2}	Switching frequency 2	R_T = 10 kΩ	775	875	975	kHz
	RT output voltage			1.2		V
	RT sync rising threshold	RT rising		2.5	2.9	V
	RT sync falling threshold	RT falling	1.6	2.0		V
	Minimum sync pulse width		100			ns
DISCONNECTION SWITCH CONTROL						
$I_{DIS-SOURCE}$	DG current source	UVLO = 2 V, Sourcing		25		uA
$I_{DIS-SINK}$	DG current sink	Inrush Control, Sinking		67		uA

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Electrical Characteristics (continued)

Unless otherwise specified, these specifications apply for –40°C ≤ T_J ≤ +125°C, V_{VIN} = 12 V, V_{VCC} = 8.3 V, R_T = 20 kΩ, no load on LO and HO. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	DG discharge switch R_{DS-ON}	Circuit Breaker		38		Ω
	DG charge pump regulation	DG to VIN, No load, V_{VIN} = 4.5 V	9.5	10.5	11.5	V
		DG to VIN, No load, V_{VIN} = 12 V			12.5	
V_{GS-DET}	V_{GS} detection threshold	DG to DS, Rising, V_{VIN} = 12 V	4.0	5.4	6.5	
	V_{GS} detection hysteresis			0.2		
	Transconductance gain	CSP to CSN to I_{DG}		12		uA/mV
SLOPE COMPENSATION						
	SLOPE output voltage		1.17	1.20	1.23	V
V_{SLOPE}	Slope compensation amplitude	R_{SLOPE} = 20 kΩ, f_{SW} = 100 kHz, 50% duty cycle, T_J = –40ºC to +125ºC	1.375	1.650	1.925	
		R_{SLOPE}= 20 kΩ, f_{SW}= 100 kHz, 50% duty cycle, T_J = 25ºC	1.400	1.650	1.900	
SOFT-START						
$I_{SS-SOURCE}$	SS current source	V_{SS} = 0 V	7.5	10	12	µA
	SS discharge switch R_{DS-ON}			13		Ω
PWM COMPARATOR						
t_{LO-OFF}	Forced LO off-time	V_{VCC} = 5.5 V		420	550	ns
		V_{VCC} = 4.5 V		360	500	
t_{ON-MIN}	Minimum LO on-time	R_{SLOPE} = 20 kΩ		150		
		R_{SLOPE} = 200 kΩ		300		
	COMP to PWM voltage drop	T_J = –40ºC to +125ºC	0.95	1.10	1.25	V
		T_J = 25ºC	1.00	1.10	1.20	
CURRENT SENSE / CYCLE-BY-CYCLE CURRENT LIMIT						
V_{CS-TH1}	Cycle-by-cycle current limit threshold	CSP to CSN, T_J = –40ºC to +125ºC	65.5	75.0	87.5	mV
		CSP to CSN, T_J = 25ºC	67.0	75.0	86.0	
		V_{CS-TH2} –V_{CS-TH1}	5			
V_{CS-TH2}	Inrush current limit threshold	CSP to CSN	80	110	133	
V_{CS-TH3}	Circuit breaker enable threshold	CSP to CSN, Rising	143	160	170	
		V_{CS-TH3} – V_{CS-TH2}	20			
V_{CS-TH4}	Circuit breaker disable threshold	CSP to CSN, Falling	4.0	11.5	16.0	
V_{CS-ZCD}	Zero cross detection threshold	CSP to CSN, Rising		7		
		CSP to CSN, Falling	0.3	6	12	
	Current sense amplifier gain			10		V/V
I_{CSP}	CSP input bias current			12		µA
I_{CSN}	CSN input bias current			11		
	Bias current matching	I_{CSP} to I_{CSN}	–1.75	1	3.75	
	CS to LO delay	Current sense / current limit delay		150		ns
HICCUP MODE RESTART						
V_{RES}	Restart threshold	RES rising	1.15	1.20	1.25	V
$V_{HCP-UPPER}$	Hiccup counter upper threshold	RES rising		4.2		
		RES rising, V_{VIN} = V_{VCC} = 4.5 V		3.6		
$V_{HCP-LOWER}$	Hiccup counter lower threshold	RES falling		2.15		
		RES falling, V_{VIN} = V_{VCC} = 4.5 V		1.85		

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Electrical Characteristics (continued)

Unless otherwise specified, these specifications apply for –40°C ≤ T_J ≤ +125°C, V_{VIN} = 12 V, V_{VCC} = 8.3 V, R_T = 20 kΩ, no load on LO and HO. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{RES-SOURCE1}$	RES current source1	Fault-state charging current	20	30	40	µA
$I_{RES-SINK1}$	RES current sink1	Normal-state discharging current		5		
$I_{RES-SOURCE2}$	RES current source2	Hiccup mode off-time charging current		10		
$I_{RES-SINK2}$	RES current sink2	Hiccup mode off-time discharging current		5		
	Hiccup cycle			8		Cycles
	RES discharge switch R_{DS-ON}			40		Ω
	Ratio of hiccup mode off-time to restart delay time			122		
HO GATE DRIVER						
V_{OHH}	HO high-state voltage drop	I_{HO} = –100 mA, V_{OHH} = V_{BST} – V_{HO}		0.15	0.24	V
V_{OLH}	HO low-state voltage drop	I_{HO} = 100 mA, V_{OLH} = V_{HO} – V_{SW}		0.1	0.18	
	HO rise time (10% to 90%)	C_{LOAD} = 4700 pF, V_{BST} = 12 V		25		ns
	HO fall time (90% to 10%)	C_{LOAD} = 4700 pF, V_{BST} = 12 V		20		
I_{OHH}	Peak HO source current	V_{HO} = 0 V, V_{SW} = 0 V, V_{BST} = 4.5 V		0.8		A
		V_{HO} = 0 V, V_{SW} = 0 V, V_{BST} = 7.6 V		1.9		
I_{OLH}	Peak HO sink current	V_{HO} = V_{BST} = 4.5 V		1.9		
		V_{HO} = V_{BST} = 7.6 V		3.2		
I_{BST}	BST charge pump sourcing current	V_{VIN} = V_{SW} = 9.0 V , V_{BST} - V_{SW} = 5.0 V	90	200		µA
	BST charge pump regulation	BST to SW, I_{BST}= –70 µA, V_{VIN} = V_{SW} = 9.0 V	5.3	6.2	6.75	V
		BST to SW, I_{BST} = –70 µA, V_{VIN} = V_{SW} = 12 V	7	8.5	9	
	BST to SW undervoltage		2.0	3.0	3.5	
	BST DC bias current	V_{BST} - V_{SW} = 12 V, V_{SW} = 0 V		30	45	µA
LO GATE DRIVER						
V_{OHL}	LO high-state voltage drop	I_{LO} = –100 mA, V_{OHL} = V_{VCC} – V_{LO}		0.15	0.25	V
V_{OLL}	LO low-state voltage drop	I_{LO} = 100 mA, V_{OLL} = V_{LO}		0.1	0.17	
	LO rise time (10% to 90%)	C_{LOAD} = 4700 pF		25		ns
	LO fall time (90% to 10%)	C_{LOAD} = 4700 pF		20		
I_{OHL}	Peak LO source current	V_{LO} = 0 V, V_{VCC} = 4.5 V		0.8		A
		V_{LO} = 0 V		2.0		
I_{OLL}	Peak LO sink current	V_{LO} = V_{VCC} = 4.5 V		1.8		
		V_{LO} = V_{VCC}		3.2		
SWITCHING CHARACTERISTICS						
t_{DLH}	LO fall to HO rise delay	No load, 50% to 50%	50	80	115	ns
t_{DHL}	HO fall to LO rise delay	No load, 50% to 50%	60	80	105	
THERMAL						
T_{SD}	Thermal shutdown	Temperature rising		165		ºC
	Thermal shutdown hysteresis			25		

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6.7 Typical Characteristics

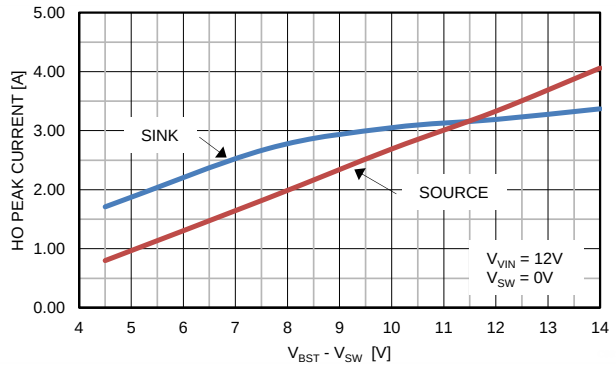

Figure 1. HO Peak Current vs V_{BST} - V_{SW}

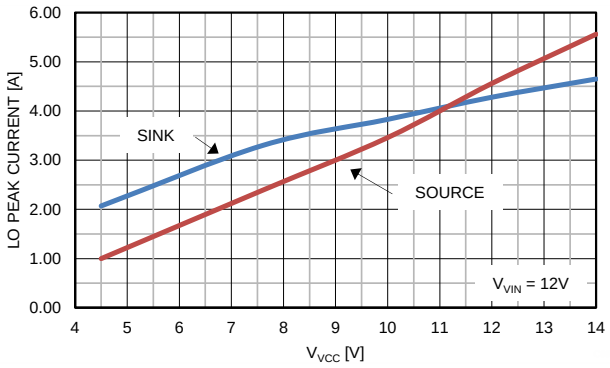

Figure 2. LO Peak Current vs V_{VCC}

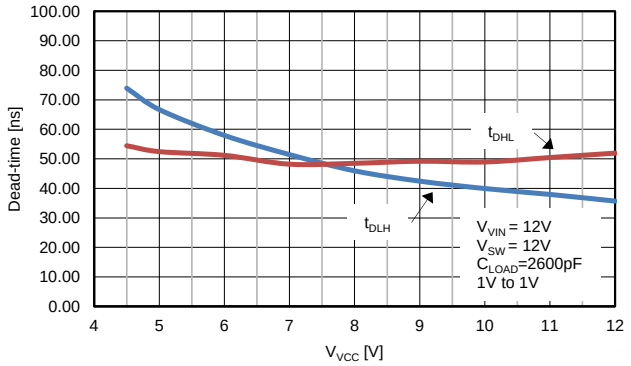

Figure 3. Dead Time vs V_{VCC}

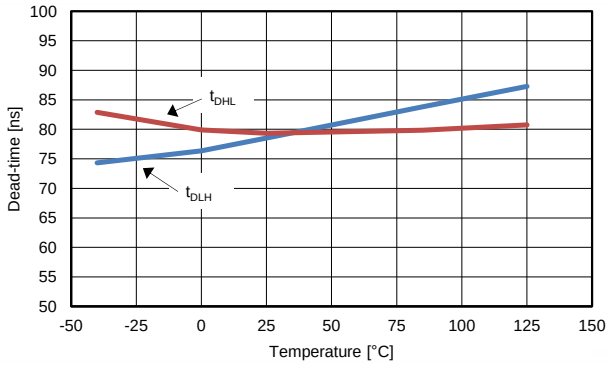

Figure 4. Dead Time vs Temperature

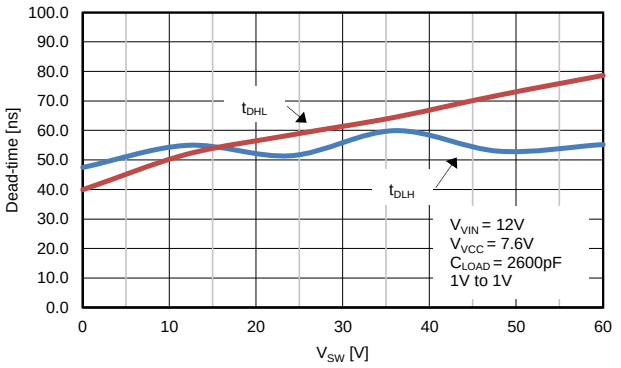

Figure 5. Dead Time vs V_{SW}

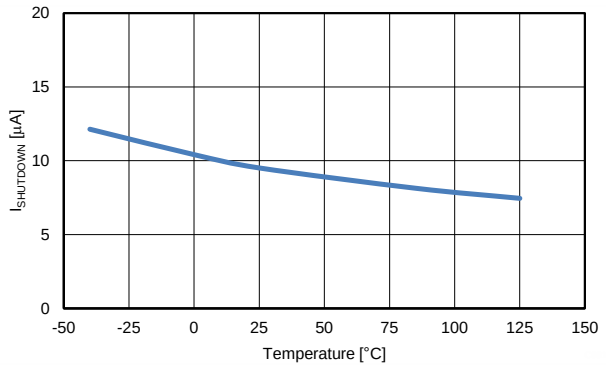

Figure 6. $I_{SHUTDOWN}$ vs Temperature

Typical Characteristics (continued)

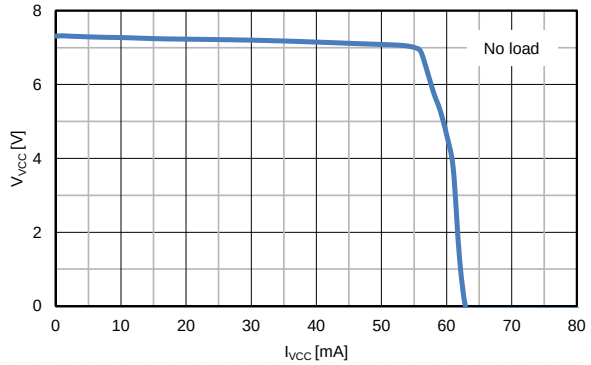

Figure 7. V_{VCC} vs I_{VCC}

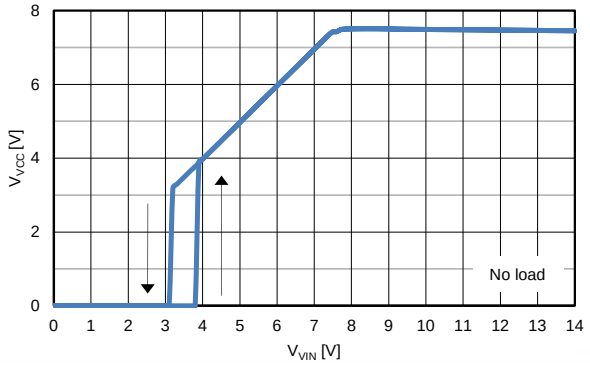

Figure 8. V_{VCC} vs V_{VIN}

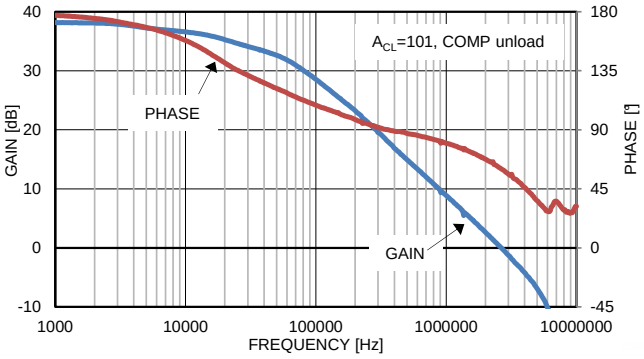

Figure 9. Error Amp Gain and Phase vs Frequency

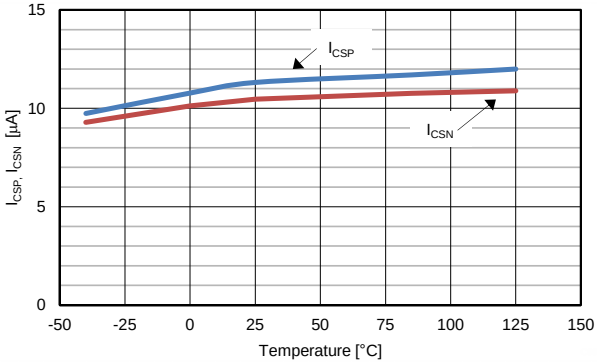

Figure 10. I_{CSP}, I_{CSN} vs Temperature

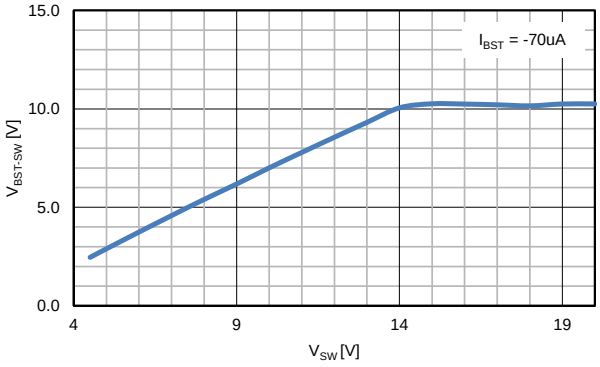

Figure 11. V_{BST-SW} vs V_{SW}

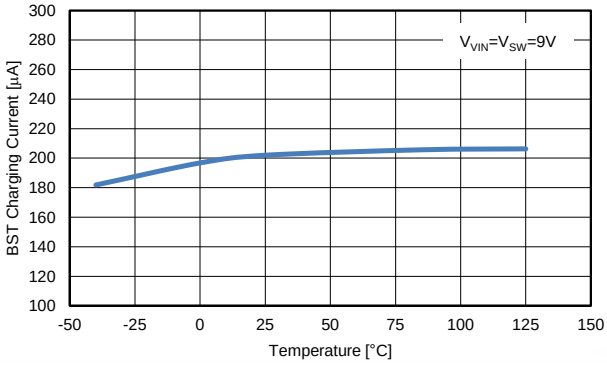

Figure 12. I_{BST} vs Temperature

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Typical Characteristics (continued)

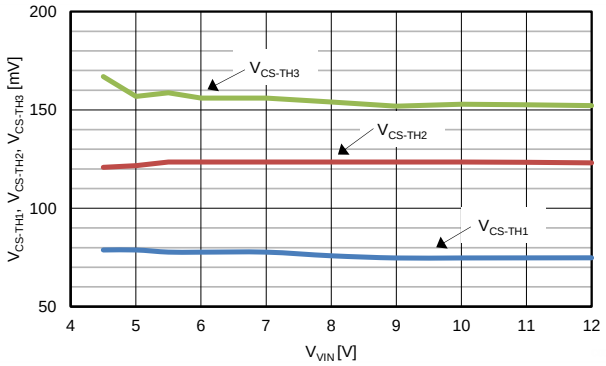


Figure 13. V_{CS-TH1}, V_{CS-TH2}, V_{CS-TH3} vs V_{VIN}

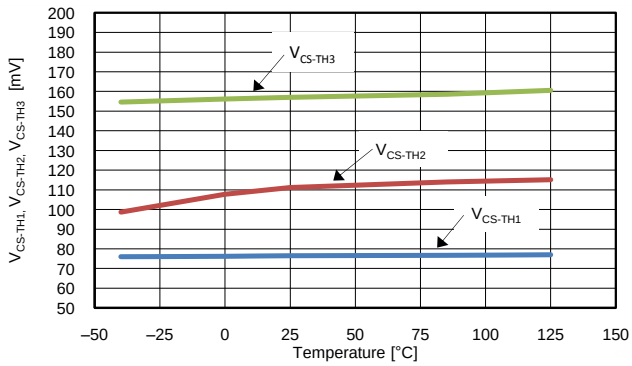


Figure 14. V_{CS-TH1} V_{CS-TH2}, V_{CS-TH3} vs Temperature

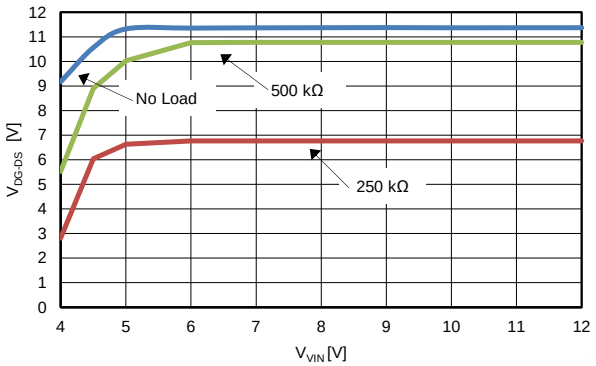


Figure 15. V_{DG-DS} vs V_{VIN}

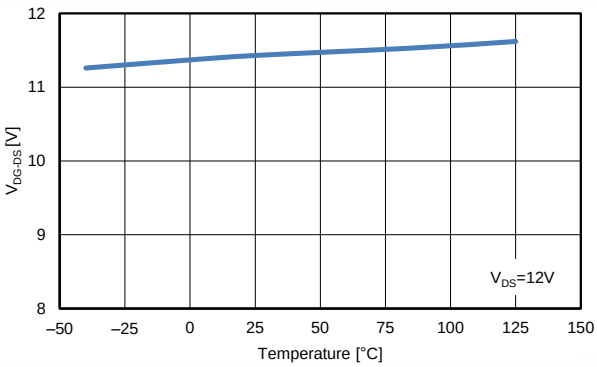


Figure 16. V_{DG-DS} vs Temperature

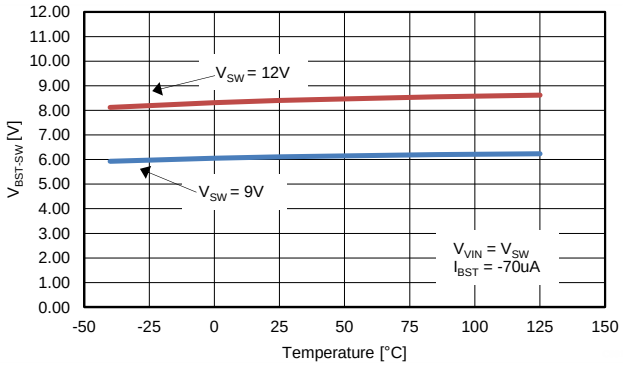


Figure 17. V_{BST-SW} vs Temperature

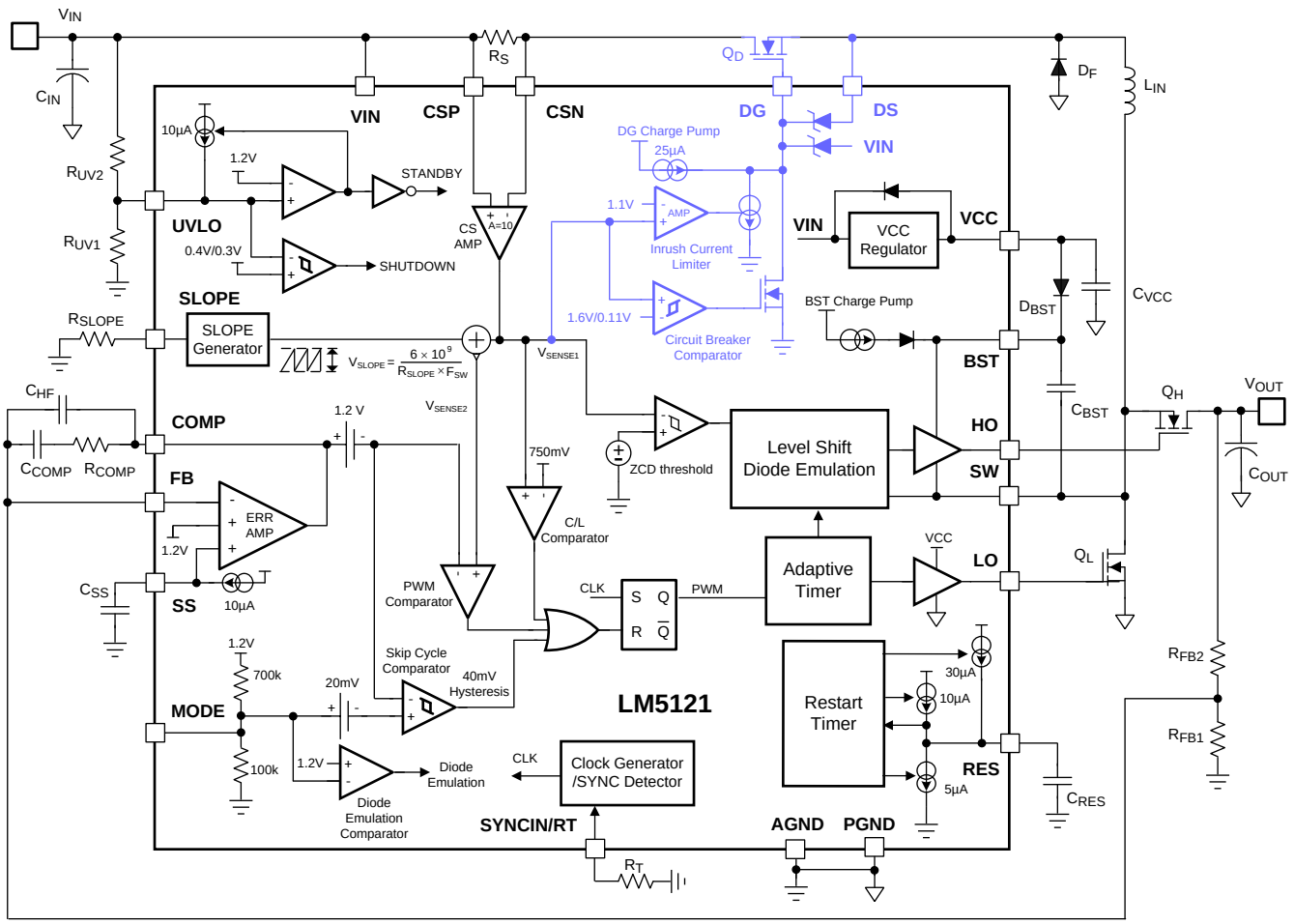
7 Detailed Description

7.1 Overview

The LM5121 wide input range synchronous boost controller features all of the functions necessary to implement a highly efficient synchronous boost regulator. The regulator control method is based upon peak current mode control. Peak current mode control provides inherent line feed-forward and ease of loop compensation. This highly integrated controller provides strong high-side and low-side N-channel MOSFET drivers with adaptive dead-time control. The switching frequency is user programmable up to 1 MHz, either set by a single resistor or synchronized to an external clock.

The control mode of high-side synchronous switch can be configured as either forced PWM (FPWM) or diode emulation mode. Fault protection features include cycle-by-cycle current limiting, hiccup mode over load protection, hiccup mode short circuit protection, thermal shutdown and remote shutdown capability by pulling down the UVLO pin. The UVLO input enables the controller when the input voltage reaches a user selected threshold, and provides tiny 9 µA shutdown quiescent current when pulled low. LM5121's unique disconnection switch control provides numerous additional advantages. True Shutdown allows disconnecting load from the input, blocking leakage current paths in shutdown mode. Inrush current control limits input current during initial charging of the output capacitor. Circuit breaker function quickly switches off the disconnection switch, terminating any severe over-current condition. Hiccup mode short circuit protection minimizes power dissipation during prolonged output short condition. Input over voltage suppression can be achieved by connecting a Zener diode from the disconnection MOSFET gate pin to ground. The device is available in 20-pin HTSSOP package featuring an exposed pad to aid in thermal dissipation.

7.2 Functional Block Diagram



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7.3 Feature Description

7.3.1 Undervoltage Lockout (UVLO)

The LM5121 features a dual level UVLO circuit. When the UVLO pin voltage is less than the 0.4-V UVLO standby threshold, the LM5121 is in the shutdown mode with all functions disabled. The shutdown comparator provides 0.1 V of hysteresis to avoid chatter during transitions. If the UVLO pin voltage is greater than 0.4 V and below 1.2 V during power up, the controller is in the standby mode with the VCC regulator operational, the disconnection switch disabled and no switching at the HO and LO outputs. This feature allows the UVLO pin to be used as a remote shutdown function by pulling the UVLO pin down below the UVLO standby threshold with an external open collector or open drain device.

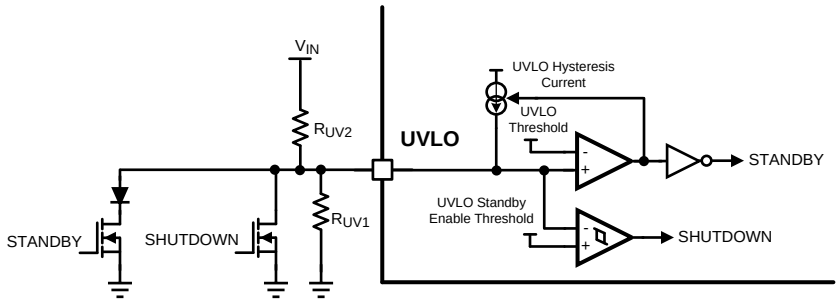

Figure 18. UVLO Remote Standby and Shutdown Control

If the UVLO pin voltage is above 1.2-V UVLO threshold and VCC voltage exceeds the VCC UV threshold, the startup sequence begins. UVLO hysteresis is accomplished with an internal 10-µA current source that is switched on or off into the impedance of the UVLO setpoint divider. When the UVLO pin voltage exceeds the 1.2 V, the current source is enabled to quickly raise the voltage at the UVLO pin. When the UVLO pin voltage falls below the 1.2-V UVLO threshold, the current source is disabled causing the voltage at the UVLO pin to quickly fall. In addition to the UVLO hysteresis current source, a 5-µs deglitch filter on both rising and falling edge of UVLO toggling helps preventing chatter during power up or down.

An external UVLO setpoint voltage divider from the supply voltage to AGND is used to set the minimum input operating voltage of the regulator. The divider must be designed such that the voltage at the UVLO pin is greater than 1.2 V when the input voltage is in the desired operating range. The maximum voltage rating of the UVLO pin is 16 V. If necessary, the UVLO pin can be clamped with an external zener diode. The UVLO pin should not be left floating. The values of R_{UV1} and R_{UV2} can be determined from Equation 1 and Equation 2.

$$R_{UV2} = \frac{V_{HYS}}{10\mu A}\left[\Omega\right]$$
$$R_{UV1} = \frac{1.2V \times R_{UV2}}{V_{IN(STARTUP)} - 1.2V}\left[\Omega\right] \quad (1)$$

where

- V_{HYS} is the desired UVLO hysteresis
- $V_{IN(STARTUP)}$ is the desired startup voltage of the regulator during turn-on. (2)

Typical shutdown voltage during turn-off can be calculated as follows:

$$V_{IN(SHUTDOWN)} = V_{IN(STARTUP)} - V_{HYS}[V] \quad (3)$$

7.3.2 High Voltage VCC Regulator

The LM5121 contains an internal high voltage regulator that provides typical 7.6-V VCC bias supply for the controller and N-channel MOSFET drivers. The input of the VCC regulator, VIN can be connected to a voltage source as high as 65 V. The VCC regulator turns on when the UVLO pin voltage is greater than 0.4 V. When the input voltage is below the VCC setpoint level, the VCC output tracks VIN with a small dropout voltage. The output of the VCC regulator is current limited at 50-mA minimum.

Feature Description (continued)

Upon power-up, the VCC regulator sources current into the capacitor connected to the VCC pin. The recommended range for the VCC capacitor is 1.0 µF to 47 µF and it is recommended to be at least 10 times greater than C_{BST} value. When operating with a VIN voltage less than 6 V, the value of VCC capacitor should be 4.7 µF or greater.

The internal power dissipation of the LM5121 device can be reduced by supplying VCC from an external supply. If an external VCC bias supply exists and the voltage is greater than 9 V and below 14.5 V. The external VCC bias supply can be applied to the VCC pin directly through a diode, as shown in Figure 19.

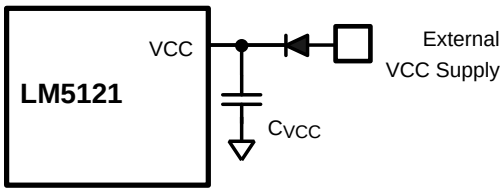

Figure 19. External Bias Supply when 9 V < V_{EXT}< 14.5 V

Shown in Figure 20 is a method to derive the VCC bias voltage with an additional winding on the boost inductor. This circuit must be designed to raise the VCC voltage above VCC regulation voltage to shut off the internal VCC regulator.

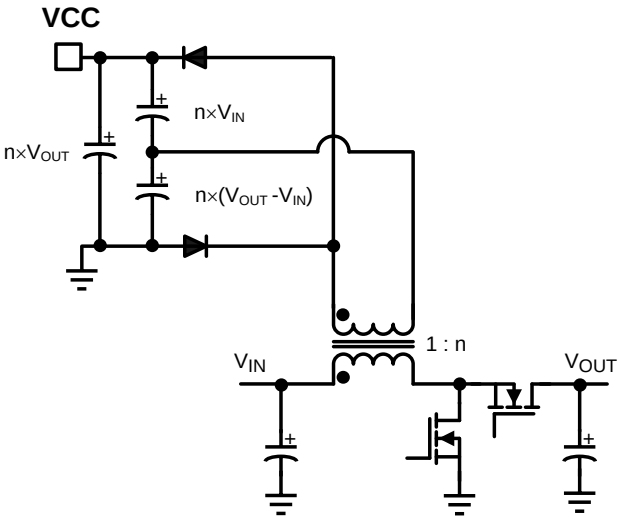

Figure 20. External Bias Supply using Transformer

The VCC regulator series pass transistor includes a diode between VCC and VIN, as shown in Figure 21, that should not be forward biased in normal operation. If the voltage of the external VCC bias supply is greater than the VIN pin voltage, an external blocking diode is required from the input power supply to the VIN pin to prevent the external bias supply from passing current to the input supply through VCC. The need for the blocking diode should be evaluated for all applications when the VCC is supplied by the external bias supply. When the input power supply voltage is less than 4.5 V, an external VCC supply should be used and the external blocking diode is required.

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Feature Description (continued)

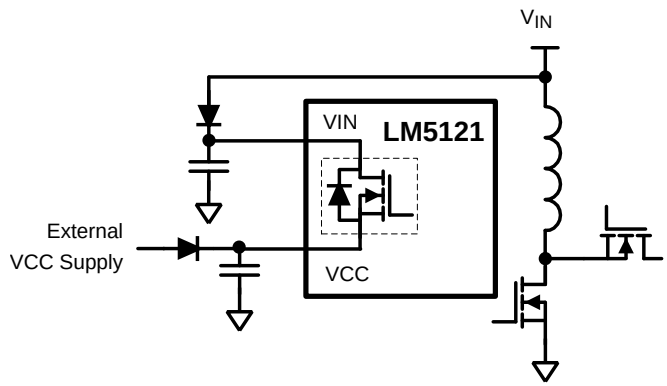

Figure 21. VIN Configuration when V_{VIN}<V_{VCC}

7.3.3 Oscillator

The LM5121 switching frequency is programmable by a single external resistor connected between the RT pin and the AGND pin. The resistor should be located very close to the device and connected directly to the RT and AGND pin. To set a desired switching frequency (f_{SW}), the resistor value can be calculated from Equation 4.

$$R_T = \frac{9 \times 10^9}{f_{SW}} [\Omega] \tag{4}$$

7.3.4 Slope Compensation

For duty cycles greater than 50%, peak current mode regulators are subject to sub-harmonic oscillation. Sub-harmonic oscillation is normally characterized by alternating wide and narrow duty cycles. This sub-harmonic oscillation can be eliminated by a technique, which adds an artificial ramp, known as slope compensation, to the sensed inductor current.

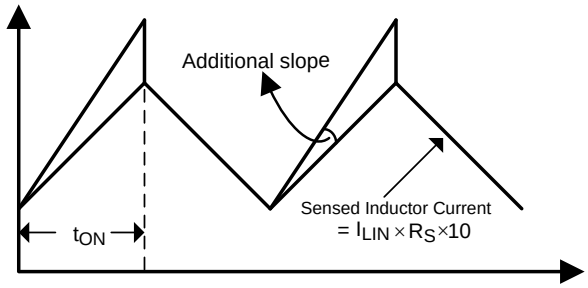

Figure 22. Slope Compensation

The slope compensation of the LM5121 is programmable by a single resistor connected between the SLOPE pin and the AGND pin. The amount of slope compensation can be calculated as follows:

$$V_{SLOPE} = \frac{6 \times 10^9}{f_{SW} \times R_{SLOPE}} \times D \quad [V]$$

where

- $$D = 1 - \frac{V_{IN}}{V_{OUT}} \tag{5}$$

R_{SLOPE} value can be determined from the following equation at minimum input voltage:

Feature Description (continued)

$$R_{SLOPE} = \frac{L_{IN} \times 6 \times 10^9}{\left[K \times V_{OUT} - V_{IN(MIN)}\right] \times R_S \times 10} \left[\Omega\right]$$

where

- K=0.82~1 as a default (6)

From the above equation, K can be calculated over the input range as follows:

$$K = \left(1 + \frac{L_{IN} \times 6 \times 10^9}{V_{IN} \times R_S \times 10 \times R_{SLOPE}}\right) \times D'$$

where

- $D' = \frac{V_{IN}}{V_{OUT}}$ (7)

In any case, K should be greater than 0.5. At higher switching frequency over 500 kHz, the K factor is recommended to be greater than or equal to 1 because the minimum on-time affects the amount of slope compensation due to internal delays.

The sum of sensed inductor current and slope compensation should be less than COMP output high voltage (V_{OH}) for proper startup with load and proper current limit operation. This limits the minimum value of R_{SLOPE} to be:

$$R_{SLOPE} > \frac{5.7 \times 10^9}{f_{SW}} \times \left(1.2 - \frac{V_{IN(MIN)}}{V_{OUT}}\right) \left[\Omega\right]$$

- This equation can be used in most cases

$$R_{SLOPE} > \frac{8 \times 10^9}{f_{SW}} \left[\Omega\right]$$

- This conservative selection should be considered when $V_{IN(MIN)}$ < 5.5 V

The SLOPE pin cannot be left floating.

7.3.5 Error Amplifier

The internal high-gain error amplifier generates an error signal proportional to the difference between the FB pin voltage and the internal precision 1.2-V reference. The output of the error amplifier is connected to the COMP pin allowing the user to provide a Type 2 loop compensation network.

R_{COMP}, C_{COMP} and C_{HF} configure the error amplifier gain and phase characteristics to achieve a stable voltage loop. This network creates a pole at DC, a mid-band zero (f_{Z_EA}) for phase boost, and a high frequency pole (f_{P_EA}). The minimum recommended value of R_{COMP} is 2 kΩ (See the *Feedback Compensation* section).

$$f_{Z_EA} = \frac{1}{2\pi \times R_{COMP} \times C_{COMP}} \left[Hz\right] \quad (9)$$

$$f_{P_EA} = \frac{1}{2\pi \times R_{COMP} \times \left(\frac{C_{COMP} \times C_{HF}}{C_{COMP} + C_{HF}}\right)} \left[Hz\right] \quad (10)$$

7.3.6 PWM Comparator

The PWM comparator compares the sum of sensed inductor current and slope compensation ramp to the voltage at the COMP pin through a 1.2-V internal COMP to PWM voltage drop and terminates the present cycle when the sum of sensed inductor current and slope compensation ramp is greater than V_{COMP} –1.2 V.

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Feature Description (continued)

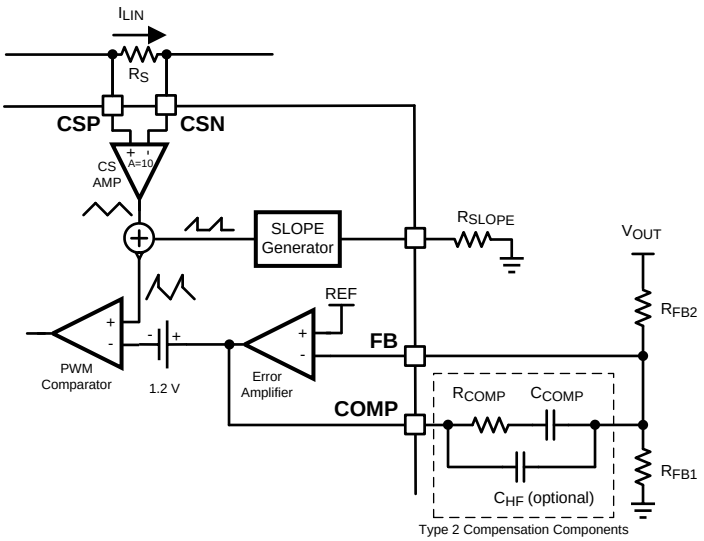

Figure 23. Feedback Configuration and PWM Comparator

7.3.7 Disconnection Switch Control

Soft turn-on is achieved by slowly turning on the disconnection switch. When the UVLO pin voltage is greater than 1.2-V UVLO threshold and the VCC voltages exceeds the VCC UV threshold, the internal charge pump at DG starts sourcing current which enhances N-channel MOSFET disconnection switch. The internal charge pump provides bias voltage at DG pin above VIN pin voltage.

Additional inrush current limiting helps to limit the maximum inrush current. In the inrush current limiting condition when the voltage across sense resistor R_S reaches the inrush current limit threshold, the DG pin voltage is controlled to limit the current flow in R_S by controlling DG pull-down current sink.

As the source voltage of the disconnection switch is charged during initial charging period, the operating point of the disconnection switch transitions from an active region into the ohmic region and the DG pin voltage is maintained by the charge pump. An internal 10 µA soft-start current source turns on when the DG to DS voltage is greater than V_{GS} detection threshold. VIN voltage is recommended to be greater than or equal to the input power supply voltage because the internal charge pump provides the DG bias voltage above the VIN voltage.

The DG pin voltage is clamped to approximately 16 V above the DS pin and 11 V above the VIN pin by internal zener diodes.

Feature Description (continued)

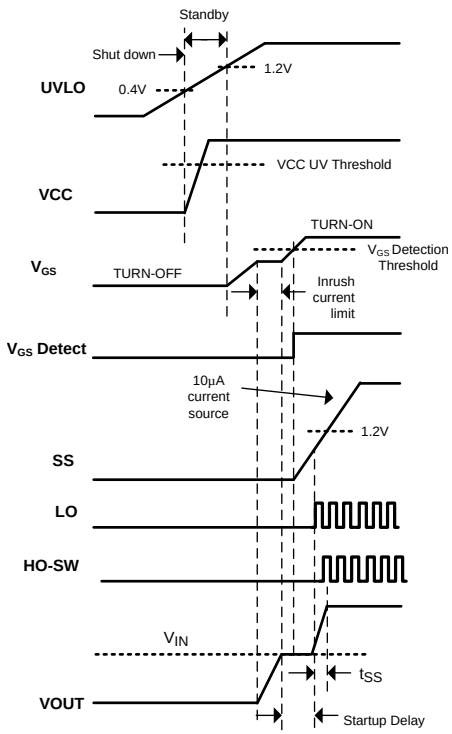

Figure 24. Start-Up Sequence

7.3.8 Soft-Start

The soft-start feature helps the regulator gradually reach the steady state operating point, thus reducing startup stresses and surges. The LM5121 regulates the FB pin to the SS pin voltage or the internal 1.2-V reference, whichever is lower. The internal 10-µA soft-start current source gradually increases the voltage on an external soft-start capacitor connected to the SS pin. This results in a gradual rise of the output voltage starting from the input voltage level to the target output voltage. The soft-start time (t_{SS}) varies with the input supply voltage and output set point and is calculated from Equation 11.

$$t_{SS} = \frac{C_{SS} \times 1.2V}{10\mu A} \times \left(1 - \frac{V_{IN}}{V_{OUT}}\right)[sec] \tag{11}$$

When UVLO pin voltage is greater than 1.2–V UVLO threshold, VCC voltage exceeds the VCC UV threshold and DG to DS voltage is greater than V_{GS} detection threshold, an internal 10-µA soft-start current source turns on. At the beginning of this soft-start sequence, V_{SS} should be allowed to fall down below 25 mV by the internal SS pull-down switch. The SS pin can be pulled down by an external switch to stop switching, but pulling up to enable switching is not recommended. The startup delay (see Figure 24) should be long enough for the high-side boot capacitor to be fully charged by the internal BST charge pump. This defines the recommended minimum C_{SS} value, which is especially important when V_{VIN} is greater than 9 V.

$$C_{SS} > 0.33 \times C_{BST} \times \left(\frac{V_{OUT}}{V_{VIN}}\right)[F] \tag{12}$$

Also, the value of C_{SS} should be large enough to charge the output capacitor during soft-start time.

$$C_{SS} > \frac{10\mu A \times V_{OUT}}{1.2V} \times \frac{C_{OUT}}{I_{OUT}}[F] \tag{13}$$

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Feature Description (continued)

7.3.9 HO and LO Drivers

The LM5121 contains two strong N-channel MOSFET gate drivers and a high-side level shifter to drive the external N-channel MOSFET switches. The high-side gate driver works in conjunction with an external bootstrap diode D_{BST}, and bootstrap capacitor C_{BST}. During the on-time of the low-side N-channel MOSFET driver, the SW pin voltage is approximately 0 V and the C_{BST} is charged from VCC through the D_{BST}. A 0.1–µF or larger ceramic capacitor, connected with short traces between the BST and SW pin, is recommended.

The LO and HO outputs are controlled with an adaptive dead-time methodology which ensures that both outputs are never enabled at the same time. When the controller commands LO to be enabled, the adaptive dead-time logic first disables HO and waits for HO-SW voltage to drop. LO is then enabled after a small delay (HO Fall to LO Rise Delay). Similarly, the HO turn-on is delayed until the LO voltage has discharged. HO is then enabled after a small delay (LO Fall to HO Rise Delay). This technique ensures adequate dead-time for any size N-channel MOSFET or parallel MOSFET configurations especially when VCC is supplied by a higher external voltage source. Use caution when adding series gate resistors, as this may decrease the effective dead-time.

Care should be exercised in selecting the N-channel MOSFET devices threshold voltage when the VIN voltage range is below the VCC regulation level or a bypass operation is required. If bypass operation is required when output voltage is less than 12 V, a logic level device should be selected for the high-side N-channel MOSFET. During startup at low input voltages, the low-side N-channel MOSFET's gate plateau voltage should be sufficiently low to completely enhance the N-channel MOSFET device. If the low-side MOSFET drive voltage is lower than the low-side MOSFET gate plateau voltage during startup, the regulator may not start properly and it may operate at the maximum duty cycle in a high power dissipation state. This condition can be avoided by selecting a lower threshold N-channel MOSFET or by increasing $V_{IN(STARTUP)}$ with the UVLO pin programming.

7.3.10 Bypass Operation ($V_{OUT} = V_{IN}$)

The LM5121 allows 100% duty cycle operation for the high-side synchronous switch when the input supply voltage is equal to or greater than the target output voltage. An internal 200 µA BST charge pump maintains sufficient high-side driver supply voltage to keep the high-side N-channel MOSFET switch on without the power stage switching. The internal BST charge pump is enabled when the UVLO pin voltage is greater than 1.2 V, the VCC voltage exceeds the VCC UV threshold and DG to DS voltage is greater than the V_{GS} detection threshold. The BST charge pump generates 5.3 V minimum BST to SW voltage when SW voltage is greater than 9 V. This requires minimum 9 V boost output voltage for proper bypass operation. The leakage current of the boot diode should be always less than the BST charge pump sourcing current to maintain a sufficient driver supply voltage at both low and high temperatures. Forced PWM mode is the recommended PWM configuration when bypass operation is required.

7.3.11 Cycle-by-Cycle Current Limit

The LM5121 features a peak cycle-by-cycle current limit function. If the CSP to CSN voltage exceeds the 75–mV cycle-by-cycle current limit threshold, the current limit comparator immediately terminates the LO output.

For the case where the inductor current overshoots the desired limit, such as inductor saturation, the current limit comparator blocks LO pulses until the current has decayed below the current limit threshold. Peak inductor current in current limit can be calculated as follows:

$$I_{PEAK(CL)} = \frac{75mV}{R_S}\left[A\right] \tag{14}$$

7.3.12 Circuit Breaker Function

In addition to the hiccup mode short circuit / overload protection, LM5121 provides a circuit breaker function for maximum safety. If the input current increases rapidly due to a fault, the current through the disconnection switch may exceed the inrush control threshold before the inrush control loop is able to respond. If the sensed current exceeds the circuit breaker threshold, the disconnection switch is quickly turned off through an internal switch at the DG pin until current sense input falls below the circuit breaker disable threshold. If the RES pin voltage is less than 1.2 V, the controller then restarts the inrush control procedure.

Feature Description (continued)

7.3.13 Clock Synchronization

The SYNCIN/RT pin can be used to synchronize the internal oscillator to an external clock. The positive going synchronization clock at the RT pin must exceed the RT sync rising threshold and the negative going synchronization clock at RT pin must exceed the RT sync falling threshold to trip the internal synchronization pulse detector.

With the configuration in Figure 25, the frequency of the external synchronization pulse is recommended to be within +/–20% of the internal oscillator frequency programmed by RT resistor. The actual operating range is ±100/40% of the programmed frequency. For example, 900 kHz external synchronization clock and 20 kΩ RT resistor are required for 450 kHz switching. The internal oscillator can be synchronized by AC coupling a positive edge into the RT pin. A 5-V amplitude pulse signal coupled through 100-pF capacitor is a good starting point. The RT resistor is always required in this configuration, whether the oscillator is free running or externally synchronized.

Care should be taken to guarantee that the RT pin voltage does not go below –0.3 V at the falling edge of the external pulse. This may limit the duty cycle of external synchronization pulse. There is approximately 400 ns delay from the rising edge of the external pulse to the rising edge of LO.

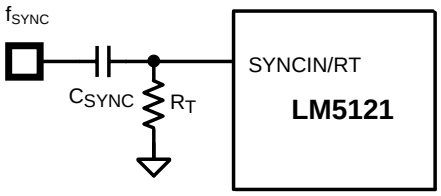

Figure 25. Oscillator Synchronization Through AC Coupling

With the configuration in Figure 26, the internal oscillator can be synchronized by connecting the external synchronization clock to the RT pin through the RT resistor with free of the duty cycle limit. The output stage of the external clock source should be a low impedance totem-pole structure and the default logic state of f_{SYNC} should be low.

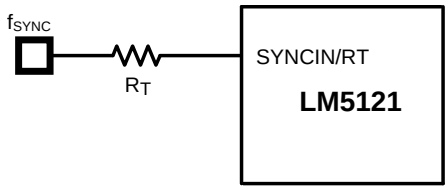

Figure 26. Oscillator Synchronization Through a Resistor

7.3.14 Maximum Duty Cycle

When operating with a high PWM duty cycle, the low-side N-channel MOSFET device is forced off each cycle. This forced LO off-time limits the maximum duty cycle of the controller. When designing a boost regulator with high switching frequency and high duty cycle requirements, check the required maximum duty cycle. The minimum input supply voltage which can achieve the target output voltage is estimated from Equation 15 .

$$V_{IN(MIN)} = f_{SW} \times V_{OUT} \times (550\,ns + margin)\ [V] \tag{15}$$

100 ns of margin is recommended.

7.3.15 Thermal Protection

Internal thermal shutdown circuitry is provided to protect the controller in the event the maximum junction temperature is exceeded. When activated, typically at 165°C, the controller is forced into a low-power shutdown mode, disabling the output drivers, disconnection switch and the VCC regulator. This feature is designed to prevent overheating and destroying the device.

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7.4 Device Functional Modes

7.4.1 Hiccup Mode Short Circuit and Overload Protection

If cycle-by-cycle current limit or inrush current limit is reached during any cycle, a 30-µA RES current is sourced into the RES capacitor for the remainder of the clock cycle. If the RES capacitor voltage exceeds the 1.2-V restart threshold, a hiccup mode protection sequence is initiated. In the hiccup mode, the DG pin is discharged to GND if the inrush current limit is reached, the SS capacitor is discharged to GND, both LO and HO outputs are disabled, and the voltage on the RES capacitor is ramped up and down between 2-V and 4-V eight times.

After the eighth RES pin cycle, the DG pin is released and charged by the DG charge pump. If a 2~3-V zener diode is connected in parallel with the RES capacitor, the regulator enters into the hiccup mode and never restarts until UVLO shutdown is cycled. Connect the RES pin directly to the AGND when the hiccup mode operation is not required.

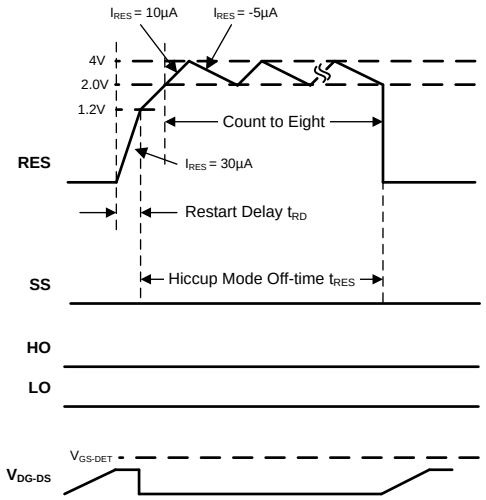

Figure 27. Hiccup Mode Short Circuit Protection (Start-Up With Output Short)

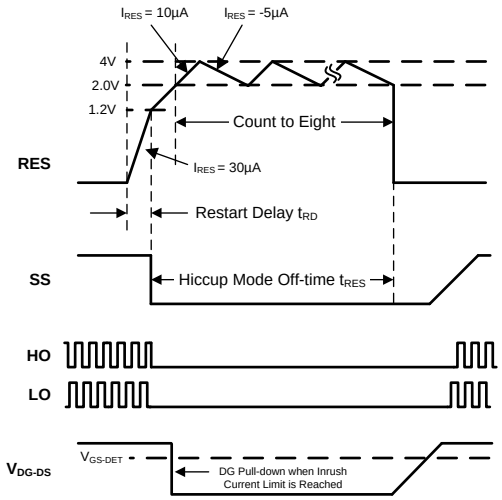

Figure 28. Hiccup Mode Overload Protection (Overload After Start-Up)

7.4.2 MODE Control (Forced PWM Mode and Diode Emulation Mode)

A fully synchronous boost regulator implemented with a high-side MOSFET rather than a diode has the capability to sink current from the output in conditions such as light load, overvoltage or load transient. The LM5121 can be configured to operate in either forced PWM mode or diode emulation mode.

Device Functional Modes (continued)

In forced PWM mode (FPWM), reverse current flow in high-side N-channel MOSFET switch is allowed and the inductor current conducts continuously at light or no load conditions. The benefit of the forced PWM mode is fast light load to heavy load transient response and constant frequency operation at light or no load conditions. To enable forced PWM mode, connect the MODE pin to VCC or tie it to a voltage greater than 1.2 V. In the FPWM mode, reverse current flow is not limited.

In the diode emulation mode, current flow in the high-side switch is only permitted in one direction (source to drain). Turn-on of the high-side switch is allowed if the CSP to CSN voltage is greater than the 7 mV rising threshold of the zero current detection circuit during low-side switch on-time. If the CSP to CSN voltage is less than 6 mV falling threshold of the zero current detection during high-side switch on-time, reverse current flow from output to input through the high-side N-channel MOSFET is prevented and discontinuous conduction mode of operation is enabled by latching off the high-side N-channel MOSFET switch for the remainder of the PWM cycle. A benefit of the diode emulation is lower power loss at light load conditions.

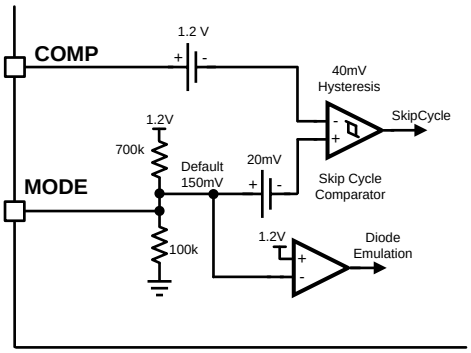

Figure 29. MODE Selection

During startup the LM5121 forces diode emulation, to support startup into a pre-biased load, until the SS pin voltage exceeds 1.2 V. Forced diode emulation is terminated by a pulse from PWM comparator when SS is greater than 1.2 V. If there are no LO pulses during the soft-start period, a 350 ns one-shot LO pulse is forced at the end of soft-start to help charge the bootstrap capacitor. Due to the internal current sense delay, configuring the LM5121 for diode emulation mode should be carefully evaluated if the inductor current ripple ratio is high and the controller is operated at very high switching frequency. The transient performance during full load to no load in FPWM mode should also be verified.

7.4.3 MODE Control (Skip Cycle Mode and Pulse Skipping Mode)

Light load efficiency of the regulator typically drops as the losses associated with switching and bias currents of the converter become a significant percentage of the total power delivered to the load. In order to increase the light load efficiency the LM5121 provides two types of light load operation in diode emulation mode.

The skip cycle mode integrated into the LM5121 controller reduces switching losses and improves efficiency in light load conditions by reducing the average switching frequency. Skip cycle operation is achieved by the skip cycle comparator. When a light load condition occurs, the COMP pin voltage naturally decreases, reducing the peak current delivered by the regulator. During COMP voltage falling, the skip cycle threshold is defined as V_{MODE} –20 mV and during COMP voltage rising, it is defined as V_{MODE} +20 mV. There is 40mV of internal hysteresis in the skip cycle comparator.

When the voltage at PWM comparator input falls below V_{MODE} –20 mV, both HO and LO outputs are disabled. The controller continues to skip switching cycles until the voltage at PWM comparator input increases to V_{MODE} +20 mV, demanding more inductor current. The number of cycles skipped depends upon the load and the response time of the frequency compensation network. The internal hysteresis of skip cycle comparator helps to produce a long skip cycle interval followed by a short burst of pulses. An internal 700 kΩ pull-up and 100 kΩ pull-down resistor sets the MODE pin to 0.15 V as a default. Since the peak current limit threshold is set to 750 mV,

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Device Functional Modes (continued)

the default skip threshold corresponds to approximately 17% of the peak level. In practice the skip level will be lower due to the added slope compensation. By adding an external pull-up resistor from MODE to the SLOPE or VCC pin or adding an external pull-down resistor to the ground, the skip cycle threshold can be programmed. Because the skip cycle comparator monitors the PWM comparator input which tracks the COMP voltage, skip cycle operation is not recommended when the bypass operation is required.

Pulse skipping operation can be achieved by connecting the MODE pin to ground. The negative 20 mV offset at the positive input of skip cycle comparator ensures the skip cycle comparator will not be triggered in normal operation. At light or no load conditions, the LM5121 skips LO pulses if the pulse width required by the regulator is less than the minimum LO on-time of the device. Pulse skipping appears as a random behavior as the error amplifier attempts to find the proper pulse width to maintain regulation at light or no load conditions.

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8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LM5121 device is a step-up dc-dc converter. The device is typically used to convert a lower dc voltage to a higher dc voltage. Use the following design procedure to select component values for the LM5121 device. Alternately, use the WEBENCH® software to generate a complete design. The WEBENCH software uses an iterative design procedure and accesses a comprehensive database of components when generating a design. This section presents a simplified discussion of the design process.

8.1.1 Feedback Compensation

The open loop response of a boost regulator is the product of the modulator transfer function and the feedback transfer function. When plotted on a dB scale, the open loop gain is shown as the sum of modulator gain and feedback gain. The modulator transfer function of a current mode boost regulator including a power stage transfer function with an embedded current loop can be simplified as one pole, one zero and one Right Half Plane (RHP) zero system.

Modulator transfer function is defined as follows:

$$\frac{\hat{V}_{OUT}(s)}{\hat{V}_{COMP}(s)} = A_M \times \frac{\left(1+\frac{s}{\omega_{Z_ESR}}\right)\times\left(1-\frac{s}{\omega_{Z_RHP}}\right)}{\left(1+\frac{s}{\omega_{P_LF}}\right)}$$

where

- $A_M(\text{Modulator DC gain}) = \frac{R_{LOAD}}{R_{S_EQ}\times A_S}\times\frac{D'}{2}$
- $\omega_{P_LF}(\text{Load pole}) = \frac{2}{R_{LOAD}\times C_{OUT}}$
- $\omega_{Z_ESR}(\text{ESR zero}) = \frac{1}{R_{ESR}\times C_{OUT}}$
- $\omega_{Z_RHP}(\text{RHP zero}) = \frac{R_{LOAD}\times (D')^2}{L_{IN_EQ}}$
- $L_{IN_EQ} = \frac{L_{IN}}{n}, R_{S_EQ} = \frac{R_S}{n}$
- n is the number of the phase. (16)

If the ESR of C_{OUT} (R_{ESR}) is small enough and the RHP zero frequency is far away from the target crossover frequency, the modulator transfer function can be further simplified to one pole system and the voltage loop can be closed with only two loop compensation components, R_{COMP} and C_{COMP}, leaving a single pole response at the crossover frequency. A single pole response at the crossover frequency yields a very stable loop with 90 degrees of phase margin.

The feedback transfer function includes the feedback resistor divider and loop compensation of the error amplifier. R_{COMP}, C_{COMP} and optional C_{HF} configure the error amplifier gain and phase characteristics, and create a pole at origin, a low frequency zero and a high frequency pole.

The feedback transfer function is defined as follows:

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Application Information (continued)

$$-\frac{\hat{V}_{COMP}}{\hat{V}_{OUT}} = A_{FB} \times \frac{1+\frac{s}{\omega_{Z_EA}}}{s \times \left(1+\frac{s}{\omega_{P_EA}}\right)}$$

where

- $A_{FB}(\text{Feedback DC gain}) = \frac{1}{R_{FB2} \times (C_{COMP} + C_{HF})}$
- $\omega_{Z_EA}(\text{Low frequency zero}) = \frac{1}{R_{COMP} \times C_{COMP}}$
- $\omega_{P_EA}(\text{High frequency pole}) = \frac{1}{R_{COMP} \times C_{HF}}$ (17)

The pole at the origin minimizes output steady state error. The low frequency zero should be set to cancel the load pole of the modulator. The high frequency pole can be used to cancel the zero created by the output capacitor ESR or to decrease noise susceptibility of the error amplifier. By placing the low frequency zero an order of magnitude less than the crossover frequency, the maximum amount of phase boost is achieved at the crossover frequency. The high frequency pole should be set above the crossover frequency since the addition of C_{HF} adds a pole in the feedback transfer function.

The crossover frequency (open loop bandwidth) is usually selected between one twentieth and one fifth of the switching frequency. In a simplified formula, the estimated crossover frequency can be defined as:

$$f_{CROSS} = \frac{R_{COMP}}{\pi \times R_{S_EQ} \times R_{FB2} \times A_S \times C_{OUT}} \times D' \text{ [Hz]}$$

where

- $D' = \frac{V_{IN}}{V_{OUT}}$ (18)

For higher crossover frequency, R_{COMP} can be increased, while proportionally decreasing C_{COMP}. Conversely, decreasing R_{COMP} while proportionally increasing C_{COMP}, results in lower bandwidth while keeping the same zero frequency in the feedback transfer function.

The modulator transfer function can be measured using a network analyzer and the feedback transfer function can be configured for the desired open loop transfer function. If the network analyzer is not available, step load transient tests can be performed to verify acceptable performance. The step load goal is minimum overshoot/undershoot with a damped response.

8.1.2 Sub-Harmonic Oscillation

Peak current mode regulator can exhibit unstable behavior when operating above 50% duty cycle. This behavior is known as sub-harmonic oscillation and is characterized by alternating wide and narrow pulses at the SW pin. Sub-harmonic oscillation can be prevented by adding a voltage ramp (slope compensation) on top of the sensed inductor current. By choosing K≥0.82~1.0, the sub-harmonic oscillation will be eliminated even with widely varying input voltage.

In time-domain analysis, the steady-state inductor current starting from an initial point returns to the same point. When the amplitude of an end cycle current error (dI_1) caused by an initial perturbation (dI_0) is less than the amplitude of dI_0 or $dI_1/dI_0 > -1$, the perturbation naturally disappears after a few cycles. When $dI_1/dI_0 < -1$, the initial perturbation no longer disappear, it results in sub-harmonic oscillation in the steady-state.

Application Information (continued)

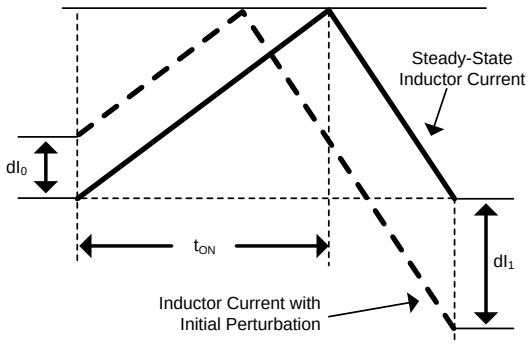

Figure 30. Effect of Initial Perturbation when $dI_1/dI_0 < -1$

dI_1/dI_0 can be calculated as:

$$\frac{dI_1}{dI_0} = 1 - \frac{1}{K} \tag{19}$$

The relationship between dI_1/dI_0 and K factor is illustrated in the graphic below.

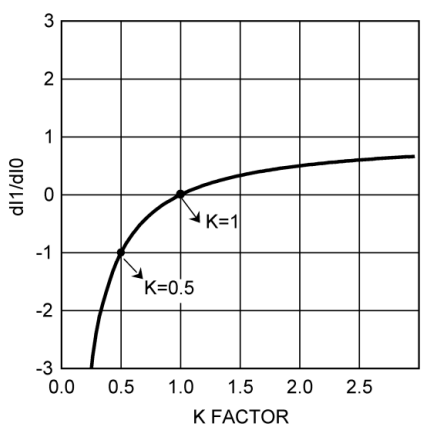

Figure 31. dI_1/dI_0 vs K Factor

The absolute minimum value of K is 0.5. When K<0.5, the amplitude of dI_1 is greater than the amplitude of dI_0 and any initial perturbation results in sub-harmonic oscillation. If K=1, any initial perturbation will be removed in one switching cycle. This is known as one-cycle damping. When $-1<dI_1/dI_0<0$, any initial perturbation will be under-damped. Any perturbation will be over-damped when $0<dI_1/dI_0<1$.

In the frequency-domain, Q, the quality factor of sampling gain term in modulator transfer function, is used to predict the tendency for sub-harmonic oscillation, which is defined as:

$$Q = \frac{1}{\pi(K - 0.5)} \tag{20}$$

The relationship between Q and K factor is illustrated in Figure 32.

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Application Information (continued)

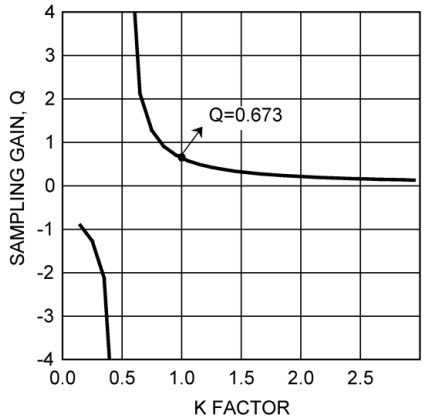

Figure 32. Sampling Gain Q vs K Factor

The recommended absolute minimum value of K is 0.5. High gain peaking when K is less than 0.5 results in sub-harmonic oscillation at $f_{SW}/2$. A higher value of K factor may introduce additional phase shift near the crossover frequency, but has the benefit of reducing noise susceptibility in the current loop. The maximum allowable value of K factor can be calculated using the maximum crossover frequency equation and frequency analysis formulas in Table 1.

Table 1. Boost Regulator Frequency Analysis

	SIMPLIFIED FORMULA	COMPREHENSIVE FORMULA (1)
MODULATOR TRANSER FUNCTION	$\frac{\hat{V}_{OUT}(s)}{\hat{V}_{COMP}(s)} = A_M \times \frac{\left(1+\frac{s}{\omega_{Z_ESR}}\right)\times\left(1-\frac{s}{\omega_{Z_RHP}}\right)}{\left(1+\frac{s}{\omega_{P_LF}}\right)}$	$\frac{\hat{V}_{OUT}(s)}{\hat{V}_{COMP}(s)} = A_M \times \frac{\left(1+\frac{s}{\omega_{Z_{ESR}}}\right)\times\left(1-\frac{s}{\omega_{Z_{RHP}}}\right)}{\left(1+\frac{s}{\omega_{P_LF}}\right)\times\left(1+\frac{s}{\omega_{p_ESR}}\right)\times\left(1+\frac{s}{\omega_{P_HF}}+\frac{s^2}{\omega_n^2}\right)}$
Modulator DC gain (2)	$A_M = \frac{R_{LOAD}}{R_{S_EQ}\times A_S}\times\frac{D'}{2}$	
RHP zero (2)	$\omega_{Z_RHP} = \frac{R_{LOAD}\times(D')^2}{L_{IN_EQ}}$	
ESR zero	$\omega_{Z_ESR} = \frac{1}{R_{ESR}\times C_{OUT}}$	$\omega_{Z_ESR} = \frac{1}{R_{ESR1}\times C_{OUT1}}$
ESR pole	Not considered	$\omega_{P_ESR} = \frac{1}{R_{ESR1}\times(C_{OUT1}//C_{OUT2})}$
Dominant load pole	$\omega_{P_LF} = \frac{2}{R_{LOAD}\times C_{OUT}}$	
Sampled gain inductor pole	Not considered	$\omega_{P_HF} = \frac{f_{SW}}{K-0.5}$ or $\omega_{P_HF} = Q\times\omega_n$
Quality factor	Not considered	$Q = \frac{1}{\pi(K-0.5)}$

(1) Comprehensive equation includes an inductor pole and a gain peaking at $f_{SW}/2$, which is caused by sampling effect of the current mode control. Also, it assumes that a ceramic capacitor C_{OUT2} (No ESR) is connected in parallel with C_{OUT1}. R_{ESR1} represents ESR of C_{OUT1}.

(2) With multiphase configuration, $L_{IN_EQ} = \frac{L_{IN}}{n}$, $R_{S_EQ} = \frac{R_S}{n}$, $R_{LOAD} = \frac{V_{OUT}}{I_{OUT}\text{ of each phase}\times n}$, and $C_{OUT} = C_{OUT}$ of each phase x n, where n = number of phases. As is the current sense amplifier gain.

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Application Information (continued)

Table 1. Boost Regulator Frequency Analysis (continued)

	SIMPLIFIED FORMULA	COMPREHENSIVE FORMULA (1)
Sub-harmonic double pole	Not considered	$\omega_n = \frac{\omega_{SW}}{2} = \pi \times f_{SW}$ or $f_n = \frac{f_{SW}}{2}$
K factor	K = 1	$K = \left(1 + \frac{L_{IN} \times 6 \times 10^9}{V_{IN} \times R_S \times 10 \times R_{SLOPE}}\right) \times D'$
FEEDBACK TRANSFER FUNCTION	$-\frac{\hat{V}_{COMP}(s)}{\hat{V}_{OUT}(s)} = A_{FB} \times \frac{1 + \frac{s}{\omega_{Z_EA}}}{s \times \left(1 + \frac{s}{\omega_{P_EA}}\right)}$	
Feedback DC gain	$A_{FB} = \frac{1}{R_{FB2} \times (C_{COMP} + C_{HF})}$	
Mid-band Gain	$A_{FB_MID} = \frac{R_{COMP}}{R_{FB2}}$	
Low frequency zero	$\omega_{Z_EA} = \frac{1}{R_{COMP} \times C_{COMP}}$	
High frequency pole	$\omega_{P_EA} = \frac{1}{R_{COMP} \times C_{HF}}$	$\omega_{P_EA} = \frac{1}{R_{COMP} \times (C_{CHF} // C_{COMP})}$
OPEN LOOP RESPONSE	$T(s) = A_M \times A_{FB} \times \frac{\left(1 + \frac{s}{\omega_{Z_ESR}}\right) \times \left(1 - \frac{s}{\omega_{Z_RHP}}\right)}{\left(1 + \frac{s}{\omega_{P_LF}}\right)} \times \frac{1 + \frac{s}{\omega_{Z_EA}}}{s \times \left(1 + \frac{s}{\omega_{P_EA}}\right)}$	$T(s) = A_M \times A_{FB} \times \frac{\left(1 + \frac{s}{\omega_{Z_ESR}}\right) \times \left(1 - \frac{s}{\omega_{Z_RHP}}\right)}{\left(1 + \frac{s}{\omega_{P_LF}}\right) \times \left(1 + \frac{s}{\omega_{p_ESR}}\right) \times \left(1 + \frac{s}{\omega_{P_{HF}}} + \frac{s^2}{\omega_n^2}\right)} \times \frac{1 + \frac{s}{\omega_{Z_EA}}}{s \times \left(1 + \frac{s}{\omega_{P_EA}}\right)}$
Crossover frequency (3) (Open loop band width)	$f_{CROSS} = \frac{R_{COMP}}{\pi \times R_{S_EQ} \times R_{FB2} \times A_S \times C_{OUT}} \times D'$	Use graphic tool
Maximum cross over frequency (4)	$f_{CROSS_MAX} = \frac{f_{SW}}{5}$ or $\frac{\omega_{Z_RHP}}{2 \times \pi \times 4}$ whichever is smaller	$f_{CROSS_MAX} = \frac{f_{SW}}{4 \times Q} \times \left(\sqrt{1 + 4 \times Q^2} - 1\right)$ or $\frac{\omega_{Z_RHP}}{2 \times \pi \times 4}$, whichever is smaller

(3) Assuming $\omega_{Z_EA} = \omega_{P_LF}$, $\omega_{P_EA} = \omega_{Z_ESR}$, $f_{CROSS} < \frac{\omega_{Z_RHP}}{2 \times \pi \times 10}$, $C_{COMP} = \frac{R_{LOAD} \times C_{OUT}}{4 \times R_{COMP}}$, and $D' = \frac{V_{IN}}{V_{OUT}}$.
(4) The frequency at which 45º phase shift occurs in modulator phase characteristics.

8.1.3 Output Overvoltage Protection

Output overvoltage protection can be achieved by adding a simple external circuit. The output overvoltage protection circuit shown in Figure 33 shuts down the LM5121 when the output voltage exceeds the overvoltage threshold set by the zener diode.

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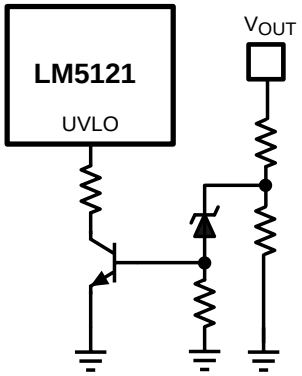

Figure 33. Output Overvoltage Protection

8.1.4 Input Transient Suppression

Input over-voltage transient suppression can be achieved by adding a zener diode from DG to ground. The DS voltage will be clamped to the zener voltage minus the gate threshold voltage of the disconnection MOSFET switch.

Since the input clamping occurs in the active region of disconnection MOSFET switch, safe operating area and the thermal properties of the disconnection MOSFET switch should be carefully considered.

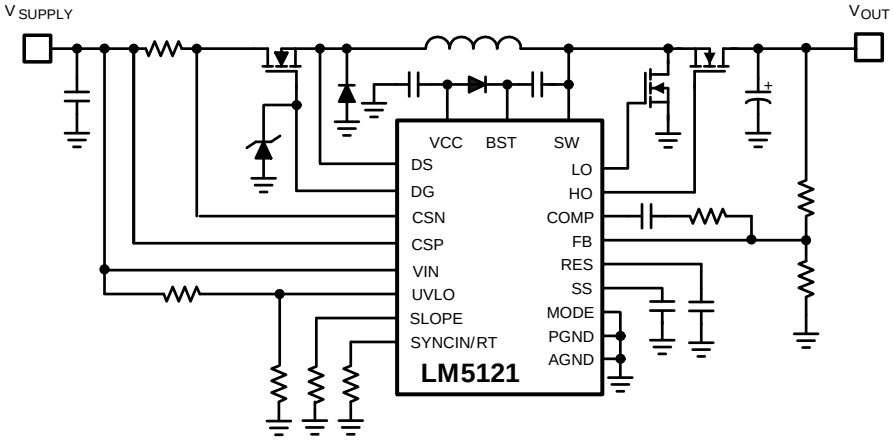

Figure 34. Input Transient Suppression

8.1.5 Inrush Current Limit Programming

Inrush current limit level can be lower than the cycle-by-cycle current limit level by adding a simple external circuit. The external inrush current limit programming circuit shown in Figure 35 and Figure 36 pull down CSN pin during inrush current limiting. Also, this configuration enables latch-off mode circuit breaker.

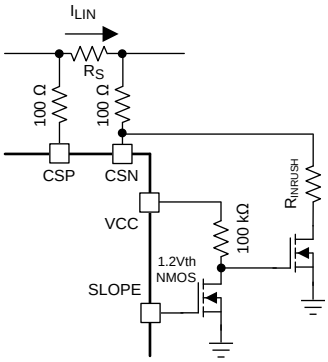

Figure 35. Inrush Current Limit Programming #1

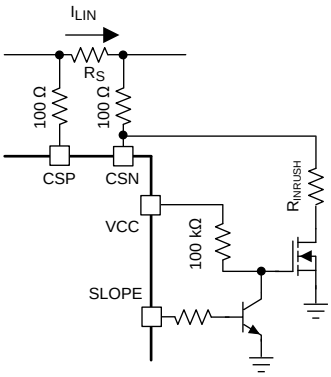

Figure 36. Inrush Current Limit Programming #2

8.1.6 Reverse Battery Protection + Disconnect Switch Control

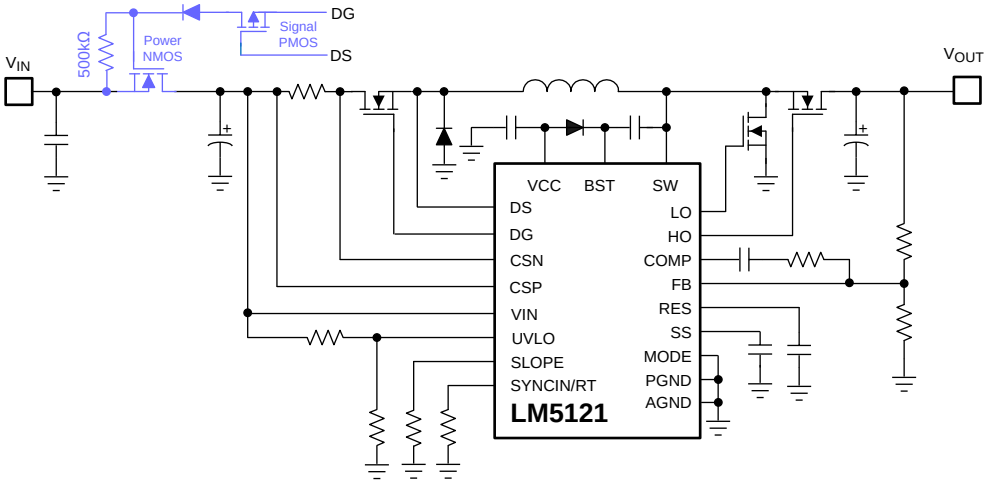

Figure 37. Reverse Battery Protection + Disconnection Switch

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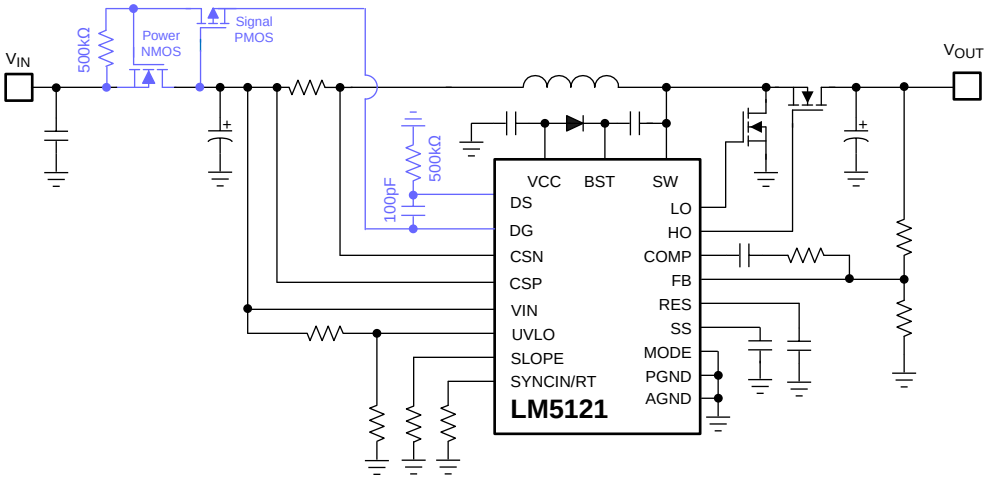

Figure 38. Reverse Battery Protection

8.2 Typical Application

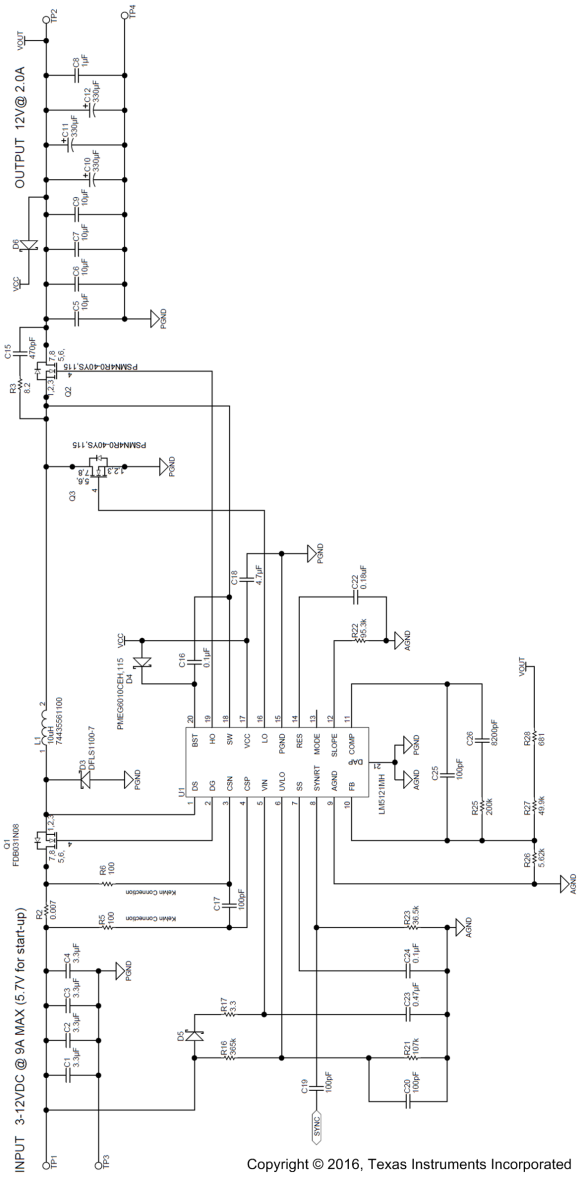

Figure 39. Schematic

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8.2.1 Design Requirements

DESIGN PARAMETERS	VALUE
Output Voltage (V_{OUT})	12 V
Full Load Current (I_{OUT})	2 A
Output Power	24 W
Minimum Input Voltage ($V_{IN(MIN)}$)	3 V (5.7 V for start-up)
Typical Input Voltage ($V_{IN(TYP)}$)	9 V
Maximum Input Voltage ($V_{IN(MAX)}$)	12 V
Switching Frequency (f_{SW})	250 kHz
Disconnection Switch Control	Yes

8.2.2 Detailed Design Procedure

8.2.2.1 Timing Resistor R_T

Generally, higher frequency applications are smaller but have higher losses. Operation at 250 kHz is selected for this example as a reasonable compromise between small size and high-efficiency. The value of R_T for 250 kHz switching frequency is calculated as follows:

$$R_T = \frac{9 \times 10^9}{f_{SW}} = \frac{9 \times 10^9}{250\ \text{kHz}} = 36.0\ \text{k}\Omega \tag{21}$$

A standard value of 36.5 kΩ is chosen for R_T.

8.2.2.2 UVLO Divider R_{UV2}, R_{UV1}

The desired startup voltage and the hysteresis are set by the voltage divider R_{UV2}, R_{UV1}. The UVLO shutdown voltage should be high enough to fully enhance the low-side N-channel MOSFET switch. For this design, the startup voltage is set to 5.5 V which is 0.2 V below 5.7 V. V_{HYS} is set to 3.7 V. This results 1.8 V of $V_{IN(SHUTDOWN)}$. The values of R_{UV2}, R_{UV1} are calculated as follows:

$$R_{UV2} = \frac{V_{HYS}}{I_{HYS}} = \frac{3.7\ \text{V}}{10\ \mu\text{A}} = 370\ \text{k}\Omega \tag{22}$$

$$R_{UV1} = \frac{1.2\text{V} \times R_{UV2}}{V_{IN(STARTUP)} - 1.2\text{V}} = \frac{1.2\text{V} \times 370\ \text{k}\Omega}{5.5\text{V} - 1.2\text{V}} = 103\ \text{k}\Omega \tag{23}$$

A standard value of 365 kΩ is selected for R_{UV2}. R_{UV1} is selected to be a standard value of 107 kΩ.

8.2.2.3 Input Inductor L_{IN}

The inductor ripple current is typically set between 20% and 40% of the full load current, as a good compromise between core loss and copper loss of the inductor. Higher ripple current allows a smaller inductor size, but places more of a burden on the output capacitor to smooth the ripple voltage on the output. For this example, a ripple ratio (RR) of 0.3, 30% of the input current was chosen. Knowing the switching frequency and the typical output voltage, the inductor value can be calculated as follows:

$$L_{IN} = \frac{V_{IN}}{I_{IN} \times RR} \times \frac{1}{f_{SW}} \times \left(1 - \frac{V_{IN}}{V_{OUT}}\right) = \frac{9\text{V}}{\frac{24\text{W}}{9\text{V}} \times 0.3} \times \frac{1}{250\ \text{kHz}} \times \left(1 - \frac{9\text{V}}{12\text{V}}\right) = 11.3\ \mu\text{H} \tag{24}$$

The closest standard value of 10 µH was chosen for L_{IN}.

The saturation current rating of the inductor should be greater than the peak inductor current, which is calculated at the minimum input voltage and full load. A 2.7 V startup voltage is used to conservatively estimate the peak inductor current.

$$I_{PEAK} = I_{IN} + \frac{1}{2} \times \frac{V_{IN}}{L_{IN} \times f_{SW}} \times \left(1 - \frac{V_{IN}}{V_{OUT}}\right) = \frac{12\text{V} \times 2\text{A}}{2.7\text{V}} + \frac{1}{2} \times \frac{2.7\text{V}}{10\ \mu\text{H} \times 250\ \text{kHz}} \times \left(1 - \frac{2.7\text{V}}{12\text{V}}\right) = 9.3\ \text{A} \tag{25}$$

8.2.2.4 Current Sense Resistor R_S

The peak input current limit threshold should be set 20~50% higher than the required peak current at low input voltage and full load, accounting for tolerances. For this example, 20% is margin is chosen.

$$R_S = \frac{V_{CS-TH1}}{I_{PEAK(CL)}} = \frac{75\ mV}{9.3A \times 1.2} = 6.7\ m\Omega \tag{26}$$

A closest standard value of 7 mΩ is selected for R_S. The maximum power loss of R_S is calculated as follows.

$$P_{LOSS(RS)} = I^2R = (9.3A \times 1.2)^2 \times 7m\Omega = 0.87W \tag{27}$$

8.2.2.5 Current Sense Filter R_{CSFP}, R_{CSFN}, C_{CS}

The current sense filter is optional. 100 pF for C_{CS} and 100 Ω for R_{CSFP} and R_{CSFN} are normal recommendations. Because CSP and CSN pins are high impedance, C_{CS} should be placed physically as close to the device.

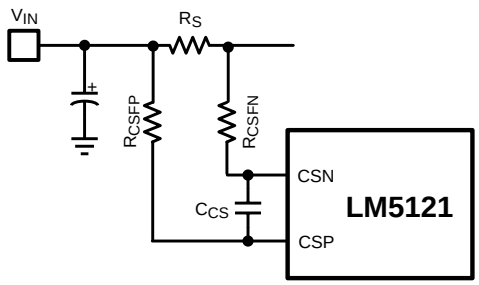

Figure 40. Current Sense Filter

8.2.2.6 Slope Compensation Resistor R_{SLOPE}

The K value is selected to be 1 at the minimum input voltage. R_{SLOPE} should be selected such that the sum of sensed inductor current and slope compensation is less than COMP output high voltage.

$$R_{SLOPE} > \frac{8 \times 10^9}{f_{SW}} = \frac{8 \times 10^9}{250\ kHz} = 32\ k\Omega \tag{28}$$

$$R_{SLOPE} = \frac{L_{IN} \times 6 \times 10^9}{\left[K \times V_{OUT} - V_{IN(MIN)}\right] \times R_S \times 10} = \frac{10\ \mu H \times 6 \times 10^9}{(1 \times 12V - 3V) \times 7m\Omega \times 10} = 95\ k\Omega \tag{29}$$

A closest standard value of 95.3 kΩ is selected for R_{SLOPE}.

8.2.2.7 Output Capacitor C_{OUT}

The output capacitors smooth the output voltage ripple and provide a source of charge during transient loading conditions. Also the output capacitors reduce the output voltage overshoot when the load is suddenly disconnected.

The ripple current rating of the output capacitor should be carefully considered. In boost regulator, the output is supplied by discontinuous current and the ripple current requirement is usually high. In practice, the ripple current requirement can be dramatically reduced by placing high quality ceramic capacitors closer to the high side MOSFET switch than the bulk aluminum capacitors.

The output voltage ripple is dominated by the ESR of the output capacitors. Parallel output capacitors are a good choice to minimize effective ESR and split the output ripple current into multiple capacitors.

In this example, three 330 µF aluminum capacitors are used to share the output ripple current and source the required charge. The maximum output ripple current can be calculated at the minimum input voltage as follows:

$$I_{RIPPLE_MAX(COUT)} = \frac{I_{OUT}}{2 \times \frac{V_{IN(MIN)}}{V_{OUT}}} = \frac{2.0A}{2 \times \frac{3V}{12V}} = 4A \tag{30}$$

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Assuming 60 mΩ of ESR per output capacitor, the output voltage ripple at the minimum input voltage is calculated as follows:

$$V_{RIPPLE_MAX(COUT)} = \frac{I_{OUT}}{\frac{V_{IN(MIN)}}{V_{OUT}}} \times \left(R_{ESR} + \frac{1}{4 \times C_{OUT} \times f_{SW}}\right) = \frac{2.0A}{\frac{3V}{12V}} \times \left(\frac{60m\Omega}{3} + \frac{1}{4 \times 3 \times 330\ \mu F \times 250\ kHz}\right) = 0.168V \tag{31}$$

In practice, four 10 µF ceramic capacitors are additionally placed before the bulk aluminum capacitors to reduce the output voltage ripple and share the output ripple current.

8.2.2.8 Input Capacitor C_{IN}

The input capacitors smooth the input voltage ripple. Assuming high quality ceramic capacitors are used for the input capacitors, the maximum input voltage ripple which occurs when the input voltage is half of the output voltage can be calculated as follows:

$$V_{RIPPLE_MAX(CIN)} = \frac{V_{OUT}}{32 \times L_{IN} \times C_{IN} \times f_{SW}^2} = \frac{12V}{32 \times 10\ \mu H \times 4 \times 3.3\ \mu F \times 250\ kHz^2} = 0.045V \tag{32}$$

The value of input capacitor is also a function of source impedance, the impedance of source power supply. More input capacitor will be required to prevent a chatter condition during power up if the impedance of source power supply is not low.

8.2.2.9 VIN Filter R_{VIN}, C_{VIN}

An R-C filter (R_{VIN}, C_{VIN}) on the VIN pin is optional. It is not required if the C_{IN} capacitors are high quality ceramic capacitors and placed physically close to the device. The filter helps to prevent faults caused by high frequency switching noise injection into the VIN pin. A 0.47 µF ceramic capacitor is used this example. Recommended filter values are 3 Ω for R_{VIN} and 0.47 µF for C_{VIN} . A larger filter with 2.2 µ to 4.7 µF C_{VIN} is recommended when the input voltage is lower than 8 V or when the required duty cycle is close to the maximum duty cycle limit.

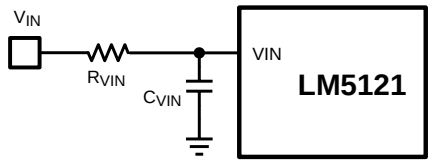

Figure 41. VIN Filter

8.2.2.10 Bootstrap Capacitor C_{BST} and Boost Diode D_{BST}

The bootstrap capacitor between the BST and SW pins supplies the gate current to charge the high-side N-channel MOSFET gate during each turn-on cycle and also supplies recovery charge for the bootstrap diode. The peak current can be several amperes. The recommended value of the bootstrap capacitor is 0.1 µF. C_{BST} should be a good quality, low ESR, ceramic capacitor located at the pins of the device to minimize potentially damaging voltage transients caused by trace inductance. The minimum value for the bootstrap capacitor is calculated as follows:

$$C_{BST} = \frac{Q_G}{\Delta V_{BST}} [F] \tag{33}$$

Where Q_G is the high-side N-channel MOSFET gate charge and ΔV_{BST} is the tolerable voltage droop on C_{BST}, which is typically less than 5% of VCC or conservatively 0.15 V . In this example, the value of the BST capacitor (C_{BST}) is 0.1 µF.

The voltage rating of D_{BST} should be greater than the peak SW node voltage plus 16 V. A low leakage diode is mandatory for bypass operation. The leakage current of D_{BST} should be low enough for the BST charge pump to maintain a sufficient high-side driver supply voltage at high temperature. A low leakage diode also prevents the possibility of excessive VCC voltage during shutdown, in high output voltage applications. If the diode leakage is excessive, a zener clamp or bleed resistor may be required on VCC. High-side driver supply voltage should be greater than the high-side N-channel MOSFET switch gate plateau at the minimum input voltage.

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8.2.2.11 VCC Capacitor C_{VCC}

The primary purpose of the VCC capacitor is to supply the peak transient currents of the LO driver and bootstrap diode as well as to provide stability for the VCC regulator. The peak driver currents can be several amperes. The value of C_{VCC} should be at least 10 times greater than the value of C_{BST}, and should be a good quality, low ESR, ceramic capacitor. C_{VCC} should be placed close to the pins of the IC to minimize potentially damaging voltage transients caused by trace inductance. A value of 4.7 µF was selected for this design example.

8.2.2.12 Output Voltage Divider R_{FB1}, R_{FB2}

R_{FB1} and R_{FB2} set the output voltage level. The ratio of these resistors is calculated as follows:

$$\frac{R_{FB2}}{R_{FB1}} = \frac{V_{OUT}}{1.2V} - 1 \tag{34}$$

The ratio between R_{COMP} and R_{FB2} determines the mid-band gain, A_{FB_MID}. A larger value for R_{FB2} may require a corresponding larger value for R_{COMP}. R_{FB2} should be large enough to keep the total divider power dissipation small. A 49.9 kΩ in series with 681 Ω was chosen for high-side feedback resistors in this example, which results in a R_{FB1} value of 5.62 kΩ for 12 V output.

8.2.2.13 Soft-Start Capacitor C_{SS}

The soft-start time (t_{SS}) is the time required for the output voltage set point to reach the target voltage from the input voltage. The soft-start time is not only proportional to the soft-start capacitor, but also depends on the input voltage. With 0.1 µF for C_{SS}, the soft-start time is calculated as follows:

$$t_{SS(MAX)} = \frac{C_{SS} \times 1.2V}{I_{SS}} \times \left(1 - \frac{V_{IN(STARTUP)}}{V_{OUT}}\right) = \frac{0.1\,\mu F \times 1.2V}{10\,\mu A} \times \left(1 - \frac{5.7V}{12V}\right) = 6.3\text{ msec} \tag{35}$$

8.2.2.14 Restart Capacitor C_{RES}

The restart capacitor determines the restart delay time t_{RD} and hiccup mode off time t_{RES} (see Figure 27). t_{RD} should be greater than $t_{SS(MAX)}$. The minimum required value of C_{RES} can be calculated at the low input voltage as follows:

$$C_{RES(MIN)} = \frac{I_{RES} \times t_{SS(MAX)}}{V_{RES}} = \frac{30\,\mu A \times 6.3\text{ msec}}{1.2V} = 0.16\,\mu F \tag{36}$$

A standard value of 0.18 µF is selected for C_{RES}.

8.2.2.15 Low-Side Power Switch Q_L

Breaking down the various losses is one way to compare the relative efficiencies of different N-channel MOSFET devices. Losses in the low-side N-channel MOSFET device can be separated into conduction loss and switching loss.

Low-side conduction loss is approximated calculated as follows:

$$P_{COND(LS)} = D \times I_{IN^2} \times R_{DS_ON(LS)} \times 1.3 = \left(1 - \frac{V_{IN}}{V_{OUT}}\right) \times \left(\frac{I_{OUT} \times V_{OUT}}{V_{IN}}\right)^2 \times R_{DS_ON(LS)} \times 1.3[W] \tag{37}$$

Where D is the duty cycle and the factor of 1.3 accounts for the increase in the N-channel MOSFET device on-resistance due to heating. Alternatively, the factor of 1.3 can be eliminated and the high temperature on-resistance of the N-channel MOSFET device can be estimated using the $R_{DS(ON)}$ vs temperature curves in the N-channel MOSFET datasheet.

Switching loss occurs during the brief transition period as the low-side N-channel MOSFET device turns on and off. During the transition period both current and voltage are present in the channel of the N-channel MOSFET device. The low-side switching loss is approximated as follows:

$$P_{SW(LS)} = 0.5 \times V_{OUT} \times I_{IN} \times (t_R + t_F) \times f_{SW}[W] \tag{38}$$

t_R and t_F are the rise and fall times of the low-side N-channel MOSFET device. The rise and fall times are usually mentioned in the N-channel MOSFET datasheet or can be empirically observed with an oscilloscope.

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An additional Schottky diode can be placed in parallel with the low-side N-channel MOSFET switch, with short connections to the source and drain in order to minimize negative voltage spikes at the SW node.

8.2.2.16 High-Side Power Switch Q_H and Additional Parallel Schottky Diode

Losses in the high-side N-channel MOSFET device can be separated into conduction loss, dead-time loss and reverse recovery loss. Switching loss is calculated only for the low-side N-channel MOSFET device. Switching loss in the high-side N-channel MOSFET device is negligible because the body diode of the high-side N-channel MOSFET device turns on before and after the high-side N-channel MOSFET switches.

High-side conduction loss is approximated as follows:

$$P_{COND(HS)} = (1-D) \times I_{IN^2} \times R_{DS_ON(HS)} \times 1.3 = \left(\frac{V_{IN}}{V_{OUT}}\right) \times \left(\frac{I_{OUT} \times V_{OUT}}{V_{IN}}\right)^2 \times R_{DS_ON(HS)} \times 1.3 [W] \quad (39)$$

Dead-time loss is approximated as follows:

$$P_{DT(HS)} = V_D \text{ x } I_{IN} \text{ x } (t_{DLH} + t_{DHL}) \text{ x } f_{SW} [W]$$

where

- V_D is the forward voltage drop of the high-side N-channel MOSFET body diode. (40)

Reverse recovery characteristics of the high-side N-channel MOSFET strongly influences efficiency, especially when the output voltage is high. Smaller reverse recovery charge helps to increase the efficiency while also minimizing switching noise.

Reverse recovery loss is approximated as follows:

$$P_{RR(HS)} = V_{OUT} \times Q_{RR} \times f_{SW} [W]$$

where

- Q_{RR} is the reverse recovery charge of the high-side N-channel MOSFET body diode. (41)

An additional Schottky diode can be placed in parallel with the high-side switch to improve efficiency. Usually, the power rating of this parallel Schottky diode can be less than the high-side switch ratings because the diode conducts only during dead-times. The power rating of the parallel diode should be equivalent or higher than high-side switch ratings if bypass operation is required, hiccup mode operation is required or a heavy load exists before the controller begins switching.

8.2.2.17 Snubber Components

A resistor-capacitor snubber network across the high-side N-channel MOSFET device reduces ringing and spikes at the switching node. Excessive ringing and spikes can cause erratic operation and can couple noise to the output. Selecting the values for the snubber is best accomplished through empirical methods. First, make sure the lead lengths for the snubber connections are very short. Start with a resistor value between 5 and 50 Ω. Increasing the value of the snubber capacitor results in more damping, but this also increases snubber losses. Select a minimum value for the snubber capacitor that provides adequate damping of the spikes on the switch waveform at heavy load. A snubber may not be necessary with an optimized layout.

8.2.2.18 Disconnect Switch Q_D Selection

The N-channel MOSFET disconnection switch (Q_D) should be selected based on the following criteria:

- The BV_{DSS} rating must be greater than the maximum input voltage, plus ringing and transients.
- The safe operating area (SOA) and the thermal properties should be considered. If required, limit the rise time of the input power supply or the maximum start-up input voltage.
- Absolute maximum rating of V_{GS} should be greater than 18 V.
- If the minimum VIN voltage is less than 6.5 V, a logic level MOSFET should be used.
- The plateau voltage during inrush current limiting is recommended to be less than $V_{GS\text{-}DET}$. If the $V_{PLATEAU}$ is greater than $V_{GS\text{-}DET}$, boost switching might start before finishing the inrush limiting.

8.2.2.19 Freewheeling Diode D_F Selection

If Q_D turns off quickly by the circuit breaker function, the inductor current continues flowing through a freewheeling diode (D_F). D_F should have enough capability to handle 150 mV/R_S of peak current during inductor current decay and the voltage rating must be greater than the maximum input voltage, plus ringing and transients. The inductor current decay time is calculated from Equation 42.

$$t_{DF} = \frac{L_{IN} \times 0.15}{R_S \times (V_{OUT} - V_{IN})} \quad [\text{sec}] \tag{42}$$

8.2.2.20 Loop Compensation Components C_{COMP}, R_{COMP}, C_{HF}

R_{COMP}, C_{COMP} and C_{HF} configure the error amplifier gain and phase characteristics to produce a stable voltage loop. For a quick start, follow the 4 steps listed below:

1. Select f_{CROSS}

   Select the cross over frequency (f_{CROSS}) at one fourth of the RHP zero or one tenth of the switching frequency whichever is lower.

   $$\frac{f_{SW}}{10} = 25 \text{ kHz} \tag{43}$$

   $$\frac{f_{Z_RHP}}{4} = \frac{R_{LOAD} \times (D')^2}{4 \times 2\pi \times L_{IN_EQ}} = \frac{\frac{V_{OUT}}{I_{OUT}} \times (\frac{V_{IN}}{V_{OUT}})^2}{4 \times 2\pi \times L_{IN_EQ}} = 13.4 \text{ kHz} \tag{44}$$

   A 13.4 kHz crossover frequency is selected. RHP zero at minimum input voltage should be considered if the input voltage range is wide.

2. Determine required R_{COMP}

   Knowing f_{CROSS}, R_{COMP} is calculated as follows:

   $$R_{COMP} = f_{CROSS} \times \pi \times R_S \times R_{FB2} \times 10 \times C_{OUT} \times \frac{V_{OUT}}{V_{IN}} = 200 \text{ k}\Omega \tag{45}$$

   A standard value of 200 kΩ is selected for R_{COMP}

3. Determine C_{COMP} to cancel load pole. Place the error amplifier zero at twice the load pole frequency. Knowing R_{COMP}, C_{COMP} is calculated as follows:

   $$C_{COMP} = \frac{R_{LOAD} \times C_{OUT}}{4 \times R_{COMP}} = 7.6\text{nF} \tag{46}$$

   A standard value of 8.2 nF is selected for C_{COMP}

4. Determine C_{HF} to cancel the ESR zero.

   Knowing R_{COMP}, R_{ESR} and C_{COMP}, C_{HF} is calculated as follows:

   $$C_{HF} = \frac{R_{ESR} \times C_{OUT} \times C_{COMP}}{R_{COMP} \times C_{COMP} - R_{ESR} \times C_{OUT}} = 103 \text{ pF} \tag{47}$$

   A standard value of 100 pF is selected for C_{HF}

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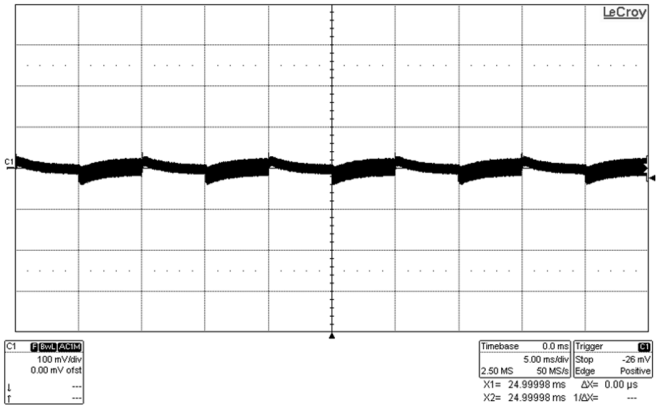
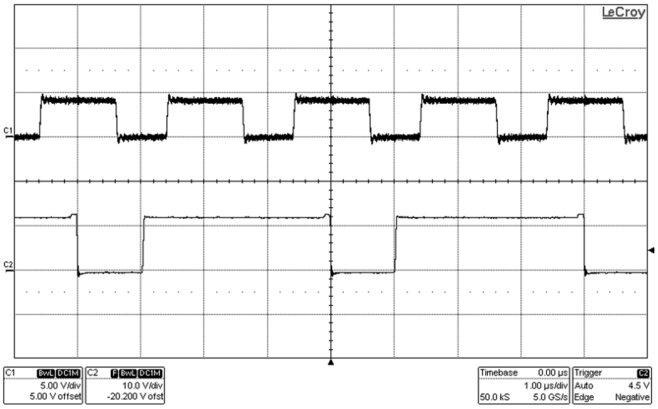
8.2.3 Application Curves



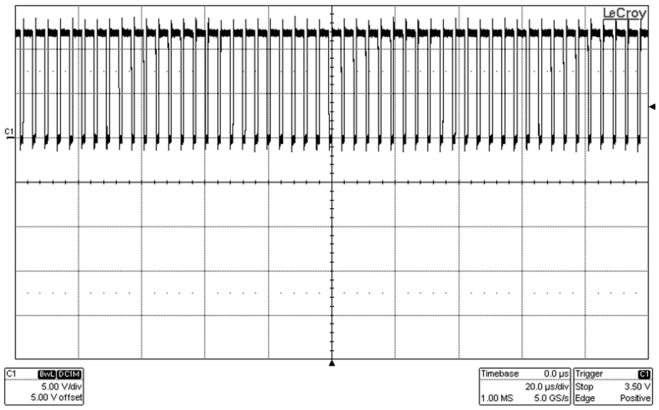
C1: Vout, V_{SUPPLY} = 9 V, 1 A to 2 A and 2 A to 1 A load transient

Figure 42. Load Transient



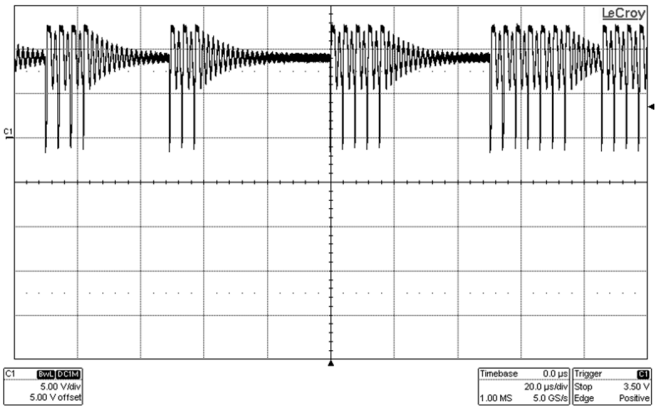
C1: F_{SYNC} , C2: SW, V_{SUPPLY} = 9 V, F_{SYNC} = 500 kHz

Figure 43. Clock Synchronization



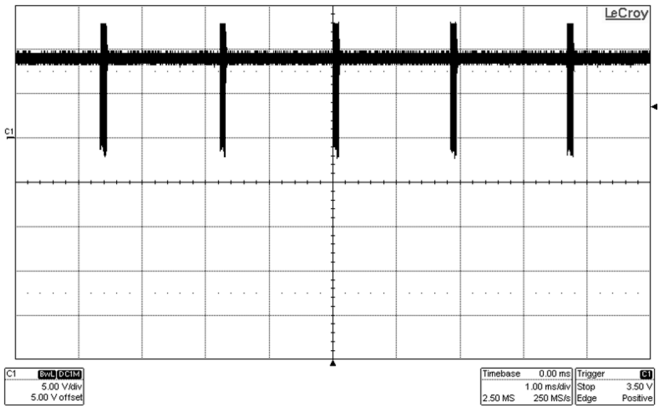
C1:SW, V_{SUPPLY} = 9 V, I_{LOAD} = 0 A

Figure 44. Forced PWM



C1: SW, V_{SUPPLY} = 9 V, I_{LOAD} = 0 A

Figure 45. Pulse Skip



C1:SW, V_{SUPPLY} = 9 V, I_{LOAD} = 0 A

Figure 46. Skip Cycle

9 Power Supply Recommendations

LM5121 is a power management device. The power supply for the device is any DC voltage source within the specified input range.

10 Layout

10.1 Layout Guidelines

In a boost regulator, the primary switching loop consists of the output capacitor and N-channel MOSFET power switches. Minimizing the area of this loop reduces the stray inductance and minimizes noise. Especially, placing high quality ceramic output capacitors as close to this loop earlier than bulk aluminum output capacitors minimizes output voltage ripple and ripple current of the aluminum capacitors.

In order to prevent a dv/dt induced turn-on of high-side switch, HO and SW should be connected to the gate and source of the high-side synchronous N-channel MOSFET switch through short and low inductance paths. In FPWM mode, the dv/dt induced turn-on can occur on the low-side switch. LO and PGND should be connected to the gate and source of the low-side N-channel MOSFET through short and low inductance paths. All of the power ground connections should be connected to a single point. Also, all of the noise sensitive low power ground connections should be connected together near the AGND pin and a single connection should be made to the single point PGND. CSP and CSN are high impedance pins and noise sensitive. CSP and CSN traces should be routed together with kelvin connections to the current sense resistor as short as possible. If needed, place 100-pF ceramic filter capacitor as close to the device. MODE pin is also high impedance and noise sensitive. If an external pull-up or pull-down resistor is used at MODE pin, the resistor should be placed as close the device. VCC, VIN and BST capacitor must be as physically close as possible to the device.

The LM5121 has an exposed thermal pad to aid power dissipation. Adding several vias under the exposed pad helps conduct heat away from the device. The junction to ambient thermal resistance varies with application. The most significant variables are the area of copper in the PC board, the number of vias under the exposed pad and the amount of forced air cooling. The integrity of the solder connection from the device exposed pad to the PC board is critical. Excessive voids greatly decrease the thermal dissipation capacity. The highest power dissipating components are the two power switches. Selecting N-channel MOSFET switches with exposed pads aids the power dissipation of these devices.

10.2 Layout Example

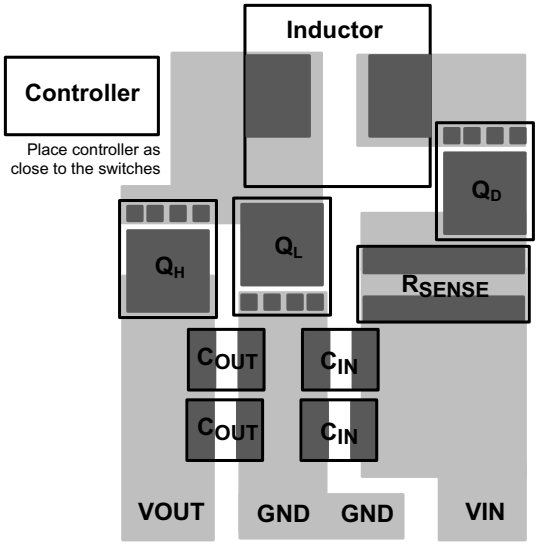


Figure 47. Power Path Layout

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11 Device and Documentation Support

11.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 2. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
LM5121	Click here	Click here	Click here	Click here	Click here
LM5121-Q1	Click here	Click here	Click here	Click here	Click here

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM5121MH/NOPB	ACTIVE	HTSSOP	PWP	20	73	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 125	LM5121 MH	Samples
LM5121MHE/NOPB	ACTIVE	HTSSOP	PWP	20	250	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 125	LM5121 MH	Samples
LM5121MHX/NOPB	ACTIVE	HTSSOP	PWP	20	2500	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 125	LM5121 MH	Samples
LM5121QMH/NOPB	ACTIVE	HTSSOP	PWP	20	73	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 125	LM5121 QMH	Samples
LM5121QMHE/NOPB	ACTIVE	HTSSOP	PWP	20	250	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 125	LM5121 QMH	Samples
LM5121QMHX/NOPB	ACTIVE	HTSSOP	PWP	20	2500	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 125	LM5121 QMH	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF LM5121, LM5121-Q1 :

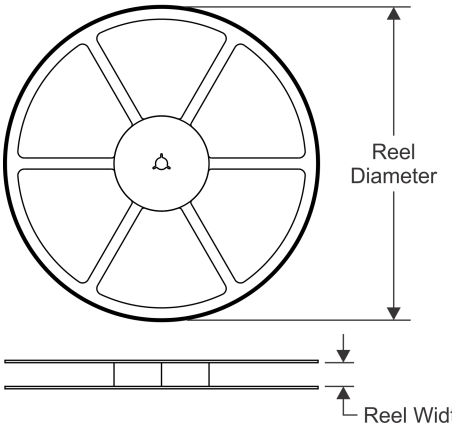
- Catalog: LM5121
- Automotive: LM5121-Q1

NOTE: Qualified Version Definitions:

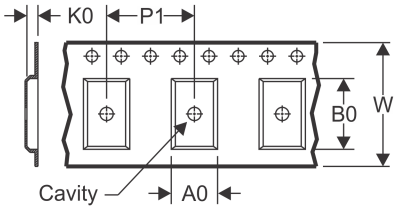
- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

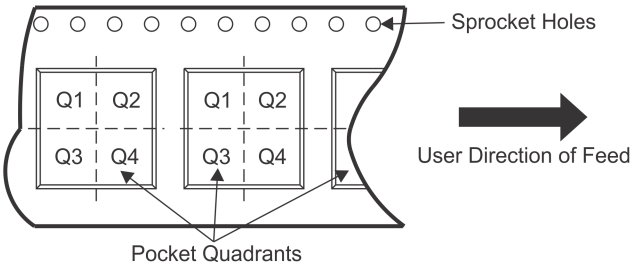


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

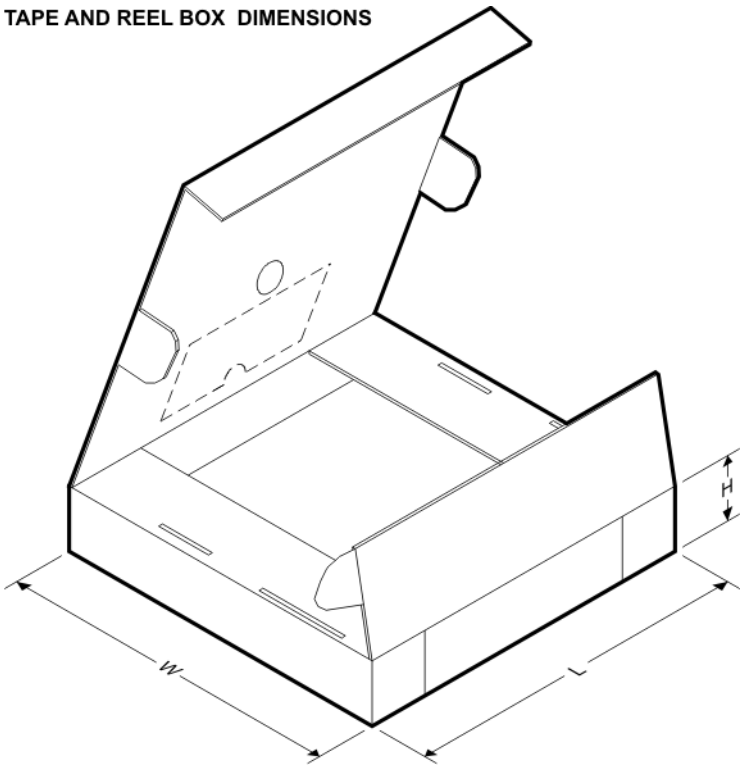
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM5121MHE/NOPB	HTSSOP	PWP	20	250	178.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
LM5121MHX/NOPB	HTSSOP	PWP	20	2500	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
LM5121QMHE/NOPB	HTSSOP	PWP	20	250	178.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
LM5121QMHX/NOPB	HTSSOP	PWP	20	2500	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1

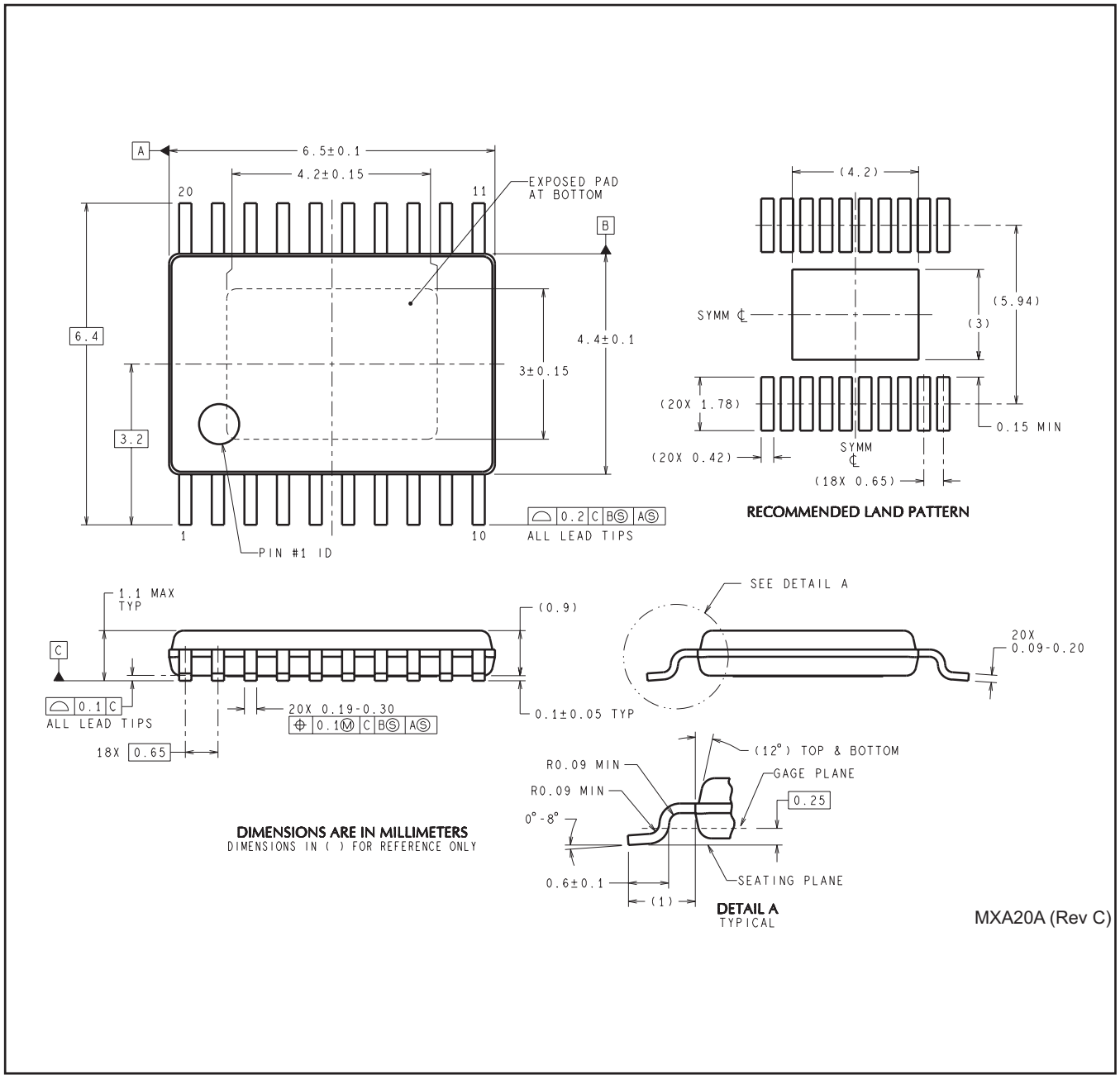
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM5121MHE/NOPB	HTSSOP	PWP	20	250	210.0	185.0	35.0
LM5121MHX/NOPB	HTSSOP	PWP	20	2500	367.0	367.0	35.0
LM5121QMHE/NOPB	HTSSOP	PWP	20	250	210.0	185.0	35.0
LM5121QMHX/NOPB	HTSSOP	PWP	20	2500	367.0	367.0	35.0

PWP0020A


A
6.5±0.1
4.2±0.15
20
11
EXPOSED PAD
AT BOTTOM
B
6.4
4.4±0.1
3±0.15
3.2
1
10
PIN #1 ID
0.2 C B S A S
ALL LEAD TIPS
(4.2)
(5.94)
SYMM ℄
(3)
(20X 1.78)
0.15 MIN
(20X 0.42)
SYMM
℄
(18X 0.65)
RECOMMENDED LAND PATTERN
1.1 MAX
TYP
(0.9)
C
0.1 C
ALL LEAD TIPS
20X 0.19-0.30
0.1 M C B S A S
18X 0.65
0.1±0.05 TYP
SEE DETAIL A
20X
0.09-0.20
(12°) TOP & BOTTOM
R0.09 MIN
GAGE PLANE
R0.09 MIN
0.25
0°-8°
0.6±0.1
SEATING PLANE
(1)
DETAIL A
TYPICAL
DIMENSIONS ARE IN MILLIMETERS
DIMENSIONS IN ( ) FOR REFERENCE ONLY
MXA20A (Rev C)

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