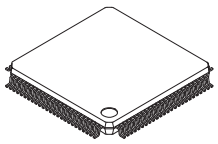
LC75808W

1/8 to 1/10-Duty LCD Driver with Key Input Function

ON Semiconductor®

www.onsemi.com



SPQFP100 14x14 / SQFP100

Overview

The LC75808W is 1/8 to 1/10 duty LCD display driver that can directly drive up to 600 segments and can control up to four general-purpose output ports. This product also incorporates a key scan circuit that accepts input from up to 30 keys to reduce printed circuit board wiring.

Features

- Key input function for up to 30 keys (A key scan is performed only when a key is pressed.)
- 1/8duty–1/4bias, 1/9duty–1/4bias, and 1/10duty–1/4bias drive schemes can be controlled from serial data.
  - 1/8duty–1/4bias : up to 480 segments
  - 1/9duty–1/4bias : up to 540 segments
  - 1/10duty–1/4bias : up to 600 segments
- Sleep mode and all segments off functions that are controlled from serial data.
- Serial data I/O supports CCB* format communication with the system controller.
- Direct display of display data without the use of a decoder provides high generality.
- Built-in display contrast adjustment circuit.
- Up to 4 general-purpose output ports are included.
- Independent LCD driver block power supply V_{LCD}.
- Provision of an on-chip voltage-detection type reset circuit prevents incorrect displays.
- The $\overline{INH}$ pin is provided. This pin turns off the display, disables key scanning, and forces the general-purpose output ports to the low level.
- RC oscillator circuit.

* Computer Control Bus (CCB) is an ON Semiconductor's original bus format and the bus addresses are controlled by ON Semiconductor.

ORDERING INFORMATION

See detailed ordering and shipping information on page 39 of this data sheet.

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Specifications

Absolute Maximum Ratings at Ta = 25°C, V_{SS} = 0 V

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{DD} max	V_{DD}	−0.3 to +7.0	V
	V_{LCD} max	V_{LCD}	−0.3 to +12.0	
Input voltage	$V_{IN}1$	CE, CL, DI, $\overline{INH}$	−0.3 to +7.0	V
	$V_{IN}2$	OSC, KI1 to KI5, TEST	−0.3 to V_{DD}+0.3	
	$V_{IN}3$	$V_{LCD}1$, $V_{LCD}2$, $V_{LCD}3$, $V_{LCD}4$	−0.3 to V_{LCD}+0.3	
Output voltage	$V_{OUT}1$	DO	−0.3 to +7.0	V
	$V_{OUT}2$	OSC, KS1 to KS6, P1 to P4	−0.3 to V_{DD}+0.3	
	$V_{OUT}3$	$V_{LCD}0$, S1 to S60, COM1 to COM10	−0.3 to V_{LCD}+0.3	
Output current	$I_{OUT}1$	S1 to S60	300	μA
	$I_{OUT}2$	COM1 to COM10	3	mA
	$I_{OUT}3$	KS1 to KS6	1	
	$I_{OUT}4$	P1 to P4	5	
Allowable power dissipation	Pd max	Ta = 85°C	200	mW
Operating temperature	Topr		−40 to +85	°C
Storage temperature	Tstg		−55 to +125	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Allowable Operating Ranges at Ta = −40 to +85°C, V_{SS} = 0 V

Parameter	Symbol	Conditions	Ratings			unit
			min	typ	max	
Supply voltage	V_{DD}	V_{DD}	4.5		6.0	V
	V_{LCD}	V_{LCD}, When the display contrast adjustment circuit is used	7.0		11.0	
	V_{LCD}	V_{LCD} , When the display contrast adjustment circuit is not used	4.5		11.0	
Output voltage	$V_{LCD}0$	$V_{LCD}0$	$V_{LCD}4$ +4.5		V_{LCD}	V
Input voltage	$V_{LCD}1$	$V_{LCD}1$		3/4($V_{LCD}0$ −$V_{LCD}4$)	$V_{LCD}0$	V
	$V_{LCD}2$	$V_{LCD}2$		2/4($V_{LCD}0$ −$V_{LCD}4$)	$V_{LCD}0$	
	$V_{LCD}3$	$V_{LCD}3$		1/4($V_{LCD}0$ −$V_{LCD}4$)	$V_{LCD}0$	
	$V_{LCD}4$	$V_{LCD}4$	0		1.5	
Input high level voltage	$V_{IH}1$	CE, CL, DI, $\overline{INH}$	0.8V_{DD}		6.0	V
	$V_{IH}2$	KI1 to KI5	0.6V_{DD}		V_{DD}	V
Input low level voltage	V_{IL}	CE, CL, DI, $\overline{INH}$, KI1 to KI5	0		0.2V_{DD}	V
Recommended external resistance	R_{OSC}	OSC		43		kΩ
Recommended external capacitance	C_{OSC}	OSC		680		pF
Guaranteed oscillation range	f_{OSC}	OSC	25	50	100	kHz
Data setup time	tds	CL, DI [Figure 2]	160			ns
Data hold time	tdh	CL, DI [Figure 2]	160			ns
CE wait time	tcp	CE, CL [Figure 2]	160			ns
CE setup time	tcs	CE, CL [Figure 2]	160			ns
CE hold time	tch	CE, CL [Figure 2]	160			ns
High level clock pulse width	tϕH	CL [Figure 2]	160			ns
Low level clock pulse width	tϕL	CL [Figure 2]	160			ns
DO output delay time	tdc	DO R_{PU} = 4.7 kΩ, C_L = 10 pF *1 [Figure 2]			1.5	μs
DO rise time	tdr	DO R_{PU} = 4.7 kΩ, C_L=10 pF *1 [Figure 2]			1.5	μs

Note: *1. Since DO is an open-drain output, these values depend on the resistance of the pull-up resistor R_{PU} and the load capacitance C_L.

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

Electrical Characteristics for the Allowable Operating Ranges

Parameter	Symbol	Conditions	Ratings			unit
			min	typ	max	
Hysteresis	V_H	CE, CL, DI, $\overline{INH}$, KI1 to KI5		$0.1V_{DD}$		V
Power-down detection voltage	V_{DET}		2.5	3.0	3.5	V
Input high level current	I_{IH}	CE, CL, DI, $\overline{INH}$: V_I = 6.0 V			5.0	μA
Input low level current	I_{IL}	CE, CL, DI, $\overline{INH}$: V_I = 0 V	-5.0			μA
Input floating voltage	V_{IF}	KI1 to KI5			$0.05V_{DD}$	V
Pull-down resistance	R_{PD}	KI1 to KI5: V_{DD} = 5.0 V	50	100	250	kΩ
Output off leakage current	I_{OFFH}	DO: V_O = 6.0 V			6.0	μA
Output high level voltage	$V_{OH}1$	S1 to S60: I_O = −20 μA	$V_{LCD}0-0.6$			V
	$V_{OH}2$	COM1 to COM10: I_O = −100 μA	$V_{LCD}0-0.6$			
	$V_{OH}3$	KS1 to KS6: I_O = −500 μA	$V_{DD}-1.0$	$V_{DD}-0.5$	$V_{DD}-0.2$	
	$V_{OH}4$	P1 to P4: I_O = −1 mA	$V_{DD}-1.0$			
Output low level voltage	$V_{OL}1$	S1 to S60: I_O = 20 μA			$V_{LCD}4+0.6$	V
	$V_{OL}2$	COM1 to COM10: I_O = 100 μA			$V_{LCD}4+0.6$	
	$V_{OL}3$	KS1 to KS6: I_O = 25 μA	0.2	0.5	1.5	
	$V_{OL}4$	P1 to P4: I_O = 1 mA			1.0	
	$V_{OL}5$	DO: I_O= 1 mA		0.1	0.5	
Output middle level voltage *2	$V_{MID}1$	S1 to S60: I_O = ±20 μA	$2/4(V_{LCD}0-V_{LCD}4)-0.6$		$2/4(V_{LCD}0-V_{LCD}4)+0.6$	V
	$V_{MID}2$	COM1 to COM10: I_O = ±100 μA	$3/4(V_{LCD}0-V_{LCD}4)-0.6$		$3/4(V_{LCD}0-V_{LCD}4)+0.6$	
	$V_{MID}3$	COM1 to COM10: I_O = ±100 μA	$1/4(V_{LCD}0-V_{LCD}4)-0.6$		$1/4(V_{LCD}0-V_{LCD}4)+0.6$	
Oscillator frequency	f_{OSC}	OSC: R_{OSC} = 43 kΩ, C_{OSC} = 680 pF	40	50	60	kHz
Current drain	$I_{DD}1$	V_{DD}: Sleep mode			100	μA
	$I_{DD}2$	V_{DD}: V_{DD} = 6.0 V, outputs open, f_{OSC} = 50 kHz		250	500	
	$I_{LCD}1$	V_{LCD}: Sleep mode			5	
	$I_{LCD}2$	V_{LCD}: V_{LCD} = 11.0 V, Outputs open, f_{OSC} = 50 kHz (When the display contrast adjustment circuit is used.)		500	1000	
	$I_{LCD}3$	V_{LCD}: V_{LCD} = 11.0 V, Outputs open, f_{OSC} = 50 kHz (When the display contrast adjustment circuit is not used.)		250	500	

Note: *2 Excluding the bias voltage generation divider resistor built into $V_{LCD}0$, $V_{LCD}1$, $V_{LCD}2$, $V_{LCD}3$, and $V_{LCD}4$. (See Figure 1.)

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

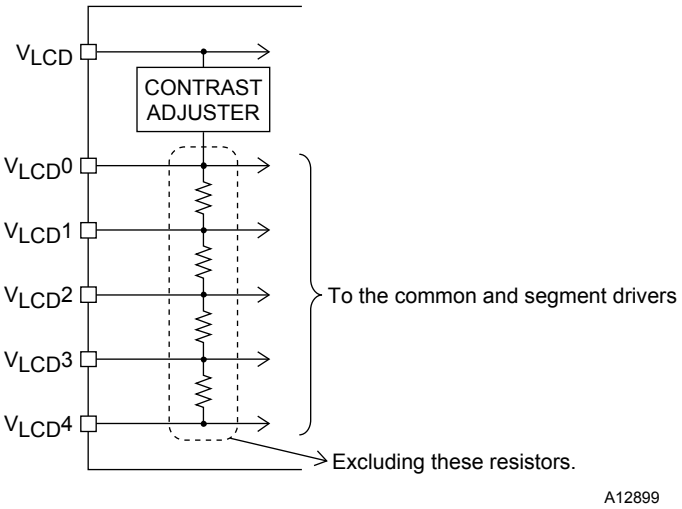
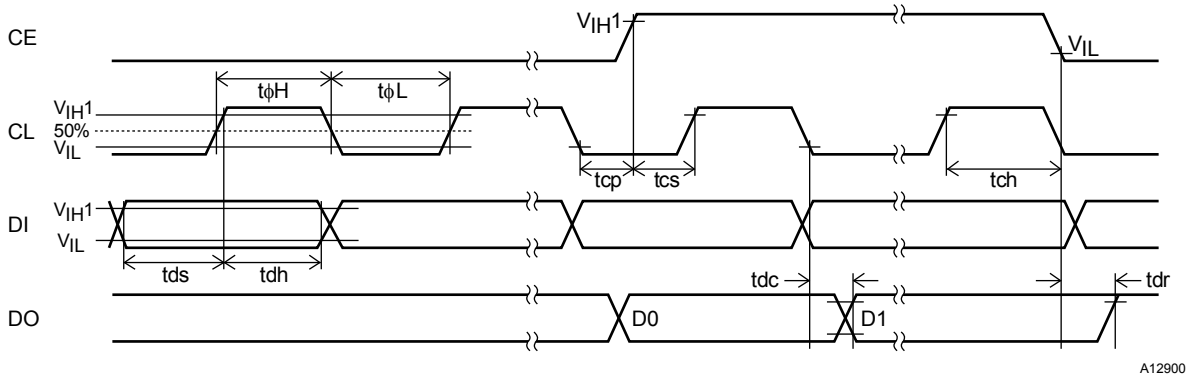


Figure 1

1. When CL is stopped at the low level



2. When CL is stopped at the high level

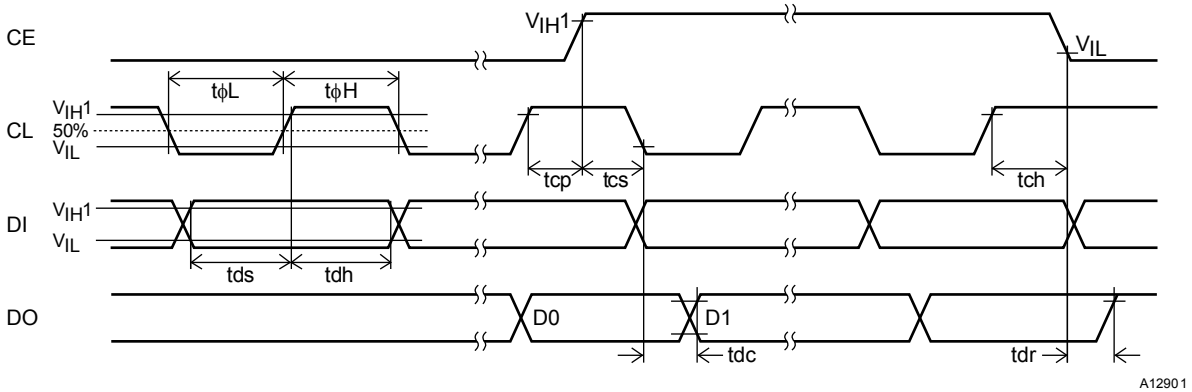
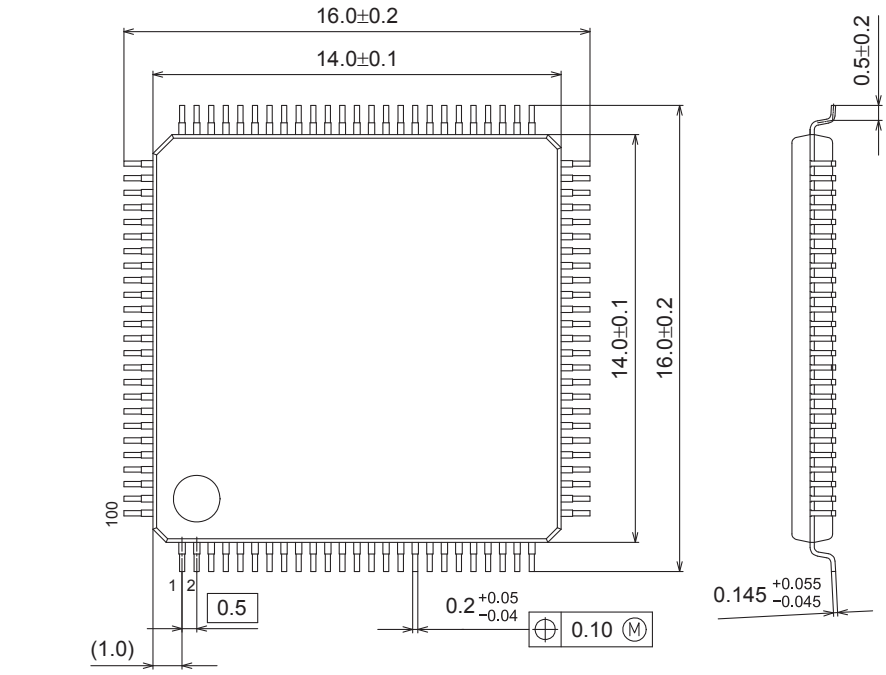


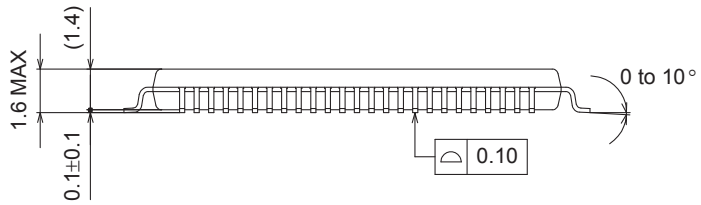
Figure 2

Package Dimensions

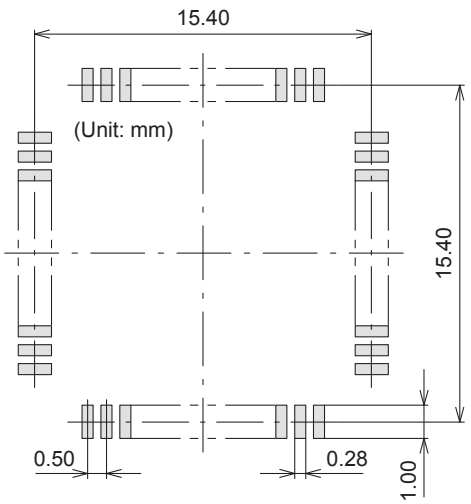
unit : mm

SPQFP100 14x14 / SQFP100
CASE 131AC
ISSUE A

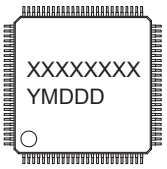




SOLDERING FOOTPRINT*



GENERIC MARKING DIAGRAM*



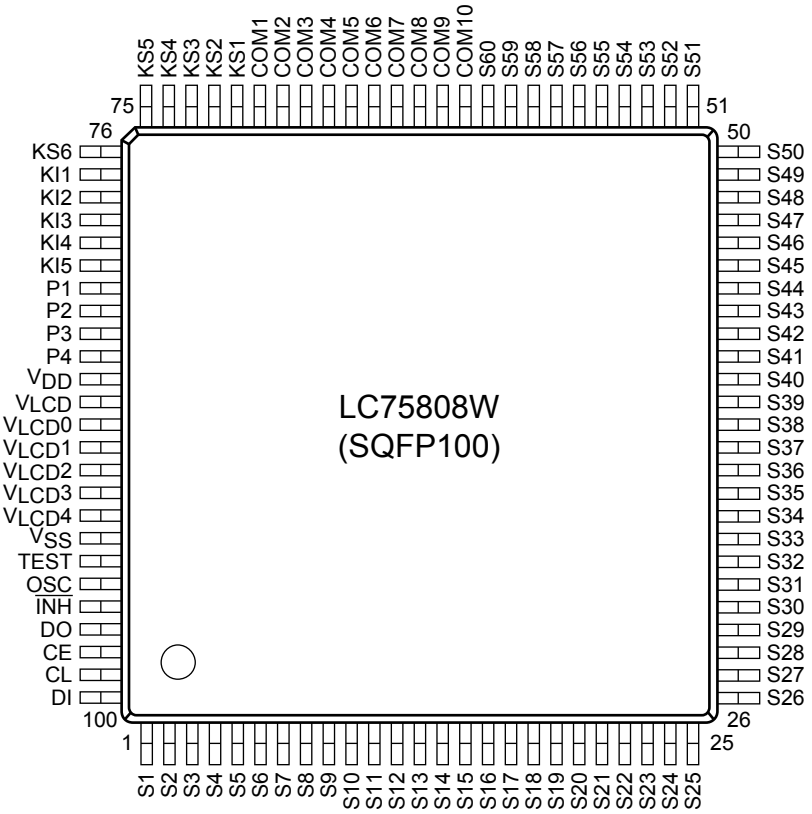
XXXXX = Specific Device Code
Y = Year
M = Month
DDD = Additional Traceability Data

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, “G” or microdot “ ▪”, may or may not be present.

NOTE: The measurements are not to guarantee but for reference only.

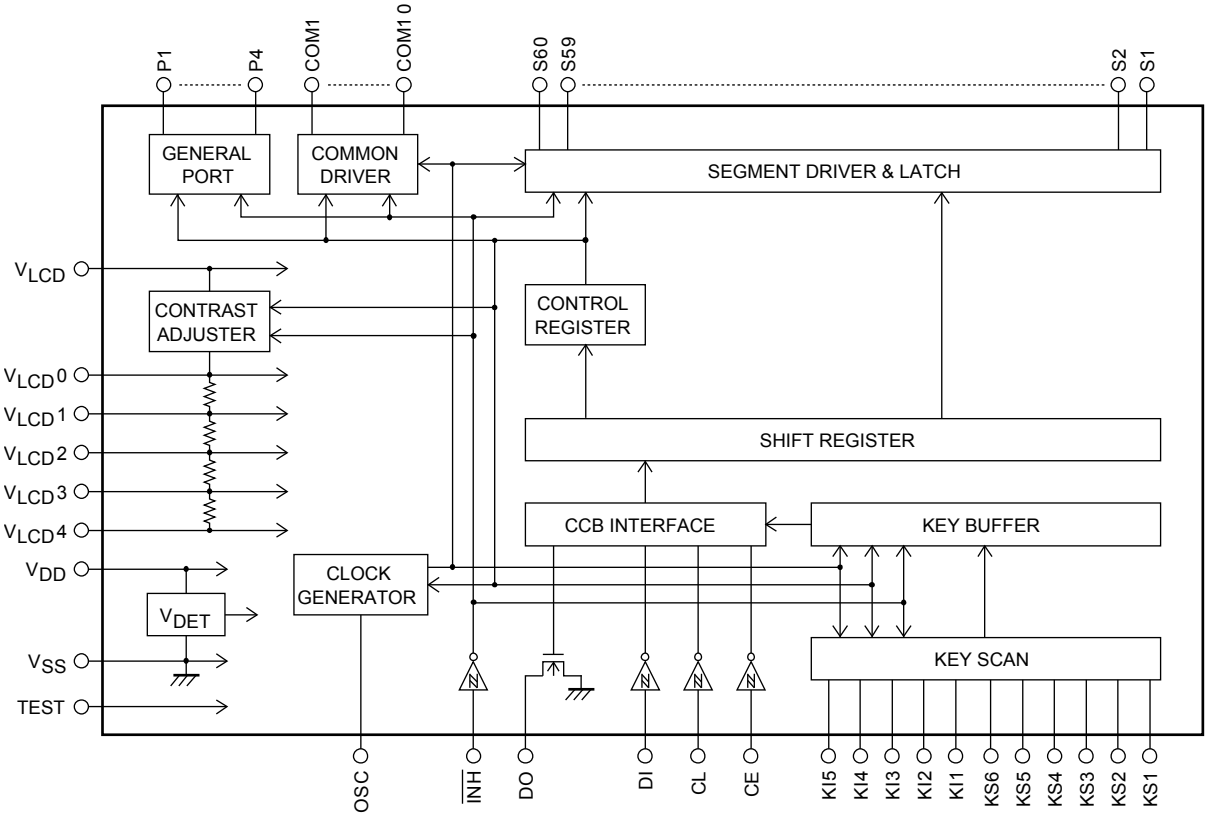
*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

Pin Assignment



Top view

Block Diagram



A12902

Pin Functions

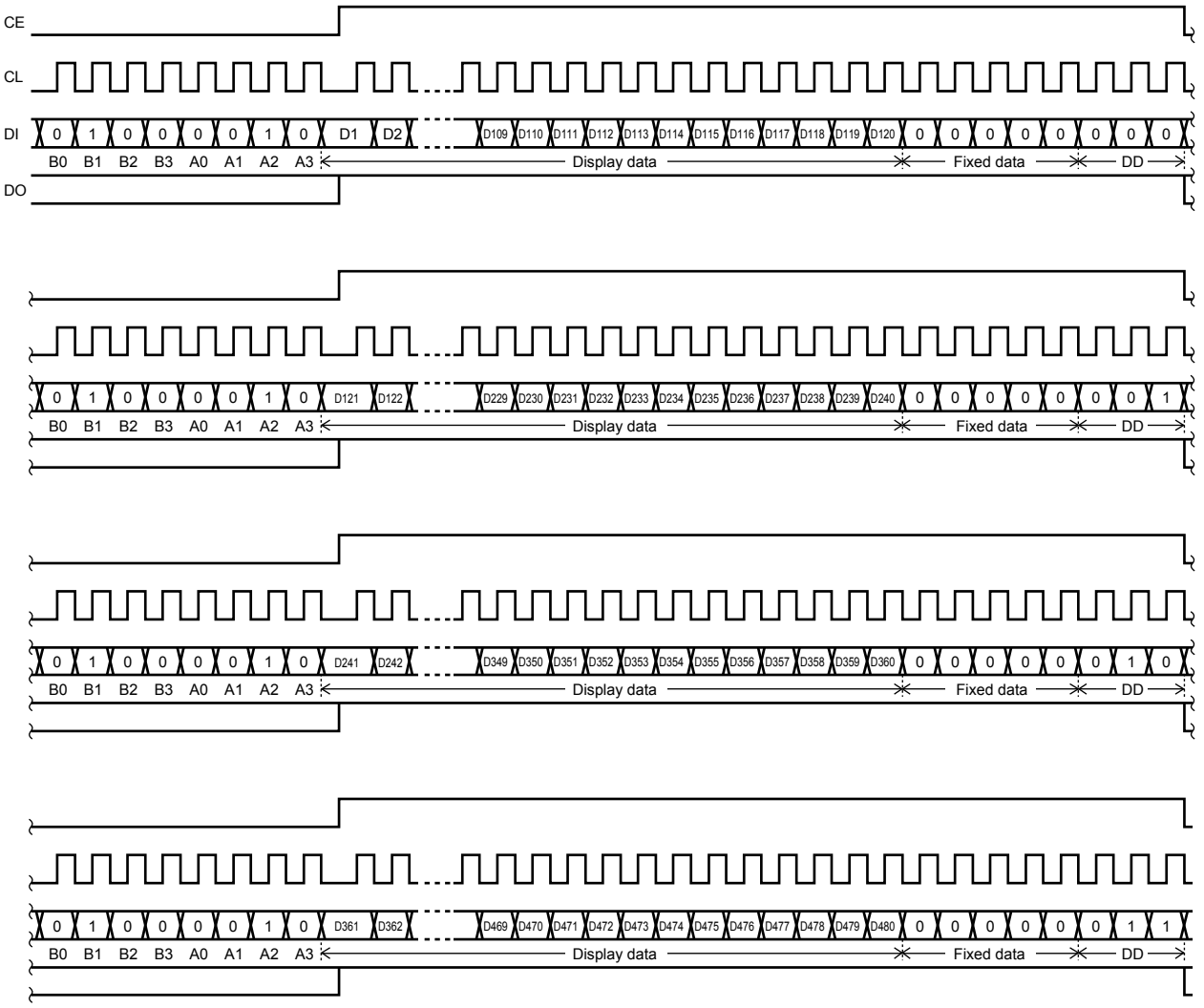
Symbol	Pin No.	Function	Active	I/O	Handling when unused
S1 to S60	1 to 60	Segment driver outputs.	-	O	OPEN
COM1 to COM10	70 to 61	Common driver outputs.	-	O	OPEN
KS1 to KS6	71 to 76	Key scan outputs. Although normal key scan timing lines require diodes to be inserted in the timing lines to prevent shorts, since these outputs are unbalanced CMOS transistor outputs, these outputs will not be damaged by shorting when these outputs are used to form a key matrix.	-	O	OPEN
KI1 to KI5	77 to 81	Key scan inputs. These pins have built-in pull-down resistors.	H	I	GND
P1 to P4	82 to 85	General-purpose output ports.	-	O	OPEN
OSC	95	Oscillator connection. An oscillator circuit is formed by connecting an external resistor and capacitor at this pin.	-	I/O	V_{DD}
CE	98	Serial data interface connections to the controller. Note that DO, being an open-drain output, requires a pull-up resistor. CE: Chip enable CL: Synchronization clock DI: Transfer data DO: Output data	H	I	GND
CL	99		↑	I	
DI	100		-	I	
DO	97		-	O	OPEN
$\overline{INH}$	96	Input that turns the display off, disables key scanning, and forces the general-purpose output ports low. • When $\overline{INH}$ is low (V_{SS}): • Display off S1 to S60 = "L" ($V_{LCD}4$). COM1 to COM10 = "L" ($V_{LCD}4$). • General-purpose output ports P1 to P4 = low (V_{SS}) • Key scanning is disabled: KS1 to KS6 = low (V_{SS}) • All the key data is reset to low. • When $\overline{INH}$ is high (V_{DD}): • Display on • The states of the general-purpose output ports can be set by the PC1 to PC4 control data. • Key scanning is enabled. However, serial data can be transferred when the $\overline{INH}$ pin is low.	L	I	V_{DD}
TEST	94	This pin must be connected to ground.	-	I	-
$V_{LCD}0$	88	LCD drive 4/4 bias voltage (high level) supply pin. The level on this pin can be changed by the display contrast adjustment circuit. However, ($V_{LCD}0$ - $V_{LCD}4$) must be greater than or equal to 4.5V. Also, external power must not be applied to this pin since the pin circuit includes the display contrast adjustment circuit.	-	O	OPEN
$V_{LCD}1$	89	LCD drive 3/4 bias voltage (middle level) supply pin. This pin can be used to supply the 3/4 ($V_{LCD}0$ - $V_{LCD}4$) voltage level externally.	-	I	OPEN
$V_{LCD}2$	90	LCD drive 2/4 bias voltage (middle level) supply pin. This pin can be used to supply the 2/4 ($V_{LCD}0$ - $V_{LCD}4$) voltage level externally.	-	I	OPEN
$V_{LCD}3$	91	LCD drive 1/4 bias voltage (middle level) supply pin. This pin can be used to supply the 1/4 ($V_{LCD}0$ - $V_{LCD}4$) voltage level externally.	-	I	OPEN
$V_{LCD}4$	92	LCD drive 0/4 bias voltage (low level) supply pin. Fine adjustment of the display contrast can be implemented by connecting an external variable resistor to this pin. However, ($V_{LCD}0$ - $V_{LCD}4$) must be greater than or equal to 4.5V, and $V_{LCD}4$ must be in the range 0 V to 1.5V, inclusive.	-	I	GND
V_{DD}	86	Logic block power supply connection. Provide a voltage of between 4.5 and 6.0V.	-	-	-
V_{LCD}	87	LCD driver block power supply connection. Provide a voltage of between 7.0 and 11.0V when the display contrast adjustment circuit is used and provide a voltage of between 4.5 and 11.0V when the circuit is not used.	-	-	-
V_{SS}	93	Power supply connection. Connect to ground.	-	-	-

Serial Data Input

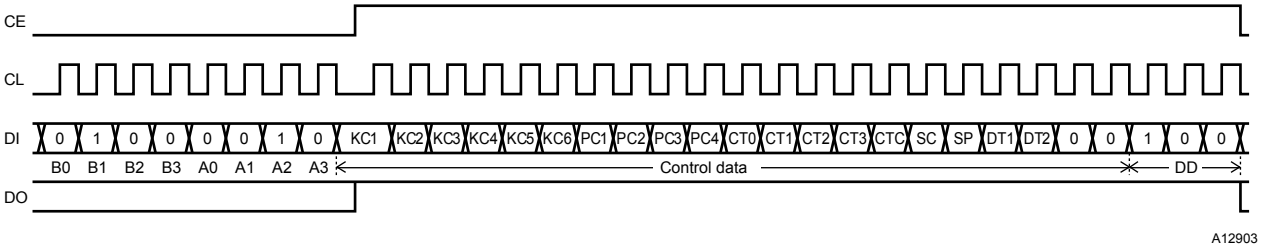
1. 1/8 duty

(1) When CL is stopped at the low level.

• When the display data is transferred.



• When the control data is transferred.



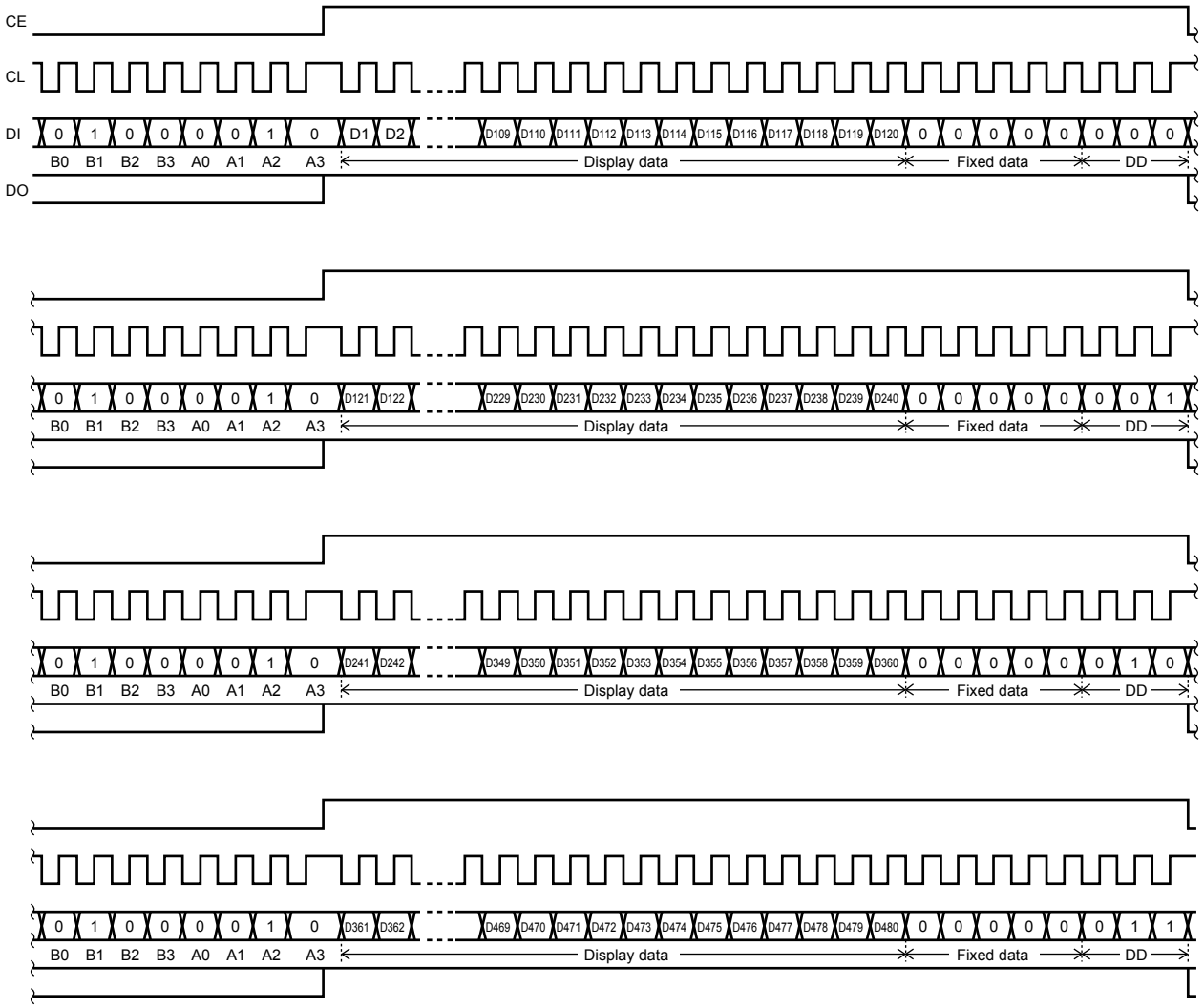
A12903

Note: B0 to B3, A0 to A3..... CCB address

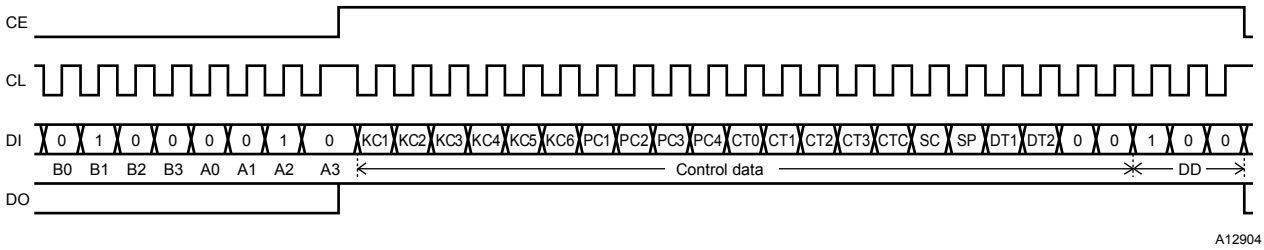
DD ..... Direction data

(2) When CL is stopped at the high level.

• When the display data is transferred.



• When the control data is transferred.



A12904

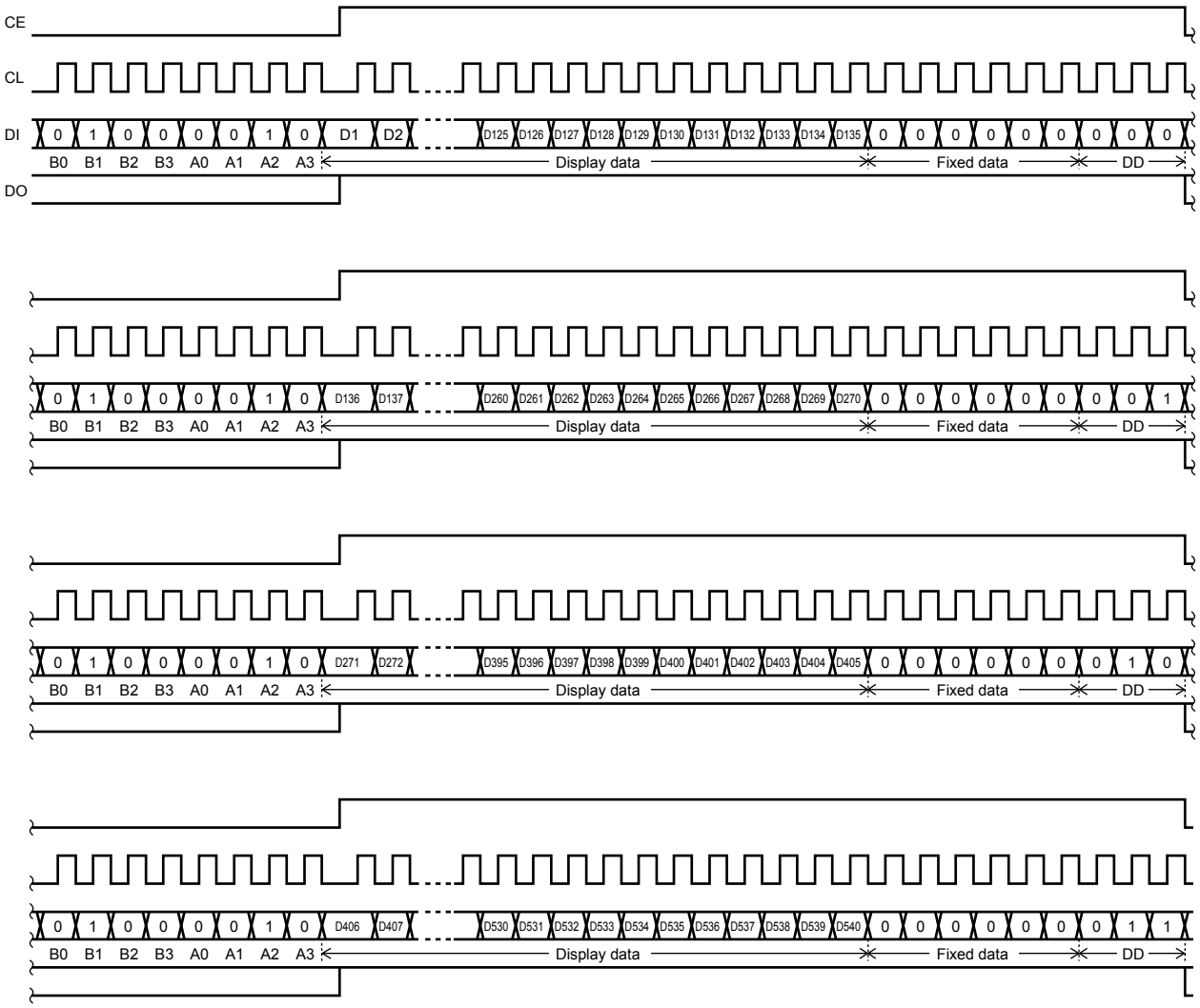
Note: B0 to B3, A0 to A3.....CCB address
DD..... Direction data

• CCB address: ……..... 42H
• D1 to D480: ..... Display data
• KC1 to KC6: ……..... Key scan output state setting data
• PC1 to PC4:……..... General-purpose output port state setting data
• CT0 to CT3, CTC: …… Display contrast setting data
• SC: ..... Segment on/off control data
• SP: ..... Normal mode/sleep mode control data
• DT1, DT2: ..... Display technique setting data

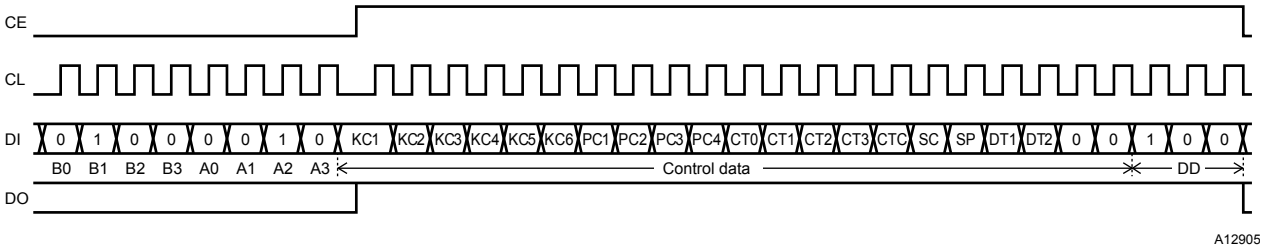
2. 1/9 duty

(1) When CL is stopped at the low level.

• When the display data is transferred.



• When the control data is transferred.



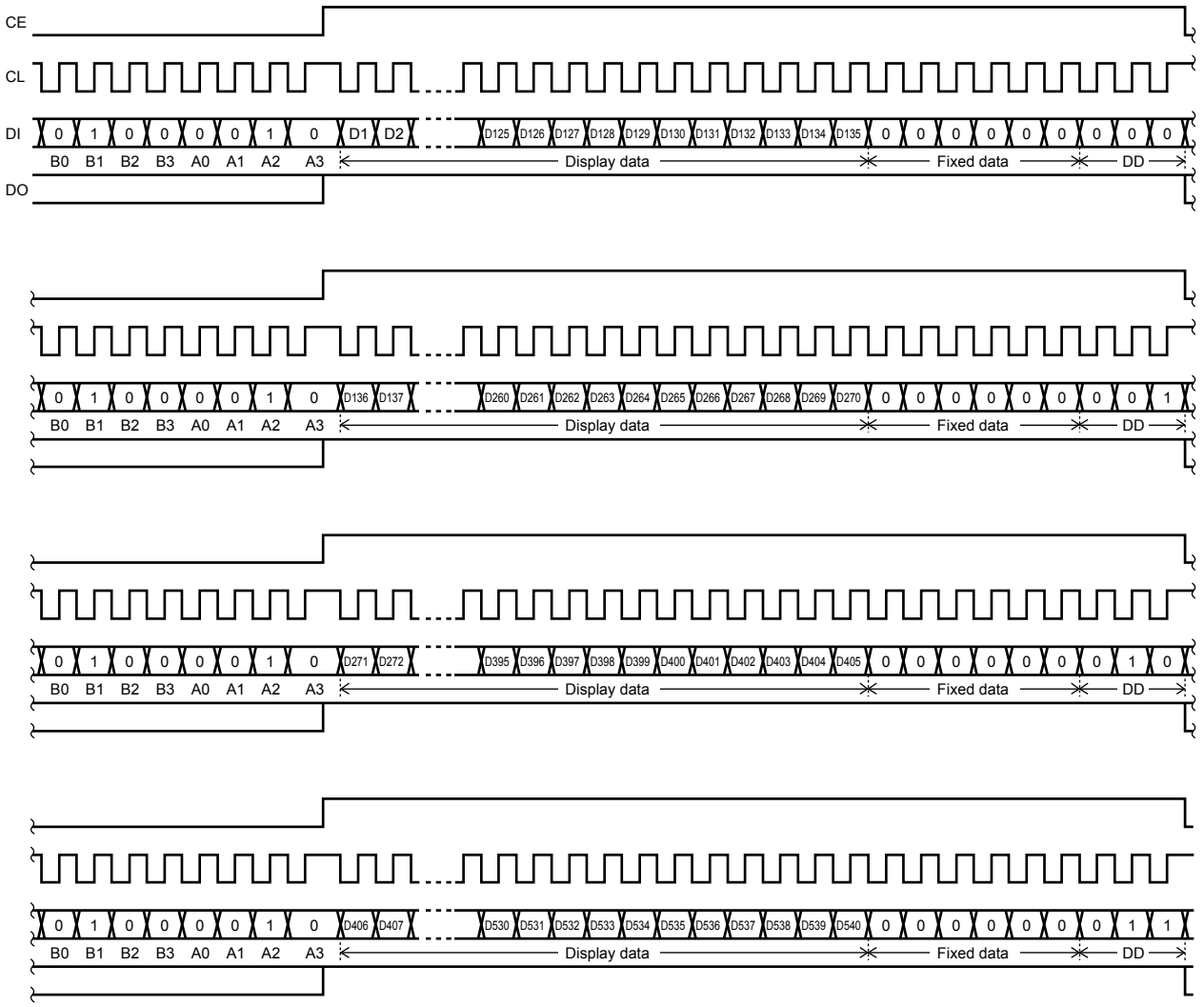
A12905

Note: B0 to B3, A0 to A3..... CCB address

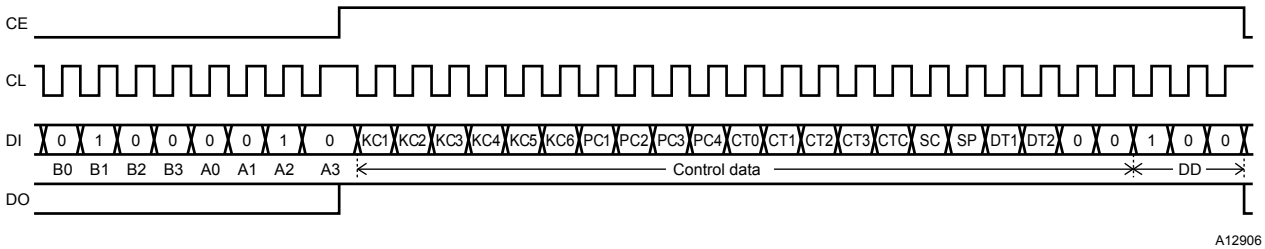
DD ..... Direction data

(2) When CL is stopped at the high level.

• When the display data is transferred.



• When the control data is transferred.



A12906

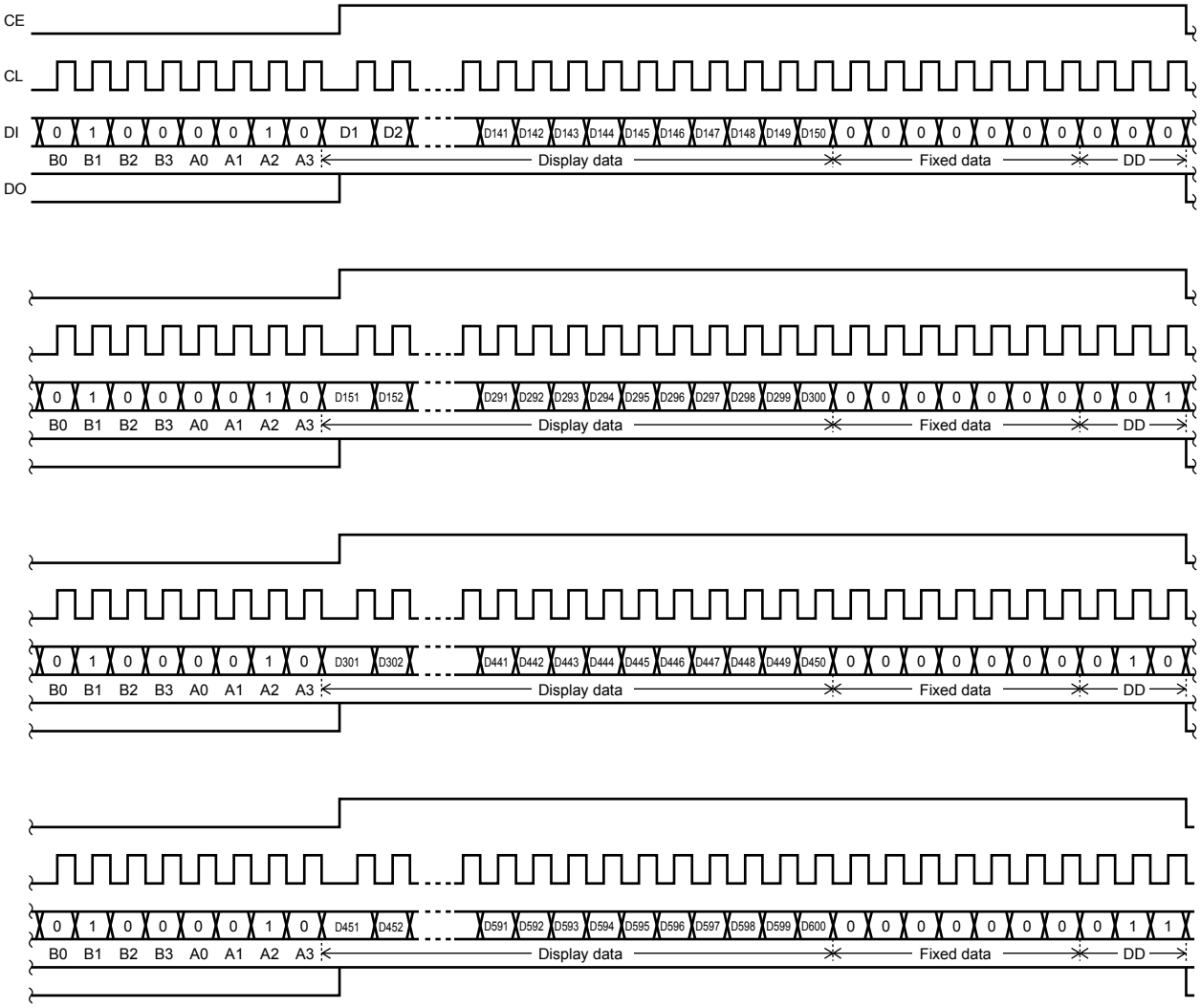
Note: B0 to B3, A0 to A3.....CCB address
DD..... Direction data

- CCB address: ……..... 42H
- D1 to D540: ..... Display data
- KC1 to KC6: ……..... Key scan output state setting data
- PC1 to PC4:……..... General-purpose output port state setting data
- CT0 to CT3, CTC: …… Display contrast setting data
- SC: ..... Segment on/off control data
- SP: ..... Normal mode/sleep mode control data
- DT1, DT2: ..... Display technique setting data

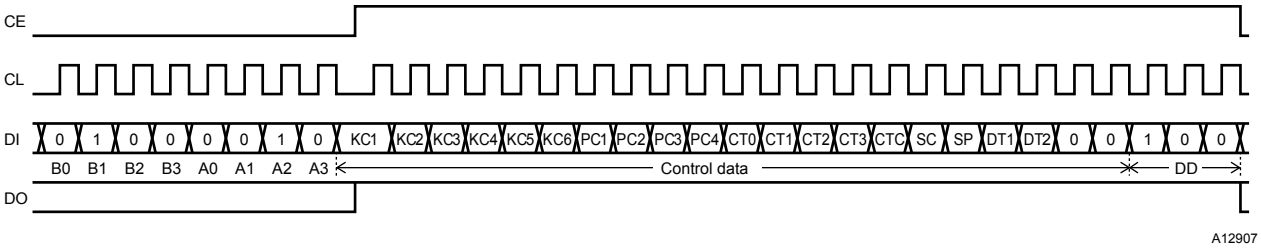
3. 1/10 duty

(1) When CL is stopped at the low level.

• When the display data is transferred.



• When the control data is transferred.



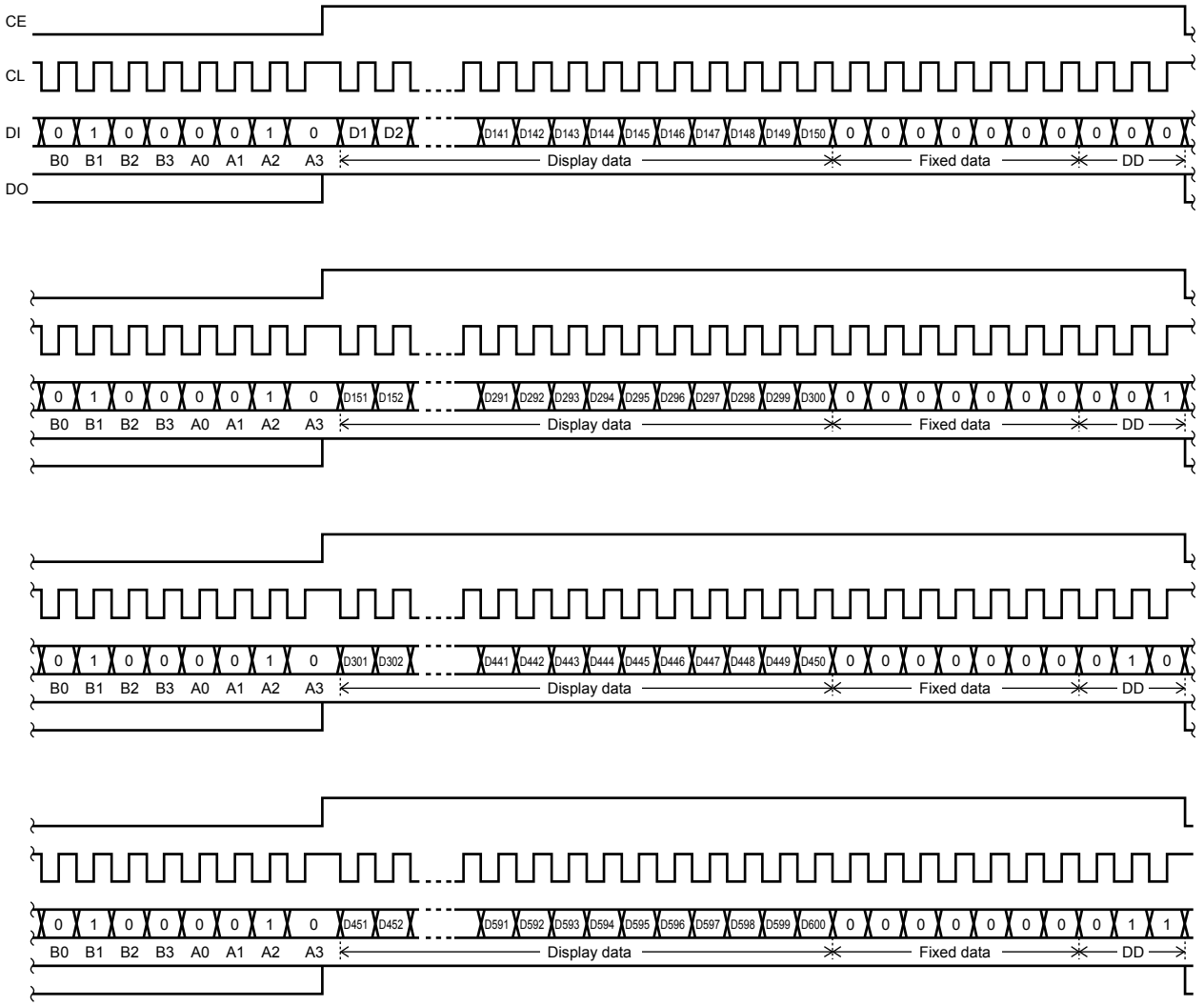
A12907

Note: B0 to B3, A0 to A3..... CCB address

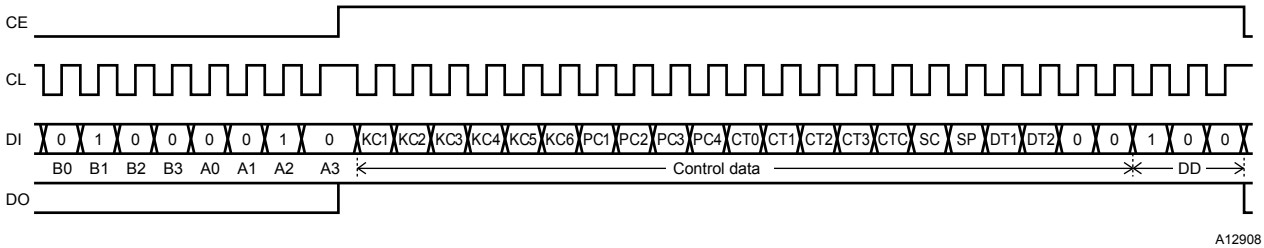
DD ..... Direction data

(2) When CL is stopped at the high level.

• When the display data is transferred.



• When the control data is transferred.



A12908

Note: B0 to B3, A0 to A3.....CCB address
DD..... Direction data

- CCB address: ……..... 42H
- D1 to D600: ..... Display data
- KC1 to KC6: ……..... Key scan output state setting data
- PC1 to PC4:……..... General-purpose output port state setting data
- CT0 to CT3, CTC: …… Display contrast setting data
- SC: ..... Segment on/off control data
- SP: ..... Normal mode/sleep mode control data
- DT1, DT2: ..... Display technique setting data

Control Data Functions

1. KC1 to KC6: Key scan output state setting data

These control data bits set the states of the key scan output pins KS1 to KS6.

Output pin	KS1	KS2	KS3	KS4	KS5	KS6
Key scan output state setting data	KC1	KC2	KC3	KC4	KC5	KC6

For example, if KC1 to KC3 are set to 1, and KC4 to KC6 are set to 0, then the output pins KS1 to KS3 will output high levels (V_{DD}) and the output pins KS4 to KS6 will output low levels (V_{SS}) in the key scan standby state.
Note that key scan output signal is not output from output pins that are set low.

2. PC1 to PC4: General-purpose output port state setting data

These control data bits set the states of the general-purpose output ports P1 to P4.

Output pin	P1	P2	P3	P4
General-purpose output port state setting data	PC1	PC2	PC3	PC4

For example, if PC1 and PC2 are set to 1, and PC3 and PC4 are set to 0, then the output pins P1 and P2 will output high levels (V_{DD}) and the output pins P3 and P4 will output low levels (V_{SS}).

3. CT0 to CT3, CTC: Display contrast setting data

These control data bits set the display contrast.

CT0 to CT3: Display contrast setting (11 steps)

CT0	CT1	CT2	CT3	LCD drive 4/4 bias voltage supply $V_{LCD}0$ level
0	0	0	0	$0.94V_{LCD}=V_{LCD}-(0.03V_{LCD}\times2)$
1	0	0	0	$0.91V_{LCD}=V_{LCD}-(0.03V_{LCD}\times3)$
0	1	0	0	$0.88V_{LCD}=V_{LCD}-(0.03V_{LCD}\times4)$
1	1	0	0	$0.85V_{LCD}=V_{LCD}-(0.03V_{LCD}\times5)$
0	0	1	0	$0.82V_{LCD}=V_{LCD}-(0.03V_{LCD}\times6)$
1	0	1	0	$0.79V_{LCD}=V_{LCD}-(0.03V_{LCD}\times7)$
0	1	1	0	$0.76V_{LCD}=V_{LCD}-(0.03V_{LCD}\times8)$
1	1	1	0	$0.73V_{LCD}=V_{LCD}-(0.03V_{LCD}\times9)$
0	0	0	1	$0.70V_{LCD}=V_{LCD}-(0.03V_{LCD}\times10)$
1	0	0	1	$0.67V_{LCD}=V_{LCD}-(0.03V_{LCD}\times11)$
0	1	0	1	$0.64V_{LCD}=V_{LCD}-(0.03V_{LCD}\times12)$

CTC: Display contrast adjustment circuit state setting

CTC	Display contrast adjustment circuit state
0	The display contrast adjustment circuit is disabled, and the $V_{LCD}0$ pin level is forced to the V_{LCD} level.
1	The display contrast adjustment circuit operates and the display contrast is adjusted.

Note that although the display contrast can be adjusted by operating the built-in display contrast adjustment circuit, it is also possible to apply fine adjustments to the contrast by connecting an external variable resistor to the $V_{LCD}4$ pin and modifying the $V_{LCD}4$ pin voltage. However, the following conditions must be met: $(V_{LCD}0 - V_{LCD}4) \geq 4.5$ V, and $1.5\ V \geq V_{LCD}4 \geq 0$ V.

4. SC: Segment on/off control data

This control data bit controls the on/off state of the segments.

SC	Display state
0	On
1	Off

However, note that when the segments are turned off by setting SC to 1, the segments are turned off by outputting segment off waveforms from the segment output pins.

5. SP: Normal mode/sleep mode control data

This control data bit controls the normal mode and sleep mode.

BU	Mode
0	Normal mode
1	Sleep mode The common and segment pins go to the $V_{LCD}4$ level and the oscillator on the OSC pin is stopped (although it operates during key scan operations) to reduce current drain. Note that the states of the general-purpose output ports P1 to P4 are set by PC1 to PC4 in the control data during sleep mode as well as normal mode.

6. DT1, DT2: Display technique setting data

These control data bits set the display technique.

DT1	DT2	Display technique	Output pins	
			COM9	COM10
0	0	1/8 duty 1/4 bias drive	Fixed at the $V_{LCD}4$ level	Fixed at the $V_{LCD}4$ level
1	0	1/9 duty 1/4 bias drive	COM9	Fixed at the $V_{LCD}4$ level
0	1	1/10 duty 1/4 bias drive	COM9	COM10

Note: COMn (n = 9 or 10): Common outputs

Display Data and Output Pin Correspondence

• 1/8 duty

Output Pin	COM1	COM2	COM3	COM4	COM5	COM6	COM7	COM8
S1	D1	D2	D3	D4	D5	D6	D7	D8
S2	D9	D10	D11	D12	D13	D14	D15	D16
S3	D17	D18	D19	D20	D21	D22	D23	D24
S4	D25	D26	D27	D28	D29	D30	D31	D32
S5	D33	D34	D35	D36	D37	D38	D39	D40
S6	D41	D42	D43	D44	D45	D46	D47	D48
S7	D49	D50	D51	D52	D53	D54	D55	D56
S8	D57	D58	D59	D60	D61	D62	D63	D64
S9	D65	D66	D67	D68	D69	D70	D71	D72
S10	D73	D74	D75	D76	D77	D78	D79	D80
S11	D81	D82	D83	D84	D85	D86	D87	D88
S12	D89	D90	D91	D92	D93	D94	D95	D96
S13	D97	D98	D99	D100	D101	D102	D103	D104
S14	D105	D106	D107	D108	D109	D110	D111	D112
S15	D113	D114	D115	D116	D117	D118	D119	D120
S16	D121	D122	D123	D124	D125	D126	D127	D128
S17	D129	D130	D131	D132	D133	D134	D135	D136
S18	D137	D138	D139	D140	D141	D142	D143	D144
S19	D145	D146	D147	D148	D149	D150	D151	D152
S20	D153	D154	D155	D156	D157	D158	D159	D160
S21	D161	D162	D163	D164	D165	D166	D167	D168
S22	D169	D170	D171	D172	D173	D174	D175	D176
S23	D177	D178	D179	D180	D181	D182	D183	D184
S24	D185	D186	D187	D188	D189	D190	D191	D192
S25	D193	D194	D195	D196	D197	D198	D199	D200
S26	D201	D202	D203	D204	D205	D206	D207	D208
S27	D209	D210	D211	D212	D213	D214	D215	D216
S28	D217	D218	D219	D220	D221	D222	D223	D224
S29	D225	D226	D227	D228	D229	D230	D231	D232
S30	D233	D234	D235	D236	D237	D238	D239	D240
S31	D241	D242	D243	D244	D245	D246	D247	D248
S32	D249	D250	D251	D252	D253	D254	D255	D256
S33	D257	D258	D259	D260	D261	D262	D263	D264
S34	D265	D266	D267	D268	D269	D270	D271	D272
S35	D273	D274	D275	D276	D277	D278	D279	D280
S36	D281	D282	D283	D284	D285	D286	D287	D288
S37	D289	D290	D291	D292	D293	D294	D295	D296
S38	D297	D298	D299	D300	D301	D302	D303	D304
S39	D305	D306	D307	D308	D309	D310	D311	D312
S40	D313	D314	D315	D316	D317	D318	D319	D320
S41	D321	D322	D323	D324	D325	D326	D327	D328
S42	D329	D330	D331	D332	D333	D334	D335	D336
S43	D337	D338	D339	D340	D341	D342	D343	D344
S44	D345	D346	D347	D348	D349	D350	D351	D352
S45	D353	D354	D355	D356	D357	D358	D359	D360

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Output Pin	COM1	COM2	COM3	COM4	COM5	COM6	COM7	COM8
S46	D361	D362	D363	D364	D365	D366	D367	D368
S47	D369	D370	D371	D372	D373	D374	D375	D376
S48	D377	D378	D379	D380	D381	D382	D383	D384
S49	D385	D386	D387	D388	D389	D390	D391	D392
S50	D393	D394	D395	D396	D397	D398	D399	D400
S51	D401	D402	D403	D404	D405	D406	D407	D408
S52	D409	D410	D411	D412	D413	D414	D415	D416
S53	D417	D418	D419	D420	D421	D422	D423	D424
S54	D425	D426	D427	D428	D429	D430	D431	D432
S55	D433	D434	D435	D436	D437	D438	D439	D440
S56	D441	D442	D443	D444	D445	D446	D447	D448
S57	D449	D450	D451	D452	D453	D454	D455	D456
S58	D457	D458	D459	D460	D461	D462	D463	D464
S59	D465	D466	D467	D468	D469	D470	D471	D472
S60	D473	D474	D475	D476	D477	D478	D479	D480

For example, the table below lists the segment output states for the S11 output pin.

Display data								Output pin state (S11)
D81	D82	D83	D84	D85	D86	D87	D88	
0	0	0	0	0	0	0	0	The LCD segments for COM1 to COM8 are off
1	0	0	0	0	0	0	0	The LCD segment for COM1 is on
0	1	0	0	0	0	0	0	The LCD segment for COM2 is on
0	0	1	0	0	0	0	0	The LCD segment for COM3 is on
0	0	0	1	0	0	0	0	The LCD segment for COM4 is on
0	0	0	0	1	0	0	0	The LCD segment for COM5 is on
0	0	0	0	0	1	0	0	The LCD segment for COM6 is on
0	0	0	0	0	0	1	0	The LCD segment for COM7 is on
0	0	0	0	0	0	0	1	The LCD segment for COM8 is on
1	1	1	1	1	1	1	1	The LCD segments for COM1 to COM8 are on

• 1/9 duty

Output Pin	COM1	COM2	COM3	COM4	COM5	COM6	COM7	COM8	COM9
S1	D1	D2	D3	D4	D5	D6	D7	D8	D9
S2	D10	D11	D12	D13	D14	D15	D16	D17	D18
S3	D19	D20	D21	D22	D23	D24	D25	D26	D27
S4	D28	D29	D30	D31	D32	D33	D34	D35	D36
S5	D37	D38	D39	D40	D41	D42	D43	D44	D45
S6	D46	D47	D48	D49	D50	D51	D52	D53	D54
S7	D55	D56	D57	D58	D59	D60	D61	D62	D63
S8	D64	D65	D66	D67	D68	D69	D70	D71	D72
S9	D73	D74	D75	D76	D77	D78	D79	D80	D81
S10	D82	D83	D84	D85	D86	D87	D88	D89	D90
S11	D91	D92	D93	D94	D95	D96	D97	D98	D99
S12	D100	D101	D102	D103	D104	D105	D106	D107	D108
S13	D109	D110	D111	D112	D113	D114	D115	D116	D117
S14	D118	D119	D120	D121	D122	D123	D124	D125	D126
S15	D127	D128	D129	D130	D131	D132	D133	D134	D135
S16	D136	D137	D138	D139	D140	D141	D142	D143	D144
S17	D145	D146	D147	D148	D149	D150	D151	D152	D153
S18	D154	D155	D156	D157	D158	D159	D160	D161	D162
S19	D163	D164	D165	D166	D167	D168	D169	D170	D171
S20	D172	D173	D174	D175	D176	D177	D178	D179	D180
S21	D181	D182	D183	D184	D185	D186	D187	D188	D189
S22	D190	D191	D192	D193	D194	D195	D196	D197	D198
S23	D199	D200	D201	D202	D203	D204	D205	D206	D207
S24	D208	D209	D210	D211	D212	D213	D214	D215	D216
S25	D217	D218	D219	D220	D221	D222	D223	D224	D225
S26	D226	D227	D228	D229	D230	D231	D232	D233	D234
S27	D235	D236	D237	D238	D239	D240	D241	D242	D243
S28	D244	D245	D246	D247	D248	D249	D250	D251	D252
S29	D253	D254	D255	D256	D257	D258	D259	D260	D261
S30	D262	D263	D264	D265	D266	D267	D268	D269	D270
S31	D271	D272	D273	D274	D275	D276	D277	D278	D279
S32	D280	D281	D282	D283	D284	D285	D286	D287	D288
S33	D289	D290	D291	D292	D293	D294	D295	D296	D297
S34	D298	D299	D300	D301	D302	D303	D304	D305	D306
S35	D307	D308	D309	D310	D311	D312	D313	D314	D315
S36	D316	D317	D318	D319	D320	D321	D322	D323	D324
S37	D325	D326	D327	D328	D329	D330	D331	D332	D333
S38	D334	D335	D336	D337	D338	D339	D340	D341	D342
S39	D343	D344	D345	D346	D347	D348	D349	D350	D351
S40	D352	D353	D354	D355	D356	D357	D358	D359	D360
S41	D361	D362	D363	D364	D365	D366	D367	D368	D369
S42	D370	D371	D372	D373	D374	D375	D376	D377	D378
S43	D379	D380	D381	D382	D383	D384	D385	D386	D387
S44	D388	D389	D390	D391	D392	D393	D394	D395	D396
S45	D397	D398	D399	D400	D401	D402	D403	D404	D405

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Output Pin	COM1	COM2	COM3	COM4	COM5	COM6	COM7	COM8	COM9
S46	D406	D407	D408	D409	D410	D411	D412	D413	D414
S47	D415	D416	D417	D418	D419	D420	D421	D422	D423
S48	D424	D425	D426	D427	D428	D429	D430	D431	D432
S49	D433	D434	D435	D436	D437	D438	D439	D440	D441
S50	D442	D443	D444	D445	D446	D447	D448	D449	D450
S51	D451	D452	D453	D454	D455	D456	D457	D458	D459
S52	D460	D461	D462	D463	D464	D465	D466	D467	D468
S53	D469	D470	D471	D472	D473	D474	D475	D476	D477
S54	D478	D479	D480	D481	D482	D483	D484	D485	D486
S55	D487	D488	D489	D490	D491	D492	D493	D494	D495
S56	D496	D497	D498	D499	D500	D501	D502	D503	D504
S57	D505	D506	D507	D508	D509	D510	D511	D512	D513
S58	D514	D515	D516	D517	D518	D519	D520	D521	D522
S59	D523	D524	D525	D526	D527	D528	D529	D530	D531
S60	D532	D533	D534	D535	D536	D537	D538	D539	D540

For example, the table below lists the segment output states for the S11 output pin.

Display data									Output pin state (S11)
D91	D92	D93	D94	D95	D96	D97	D98	D99	
0	0	0	0	0	0	0	0	0	The LCD segments for COM1 to COM9 are off
1	0	0	0	0	0	0	0	0	The LCD segment for COM1 is on
0	1	0	0	0	0	0	0	0	The LCD segment for COM2 is on
0	0	1	0	0	0	0	0	0	The LCD segment for COM3 is on
0	0	0	1	0	0	0	0	0	The LCD segment for COM4 is on
0	0	0	0	1	0	0	0	0	The LCD segment for COM5 is on
0	0	0	0	0	1	0	0	0	The LCD segment for COM6 is on
0	0	0	0	0	0	1	0	0	The LCD segment for COM7 is on
0	0	0	0	0	0	0	1	0	The LCD segment for COM8 is on
0	0	0	0	0	0	0	0	1	The LCD segment for COM9 is on
1	1	1	1	1	1	1	1	1	The LCD segments for COM1 to COM9 are on

• 1/10 duty

Output Pin	COM1	COM2	COM3	COM4	COM5	COM6	COM7	COM8	COM9	COM10
S1	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10
S2	D11	D12	D13	D14	D15	D16	D17	D18	D19	D20
S3	D21	D22	D23	D24	D25	D26	D27	D28	D29	D30
S4	D31	D32	D33	D34	D35	D36	D37	D38	D39	D40
S5	D41	D42	D43	D44	D45	D46	D47	D48	D49	D50
S6	D51	D52	D53	D54	D55	D56	D57	D58	D59	D60
S7	D61	D62	D63	D64	D65	D66	D67	D68	D69	D70
S8	D71	D72	D73	D74	D75	D76	D77	D78	D79	D80
S9	D81	D82	D83	D84	D85	D86	D87	D88	D89	D90
S10	D91	D92	D93	D94	D95	D96	D97	D98	D99	D100
S11	D101	D102	D103	D104	D105	D106	D107	D108	D109	D110
S12	D111	D112	D113	D114	D115	D116	D117	D118	D119	D120
S13	D121	D122	D123	D124	D125	D126	D127	D128	D129	D130
S14	D131	D132	D133	D134	D135	D136	D137	D138	D139	D140
S15	D141	D142	D143	D144	D145	D146	D147	D148	D149	D150
S16	D151	D152	D153	D154	D155	D156	D157	D158	D159	D160
S17	D161	D162	D163	D164	D165	D166	D167	D168	D169	D170
S18	D171	D172	D173	D174	D175	D176	D177	D178	D179	D180
S19	D181	D182	D183	D184	D185	D186	D187	D188	D189	D190
S20	D191	D192	D193	D194	D195	D196	D197	D198	D199	D200
S21	D201	D202	D203	D204	D205	D206	D207	D208	D209	D210
S22	D211	D212	D213	D214	D215	D216	D217	D218	D219	D220
S23	D221	D222	D223	D224	D225	D226	D227	D228	D229	D230
S24	D231	D232	D233	D234	D235	D236	D237	D238	D239	D240
S25	D241	D242	D243	D244	D245	D246	D247	D248	D249	D250
S26	D251	D252	D253	D254	D255	D256	D257	D258	D259	D260
S27	D261	D262	D263	D264	D265	D266	D267	D268	D269	D270
S28	D271	D272	D273	D274	D275	D276	D277	D278	D279	D280
S29	D281	D282	D283	D284	D285	D286	D287	D288	D289	D290
S30	D291	D292	D293	D294	D295	D296	D297	D298	D299	D300
S31	D301	D302	D303	D304	D305	D306	D307	D308	D309	D310
S32	D311	D312	D313	D314	D315	D316	D317	D318	D319	D320
S33	D321	D322	D323	D324	D325	D326	D327	D328	D329	D330
S34	D331	D332	D333	D334	D335	D336	D337	D338	D339	D340
S35	D341	D342	D343	D344	D345	D346	D347	D348	D349	D350
S36	D351	D352	D353	D354	D355	D356	D357	D358	D359	D360
S37	D361	D362	D363	D364	D365	D366	D367	D368	D369	D370
S38	D371	D372	D373	D374	D375	D376	D377	D378	D379	D380
S39	D381	D382	D383	D384	D385	D386	D387	D388	D389	D390
S40	D391	D392	D393	D394	D395	D396	D397	D398	D399	D400
S41	D401	D402	D403	D404	D405	D406	D407	D408	D409	D410
S42	D411	D412	D413	D414	D415	D416	D417	D418	D419	D420
S43	D421	D422	D423	D424	D425	D426	D427	D428	D429	D430
S44	D431	D432	D433	D434	D435	D436	D437	D438	D439	D440
S45	D441	D442	D443	D444	D445	D446	D447	D448	D449	D450

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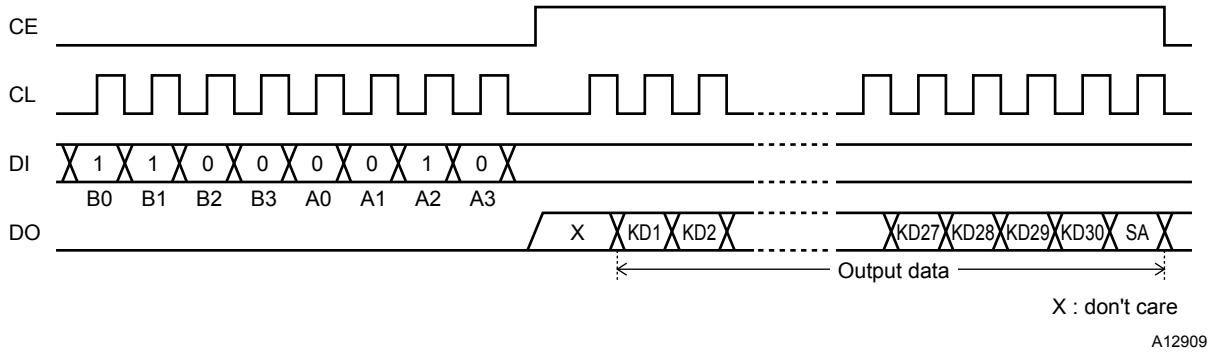
Output Pin	COM1	COM2	COM3	COM4	COM5	COM6	COM7	COM8	COM9	COM10
S46	D451	D452	D453	D454	D455	D456	D457	D458	D459	D460
S47	D461	D462	D463	D464	D465	D466	D467	D468	D469	D470
S48	D471	D472	D473	D474	D475	D476	D477	D478	D479	D480
S49	D481	D482	D483	D484	D485	D486	D487	D488	D489	D490
S50	D491	D492	D493	D494	D495	D496	D497	D498	D499	D500
S51	D501	D502	D503	D504	D505	D506	D507	D508	D509	D510
S52	D511	D512	D513	D514	D515	D516	D517	D518	D519	D520
S53	D521	D522	D523	D524	D525	D526	D527	D528	D529	D530
S54	D531	D532	D533	D534	D535	D536	D537	D538	D539	D540
S55	D541	D542	D543	D544	D545	D546	D547	D548	D549	D550
S56	D551	D552	D553	D554	D555	D556	D557	D558	D559	D560
S57	D561	D562	D563	D564	D565	D566	D567	D568	D569	D570
S58	D571	D572	D573	D574	D575	D576	D577	D578	D579	D580
S59	D581	D582	D583	D584	D585	D586	D587	D588	D589	D590
S60	D591	D592	D593	D594	D595	D596	D597	D598	D599	D600

For example, the table below lists the segment output states for the S11 output pin.

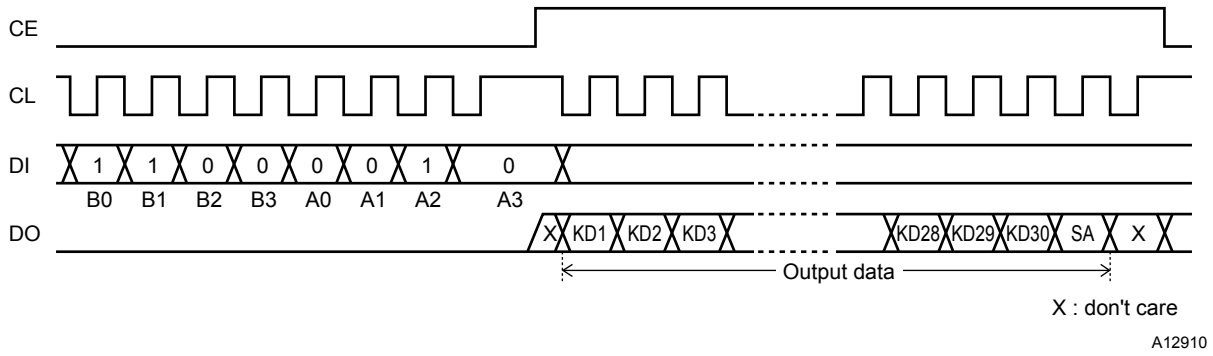
Display data										Output pin state (S11)
D101	D102	D103	D104	D105	D106	D107	D108	D109	D110	
0	0	0	0	0	0	0	0	0	0	The LCD segments for COM1 to COM10 are off
1	0	0	0	0	0	0	0	0	0	The LCD segment for COM1 is on
0	1	0	0	0	0	0	0	0	0	The LCD segment for COM2 is on
0	0	1	0	0	0	0	0	0	0	The LCD segment for COM3 is on
0	0	0	1	0	0	0	0	0	0	The LCD segment for COM4 is on
0	0	0	0	1	0	0	0	0	0	The LCD segment for COM5 is on
0	0	0	0	0	1	0	0	0	0	The LCD segment for COM6 is on
0	0	0	0	0	0	1	0	0	0	The LCD segment for COM7 is on
0	0	0	0	0	0	0	1	0	0	The LCD segment for COM8 is on
0	0	0	0	0	0	0	0	1	0	The LCD segment for COM9 is on
0	0	0	0	0	0	0	0	0	1	The LCD segment for COM10 is on
1	1	1	1	1	1	1	1	1	1	The LCD segments for COM1 to COM10 are on

Serial Data Output

1. When CL is stopped at the low level



2. When CL is stopped at the high level



Note: B0 to B3, A0 to A3…….. CCB address ‘43H’
KD1 to KD30 ..... Key data
SA ..... Sleep acknowledge data

Note: <u>If a key data read operation is executed when DO is high, the read key data (KD1 to KD30) and sleep acknowledge data(SA) will be invalid.</u>

Output Data

1. KD1 to KD30: Key data

When a key matrix of up to 30 keys is formed from the KS1 to KS6 output pins and the KI1 to KI5 input pins and one of those keys is pressed, the key output data corresponding to that key will be set to 1. The table shows the relationship between those pins and the key data bits.

	KI1	KI2	KI3	KI4	KI5
KS1	KD1	KD2	KD3	KD4	KD5
KS2	KD6	KD7	KD8	KD9	KD10
KS3	KD11	KD12	KD13	KD14	KD15
KS4	KD16	KD17	KD18	KD19	KD20
KS5	KD21	KD22	KD23	KD24	KD25
KS6	KD26	KD27	KD28	KD29	KD30

When the states of the KS1 to KS6 output pins during key scan standby are set to low for KS1 and KS2 and to high for KS3 to KS6 by the KC1 to KC6 bits in the control data and a key matrix of up to 20 keys is formed from the KS3 to KS6 output pins and the KI1 to KI5 input pins, the KD1 to KD10 key data bits will be set to 0.

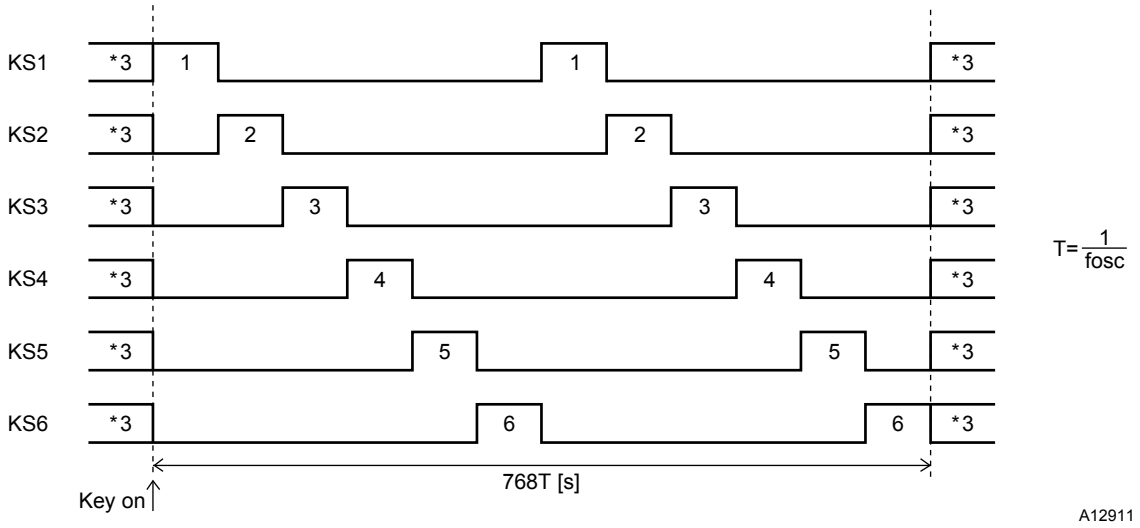
2. SA: Sleep acknowledge data

This output data bit is set to the state when the key was pressed. Also, while DO will be low in this case, if serial data is input and the mode is set (to normal or sleep mode) during this period, that mode will be set. SA will be 1 in sleep mode and 0 in normal mode.

Key Scan Operation Functions

1. Key scan timing

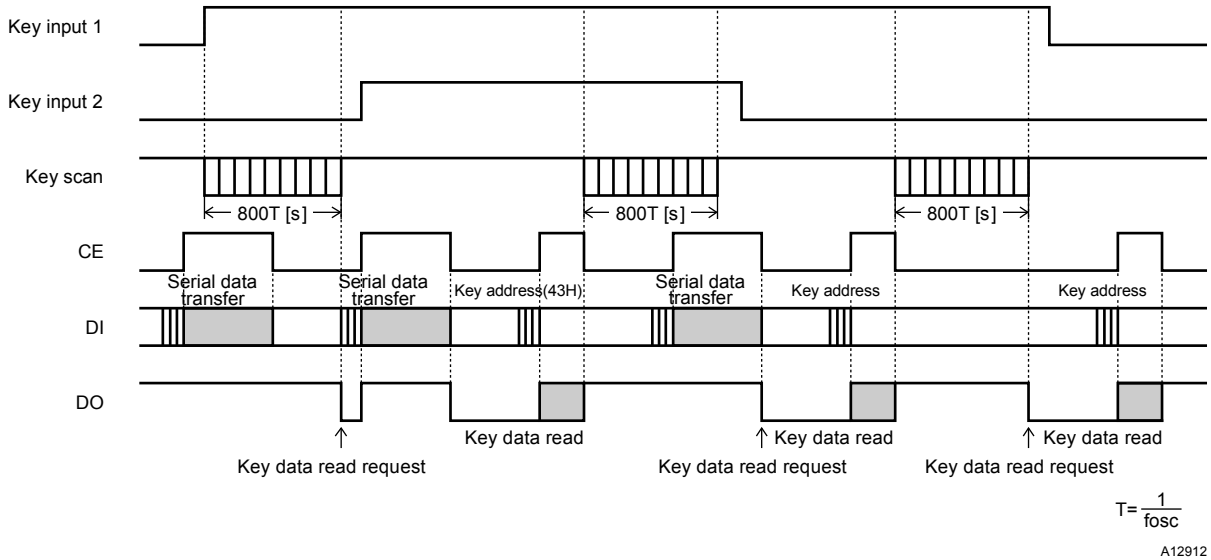
The key scan period is 384T(s). To reliably determine the on/off state of the keys, the LC75808W scans the keys twice and determines that a key has been pressed when the key data agrees. It outputs a key data read request (a low level on DO) 800T(s) after starting a key scan. If the key data dose not agree and a key was pressed at that point, it scans the keys again. Thus the LC75808W cannot detect a key press shorter than 800T(s).



Note: *3. Note that the high/low states of these pins are determined by the KC1 to KC6 bits in the control data, and that key scan output signals are not output from pins that are set to low.

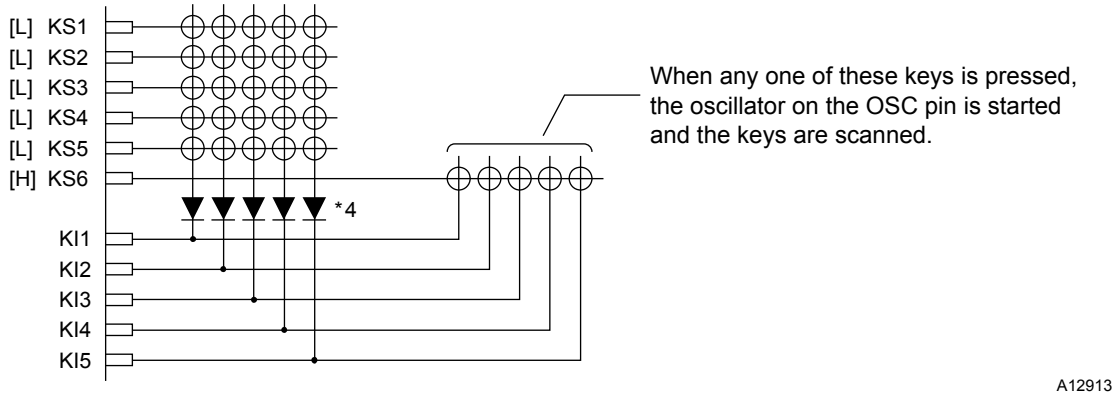
2. In normal mode

- The pins KS1 to KS6 are set to high or low by the KC1 to KC6 bits in the control data.
- If a key on one of the lines corresponding to a KS1 to KS6 pin which is set high is pressed, a key scan is started and the keys are scanned until all keys are released. Multiple key presses are recognized by determining whether multiple key data bits are set.
- If a key is pressed for longer than 800T(s) (Where $T=\frac{1}{f_{OSC}}$) the LC75808W outputs a key data read request (a low level on DO) to the controller. The controller acknowledges this request and reads the key data. However, if CE is high during a serial data transfer, DO will be set high.
- After the controller reads the key data, the key data read request is cleared (DO is set high) and the LC75808W performs another key scan. Also note that DO, being an open-drain output, requires a pull-up resistor (between 1 kΩ and 10 kΩ).

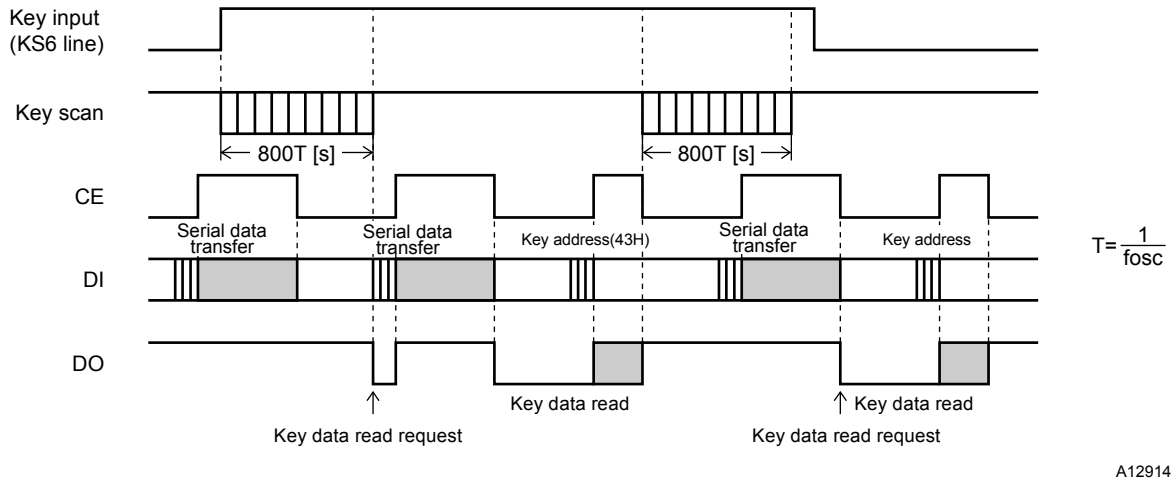


3. In sleep mode
   - The pins KS1 to KS6 are set to high or low by the KC1 to KC6 bits in the control data.
   - If a key on one of the lines corresponding to a KS1 to KS6 pin which is set high is pressed, the oscillator on the OSC pin is started and a key scan is performed. Keys are scanned until all keys are released. Multiple key presses are recognized by determining whether multiple key data bits are set.
   - If a key is pressed for longer than 800T(s)(where $T=\frac{1}{f_{OSC}}$) the LC75808W outputs a key data read request (a low level on DO) to the controller. The controller acknowledges this request and reads the key data. However, if CE is high during a serial data transfer, DO will be set high.
   - After the controller reads the key data, the key data read request is cleared (DO is set high) and the LC75808W performs another key scan. However, this dose not clear sleep mode. Also note that DO, being an open-drain output, requires a pull-up resistor (between 1 kΩ and 10 kΩ).
   - Sleep mode key scan example

Example: When the control data bits KC1 to KC5 are 0, KC6 is 1, and SP is 1. (sleep with only KS6 high)



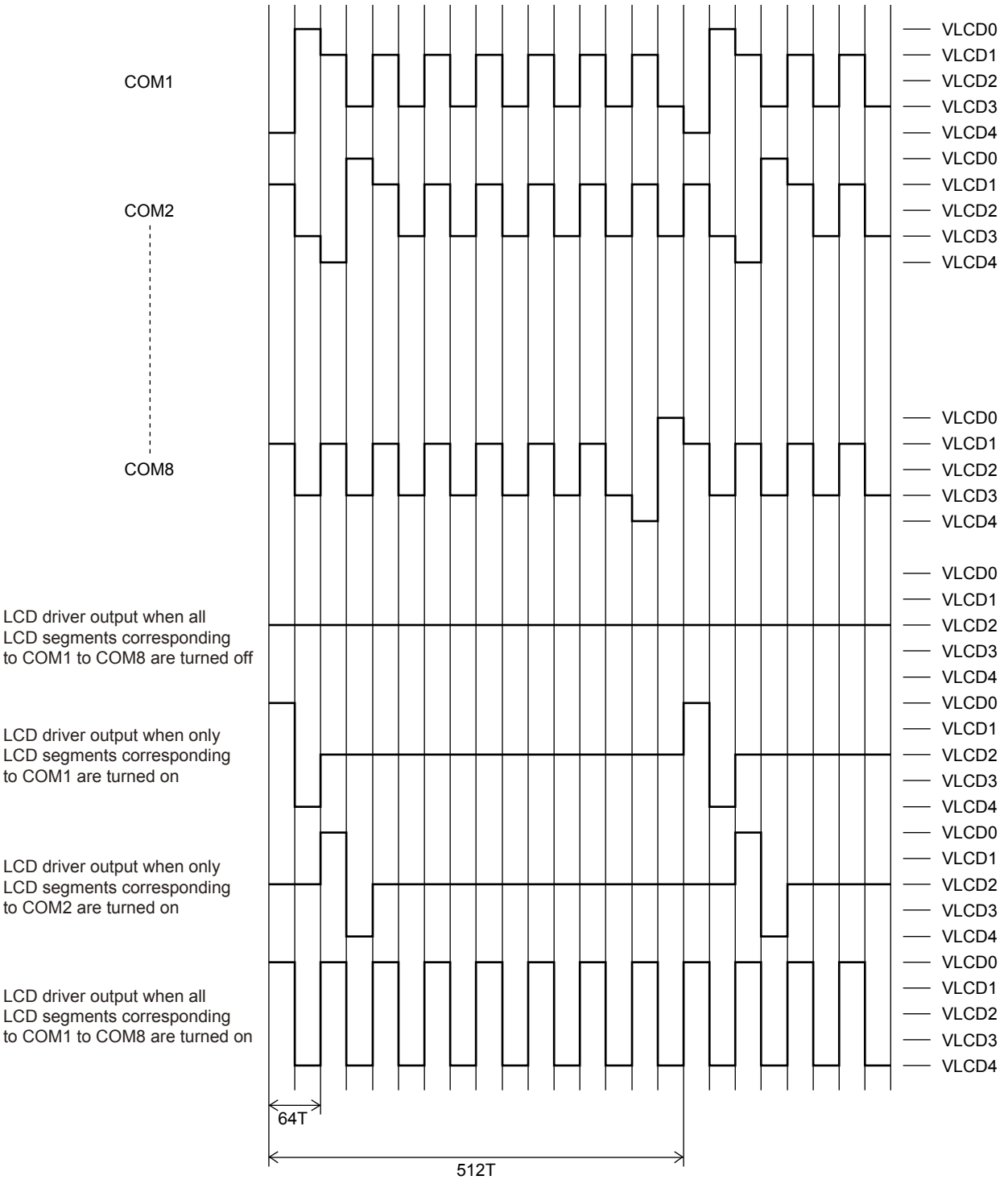
Note: *4. These diodes are required to reliable recognize multiple key presses on the KS6 line when sleep mode state with only KS6 high, as in the above example. That is, these diodes prevent incorrect operations due to sneak currents in the KS6 key scan output signal when keys on the KS1 to KS5 lines are pressed at the same time.



Multiple Key Presses

Although the LC75808W is capable of key scanning without inserting diodes for dual key presses, triple key presses on the KI1 to KI5 input pin lines, or multiple key presses on the KS1 to KS6 output pin lines, multiple presses other than these cases may result in keys that were not pressed recognized as having been pressed. Therefore, a diode must be inserted in series with each key. Applications that do not recognize multiple key presses of three or more keys should check the key data for three or more 1 bits and ignore such data.

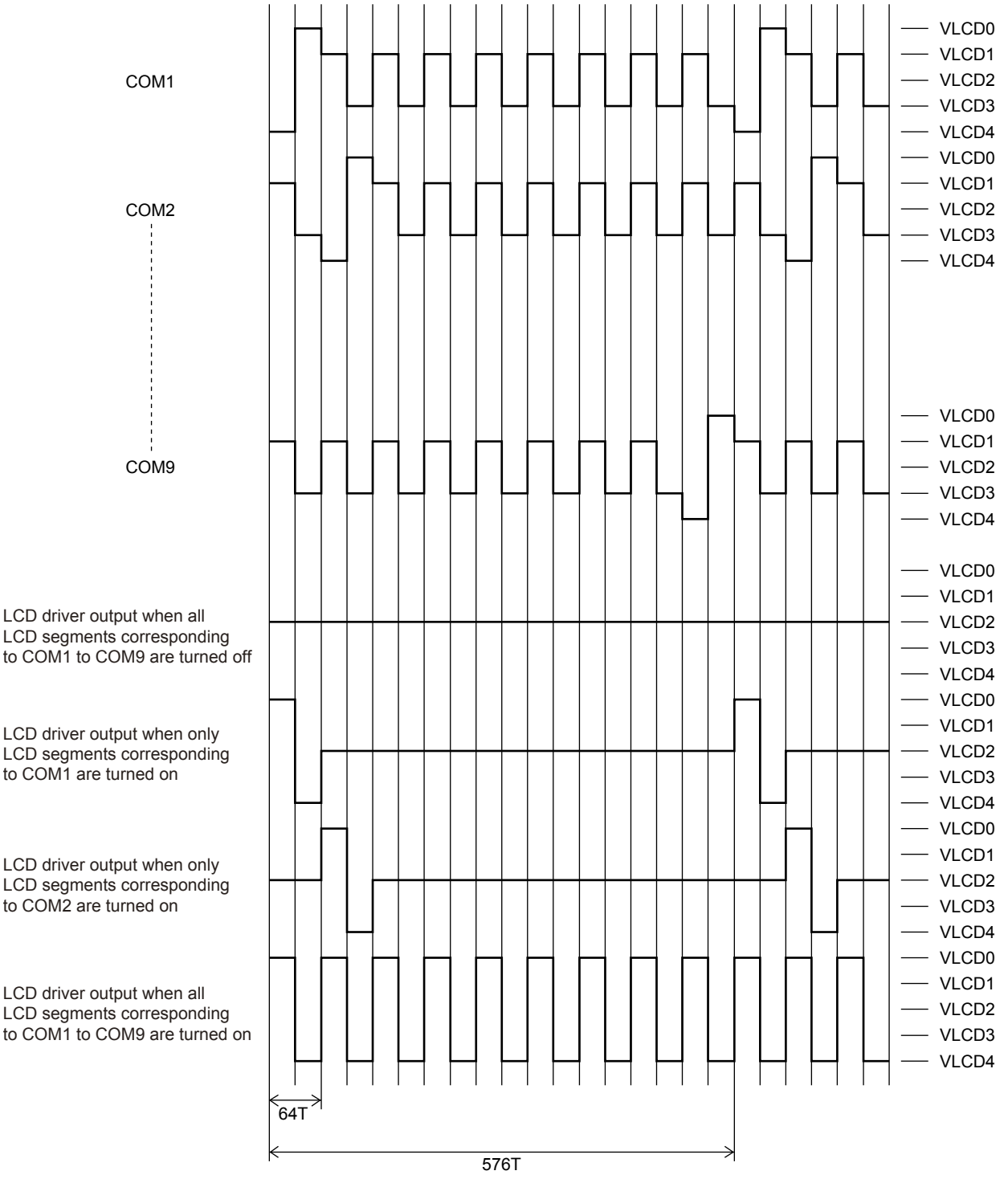
1/8 Duty, 1/4 Bias Drive Technique



$$T=\frac{1}{fosc}$$

A12915

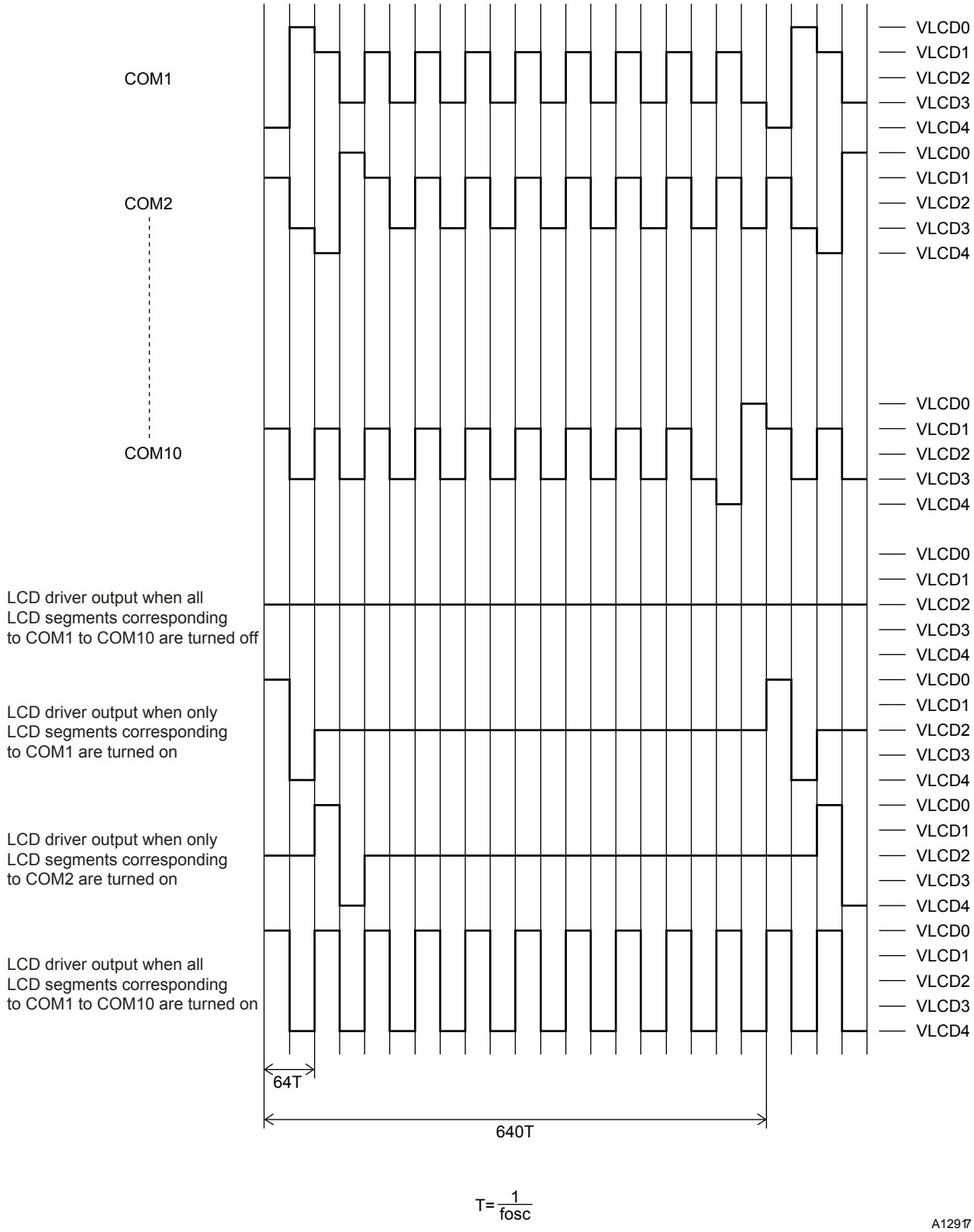
1/9 Duty, 1/4 Bias Drive Technique



$$T=\frac{1}{fosc}$$

A12916

1/10 Duty, 1/4 Bias Drive Technique



$$T = \frac{1}{fosc}$$

A12917

Voltage Detection Type Reset Circuit (V_{DET})

This circuit generates an output signal and resets the system when logic block power is first applied and when the voltage drops, i.e., when the logic block power supply voltage is less than or equal to the power down detection voltage V_{DET}, which is 3.0 V, typical. To assure that this function operates reliably, a capacitor must be added to the logic block power supply line so that the logic block power supply voltage V_{DD} rise time when the logic block power is first applied and the logic block power supply voltage V_{DD} fall time when the voltage drops are both at least 1 ms. (See Figure 3, 4, and 5.)

Power Supply Sequence

The following sequences must be observed when power is turned on and off. (See Figure 3, 4, and 5.)

- Power on: Logic block power supply(V_{DD}) on → LCD driver block power supply(V_{LCD}) on
- Power off: LCD driver block power supply(V_{LCD}) off → Logic block power supply(V_{DD}) off

However, if the logic and LCD driver blocks use a shared power supply, then the power supplies can be turned on and off at the same time.

System Reset

1. Reset Function

The LC75808W performs a system reset with the V_{DET}. When a system reset is applied, the display is turned off, key scanning is disabled, the key data is reset, and the general-purpose output ports are set to and held at the low level (V_{SS}). These states that are created as a result of the system reset can be cleared by executing the instruction described below. (See figure 3, 4, and 5.)

- Clearing the display off state

Transferring all the serial data (the display data and the control data) creates a state in which the display is turned on.

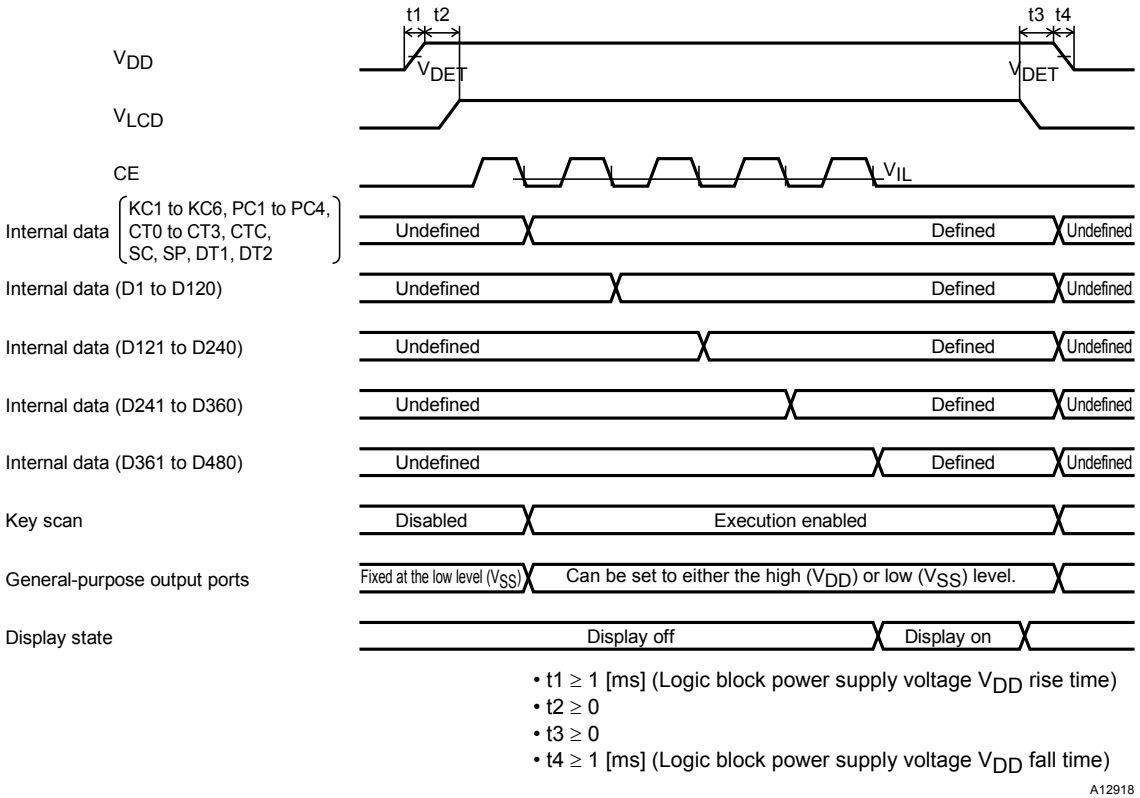
- Clearing the key scan disabled and key data reset states

Transferring the control data not only creates a state in which key scanning can be performed, but also clears the key data reset.

- Clearing the general-purpose output ports locked at the low level (V_{SS}) state

Transferring the control data clears the general-purpose output ports locked at the low level (V_{SS}) state and sets the states of the general-purpose output ports.

- 1/8 duty

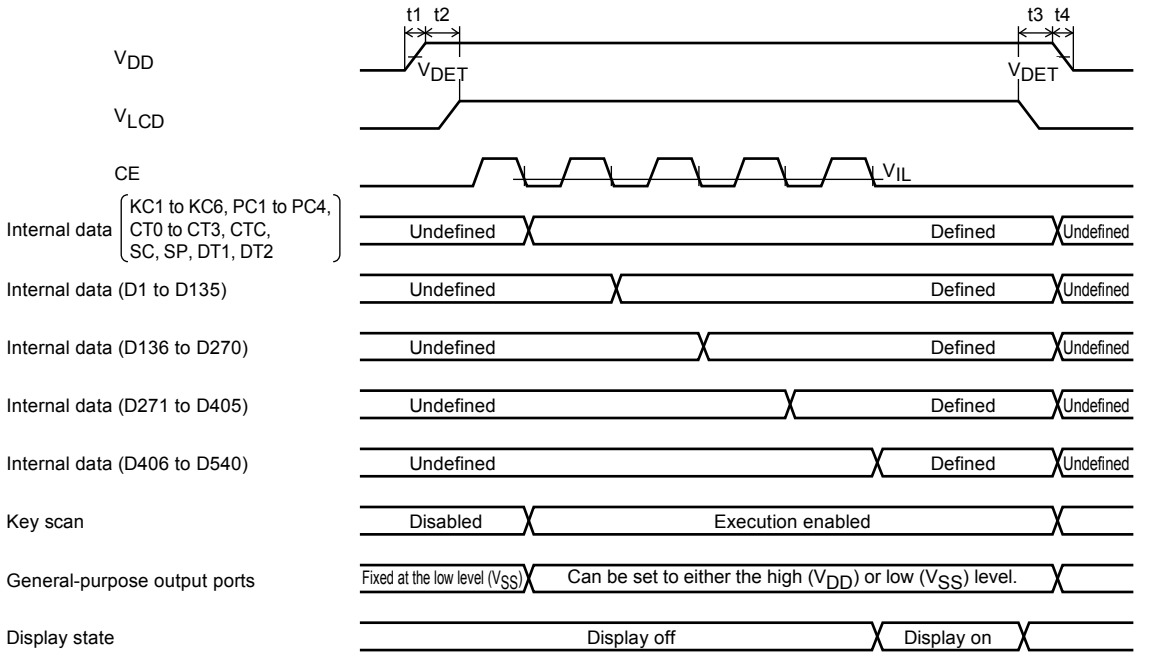


- t1 ≥ 1 [ms] (Logic block power supply voltage V_{DD} rise time)
- t2 ≥ 0
- t3 ≥ 0
- t4 ≥ 1 [ms] (Logic block power supply voltage V_{DD} fall time)

A12918

Figure 3

• 1/9 duty

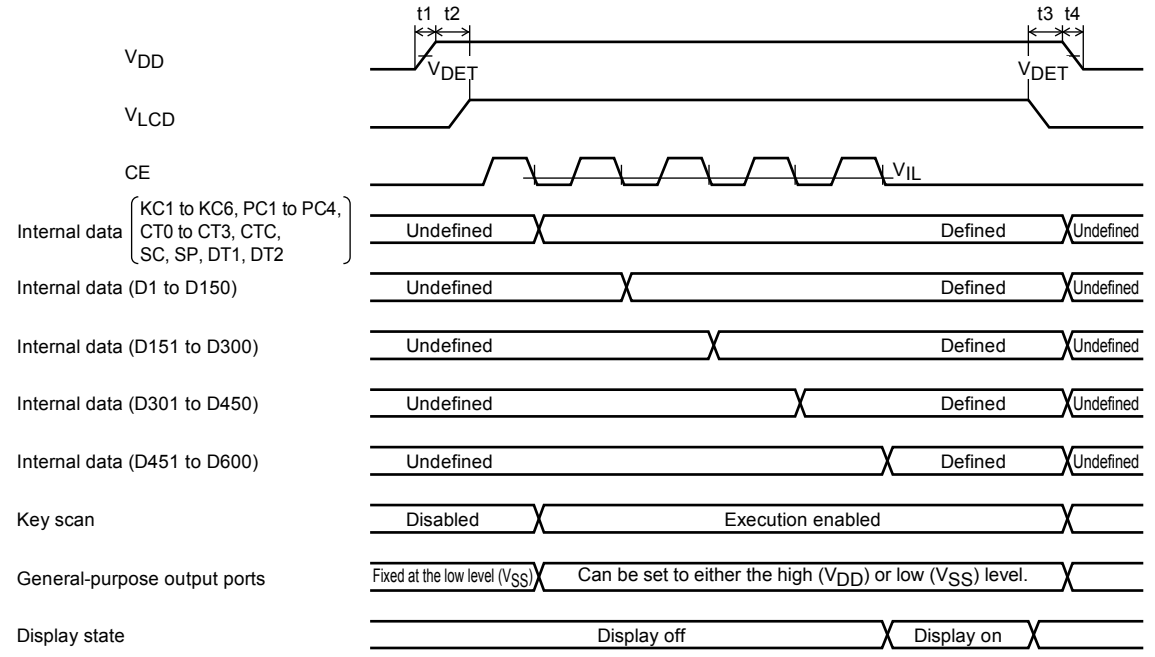


- t1 ≥ 1 [ms] (Logic block power supply voltage V_{DD} rise time)
- t2 ≥ 0
- t3 ≥ 0
- t4 ≥ 1 [ms] (Logic block power supply voltage V_{DD} fall time)

A12919

Figure 4

• 1/10 duty



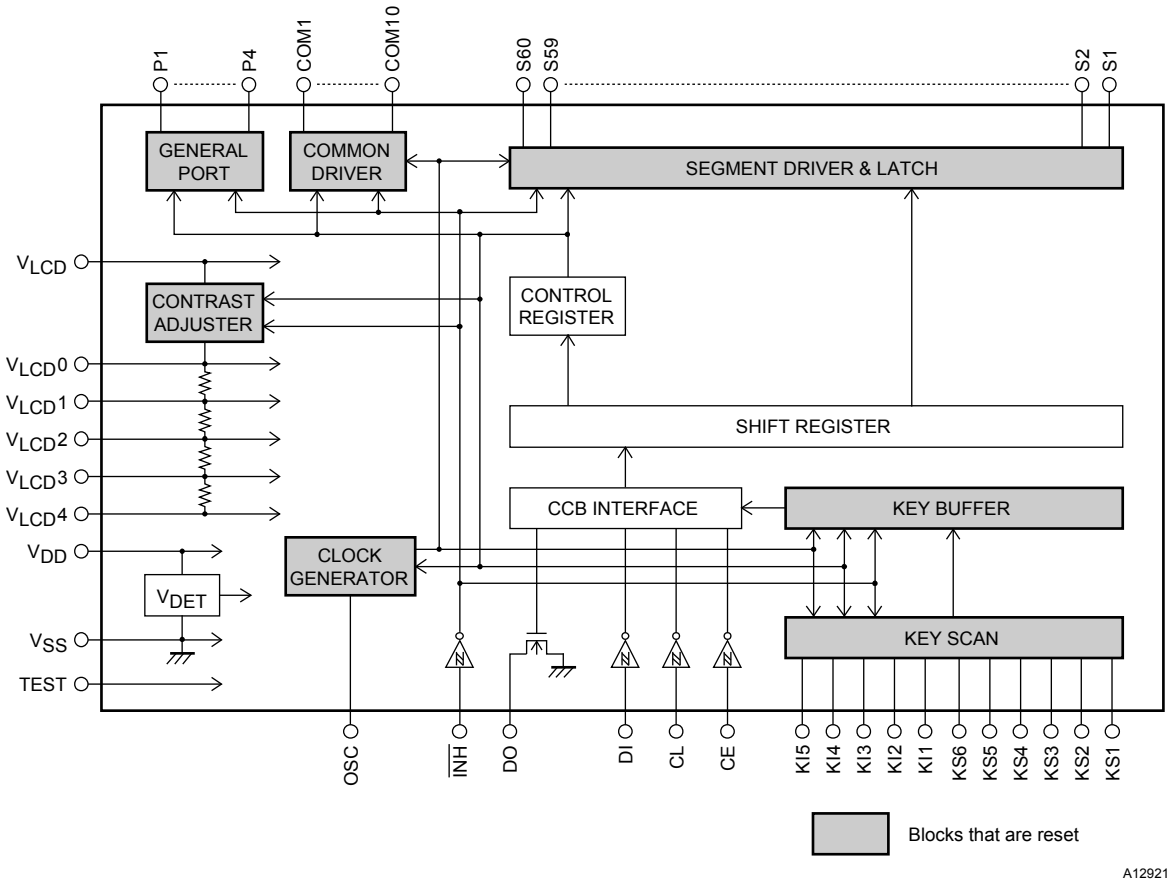
- t1 ≥ 1 [ms] (Logic block power supply voltage V_{DD} rise time)
- t2 ≥ 0
- t3 ≥ 0
- t4 ≥ 1 [ms] (Logic block power supply voltage V_{DD} fall time)

A12920

Figure 5

2. LC75808W internal block states during the system reset

- CLOCK GENERATOR
  Reset is applied and the base clock is stopped. However, the OSC pin state (normal or sleep mode) is determined after the SP control data bit is transferred.
- COMMON DRIVER, SEGMENT DRIVER & LATCH
  Reset is applied and the display is turned off. However, display data can be input to the latch circuit in this state.
- CONTRAST ADJUSTER
  Reset is applied and operation of the display contrast adjustment circuit is disabled. After that, once CT0 to CT3 and CTC in the control data have been transferred to the IC it will then be possible to set the display contrast.
- KEY SCAN, KEY BUFFER
  Reset is applied, these circuits are forcibly initialized internally, and key scan operation is disabled. Also, the key data is all set to 0. After that, once KC1 to KC6 in the control data have been transferred to the IC it will then be possible to perform key scan operations.
- GENERAL PORT
  Reset is applied and the states of the general-purpose output ports are held fixed at the low level (V_{SS}).
- CCB INTERFACE, SHIFT REGISTER, CONTROL REGISTER
  Since serial data transfer is possible, these circuits are not reset.



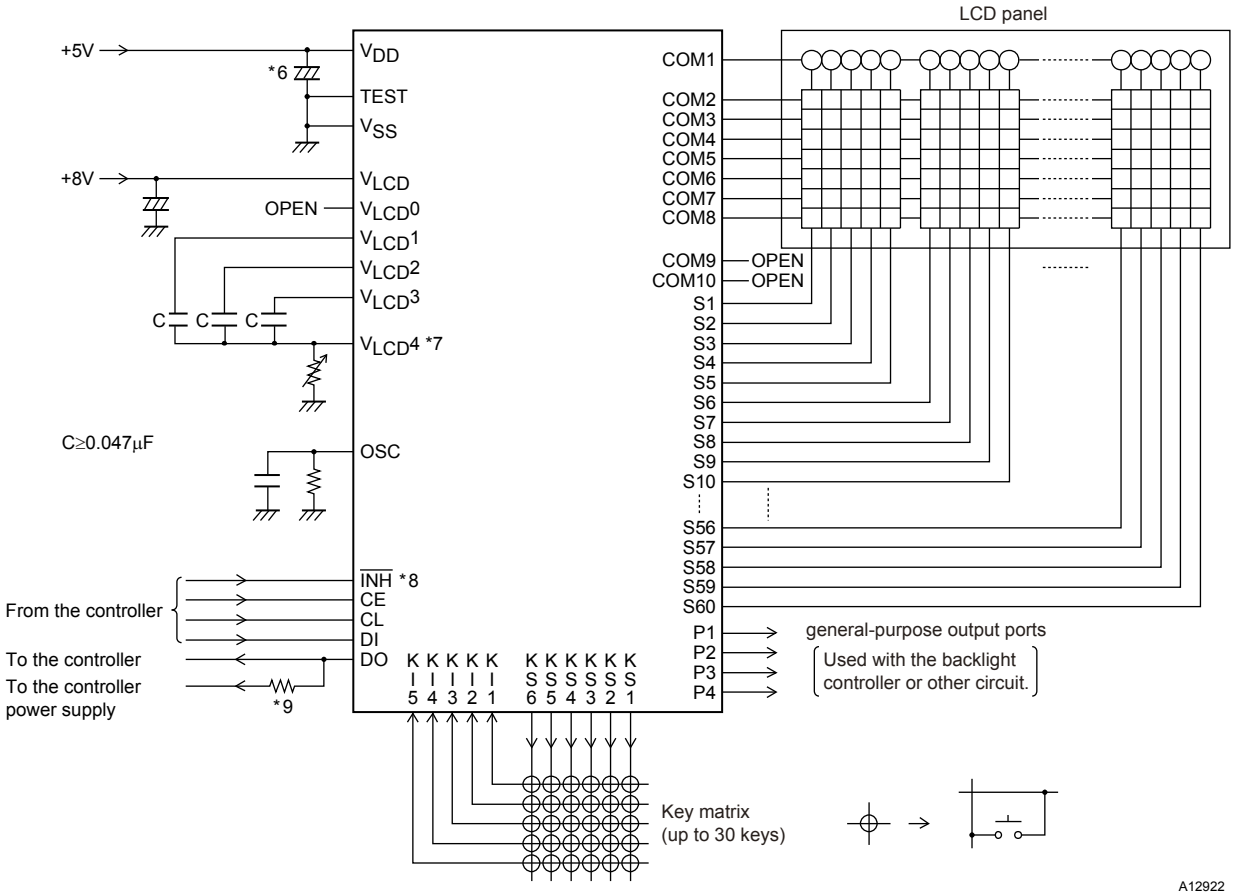
3. Output pin states during the system reset

Output pin	State during reset
S1 to S60	L($V_{LCD}4$)
COM1 to COM10	L($V_{LCD}4$)
KS1 to KS6	L(V_{SS})
P1 to P4	L(V_{SS})
DO	H *5

Note: *5. Since this output pin is an open-drain output, a pull-up resistor of between 1kΩ and 10 kΩ is required. This pin is held at the high level even if a key data read operation is performed before the KC1 to KC6 control data has been transferred to the IC.

Sample Application Circuit 1

1/8 duty, 1/4 bias drive technique (for use with normal panels)



Note: *6. Add a capacitor to the logic block power supply line so that the logic block power supply voltage V_{DD} rise time when power is applied and the logic block power supply voltage V_{DD} fall time when power drops are both at least 1ms, as the LC75808W is reset by the V_{DET}.

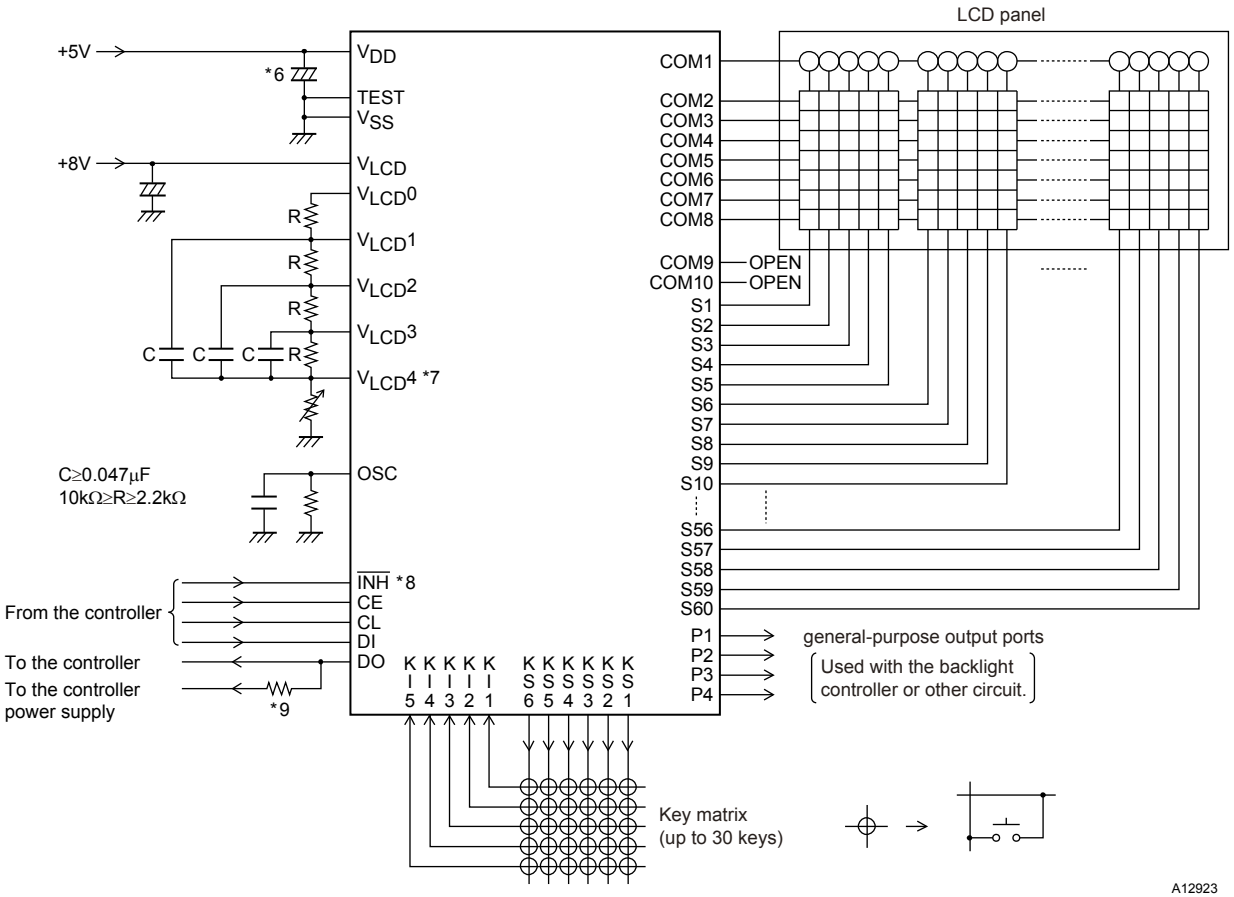
*7. If a variable resistor is not used for display contrast fine adjustment, the $V_{LCD}4$ pin must be connected to ground.

*8. If the function of the $\overline{INH}$ pin is not used, the $\overline{INH}$ pin must be connected to the logic block power supply V_{DD}.

*9. The DO pin, being an open-drain output, requires a pull-up resistor. Select a resistance (between 1 kΩ to 10 kΩ) appropriate for the capacitance of the external wiring so that signal waveforms are not degraded.

Sample Application Circuit 2

1/8 duty, 1/4 bias drive technique (for use with large panels)



Note: *6. Add a capacitor to the logic block power supply line so that the logic block power supply voltage V_{DD} rise time when power is applied and the logic block power supply voltage V_{DD} fall time when power drops are both at least 1ms, as the LC75808W is reset by the V_{DET}.

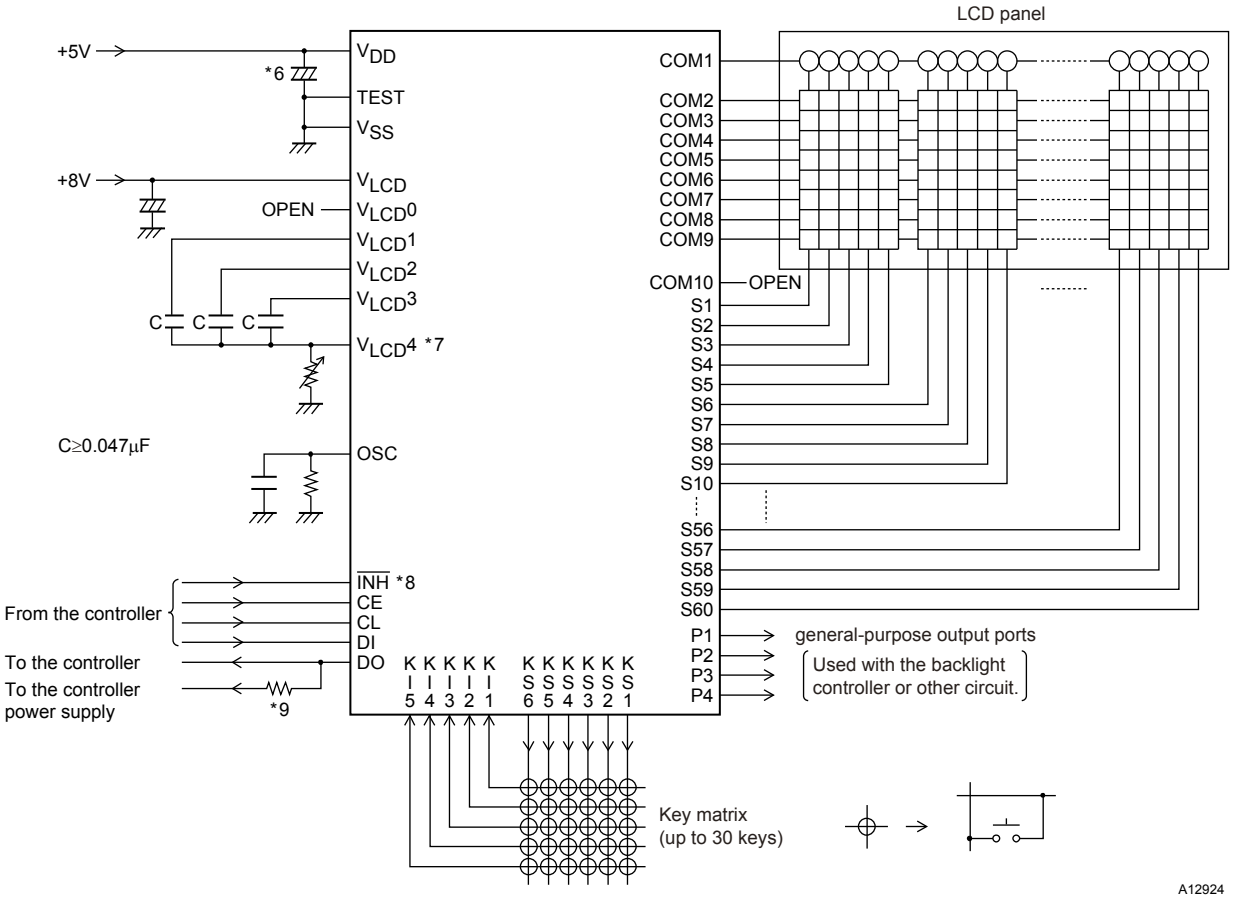
*7. If a variable resistor is not used for display contrast fine adjustment, the $V_{LCD}4$ pin must be connected to ground.

*8. If the function of the $\overline{INH}$ pin is not used, the $\overline{INH}$ pin must be connected to the logic block power supply V_{DD}.

*9. The DO pin, being an open-drain output, requires a pull-up resistor. Select a resistance (between 1 kΩ to 10 kΩ) appropriate for the capacitance of the external wiring so that signal waveforms are not degraded.

Sample Application Circuit 3

1/9 duty, 1/4 bias drive technique (for use with normal panels)



Note: *6. Add a capacitor to the logic block power supply line so that the logic block power supply voltage V_{DD} rise time when power is applied and the logic block power supply voltage V_{DD} fall time when power drops are both at least 1ms, as the LC75808W is reset by the V_{DET}.

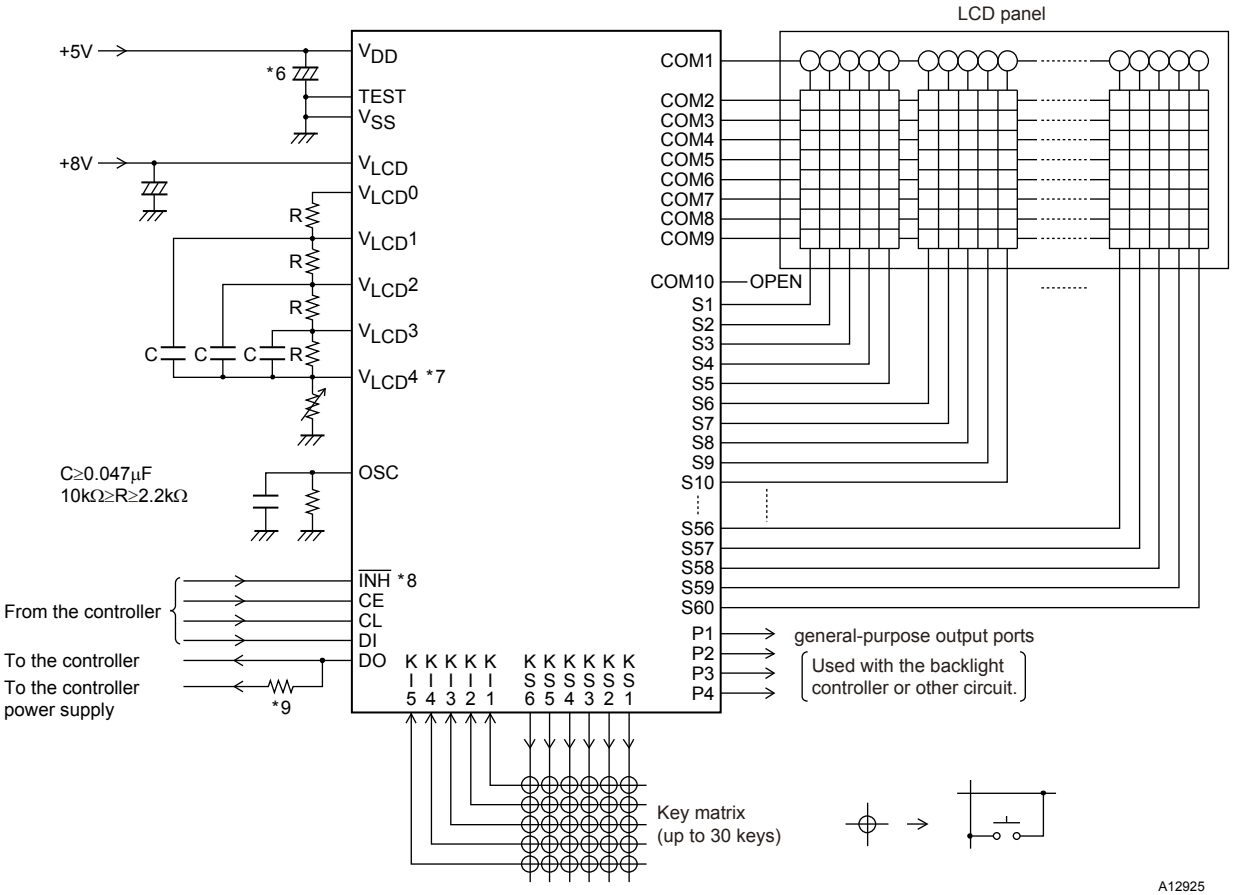
*7. If a variable resistor is not used for display contrast fine adjustment, the $V_{LCD}4$ pin must be connected to ground.

*8. If the function of the $\overline{INH}$ pin is not used, the $\overline{INH}$ pin must be connected to the logic block power supply V_{DD}.

*9. The DO pin, being an open-drain output, requires a pull-up resistor. Select a resistance (between 1 kΩ to 10 kΩ) appropriate for the capacitance of the external wiring so that signal waveforms are not degraded.

Sample Application Circuit 4

1/9 duty, 1/4 bias drive technique (for use with large panels)



Note: *6. Add a capacitor to the logic block power supply line so that the logic block power supply voltage V_{DD} rise time when power is applied and the logic block power supply voltage V_{DD} fall time when power drops are both at least 1 ms, as the LC75808W is reset by the V_{DET}.

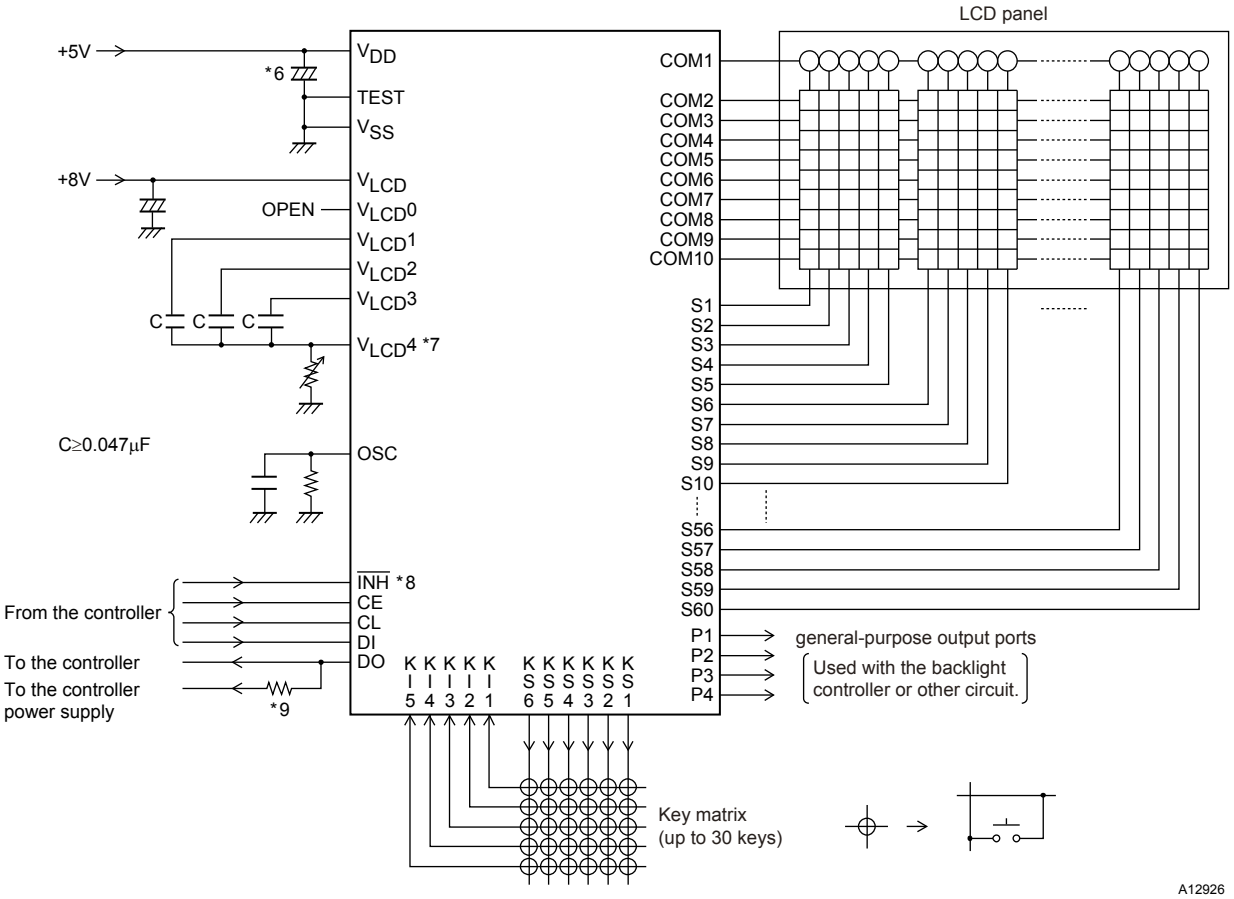
*7. If a variable resistor is not used for display contrast fine adjustment, the $V_{LCD}4$ pin must be connected to ground.

*8. If the function of the $\overline{INH}$ pin is not used, the $\overline{INH}$ pin must be connected to the logic block power supply V_{DD}.

*9. The DO pin, being an open-drain output, requires a pull-up resistor. Select a resistance (between 1 kΩ to 10 kΩ) appropriate for the capacitance of the external wiring so that signal waveforms are not degraded.

Sample Application Circuit 5

1/10 duty, 1/4 bias drive technique (for use with normal panels)



Note: *6. Add a capacitor to the logic block power supply line so that the logic block power supply voltage V_{DD} rise time when power is applied and the logic block power supply voltage V_{DD} fall time when power drops are both at least 1 ms, as the LC75808W is reset by the V_{DET}.

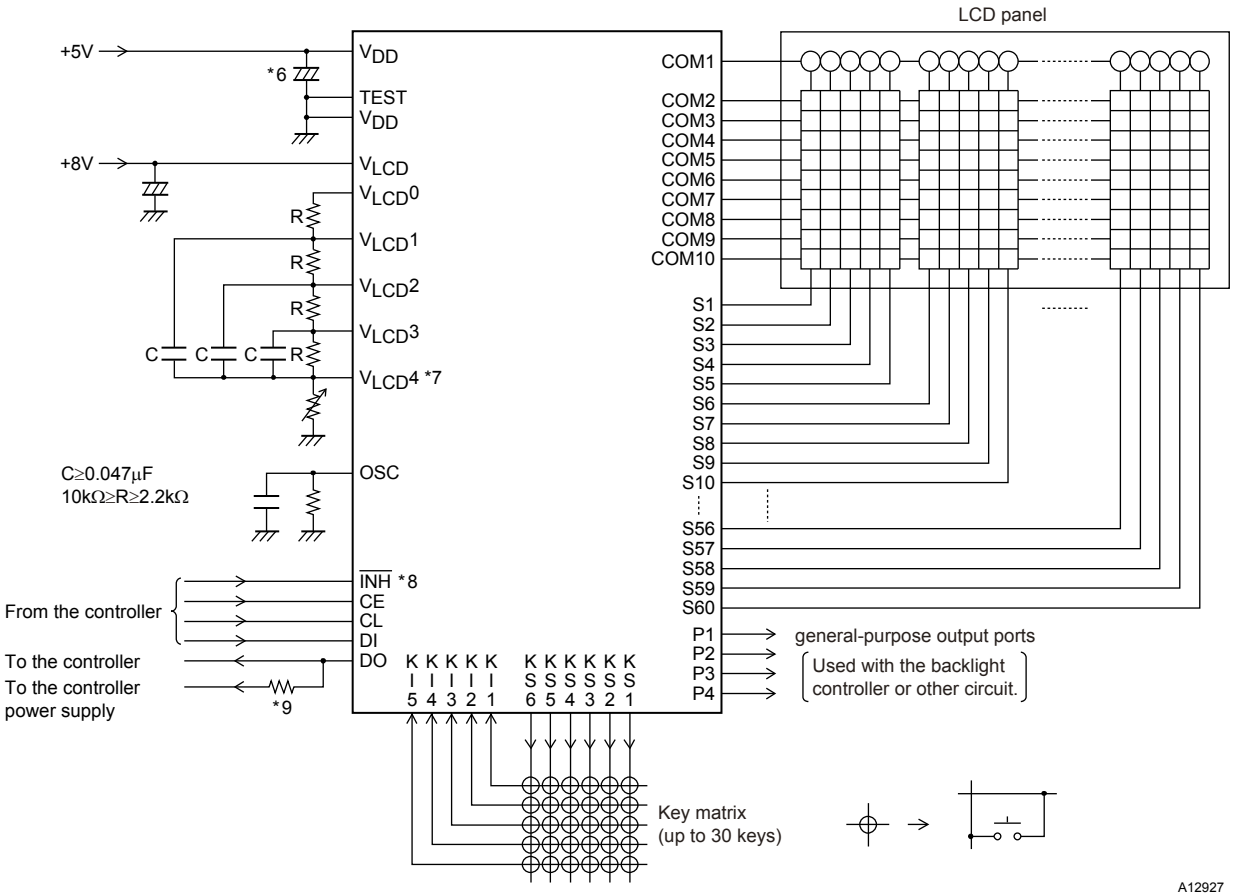
*7. If a variable resistor is not used for display contrast fine adjustment, the $V_{LCD}4$ pin must be connected to ground.

*8. If the function of the $\overline{INH}$ pin is not used, the $\overline{INH}$ pin must be connected to the logic block power supply V_{DD}.

*9. The DO pin, being an open-drain output, requires a pull-up resistor. Select a resistance (between 1 kΩ to 10 kΩ) appropriate for the capacitance of the external wiring so that signal waveforms are not degraded.

Sample Application Circuit 6

1/10 duty, 1/4 bias drive technique (for use with large panels)



Note: *6. Add a capacitor to the logic block power supply line so that the logic block power supply voltage V_{DD} rise time when power is applied and the logic block power supply voltage V_{DD} fall time when power drops are both at least 1ms, as the LC75808W is reset by the V_{DET}.

*7. If a variable resistor is not used for display contrast fine adjustment, the $V_{LCD}4$ pin must be connected to ground.

*8. If the function of the $\overline{INH}$ pin is not used, the $\overline{INH}$ pin must be connected to the logic block power supply V_{DD}.

*9. The DO pin, being an open-drain output, requires a pull-up resistor. Select a resistance (between 1 kΩ to 10 kΩ) appropriate for the capacitance of the external wiring so that signal waveforms are not degraded.

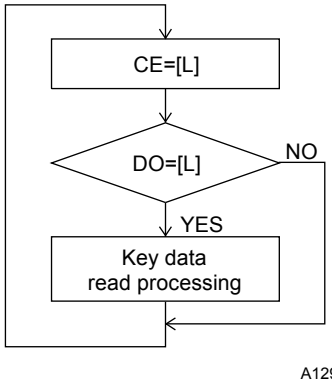
Notes on Transferring Display Data from the Controller

The display data is transferred to the LC75808W in four operations. All of the display data should be transferred within 30 ms to maintain the quality of the displayed image.

Notes on the Controller Key Data Read Techniques

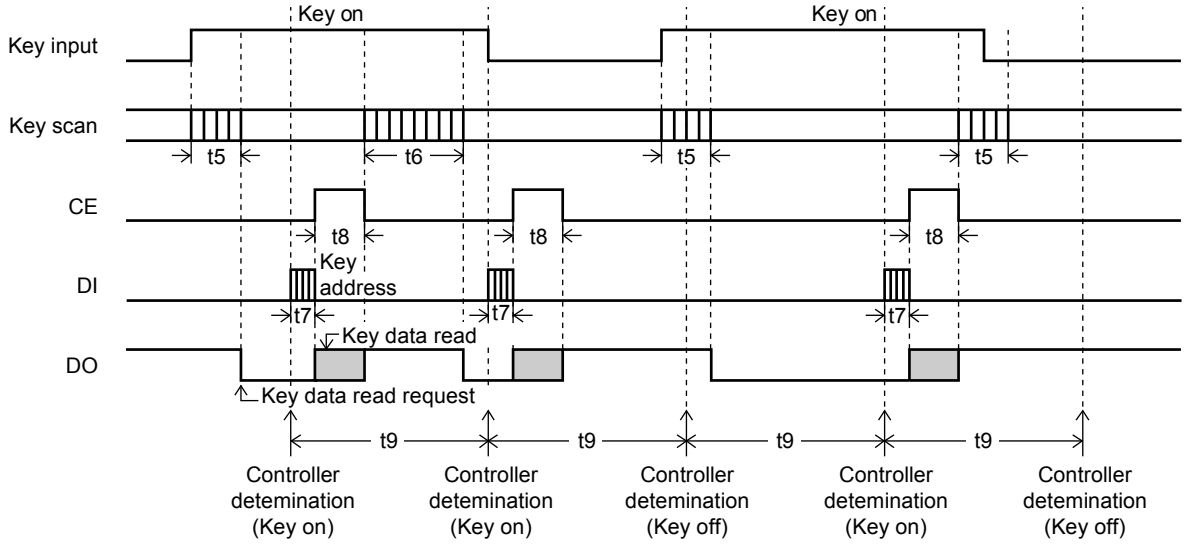
1. Timer based key data acquisition

• Flowchart



A12928

• Timing chart



A12929

t5: Key scan execution time when the key data agreed for two key scans. (800T(s))
t6: Key scan execution time when the key data did not agree for two key scans and the key scan was executed again. (1600T(s))
t7: Key address (43H) transfer time
t8: Key data read time

$$T = \frac{1}{f_{OSC}}$$

• Explanation

In this technique, the controller uses a timer to determine key on/off states and read the key data. The controller must check the DO state when CE is low every t9 period without fail. If DO is low, the controller recognizes that a key has been pressed and executes the key data read operation.

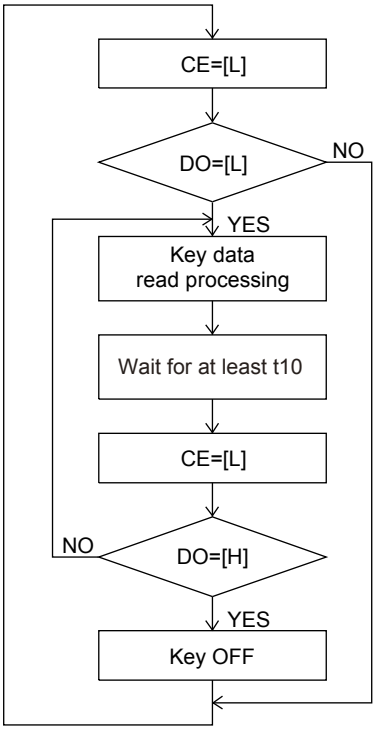
The period t9 in this technique must satisfy the following condition.

$t9 > t6 + t7 + t8$

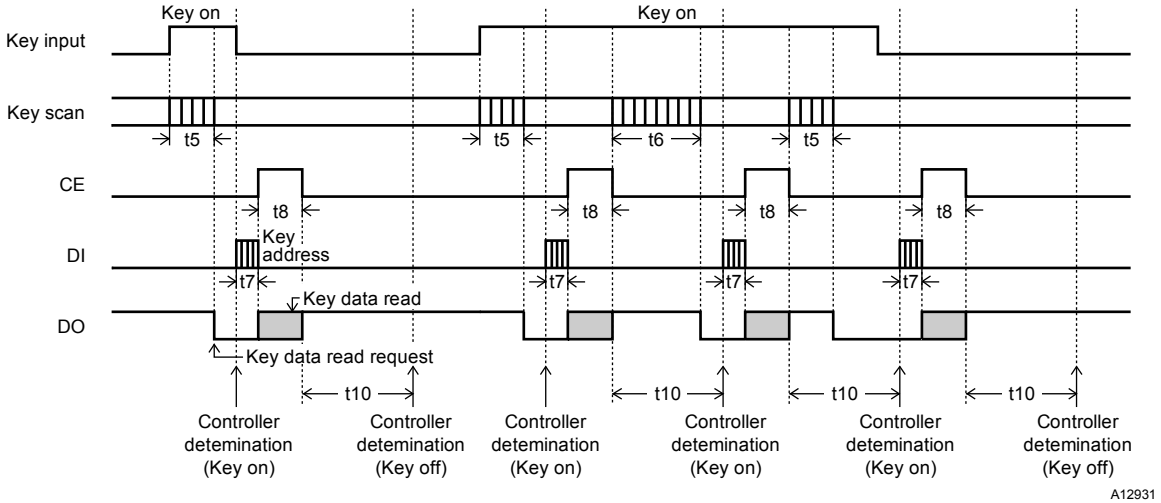
If a key data read operation is executed when DO is high, the read key data (KD1 to KD30) and sleep acknowledge data (SA) will be invalid.

2. Interrupt based key data acquisition

• Flowchart



• Timing chart



t5: Key scan execution time when the key data agreed for two key scans. (800T(S))
t6: Key scan execution time when the key data did not agree for two key scans and the key scan was executed again. (1600T(S))
t7: Key address (43H) transfer time
t8: Key data read time

$$T = \frac{1}{f_{OSC}}$$

• Explanation

In this technique, the controller uses interrupts to determine key on/off states and read the key data. The controller must check the DO state when CE is low. If DO is low, the controller recognizes that a key has been pressed and executes the key data read operation. After that the next key on/off determination is performed after the time t10 has elapsed by checking the DO state when CE is low and reading the key data. The period t10 in this technique must satisfy the following condition.

$t10 > t6$

If a key data read operation is executed when DO is high, the read key data (KD1 to KD30) and sleep acknowledge data (SA) will be invalid.

ORDERING INFORMATION

Device	Package	Shipping (Qty / Packing)
LC75808W-E	SPQFP100 14x14 / SQFP100 (Pb-Free / Halogen Free)	300 / Tray Foam
LC75808W-SH-E	SPQFP100 14x14 / SQFP100 (Pb-Free)	60 / Tray Foam
LC75808WS-E	SPQFP100 14x14 / SQFP100 (Pb-Free / Halogen Free)	300 / Tray Foam

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