ADC12J4000EVM User's Guide

User's Guide

Literature Number: SLAU551B
January 2014–Revised August 2015

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Introduction

The ADC12J4000EVM is an evaluation board used to evaluate the ADC12J4000 analog-to-digital converter (ADC) from Texas Instruments. The ADC12J4000 device is a single-channel, 12-bit ADC capable of operating at sampling rates up to 4 Giga-samples per second (GSPS). The ADC12J4000 device output data is transmitted over a standard JESD204B high-speed serial interface.

This evaluation board also includes the following important features:

- Transformer-coupled signal input network allowing a single-ended signal source from 400 MHz to 3 GHz
- The TRF3765 clock synthesizer generates the ADC sampling clock
- The LMK04828 system clock generator generates SYSREF and FPGA reference clocks for the high-speed serial interface
- Transformer-coupled clock input network to test the ADC performance with an external low-noise clock source
- LM95233 temperature sensor
- High-speed serial data output over a High Pin Count FMC interface connector
- Device register programming through USB connector and FTDI USB-to-SPI bus translator

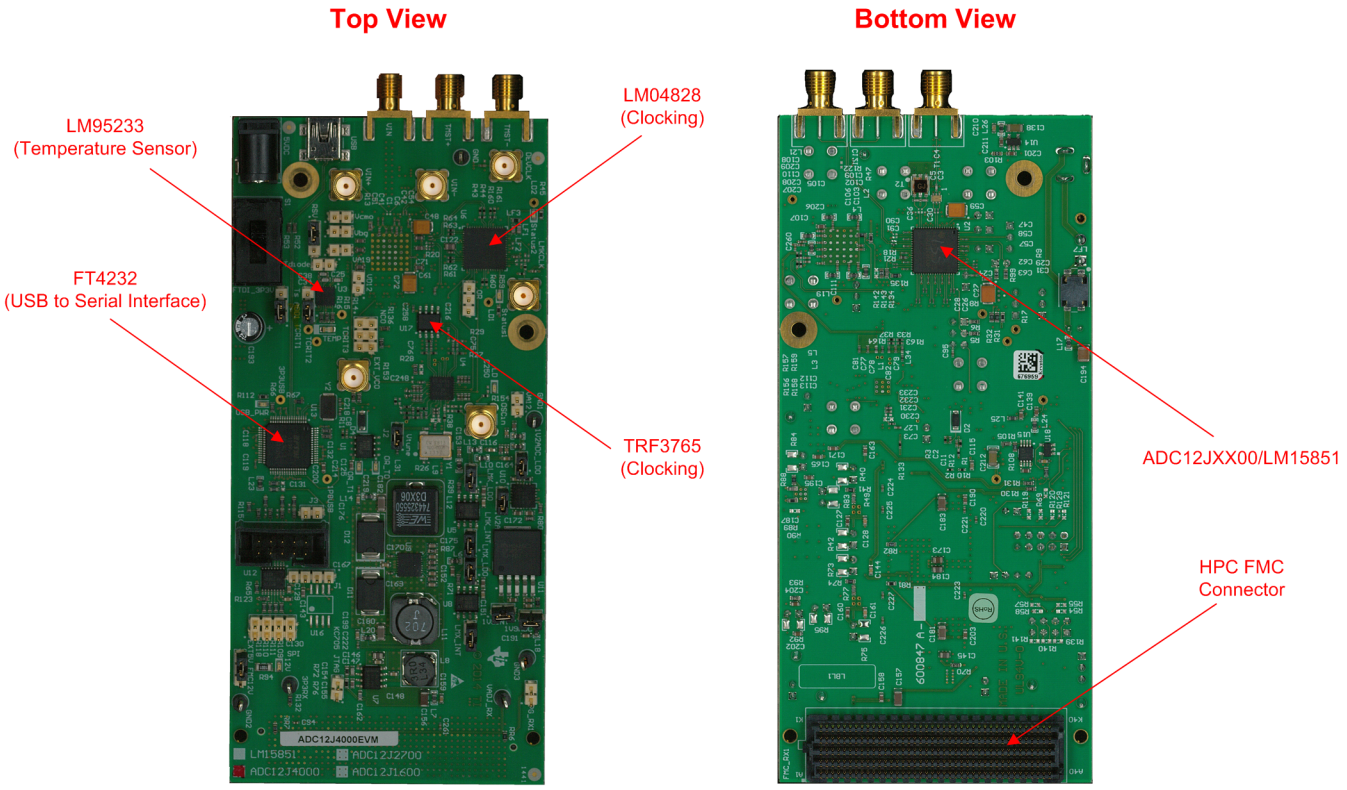

Figure 1-1. EVM Orientation

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The digital data from the ADC12J4000EVM board is quickly and easily captured with the TSW14J56EVM data capture board. The TSW14J56EVM captures the high-speed serial data, decodes the data, stores the data in memory, and then uploads it to a connected PC through a USB interface for analysis. The High-Speed Data Converter Pro (HSDC Pro) software on the PC communicates with the hardware and processes the data.

With proper hardware selection in the HSDC Pro software, the TSW14J56 device is automatically configured to support a wide range of operating speeds of the ADC12J4000EVM, but the device may not cover the full operating range of the ADC device. Serial data rates (and corresponding sampling rates) of 10 Gb/s (4 GSPS) down to 1 Gb/s (1 GSPS) are supported.

In the following sections of this document, the ADC12J4000EVM evaluation board is referred to as the *EVM* and the ADC12J4000 device is referred to as the *ADC* device.

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Equipment

This section describes how to setup the EVM on the bench with the proper equipment to evaluate the full performance of the ADC device.

2.1 Evaluation Board Feature Identification Summary

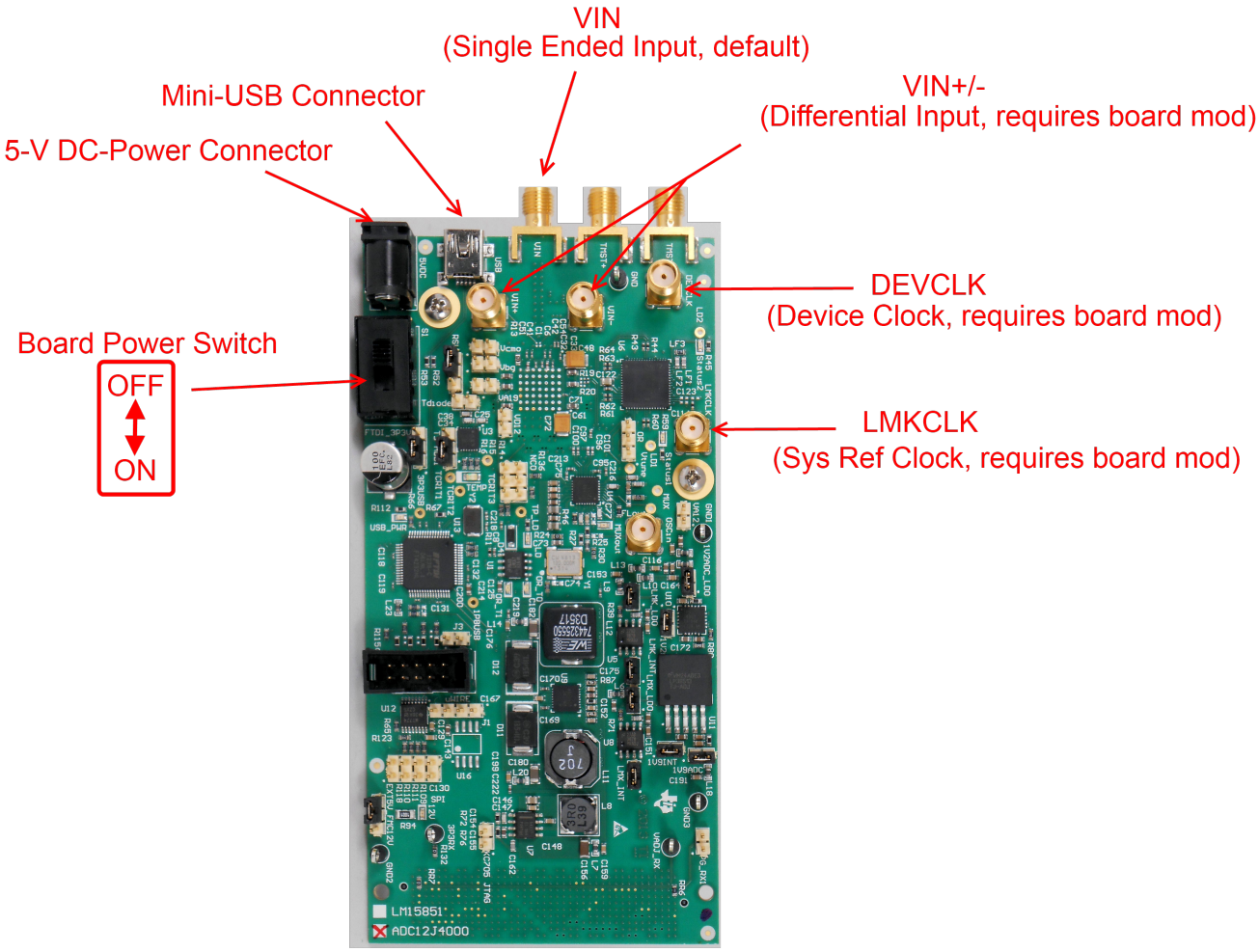

Figure 2-1. EVM Feature Locations

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2.2 Required Equipment

The following equipment and documents are included in the EVM evaluation kit:

- Evaluation board (EVM)
- Mini-USB cable
- 110 V to 240 V AC to 5-V DC-Power Adapter

The following equipment is not included in the EVM evaluation kit, but is required for evaluation of this product:

- TSW14J56EVM data capture board plus 5-V power supply and mini-USB cable
- High-Speed Data Converter Pro software
- PC computer running Windows XP, 7, or 8
- One low-noise signal generator for analog input. TI recommends the following generators:
  - HP HP8644B
  - Rohde & Schwarz™ SMA100A
- Bandpass filter for analog input signal (500 MHz or desired frequency). The following filters are recommended:
  - Bandpass filter, greater than or equal to 60 dB harmonic attenuation, less than or equal to 5% bandwidth, greater than 18-dBm power, less than 5 dB insertion loss
  - Trilithic™ 5VH-series tunable BPF
  - K&L Microwave™ BT-series tunable BPF
  - TTE KC6 or KC7-series fixed BPF
- Signal-path cables, SMA or BNC (or both SMA and BNC)

By default, the ADC12J4000EVM has an onboard clocking solution. A few small board modifications enable external clocking. If external clocking is used, the following equipment is recommended.

- Two low-noise signal generators. TI recommends similar models to the an analog input source.
- A bandpass filter for the DEVCLK input. TI recommends a filter similar to the analog-input path filter.

NOTE: The clock source used to drive the LMK04828 (labeled LMKCLK) must be half of the frequency used to drive the ADC12J4000 sampling clock (labeled DEVCLK). The clock generators must be frequency locked using a common 10 MHz reference.

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Setup Procedure

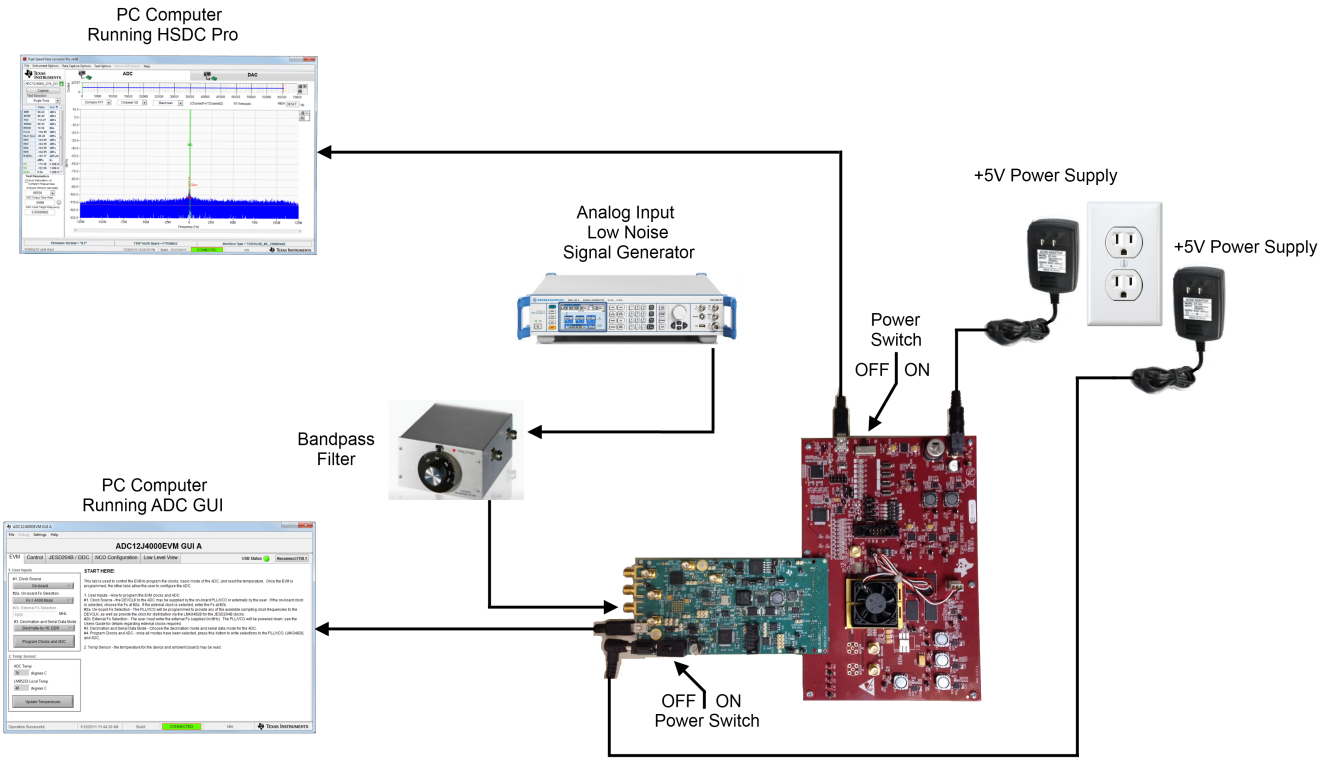

Figure 3-1. EVM Test Setup

NOTE: The HSDC Pro software must be installed before connecting the TSW14J56EVM to the PC for the first time.

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3.1 Install the High Speed Data Converter (HSDC) Pro Software

Download the most recent version of the HSDC Pro software from www.ti.com/tool/dataconverterpro-sw. Follow the installation instructions to install the software.

3.2 Install the Configuration GUI Software

1. Download the Configuration GUI software from the EVM tool folder at http://www.ti.com/tool/ADC12J4000EVM.
2. Extract files from the .zip file.
3. Run the setup.exe executable file and follow the instructions.

3.3 Connect the EVM and TSW14J56EVM

With the power off, connect the ADC12J4000EVM to the TSW14J56EVM through the FMC connector as shown in Figure 3-1. Ensure that the standoffs provide the proper height for robust connector connections.

3.4 Connect the Power Supplies to the Boards (Power Off)

1. Confirm that the power switch on the TSW14J56EVM is in the off position. Connect the 5-V power supply adapter to the TSW14J56EVM.
2. Confirm that the 5-V power supply for the ADC12J4000EVM is turned off. Connect the 5-V power supply to the power connector (the power connector that is the closest to the USB connector).

CAUTION

Do not turn on the power to any board. Powering up the boards in the incorrect order could potentially cause damage to one of the boards.

3.5 Connect the Signal Generators to the EVM (*RF outputs disabled until directed)

1. Connect a signal generator to the VIN input of the ADC12J4000EVM through a bandpass filter and attenuator at the SMA connector. This must be a low-noise signal generator. TI recommends a Trilithic-tunable bandpass filter to filter the signal from the generator. Configure the signal generator for 497.97MHz, 0 dBm.

   If external Clocking is Used (Optional)

2. Connect a signal generator to the DEVCLK input of the EVM through a bandpass filter. This signal generator must be a low-noise signal generator. TI recommends a Trilithic-tunable bandpass filter to filter the signal coming from the generator. Configure the signal generator for 4 GHz. For best performance when using an RF signal generator, the power input to the CLK SMA connector must be 11 dBm (2.2 Vpp into 50 Ω) must be at least 4 dBm to function. Therefore, the signal generator must increase above 11 dB by an amount equal to any additional attenuation in the clock signal path, such as the insertion loss of the bandpass filter. For example, if the filter insertion loss is 2 dB, the signal generator must be set to 11 dBm + 2 dB = 13 dBm.
3. Connect a signal generator to the LMKCLK input of the EVM through a bandpass filter. Configure the signal generator to 2 GHz.

NOTE:

1. LMKCLK must be set to half the frequency of the DEVCLK.
2. Ensure that the DEVCLK and LMKCLK sources are frequency locked using a common 10-MHz reference to ensure functionality. Frequency locking the input signal generator to the other generators can also be done if coherent sampling is desired.
3. Do not turn on the RF output of any signal generator at this time.

3.6 Turn On the TSW14J56EVM Power and Connect to the PC

1. Turn on the power switch of the TSW14J56EVM.

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2. Connect a mini-USB cable from the PC to the TSW14J56EVM.
3. If this is the first time connecting the TSW14J56EVM to the PC, then follow the on-screen instructions to automatically install the device drivers. See the TSW14J56EVM user's guide (SLWU086) for specific instructions.

3.7 Turn On the ADC12J4000EVM Power Supplies and Connect to the PC

1. Turn on the 5-V power supply to power up the EVM.
2. Connect the EVM to the PC with the mini-USB cable.

3.8 Turn On the Signal Generator RF Outputs

Turn on the RF signal output of the signal generator connected to VIN. If external clocking is used, turn on the RF signal outputs connected to DEVCLK and LMKCLK.

3.9 Open the ADC12J4000EVM GUI and Program the ADC and Clocks

The Device Configuration GUIis installed separately from the HSDC Pro installation and is a stand-alone GUI.

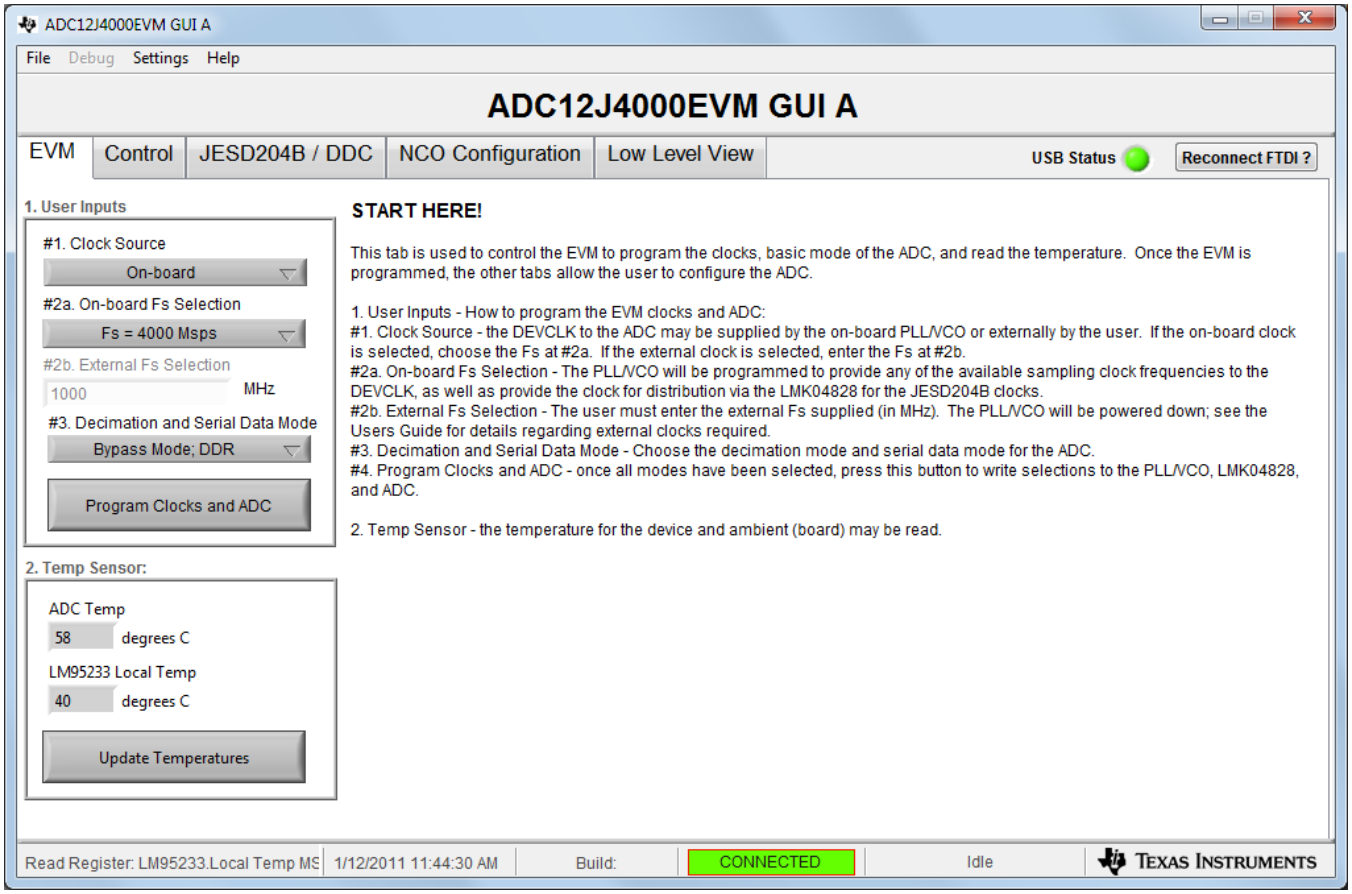

Figure 3-2. Configuration GUI EVM Tab

Figure 3-2 and Figure 3-4 show the GUI open to the *EVM* tab and *Control* tab respectively. Tabs at the top of the panel organize the configuration into device and EVM features with user-friendly controls and a low-level tab for directly configuring the registers. The EVM has three configurable devices, namely the ADC12J4000, LMK04828, and TRF3765. The register map for each device is provided in the device data sheet (SLAS989, SNAS605, and SNAS601, respectively).

1. Open the ADC12J4000EVM GUI

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2. Select the onboard clock as the clock source
3. Select Fs = 4000 Msps as the onboard Fs selection
4. a. If raw output data is desired, select Bypass Mode; DDR for the decimation and serial data mode.
   b. If decimation is desired, select one of the decimate options. Decimate-by-16; DDR for example.
5. Click *Program Clocks and ADC* (Note: This action will over-write any previous device register settings.)

3.10 Configure NCO Tab (if Decimation is Selected)

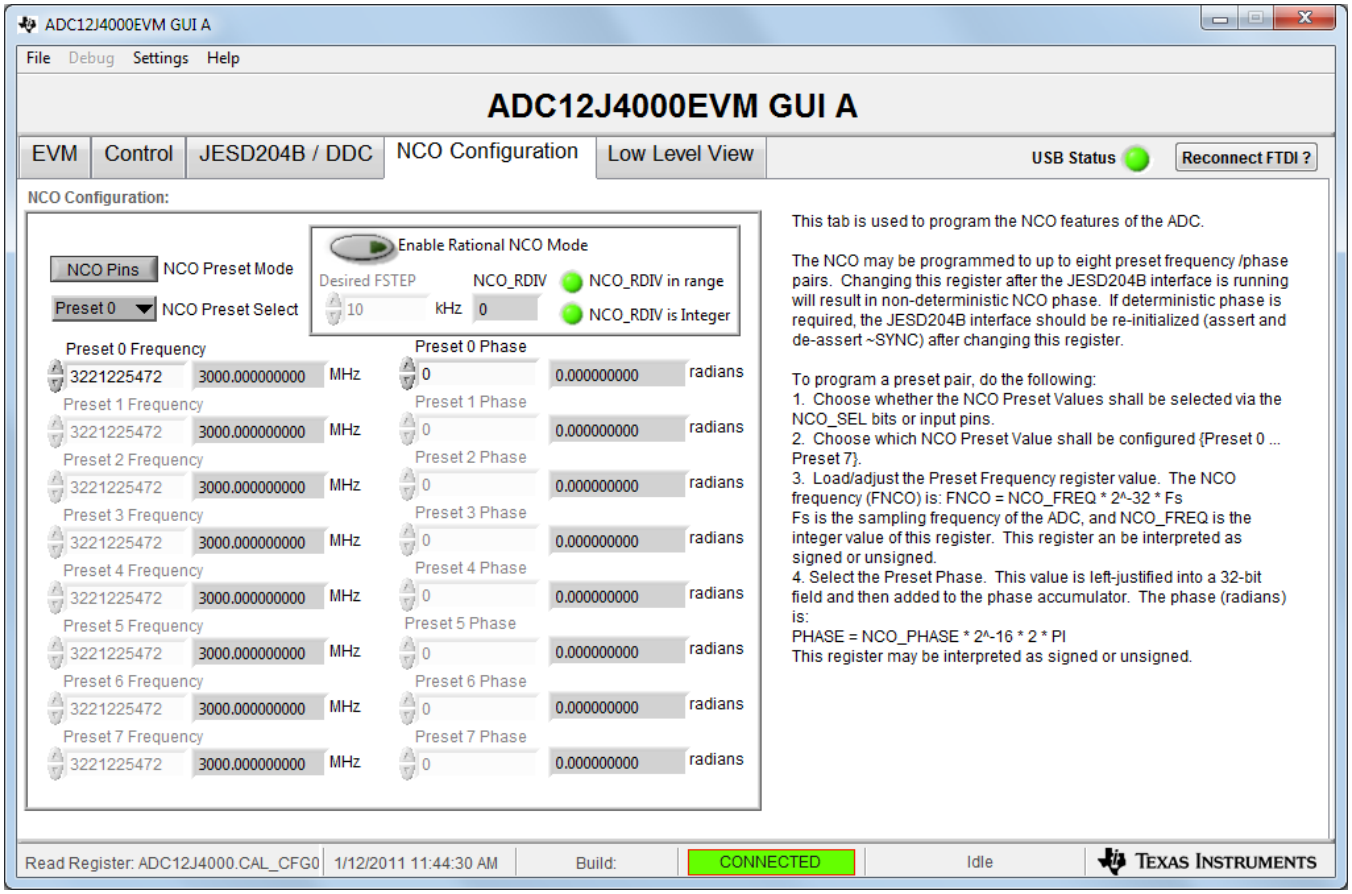

Figure 3-3. Configure NCO Tab

1. Select *Register Bits* as NCO Configuration
2. Select *Preset 0* for NCO Preset Select
3. Change *Preset 0* Frequency to 583951944, which corresponds to an NCO frequency of 543.847627938 MHz.

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3.11 Calibrate the ADC Device on the EVM

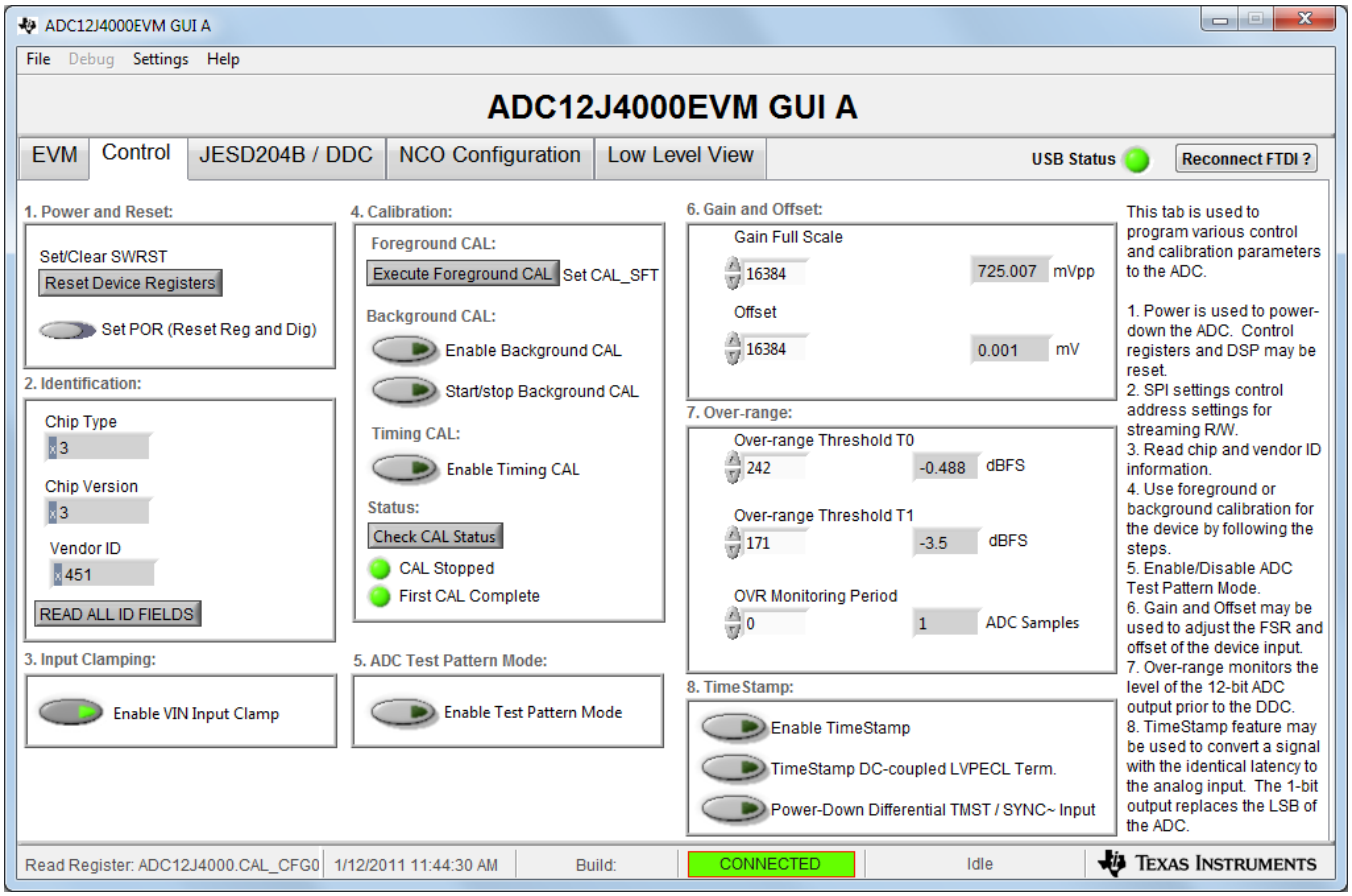

Figure 3-4. Configuration GUI ADC Control

1. With the EVM GUI open on the PC, navigate to the *Control* tab.
2. Click *Execute Foreground CAL* to calibrate the ADC.

NOTE: This calibrate button executes a calibration sequence that is required for full performance. This calibration is performed automatically during the Section 3.9 step but must be performed again, any time the sampling rate changes, after significant temperature change of the ADC, or after exiting the power-down mode. See the ADC12J4000 device data sheet, SLAS989, for details regarding the necessary calibration sequence.

3. If Background Calibration Mode is desired, first click the "Enable Background CAL" button to enable the mode and then click the "Start/Stop Background CAL" button. Then click the Execute Foreground CAL button once to properly initiate the calibration process.
4. To stop Background Calibration Mode, first click the "Start/Stop Background CAL" button, then click the "Enable Background CAL" button. Then click the Execute Foreground CAL button once to properly calibration the device in Foreground Mode.

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3.12 Open the HSDC Software and Load the FPGA Image to the TSW14J56EVM

1. Open the HSDC Pro software.
2. Click *OK* to confirm the serial number of the TSW14J56EVM device.
3. Select the *ADC12J4000_BYPASS* device from the ADC select drop-down in the top left corner.
4. When prompted click *Yes* to update the firmware.

NOTE: There are 3 new device files labeled ADC12J4000A_D10_DDR, ADC12J4000A_D20_DDR.ini and ADC12J4000A_D20_SDR.ini. These should be used with the new ADC12J4000EVM Rev A. The original files without the A suffix are still available for compatibility with the earlier revision EVM.

If the user configures the EVM with options other than the default register values, different instructions may be required for selecting the device in HSDC Pro. See Appendix B for more details.

5. Enter the ADC Output Data Rate ($f_{(SAMPLE)}$) as 4000M or the desired output sample rate. This number must be equal to the actual sampling rate of the device and must be updated if the sampling rate changes.

3.13 Verify the TSW14J56EVM Switch Settings and Status LEDs

1. Observe the switches and jumpers on the TSW14J56EVM and verify that they are in the correct position. See the TSW14J56EVM user guide (SLWU086) for more information regarding the proper (default) switch and jumper settings.
2. Verify the status of the D1 to D8 LEDs on the TSW14J56EVM. See the TSW14J56EVM user guide (SLWU086) for more information regarding the status LEDs.

3.14 Capture Data Using the HSDC Pro Software

1. Select the test to perform.
2. Select the data view.
3. Select the channel to view.
4. Click the capture button to capture new data.

Additional tips:

- Use the *Notch Frequency Bins* from the *Test Options* file menu to remove bins around DC (eliminate DC noise and offset) or the fundamental (eliminate phase noise from signal generators).
- Open the *Capture Option* dialog from the *Data Capture Options* file menu to change the capture depth or to enable FFT averaging.
- For analyzing only a portion of the spectrum, use the *Single Tone* test with the *Bandwidth Integration Markers* from the *Test Options* file menu. The *Channel Power* test is also useful.
- For analyzing only a subset of the captured data, set the *Analysis Window (samples)* setting to a value less than the number total samples captured and move the green or red markers in the small transient data window at the top of the screen to select the data subset of interest.

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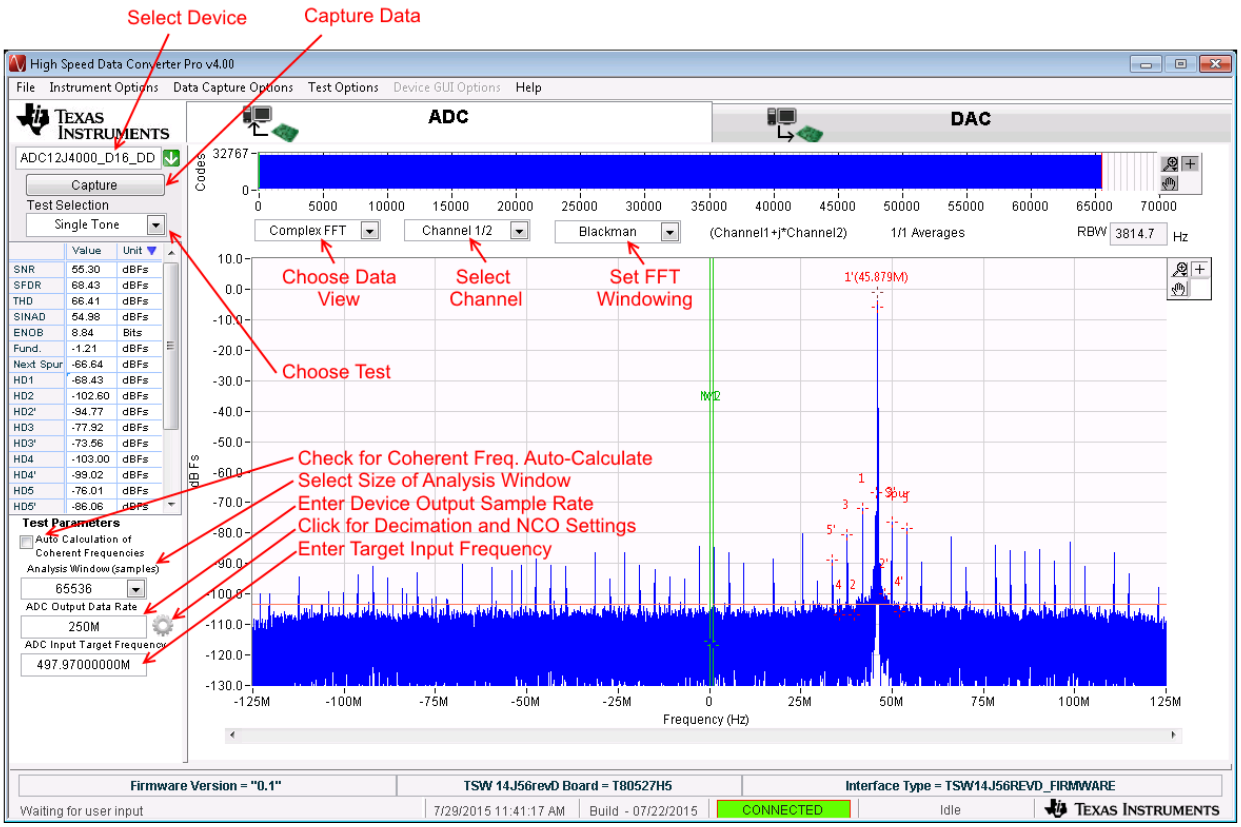

Figure 3-5. High Speed Data Converter Pro (HSDC) GUI

When using decimation and NCO features, the Additional Device Parameters window can be used to entire the following details:

1. ADC Sampling Rate
2. ADC Input Signal Frequency
3. NCO Frequency
4. Decimation Factor

The HSDC Pro GUI will calculate the ADC Output Data Rate based on these inputs. The Fundamental and Harmonic frequency locations will also be calculated and identified in the FFT display.

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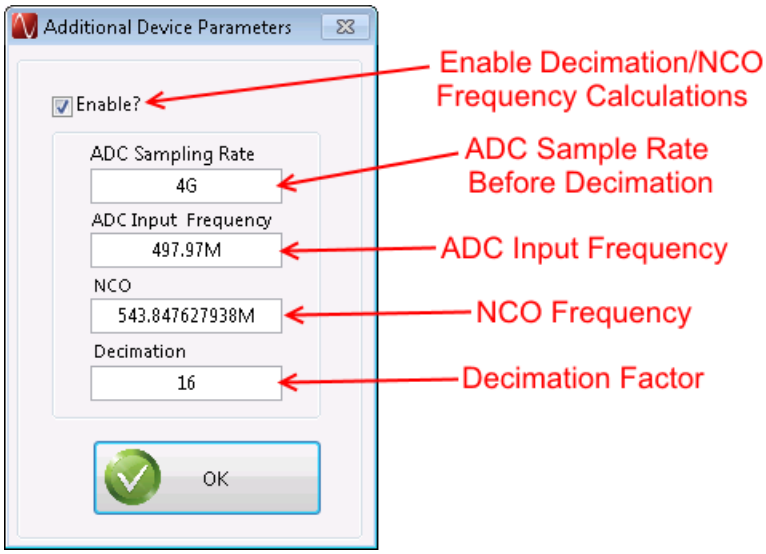

Figure 3-6. Additional Device Parameters Tab

3.15 Re-Verify TSW14J56EVM Status LEDs

Verify the status of the D1 to D8 LEDs on the TSW14J56EVM. See the TSW14J56EVM user guide (SLWU086) for more information regarding the status LEDs.

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Device Configuration

The ADC device is programmable through the serial programming interface (SPI) bus accessible through the FTDI USB-to-SPI converter located on the EVM. A GUI is provided to write instructions on the bus and program the registers of the ADC device.

For more information about the registers in the ADC device, see the ADC12J4000 data sheet (SLAS989) .

4.1 Supported JESD204B Device Features

The ADC device supports some configuration of the JESD204B interface. Due to limitations in the TSW14J56EVM firmware, all JESD204B link features of the ADC device are not supported. Table 4-1 lists the supported and non-supported features.

Table 4-1. Supported and Non-Supported Features of the JESD204B Device

JESD204B FEATURE	SUPPORTED BY ADC DEVICE	SUPPORTED BY TSW14J56EVM
Number of lanes per channel (L)	L = 1, 2, 3, 4, 5, 8[(1)]	L = 1,2,4,8 supported L = 3 and 5 not currently supported
Number of frames per multiframe (K)	K_{min} = 2–12[(1)] K_{max} = 32	Most values of K supported, constrained by requirement that K × F = 4^n
Scrambling	Supported	Supported
Test patterns	PBRS7, PBRS11, PBRS15, Ramp, D21.5, K28.5, Repeat ILA, Modified RPAT, Long/Short Transport, Serial Out 0, Serial Out 1, Bypass Lane ID, ADC Test Pattern[(1)]	ILA, Ramp, Long/Short Transport and ADC Test Pattern are supported. Other patterns not supported at this time.
Speed	Lane rates from 1 to 10 Gbps[(1)]	Lane rates from 2 to 10 Gbps currently supported. $f_{(SAMPLE)}$ parameter must be properly set in HSDC Pro GUI.

(1) Dependent on bypass or decimation mode and output rate selection. Always disable the JESD204 block before enabling any of the JESD204B settings. Once the settings are changed, re-enable the JESD204 block.

4.2 Tab Organization

Control of the ADC device features are available in the EVM, JESD204B/DDC, NCO Configuration, and Low-Level View tabs.

4.3 Low-Level Control

The Low-Level tab, listed in Figure 4-1, allows configuration of the devices at the bit-field level. At any time, the following controls can be used to configure or read from the device.

Table 4-2. Low-Level Controls

CONTROL	DESCRIPTION
Register map summary	Displays the devices on the EVM, registers for those devices, and the states of the registers • Clicking on a register field allows individual bit manipulation in the register data cluster • The value column shows the value of the register at the time the GUI was last updated • The LR column shows the value of the register at the time the register was last read
Write register button	Write to the register highlighted in the register map summary with the value in the Write Data field

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Table 4-2. Low-Level Controls (continued)

CONTROL	DESCRIPTION
Write all button	Update all registers shown in the register map summary with the values shown in the Register Map Summary Can be used to re-synchronize the GUI with the state of the hardware
Read register button	Read from the register highlighted in the register map summary and display the results in the Read Data field
Read-all button	Read from all register in the register map summary and display current state of hardware
Load configuration button	Load a configuration file from disk and register address/data values in the file
Save configuration button	Save a configuration file to disk that contains the current state of the configuration registers
Register data cluster	Manipulate individual accessible bits of the register highlighted in the register map summary
Individual register cluster with read or write register buttons	Perform a generic read or write command to the device shown in the *Block* drop-down box using the address and write data information

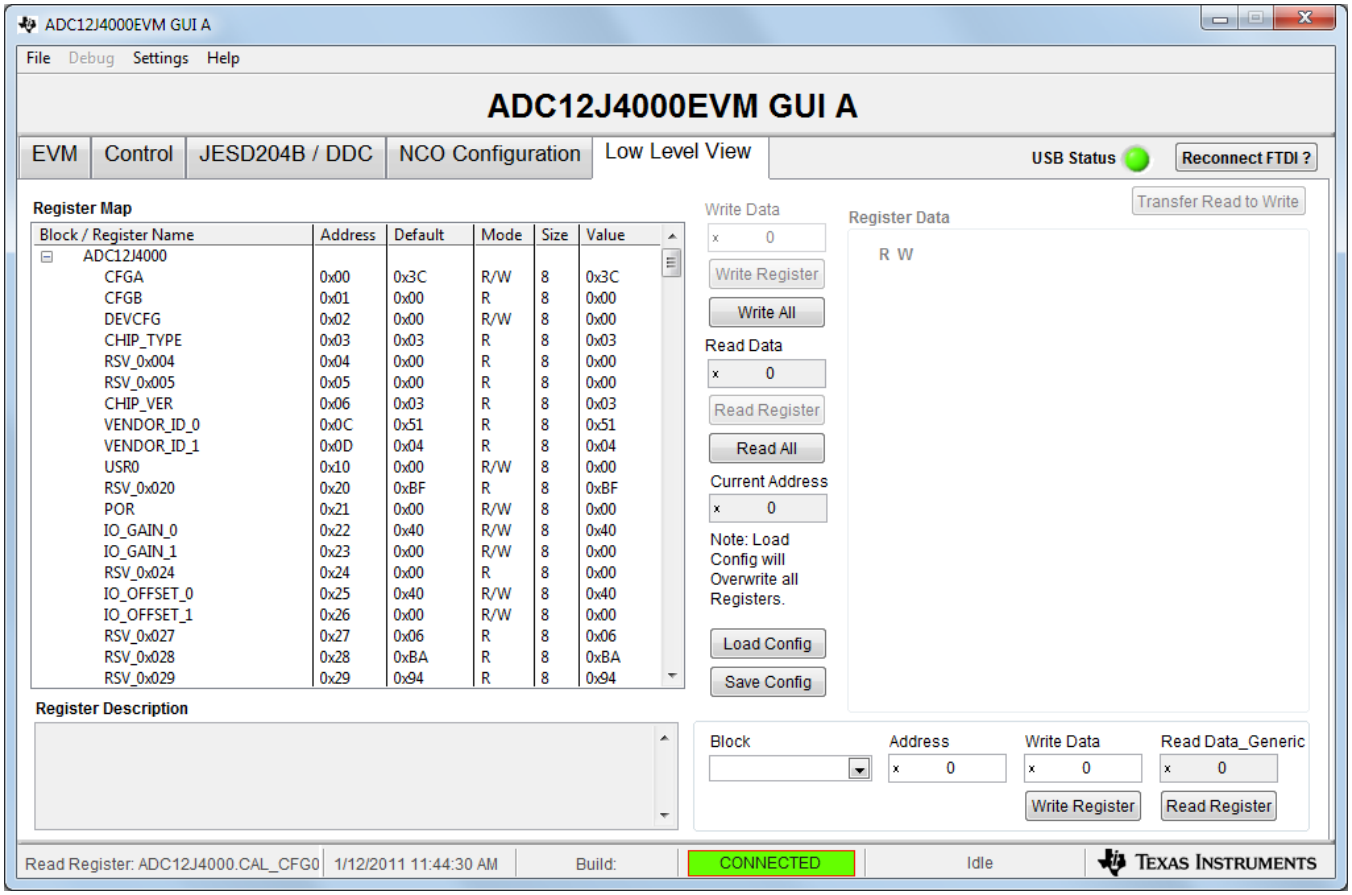

Figure 4-1. Low-Level Register Control Tab

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Evaluation Troubleshooting

Table 5-1. Troubleshooting

Issue	Troubleshoot
General problems	• Verify the test setup shown in Figure 3-1, and repeat the setup procedure as described in this document. • Check power supply to EVM and TSW14J56EVM. Verify that the power switches are in the on position. • Check signal and clock connections to EVM. • Visually check the top and bottom sides of the board to verify that nothing looks discolored or damaged. • Ensure the board to board FMC connection is secure. • Try pressing the CPU_RESET button on the TSW14J56EVM. Also try clicking *Instrument Options → Reset Board* after changing the ADC configuration. • Try power-cycling the external power supply to the EVM, and reprogram the LMK and ADC devices.
TSW14J56 LEDs are not correct	• Verify the settings of the configuration switches on the TSW14J56EVM. • Verify that the clock going to the CLK input is connected and the appropriate LEDs are blinking. • Verify that the ADC device internal registers are configured properly. • If LEDs are not blinking, reprogram the ADC EVM devices. • Try pressing the CPU_RESET button on the TSW14J56EVM. • Try capturing data in HSDC Pro to force an LED status update
Configuration GUI is not working properly	• Verify that the USB cable is plugged into the EVM and the PC. • Check the computer device manager and verify that a *USB serial device* is recognized when the EVM is connected to the PC. • Verify that the green *USB Status* LED light in the top right corner of the GUI is lit. If it is not lit, click the *Reconnect FTDI* button. • Try restarting the configuration GUI.
Configuration GUI is not able to connect to the EVM	• Use the free FT_PROG software from FTDI chip and verify that the on-board FTDI chip is programmed with the product description *ADC12J4000_A0*.
HSDC Pro software is not capturing good data or analysis results are incorrect.	• Verify that the TSW14J56EVM is properly connected to the PC with a mini-USB cable and that the board serial number is properly identified by the HSDC software. • Check that the proper ADC device mode is selected. The mode should match in HSDC Pro and the ADC GUI. • Check that the analysis parameters are properly configured.
HSDC Pro software gives a time-out error when capturing data	• Try to reprogram the LMK device and reset the JESD204 link. • Verify that the ADC sampling rate is correctly set in the HSDC software.
Sub-optimal measured performance	• Try clicking *Execute Foreground CAL* on the *Control* tab of the configuration GUI to recalibrate the ADC. • Check that the spectral analysis parameters are properly configured. • Verify that bandpass filters are used in the clock and input signal paths and that low-noise signal sources are used.

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References

A.1 Technical Reference Documents

- ADC12J4000 data sheet, SLAS989
- TSW14J56EVM user's guide, SLWU086
- User's guide for the High Speed Data Converter Pro Software, also available in the help menu of the software, SLWU087
- LMK04828 data sheet, SNAS605
- TRF3765 data sheet, SLWS230
- FTDI USB to Serial Driver Installation Manual, www.ftdichip.com/Support/Documents/InstallGuides.htm

A.2 TSW14J56EVM Operation

Refer to the TSW14J56EVM user guide SLWU086 for configuration and status information.

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HSDC Pro Settings for Optional ADC Device Configuration

B.1 Changing the Number of Frames per Multi-Frame (K)

Changing the number of frames per multi-frame output by the JESD204 transmitter (ADC device) is configured using the K parameter on the JESD204B tab in the Configuration GUI. This parameter must be matched by the receiving device, and the SYSREF frequency must also be programmed to a compatible frequency.

B.2 Customizing the EVM for Optional Clocking Support

By default, the TRF3765 is configured to generate the device clock with an onboard crystal oscillator and the LMK04828 is used as a clock distribution and provides the system reference clock for the FPGA. The EVM can be configured to use external clocks with the following steps (see Figure B-1):

1. Modify the Hardware:
   (a) Remove C32 and C33. Populate C30 and C36.
   (b) Remove C112 and C113. Populate C114 and C123.
2. Connect the Signal Generators:
   (a) Connect the 10-MHz reference from Sig Gen 1 to Sig Gen 2.
   (b) Configure Sig Gen 2 to use the 10 MHz reference input from Sig Gen 1.
   (c) Sig Gen 1 connects to DEVCLK. Set to the generator frequency to the desired F_{DEVCLK}.
   (d) Sig Gen 2 connects to LMKCLK. Set the generator frequency as follows:
   $F_{LMKCLK} = F_{DEVCLK} / 2$
3. Program the GUI:
   (a) In the EVM tab, set the Clock Source to *External*.
   (b) Enter the Sampling Frequency (F_{DEVCLK}) in step 2(b).

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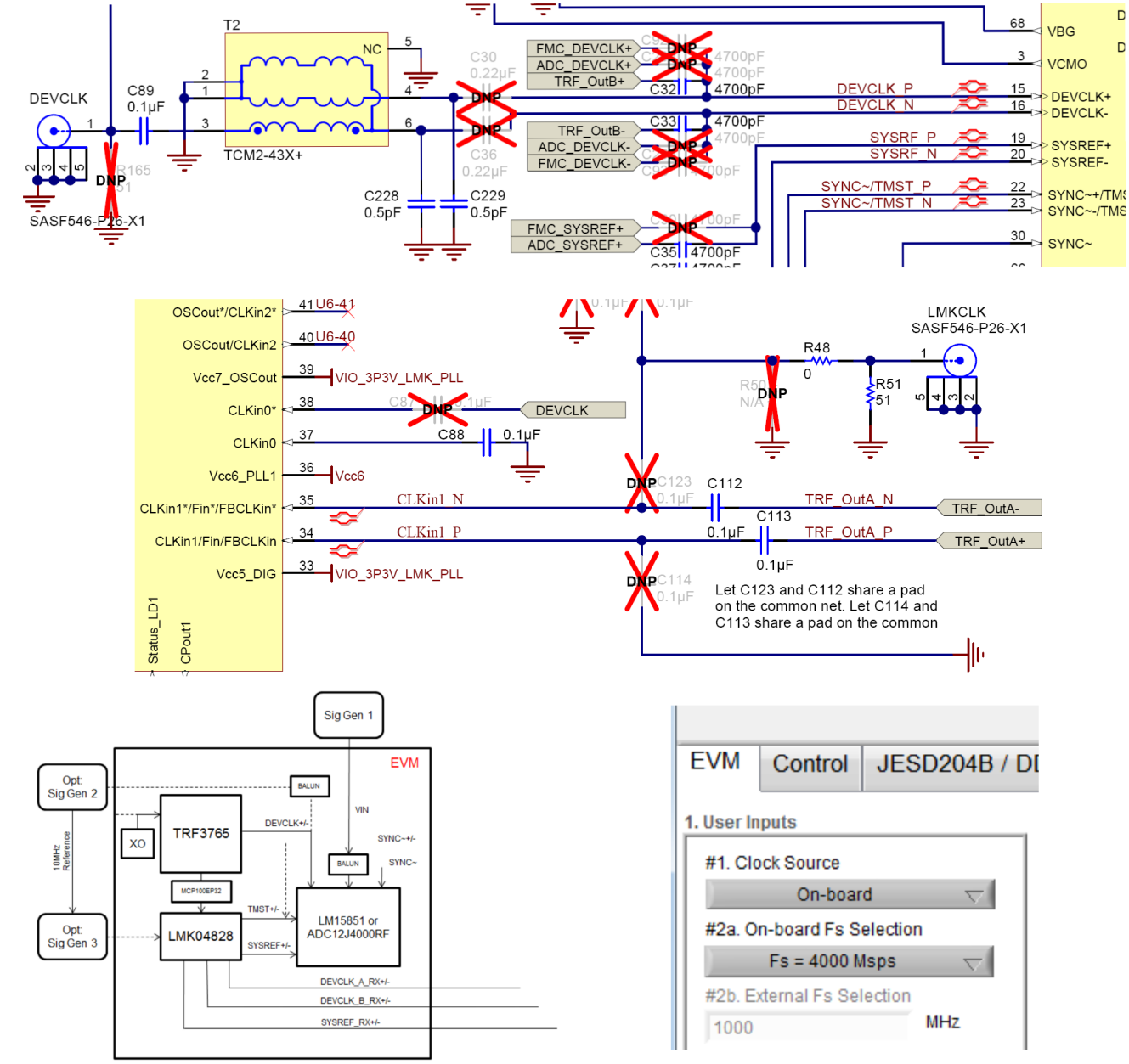

Figure B-1. Configuration for Optional Clocking Support

The TRF3765 and LMK04828 may be reconfigured to exercise more features, but this EVM is not intended to be a full evaluation platform for these devices. For a full evaluation platform see the LMK04828 tool folder: www.ti.com/tool/lmk04828bevm and the TRF3765 tool folder: http://www.ti.com/tool/trf3765evm.

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Revision History

Changes from Original (January 2014) to A Revision	Page
• Removed *Preliminary* watermark	4
• Changed *EVM Orientation* image and labels.	4
• Updated NCO frequencies	14

Revision History

Changes from A Revision (Month Year) to B Revision	Page
• Changed all instances of LMX2581 to TRF3765 including links to documents and tool folders.	1
• Changed note in *Required Equipment* section.	8
• Changed *EVM Test Setup* image.	10
• Changed note in *Connect the Signal Generators to the EVM (RF Signal Off)* section.	11
• Changed *Configuration GUI EVM Tab* image.	12
• Changed *Configuration NCO Tab* image.	13
• Changed *Configuration GUI ADC Control* image.	14
• Changed *High Speed Data Converter Pro (HSDC) GUI* image.	16
• Added *Additional Device Parameters* image and text.	17
• Changed *Low-Level Register Control Tab* image.	20
• Changed *Appendix B: LED Configuration* to point to the *TSW14J56EVM User Guide.*	24
• Changed *Configuration for Optional Clocking Support* image.	27

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

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