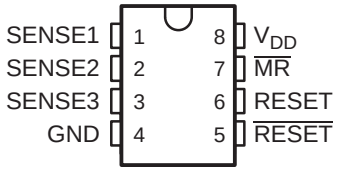
TRIPLE PROCESSOR SUPERVISORS

FEATURES

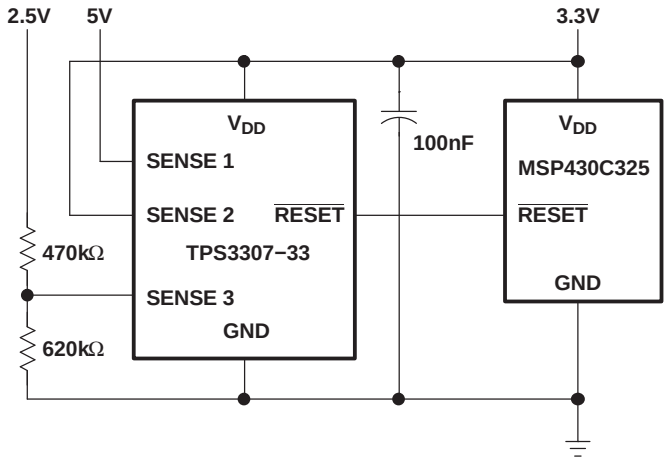
- **Triple Supervisory Circuits for DSP and Processor-Based Systems**
- **Power-On Reset Generator With Fixed Delay Time of 200ms, No External Capacitor Needed**
- **Temperature-Compensated Voltage Reference**
- **Maximum Supply Current of 40μA**
- **Supply Voltage Range: 2V to 6V**
- **Defined $\overline{\text{RESET}}$ Output From $V_{DD} \geq 1.1V$**
- **MSOP-8 and SO-8 Packages**
- **Temperature Range : – 40°C to +85°C**

D OR DGN PACKAGE
(TOP VIEW)



TYPICAL APPLICATIONS

Figure 1 lists some of the typical applications for the TPS3307 family, and a schematic diagram for a processor-based system application. This application uses TI part numbers TPS3307-33 and MSP430C325.



- **Applications using DSPs, Microcontrollers or Microprocessors**
- **Industrial Equipment**
- **Programmable Controls**
- **Automotive Systems**
- **Portable/Battery Powered Equipment**
- **Intelligent Instruments**
- **Wireless Communication Systems**
- **Notebook/Desktop Computers**

Figure 1. Applications Using the TPS3307 Family

DESCRIPTION

The TPS3307 family is a series of micropower supply voltage supervisors designed for circuit initialization primarily in DSP and processor-based systems, which require more than one supply voltage.

The product spectrum of the TPS3307-xx is designed for monitoring three independent supply voltages: 3.3V/1.8V/adj, 3.3V/2.5V/adj or 3.3V/5V/adj. The adjustable SENSE input allows the monitoring of any supply voltage >1.25V.

The various supply voltage supervisors are designed to monitor the nominal supply voltage as shown in the following supply voltage monitoring table.

During power-on, $\overline{\text{RESET}}$ is asserted when the supply voltage V_{DD} becomes higher than 1.1V. Thereafter, the supply voltage supervisor monitors the SENSE*n* inputs and keeps $\overline{\text{RESET}}$ active as long as SENSE*n* remain below the threshold voltage V_{IT+}.

An internal timer delays the return of the $\overline{\text{RESET}}$ output to the inactive state (high) to ensure proper system reset. The delay time, $t_{d\ (typ)}$ = 200ms, starts after all SENSE*n* inputs have risen above the threshold voltage V_{IT+}. When the voltage at any SENSE input drops below the threshold voltage V_{IT-}, the $\overline{\text{RESET}}$ output becomes active (low) again.

The TPS3307-xx family of devices incorporates a manual reset input, $\overline{\text{MR}}$. A low level at $\overline{\text{MR}}$ causes $\overline{\text{RESET}}$ to become active. In addition to the active-low $\overline{\text{RESET}}$ output, the TPS3307-xx family includes an active-high RESET output.

The devices are available in either 8-pin MSOP or standard 8-pin SO packages.

The TPS3307-xx devices are characterized for operation over a temperature range of –40°C to +85°C.

SUPPLY VOLTAGE MONITORING

DEVICE	NOMINAL SUPERVISED VOLTAGE			THRESHOLD VOLTAGE (TYP)		
	SENSE1	SENSE2	SENSE3	SENSE1	SENSE2	SENSE3
TPS3307-18	3.3V	1.8V	User defined	2.93V	1.68V	1.25V(1)
TPS3307-25	3.3V	2.5V	User defined	2.93V	2.25V	1.25V(1)
TPS3307-33	5V	3.3V	User defined	4.55V	2.93V	1.25V(1)

(1) The actual sense voltage has to be adjusted by an external resistor divider according to the application requirements.

AVAILABLE OPTIONS(1)

T_A	PACKAGED DEVICES		MARKING DGN PACKAGE	CHIP FORM (Y)
	SMALL OUTLINE (D)	PowerPAD™ µ-SMALL OUTLINE (DGN)		
–40°C to +85°C	TPS3307-18D	TPS3307-18DGN	TIAAP	TPS3307-18Y
	TPS3307-25D	TPS3307-25DGN	TIAAQ	TPS3307-25Y
	TPS3307-33D	TPS3307-33DGN	TIAAR	TPS3307-33Y

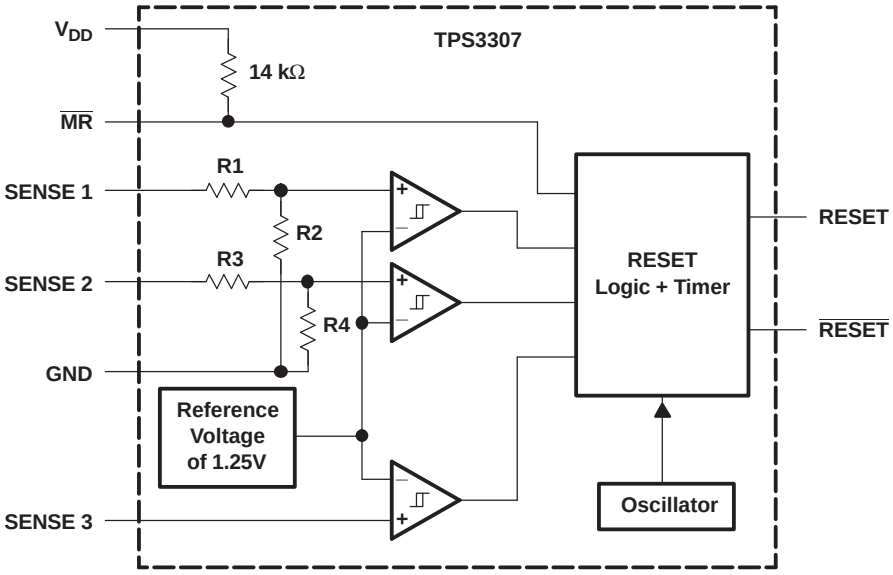
(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

Function/Truth Tables

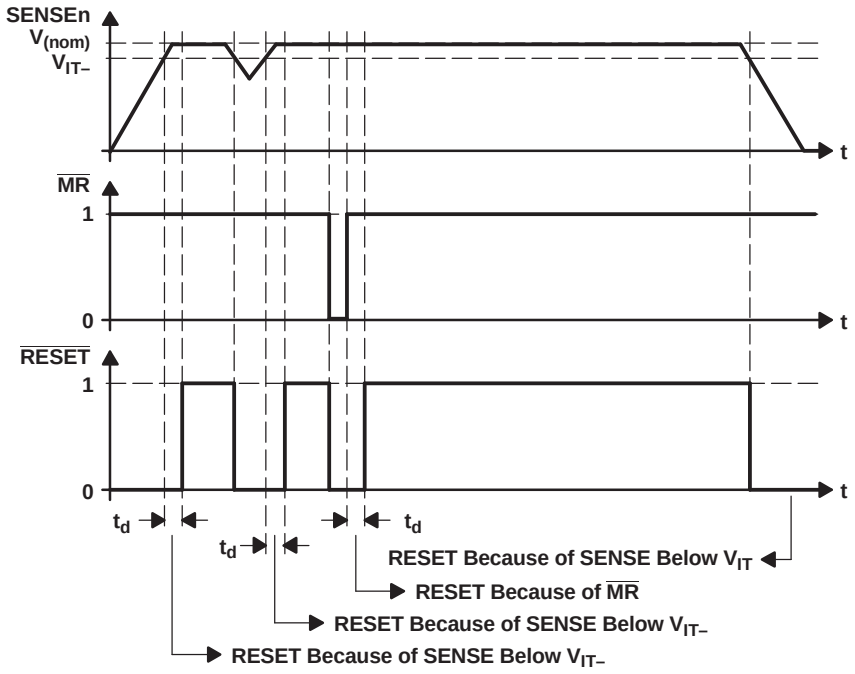
$\overline{\text{MR}}$	SENSE1 > V_{IT1}	SENSE2 > V_{IT2}	SENSE3 > V_{IT3}	$\overline{\text{RESET}}$	RESET
L	X(1)	X(1)	X	L	H
H	0	0	0	L	H
H	0	0	1	L	H
H	0	1	0	L	H
H	0	1	1	L	H
H	1	0	0	L	H
H	1	0	1	L	H
H	1	1	0	L	H
H	1	1	1	H	L

(1) X = Don't care

Functional Block Diagram



Timing Diagram



TPS3307Y Chip Information

These chips, when properly assembled, display characteristics similar to those of the TPS3307. Thermal compression or ultrasonic bonding may take place on the doped aluminium bonding pads. The chips may be mounted with conductive epoxy or a gold-silicon preform.

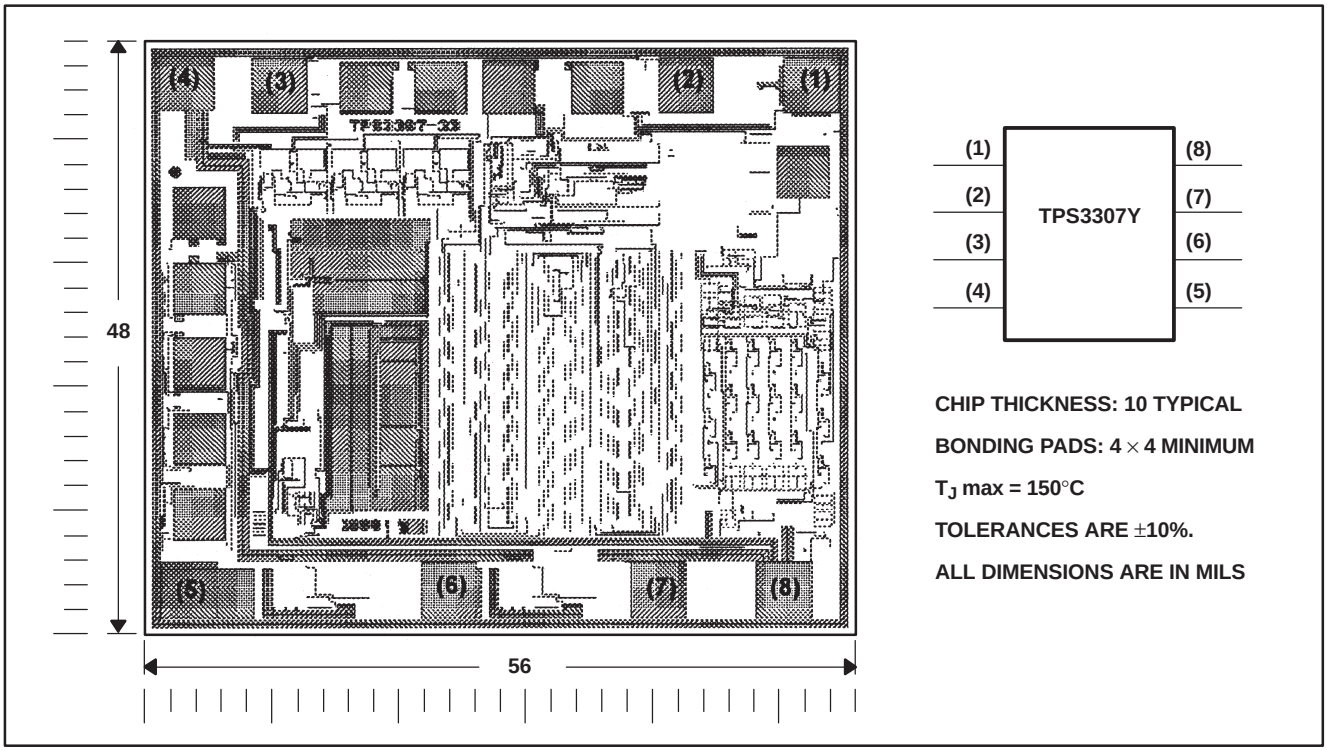


Table 2. Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
GND	4		Ground
$\overline{MR}$	7	I	Manual reset
$\overline{RESET}$	5	O	Active-low reset output
RESET	6	O	Active-high reset output
SENSE1	1	I	Sense voltage input 1
SENSE2	2	I	Sense voltage input 2
SENSE3	3	I	Sense voltage input 3
V_{DD}	8		Supply voltage

Absolute Maximum Ratings(1)

Over operating free-air temperature range (unless otherwise noted).

	UNIT
Supply voltage, V_{DD}(2)	7V
$\overline{MR}$ pin	–0.3V to V_{DD} +0.3V
All other pins(2)	–0.3V to 7V
Maximum low output current, I_{OL}	5mA
Maximum high output current, I_{OH}	–5mA
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{DD}$)	±20mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{DD}$)	±20mA
Continuous total power dissipation	See Dissipation Rating Table
Operating free-air temperature range, T_A	–40°C to +85°C
Storage temperature range, T_{stg}	–65°C to +150°C
Soldering temperature	+260°C

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to GND. For reliable operation the device must not be operated at 7V for more than t = 1000h continuously.

Dissipation Rating Table

PACKAGE	$T_A \le +25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = +25°C$	$T_A = +70°C$ POWER RATING	$T_A = +85°C$ POWER RATING
DGN	2.14W	17.1mW/°C	1.37W	1.11W
D	725mW	5.8mW/°C	464mW	377mW

Recommended Operating Conditions

At specified temperature range.

	MIN	MAX	UNIT
Supply voltage, V_{DD}	2	6	V
Input voltage at $\overline{MR}$ and SENSE3, V_I	0	V_{DD} + 0.3	V
Input voltage at SENSE1 and SENSE2, V_I	0	$(V_{DD}+0.3)V_{IT}/1.25V$	V
High-level input voltage at $\overline{MR}$, V_{IH}	0.7 x V_{DD}		V
Low-level input voltage at $\overline{MR}$, V_{IL}		0.3 × V_{DD}	V
Input transition rise and fall rate at $\overline{MR}$, $\Delta t/\Delta V$		50	ns/V
Operating free-air temperature range, T_A	–40	+85	°C

Electrical Characteristics

Over recommended operating free-air temperature range (unless otherwise noted).

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage		V_{DD} = 2V to 6V, I_{OH} = –20 µA	V_{DD} – 0.2V			V
			V_{DD} = 3.3V, I_{OH} = –2mA	V_{DD} – 0.4V			
			V_{DD} = 6V, I_{OH} = –3mA	V_{DD} – 0.4V			
V_{OL}	Low-level output voltage		V_{DD} = 2V to 6V, I_{OL} = 20µA			0.2	V
			V_{DD} = 3.3V, I_{OL} = 2mA			0.4	
			V_{DD} = 6V, I_{OL} = 3mA			0.4	
	Power-up reset voltage(1)		$V_{DD} \geq$ 1.1V, I_{OL} = 20µA			0.4	V
$V_{IT–}$	Negative-going input threshold voltage(2)	VSENSE3	V_{DD} = 2V to 6V, T_A = 0°C to +85°C	1.22	1.25	1.28	V
		VSENSE1, VSENSE2		1.64	1.68	1.72	
				2.20	2.25	2.30	
				2.86	2.93	3	
				4.46	4.55	4.64	
		VSENSE3	V_{DD} = 2V to 6V, T_A = –40°C to +85°C	1.22	1.25	1.29	V
		VSENSE1, VSENSE2		1.64	1.68	1.73	V
				2.20	2.25	2.32	
				2.86	2.93	3.02	
				4.46	4.55	4.67	
V_{hys}	Hysteresis at VSENSEn input		$V_{IT–}$= 1.25V		10		mV
			$V_{IT–}$= 1.68V		15		
			$V_{IT–}$= 2.25V		20		
			$V_{IT–}$= 2.93V		30		
			$V_{IT–}$= 4.55V		40		
I_H	High-level input current	$\overline{MR}$	$\overline{MR}$ = 0.7 × V_{DD}, V_{DD} = 6V		–130	–180	µA
		SENSE1	VSENSE1 = V_{DD} = 6V		5	8	
		SENSE2	VSENSE2 = V_{DD} = 6V		6	9	
		SENSE3	VSENSE3 = V_{DD}	–25		25	nA
I_L	Low-level input current	$\overline{MR}$	$\overline{MR}$ = 0V, V_{DD} = 6V		–430	–600	µA
		SENSEn	VSENSE1,2,3 = 0V	–25		25	nA
I_{DD}	Supply current					40	µA
C_i	Input capacitance		V_I = 0V to V_{DD}		10		pF

(1) The lowest supply voltage at which $\overline{RESET}$ becomes active. t_r, $V_{DD} \geq$ 15µs/V

(2) To ensure best stability of the threshold voltage, a bypass capacitor (ceramic 0.1µF) should be placed close to the supply terminals.

Timing Requirements

At V_{DD} = 2V to 6V, R_L = 1MΩ, C_L = 50pF, T_A = +25°C.

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_w	Pulse width	SENSEn	$V_{SENSEnL} = V_{IT-} - 0.2V$, $V_{SENSEnH} = V_{IT+} + 0.2V$	6			µs
		$\overline{MR}$	$V_{IH} = 0.7 \times V_{DD}$, $V_{IL} = 0.3 \times V_{DD}$	100			ns

Switching Characteristics

At V_{DD} = 2V to 6V, R_L = 1MΩ, C_L = 50pF, T_A = +25°C.

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_d	Delay time		$V_{I(SENSEn)} \geq V_{IT+} + 0.2V$, $\overline{MR} \geq 0.7 \times V_{DD}$. See Timing Diagram.	140	200	280	ms
t_{PHL}	Propagation (delay) time, high-to-low level output	$\overline{MR}$ to $\overline{RESETMR}$ to RESET	$V_{I(SENSEn)} \geq V_{IT+} + 0.2V$, $V_{IH} = 0.7 \times V_{DD}$, $V_{IL} = 0.3 \times V_{DD}$		200	500	ns
t_{PLH}	Propagation (delay) time, low-to-high level output	$\overline{MR}$ to $\overline{RESETMR}$ to RESET					
t_{PHL}	Propagation (delay) time, high-to-low level output	SENSEn to $\overline{RESET}$ SENSEn to RESET	$V_{IH} = V_{IT+} + 0.2V$, $V_{IL} = V_{IT-} - 0.2V$, $\overline{MR} \geq 0.7 \times V_{DD}$		1	5	µs
t_{PLH}	Propagation (delay) time, low-to-high level output	SENSEn to $\overline{RESET}$ SENSEn to RESET					

Typical Characteristics

NORMALIZED SENSE THRESHOLD VOLTAGE vs FREE-AIR TEMPERATURE AT V_{DD}

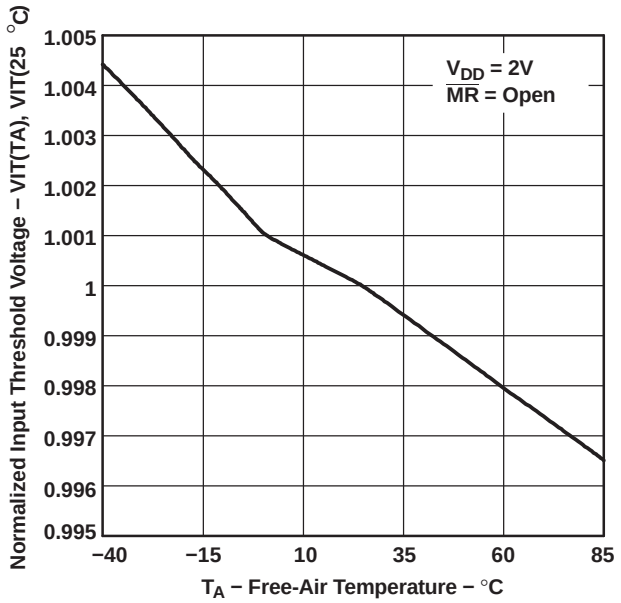


Figure 2.

SUPPLY CURRENT vs SUPPLY VOLTAGE

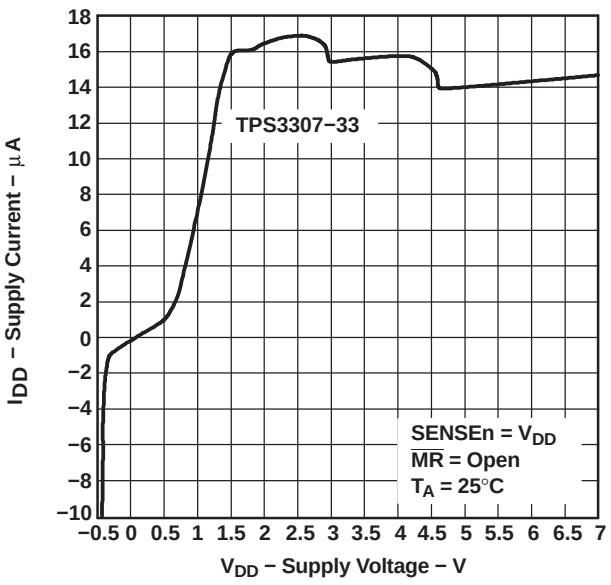


Figure 3.

INPUT CURRENT vs INPUT VOLTAGE AT $\overline{MR}$

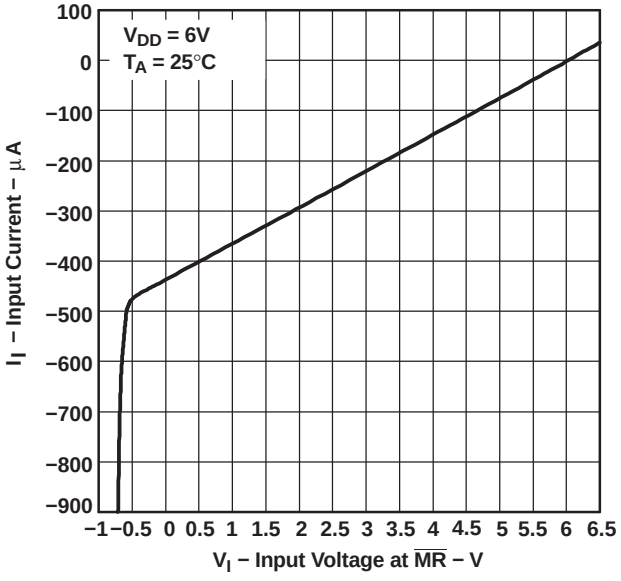


Figure 4.

MINIMUM PULSE DURATION AT SENSE vs THRESHOLD OVERDRIVE

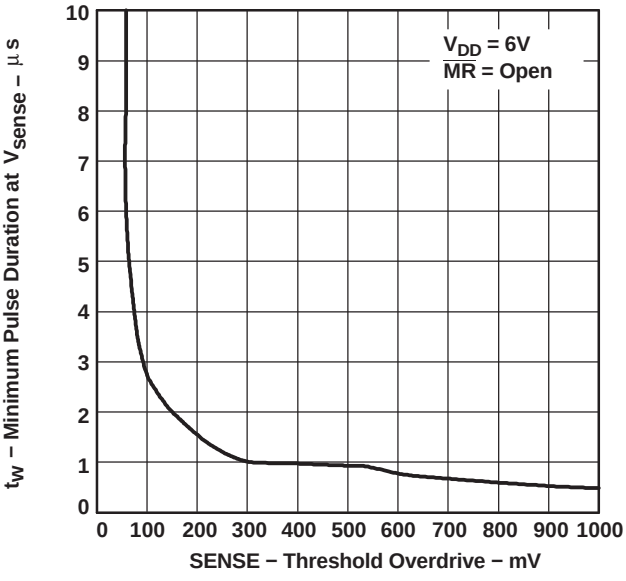


Figure 5.

Typical Characteristics (continued)

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

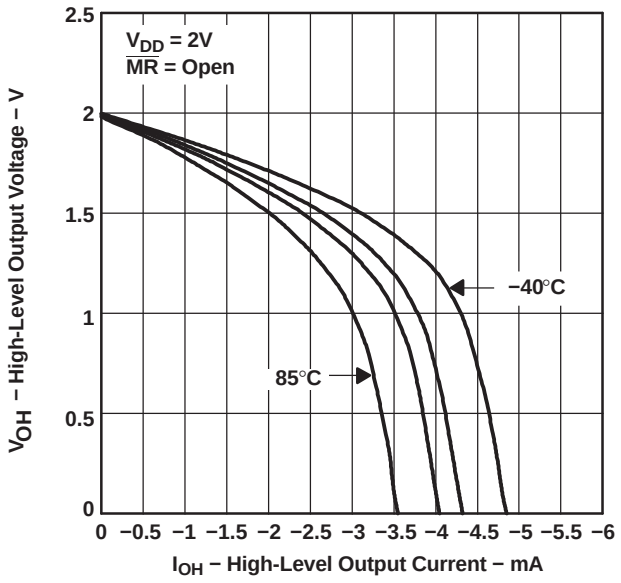


Figure 6.

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

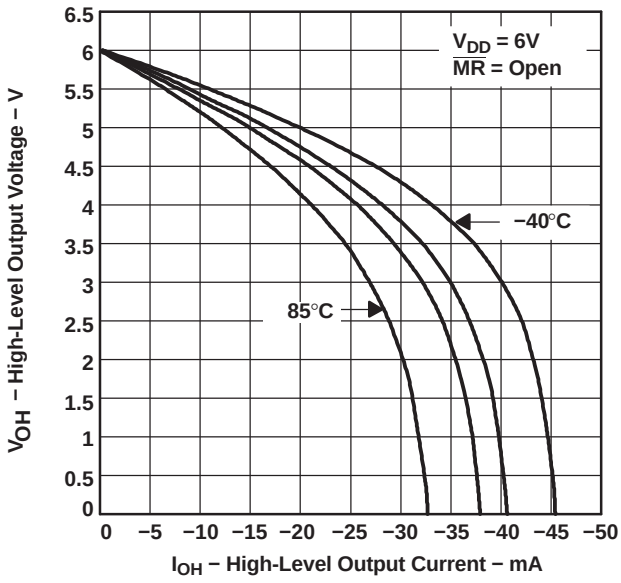


Figure 7.

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

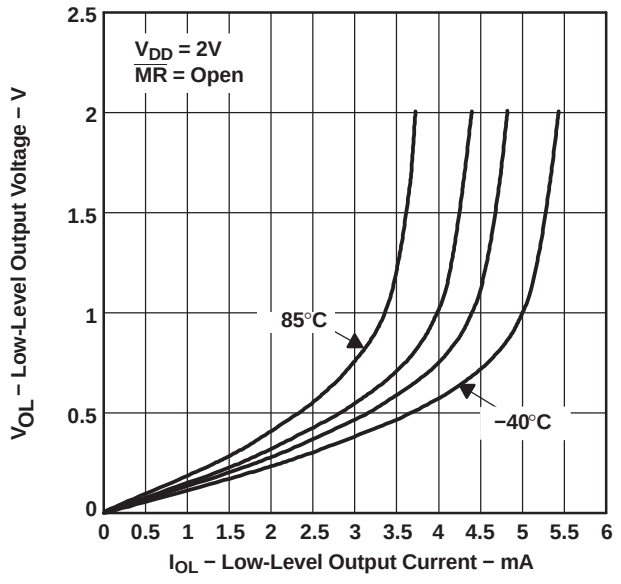


Figure 8.

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

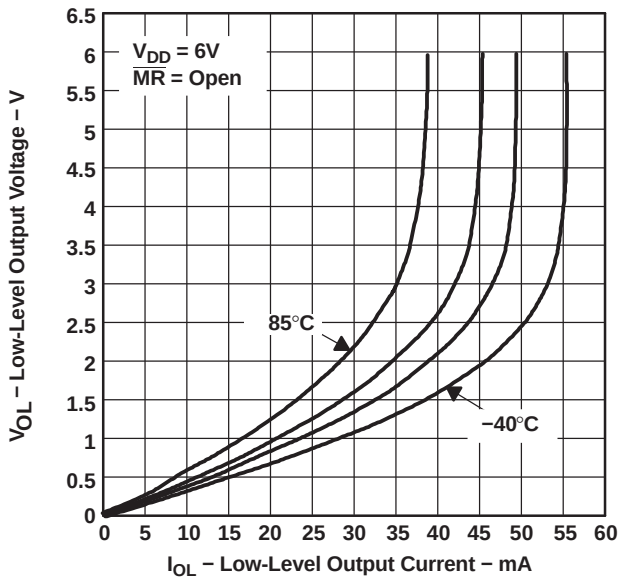


Figure 9.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS3307-18D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	30718	Samples
TPS3307-18DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	30718	Samples
TPS3307-18DGN	ACTIVE	HVSSOP	DGN	8	80	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AAP	Samples
TPS3307-18DGNG4	ACTIVE	HVSSOP	DGN	8	80	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AAP	Samples
TPS3307-18DGNR	ACTIVE	HVSSOP	DGN	8	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AAP	Samples
TPS3307-18DGNRG4	ACTIVE	HVSSOP	DGN	8	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AAP	Samples
TPS3307-18DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	30718	Samples
TPS3307-18DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	30718	Samples
TPS3307-25D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	30725	Samples
TPS3307-25DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	30725	Samples
TPS3307-25DGN	ACTIVE	HVSSOP	DGN	8	80	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AAQ	Samples
TPS3307-25DGNG4	ACTIVE	HVSSOP	DGN	8	80	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AAQ	Samples
TPS3307-25DGNR	ACTIVE	HVSSOP	DGN	8	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AAQ	Samples
TPS3307-25DGNRG4	ACTIVE	HVSSOP	DGN	8	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AAQ	Samples
TPS3307-25DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	30725	Samples
TPS3307-25DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	30725	Samples
TPS3307-33D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	30733	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS3307-33DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	30733	Samples
TPS3307-33DGN	ACTIVE	HVSSOP	DGN	8	80	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AAR	Samples
TPS3307-33DGNR	ACTIVE	HVSSOP	DGN	8	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AAR	Samples
TPS3307-33DGNRG4	ACTIVE	HVSSOP	DGN	8	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AAR	Samples
TPS3307-33DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	30733	Samples
TPS3307-33DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	30733	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF TPS3307 :

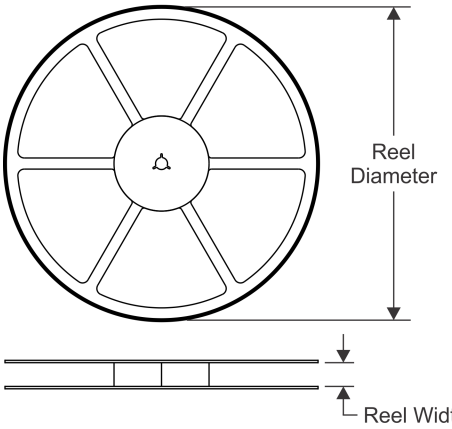
- Enhanced Product: TPS3307-EP

NOTE: Qualified Version Definitions:

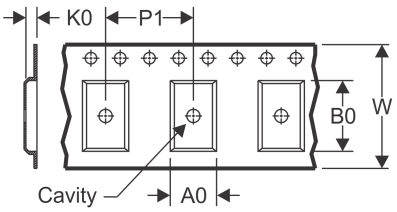
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

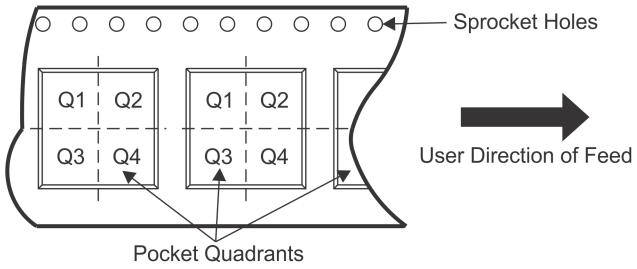


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

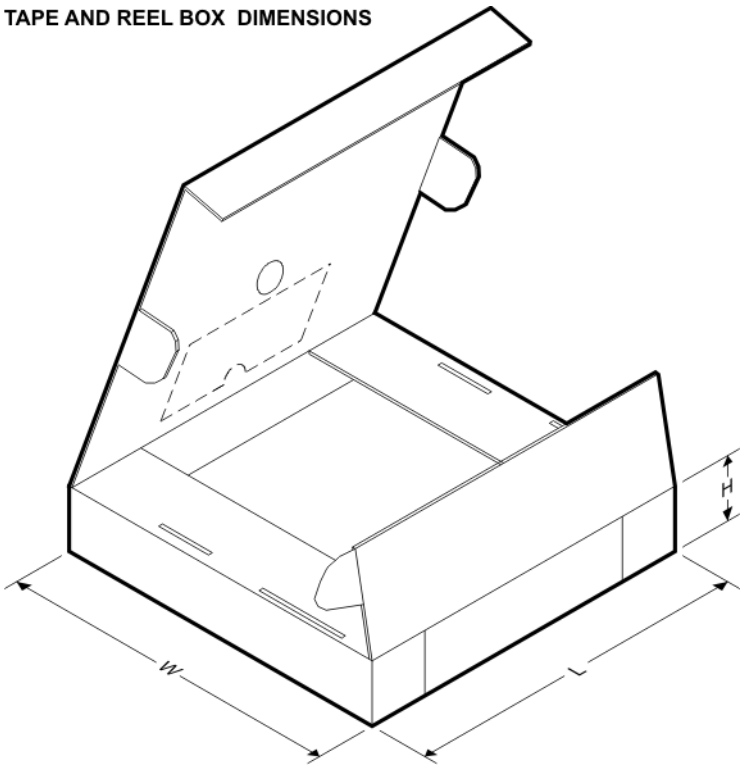
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

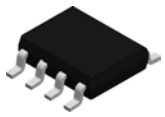
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS3307-18DGNR	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS3307-18DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TPS3307-25DGNR	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS3307-25DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TPS3307-33DGNR	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS3307-33DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS3307-18DGNR	HVSSOP	DGN	8	2500	358.0	335.0	35.0
TPS3307-18DR	SOIC	D	8	2500	350.0	350.0	43.0
TPS3307-25DGNR	HVSSOP	DGN	8	2500	358.0	335.0	35.0
TPS3307-25DR	SOIC	D	8	2500	350.0	350.0	43.0
TPS3307-33DGNR	HVSSOP	DGN	8	2500	358.0	335.0	35.0
TPS3307-33DR	SOIC	D	8	2500	350.0	350.0	43.0

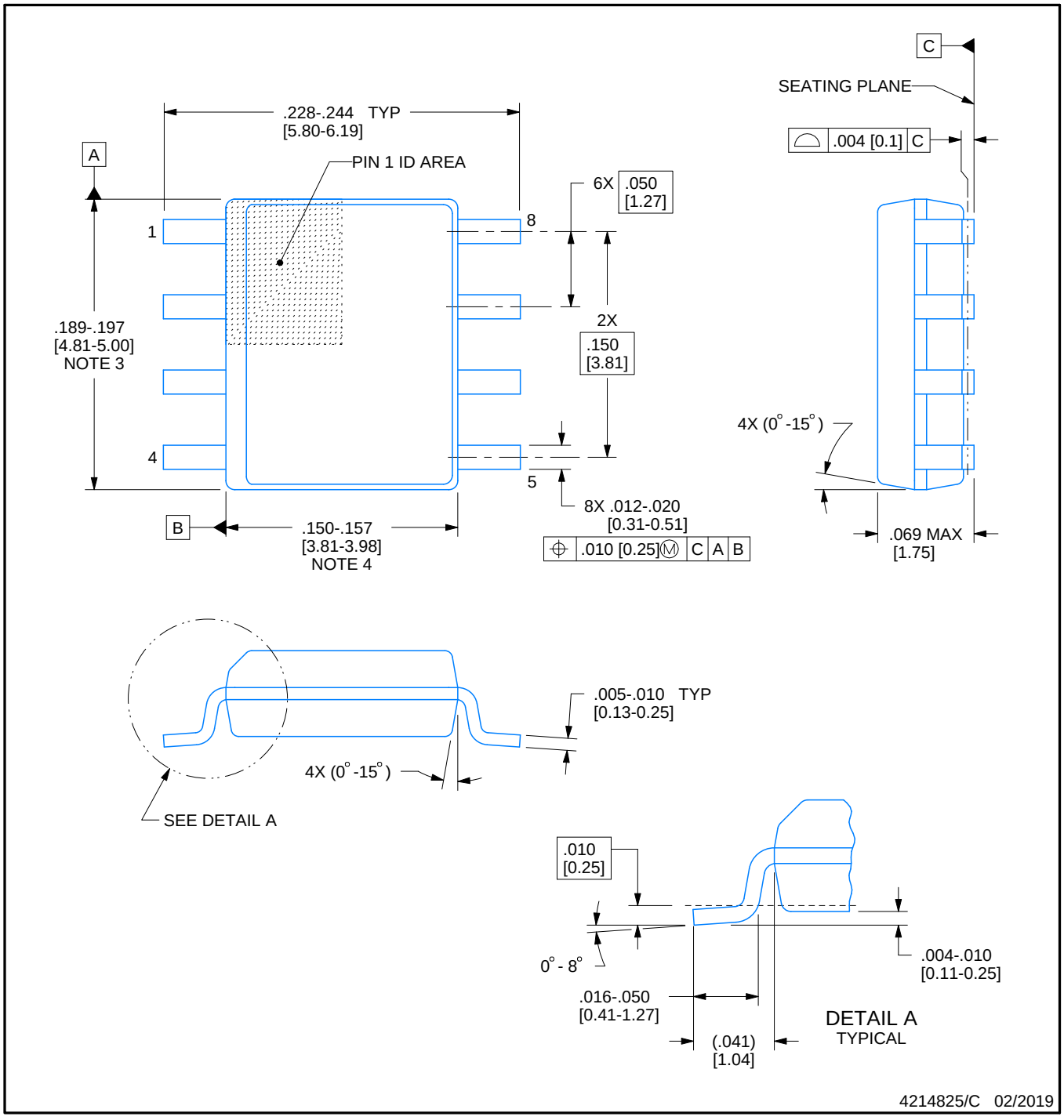


PACKAGE OUTLINE

D0008A

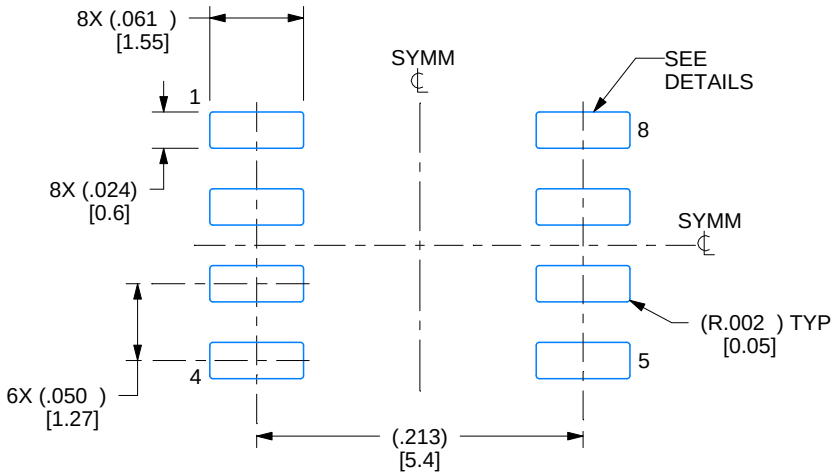
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

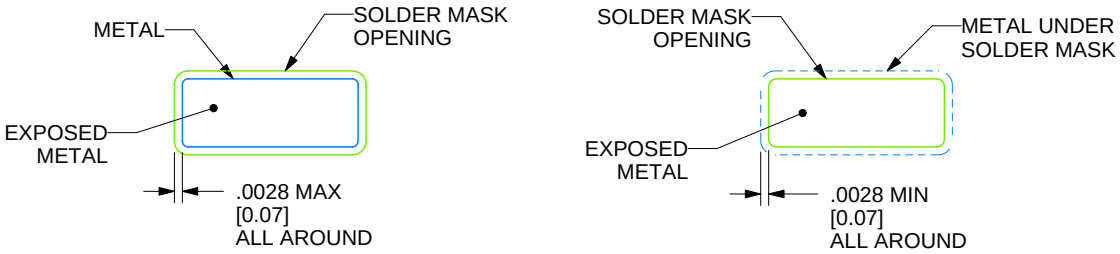


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

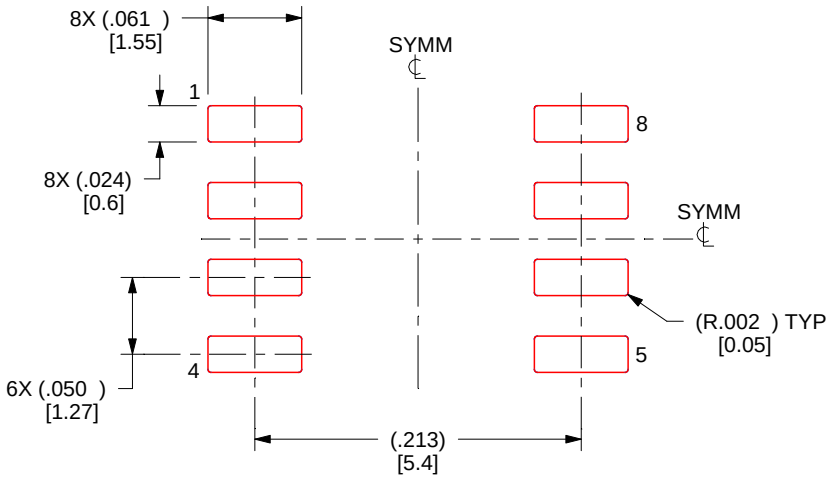
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



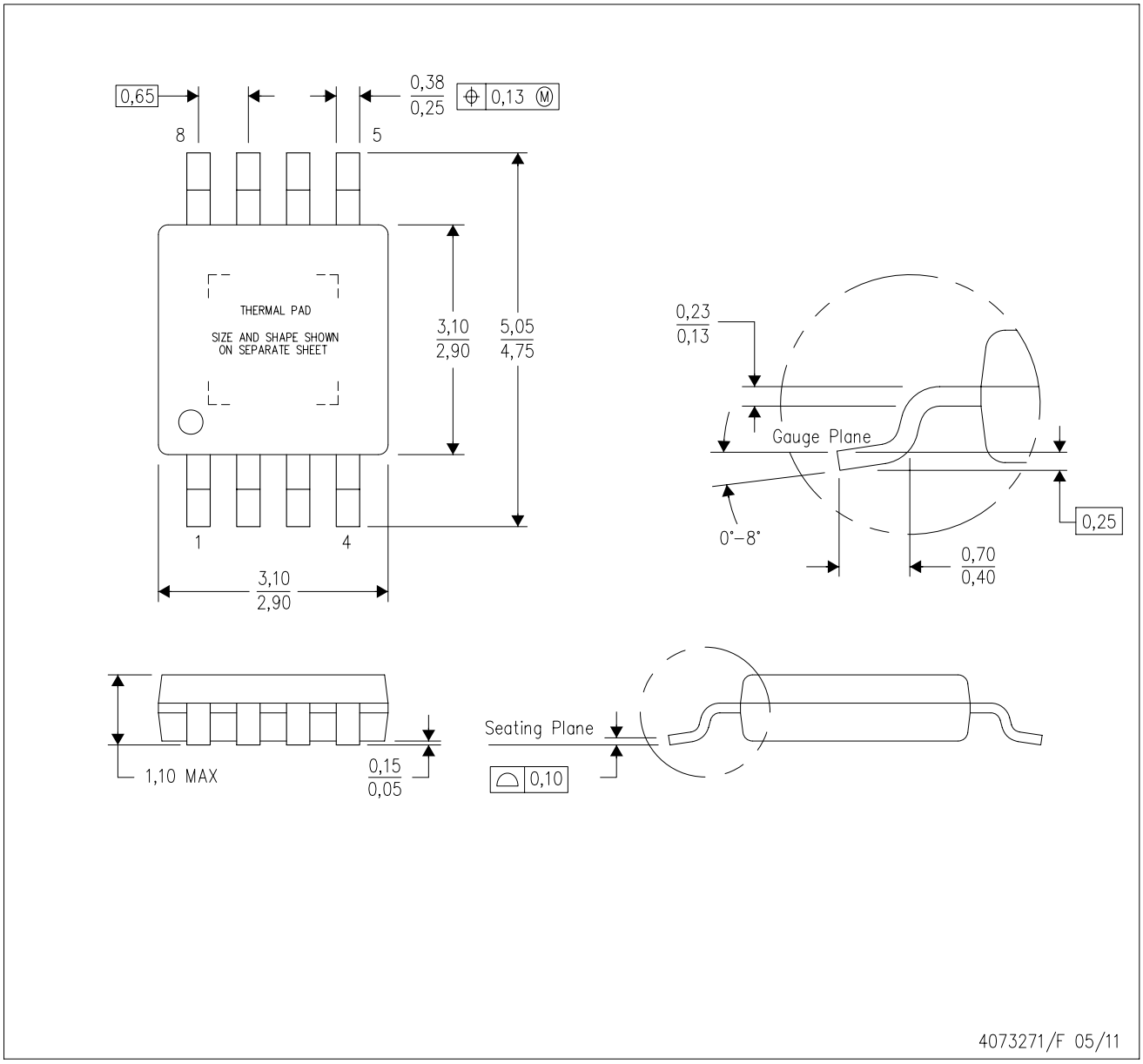
SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DGN (S–PDSO–G8) PowerPAD™ PLASTIC SMALL OUTLINE

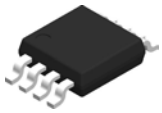


NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–187 variation AA–T

PowerPAD is a trademark of Texas Instruments.

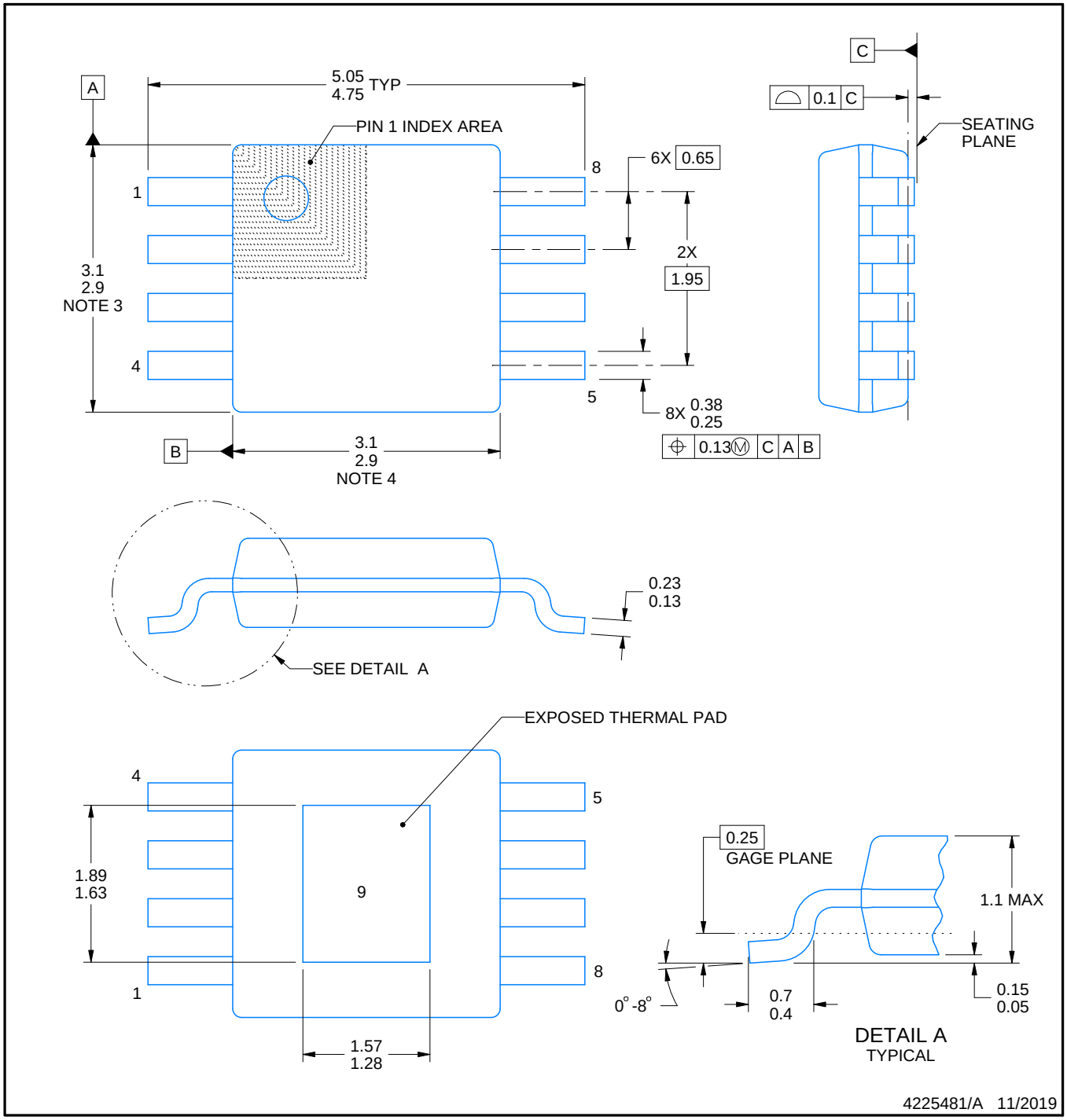
PACKAGE OUTLINE

DGN0008D



PowerPAD™ VSSOP - 1.1 mm max height

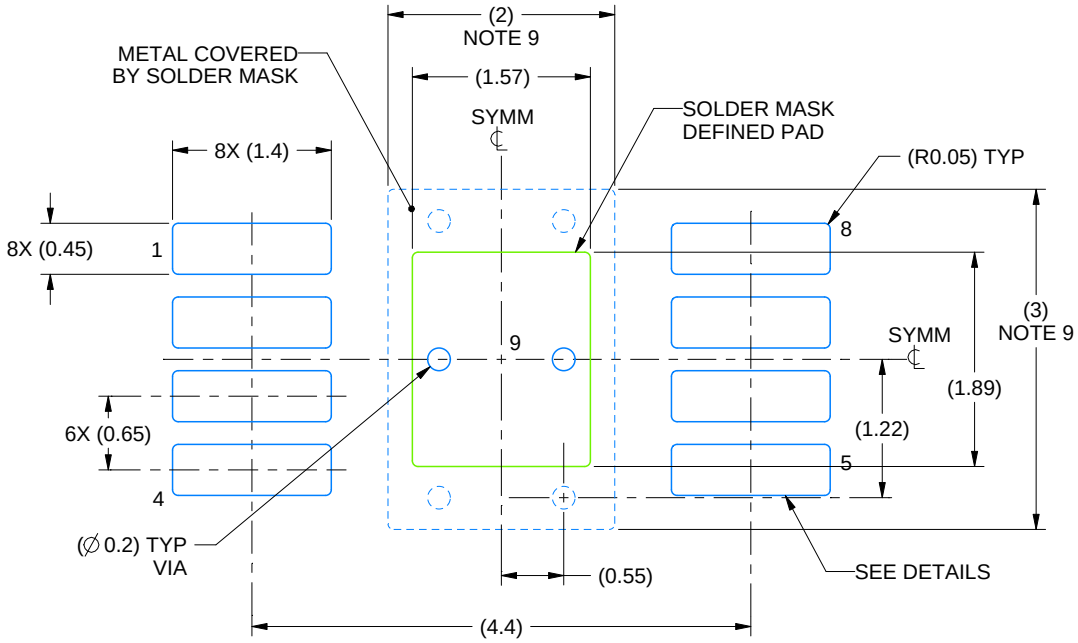
SMALL OUTLINE PACKAGE



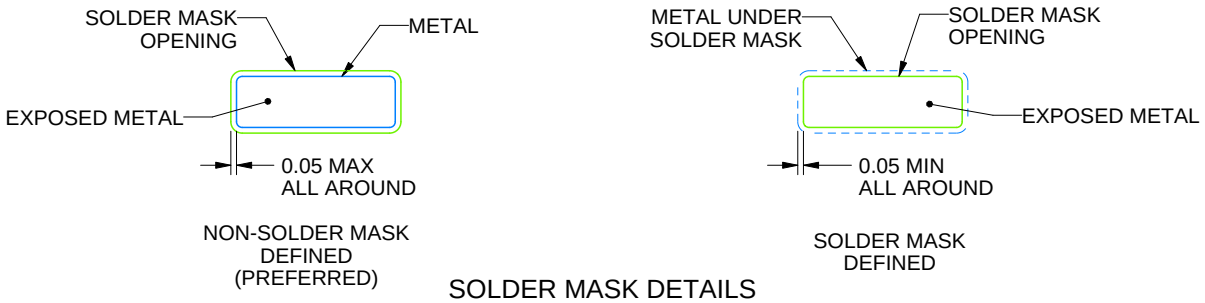
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

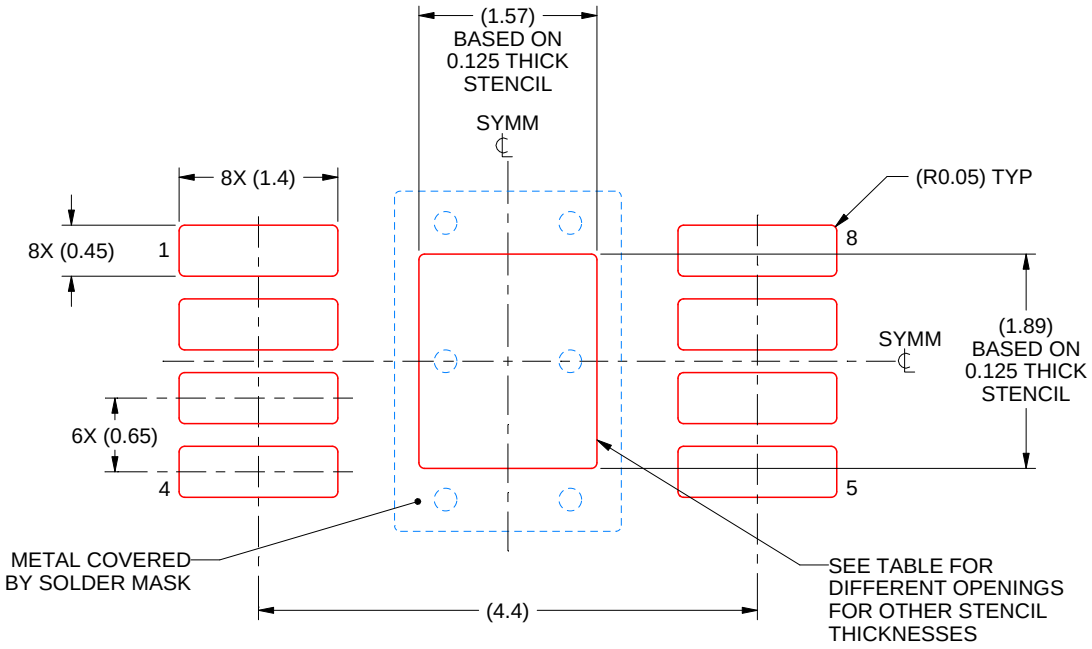


SOLDER MASK DETAILS

4225481/A 11/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD 9:
100% PRINTED SOLDER COVERAGE BY AREA
SCALE: 15X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	1.76 X 2.11
0.125	1.57 X 1.89 (SHOWN)
0.15	1.43 X 1.73
0.175	1.33 X 1.60

4225481/A 11/2019

NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

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