Document Number: MW7IC915N
Rev. 2, 12/2013

RoHS

# RF LDMOS Wideband Integrated Power Amplifier

**MW7IC915NT1**

**728–960 MHz, 1.6 W AVG., 28 V
SINGLE W-CDMA
RF LDMOS WIDEBAND
INTEGRATED POWER AMPLIFIER**



**PQFN 8 × 8
PLASTIC**

The MW7IC915N wideband integrated circuit is designed with on-chip matching that makes it usable from 698 to 960 MHz. This multi-stage structure is rated for 26 to 32 volt operation and covers all typical cellular base station modulation formats.

**Driver Application — 900 MHz**

- Typical Single-Carrier W-CDMA Performance: $V_{DD}$ = 28 Volts, $I_{DQ1}$ = 52 mA, $I_{DQ2}$ = 134 mA, $P_{out}$ = 1.6 Watts Avg., IQ Magnitude Clipping, Channel Bandwidth = 3.84 MHz, Input Signal PAR = 7.5 dB @ 0.01% Probability on CCDF.

| Frequency | $G_{ps}$ (dB) | PAE (%) | ACPR (dBc) |
|---|---|---|---|
| 865 MHz | 37.9 | 17.1 | -50.4 |
| 880 MHz | 38.0 | 17.4 | -50.6 |
| 895 MHz | 37.8 | 17.5 | -51.3 |

- Capable of Handling 10:1 VSWR, @ 32 Vdc, 880 MHz, $P_{out}$ = 23.5 Watts CW (3 dB Input Overdrive from Rated $P_{out}$)
- Stable into a 5:1 VSWR. All Spurs Below -60 dBc @ 30 to 41.5 dBm CW $P_{out}$.
- Typical $P_{out}$ @ 1 dB Compression Point ≃ 15.5 Watts CW

**Driver Application — 700 MHz**

- Typical Single-Carrier W-CDMA Performance: $V_{DD}$ = 28 Volts, $I_{DQ1}$ = 50 mA, $I_{DQ2}$ = 144 mA, $P_{out}$ = 1.6 Watts Avg., IQ Magnitude Clipping, Channel Bandwidth = 3.84 MHz, Input Signal PAR = 7.5 dB @ 0.01% Probability on CCDF.

| Frequency | $G_{ps}$ (dB) | PAE (%) | ACPR (dBc) |
|---|---|---|---|
| 728 MHz | 37.8 | 17.2 | -49.5 |
| 748 MHz | 37.8 | 17.3 | -50.5 |
| 768 MHz | 37.7 | 17.3 | -51.4 |

**Features**

- Characterized with Series Equivalent Large-Signal Impedance Parameters and Common Source S-Parameters
- On-Chip Matching (50 Ohm Input, DC Blocked)
- Integrated Quiescent Current Temperature Compensation with Enable/Disable Function (1)
- Integrated ESD Protection
- In Tape and Reel. T1 Suffix = 1,000 Units, 16 mm Tape Width, 13-inch Reel.

1. Refer to AN1977, *Quiescent Current Thermal Tracking Circuit in the RF Integrated Circuit Family* and to AN1987, *Quiescent Current Control for the RF Integrated Circuit Device Family*. Go to http://www.freescale.com/rf. Select Documentation/Application Notes - AN1977 or AN1987.

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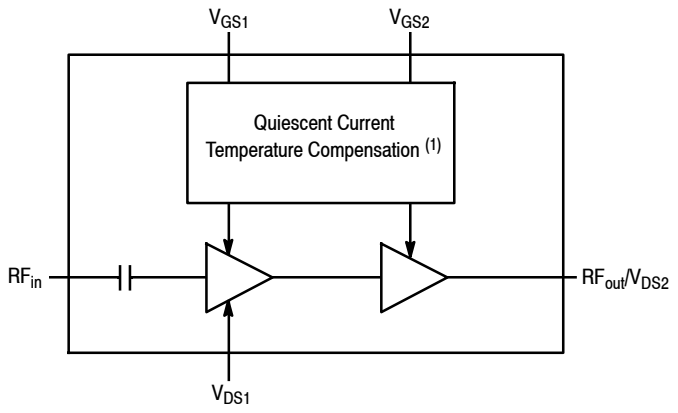



**Figure 1. Functional Block Diagram**

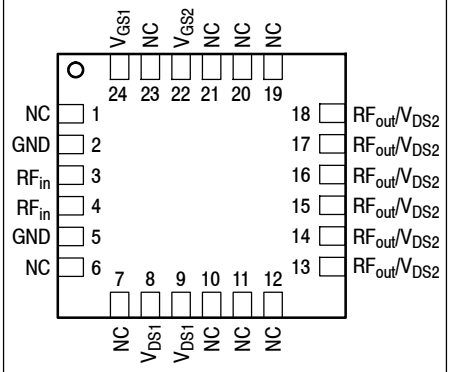



**Figure 2. Pin Connections**

1. Refer to AN1977, *Quiescent Current Thermal Tracking Circuit in the RF Integrated Circuit Family* and to AN1987, *Quiescent Current Control for the RF Integrated Circuit Device Family*. Go to http://www.freescale.com/rf. Select Documentation/Application Notes - AN1977 or AN1987.

**Table 1. Maximum Ratings**

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain-Source Voltage | $V_{DSS}$ | -0.5, +65 | Vdc |
| Gate-Source Voltage | $V_{GS}$ | -6.0, +10 | Vdc |
| Operating Voltage | $V_{DD}$ | 32, +0 | Vdc |
| Storage Temperature Range | $T_{stg}$ | -65 to +150 | °C |
| Operating Junction Temperature (1) | $T_J$ | 150 | °C |
| Input Power | $P_{in}$ | 17 | dBm |

**Table 2. Thermal Characteristics**

| Characteristic | | Symbol | Value (1,2) | Unit |
|---|---|---|---|---|
| Thermal Resistance, Junction to Case | | $R_{\theta JC}$ | | °C/W |
| W-CDMA Application | Stage 1, 28 Vdc, $I_{DQ1}$ = 60 mA | | 7.5 | |
| (Case Temperature 82°C, $P_{out}$ = 1.6 W CW) | Stage 2, 28 Vdc, $I_{DQ2}$ = 130 mA | | 3.2 | |

**Table 3. ESD Protection Characteristics**

| Test Methodology | Class |
|---|---|
| Human Body Model (per JESD22-A114) | 1B |
| Machine Model (per EIA/JESD22-A115) | A |
| Charge Device Model (per JESD22-C101) | III |

**Table 4. Moisture Sensitivity Level**

| Test Methodology | Rating | Package Peak Temperature | Unit |
|---|---|---|---|
| Per JESD22-A113, IPC/JEDEC J-STD-020 | 3 | 260 | °C |

1. MTTF calculator available at http://www.freescale.com/rf. Select Software & Tools/Development Tools/Calculators to access MTTF calculators by product.
2. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers.* Go to http://www.freescale.com/rf. Select Documentation/Application Notes - AN1955.

**Table 5. Electrical Characteristics** ($T_A$ = 25°C unless otherwise noted)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **Stage 1 — Off Characteristics** | | | | | |
| Zero Gate Voltage Drain Leakage Current ($V_{DS}$ = 65 Vdc, $V_{GS}$ = 0 Vdc) | $I_{DSS}$ | — | — | 10 | μAdc |
| Zero Gate Voltage Drain Leakage Current ($V_{DS}$ = 28 Vdc, $V_{GS}$ = 0 Vdc) | $I_{DSS}$ | — | — | 1 | μAdc |
| Gate-Source Leakage Current ($V_{GS}$ = 1.5 Vdc, $V_{DS}$ = 0 Vdc) | $I_{GSS}$ | — | — | 1 | μAdc |
| **Stage 1 — On Characteristics** | | | | | |
| Gate Threshold Voltage ($V_{DS}$ = 10 Vdc, $I_D$ = 9 μAdc) | $V_{GS(th)}$ | 1 | 2 | 3 | Vdc |
| Gate Quiescent Voltage ($V_{DS}$ = 28 Vdc, $I_D$ = 52 mAdc) | $V_{GS(Q)}$ | — | 3 | — | Vdc |
| Fixture Gate Quiescent Voltage ($V_{DD}$ = 28 Vdc, $I_D$ = 52 mAdc, Measured in Functional Test) | $V_{GG(Q)}$ | 5.5 | 6.3 | 7 | Vdc |
| **Stage 2 — Off Characteristics** | | | | | |
| Zero Gate Voltage Drain Leakage Current ($V_{DS}$ = 65 Vdc, $V_{GS}$ = 0 Vdc) | $I_{DSS}$ | — | — | 10 | μAdc |
| Zero Gate Voltage Drain Leakage Current ($V_{DS}$ = 28 Vdc, $V_{GS}$ = 0 Vdc) | $I_{DSS}$ | — | — | 1 | μAdc |
| Gate-Source Leakage Current ($V_{GS}$ = 1.5 Vdc, $V_{DS}$ = 0 Vdc) | $I_{GSS}$ | — | — | 1 | μAdc |
| **Stage 2 — On Characteristics** | | | | | |
| Gate Threshold Voltage ($V_{DS}$ = 10 Vdc, $I_D$ = 36 μAdc) | $V_{GS(th)}$ | 1 | 2 | 3 | Vdc |
| Gate Quiescent Voltage ($V_{DS}$ = 28 Vdc, $I_D$ = 134 mAdc) | $V_{GS(Q)}$ | — | 2.9 | — | Vdc |
| Fixture Gate Quiescent Voltage ($V_{DD}$ = 28 Vdc, $I_D$ = 134 mAdc, Measured in Functional Test) | $V_{GG(Q)}$ | 3.8 | 4.6 | 5.3 | Vdc |
| Drain-Source On-Voltage ($V_{GS}$ = 10 Vdc, $I_D$ = 3.6 Adc) | $V_{DS(on)}$ | 0.1 | 0.3 | 0.8 | Vdc |

**Functional Tests** (1) (In Freescale Test Fixture, 50 ohm system) $V_{DD}$ = 28 Vdc, $I_{DQ1}$ = 52 mA, $I_{DQ2}$ = 134 mA, $P_{out}$ = 1.6 W Avg., f = 880 MHz, Single-Carrier W-CDMA, IQ Magnitude Clipping, Input Signal PAR = 7.5 dB @ 0.01% Probability on CCDF. ACPR measured in 3.84 MHz Channel Bandwidth @ ±5 MHz Offset.

| | | | | | |
|---|---|---|---|---|---|
| Power Gain | $G_{ps}$ | 35.0 | 38.0 | 41.0 | dB |
| Power Added Efficiency | PAE | 15.0 | 17.4 | — | % |
| Adjacent Channel Power Ratio | ACPR | — | -50.6 | -47.0 | dBc |
| Input Return Loss | IRL | — | -22 | -9 | dB |

**Typical Performance over Frequency** (In Freescale Test Fixture, 50 ohm system) $V_{DD}$ = 28 Vdc, $I_{DQ1}$ = 52 mA, $I_{DQ2}$ = 134 mA, $P_{out}$ = 1.6 W Avg., Single-Carrier W-CDMA, IQ Magnitude Clipping, Input Signal PAR = 7.5 dB @ 0.01% Probability on CCDF. ACPR measured in 3.84 MHz Channel Bandwidth @ ±5 MHz Offset.

| Frequency | $G_{ps}$ (dB) | PAE (%) | ACPR (dBc) | IRL (dB) |
|---|---|---|---|---|
| 865 MHz | 37.9 | 17.1 | -50.4 | -21 |
| 880 MHz | 38.0 | 17.4 | -50.6 | -22 |
| 895 MHz | 37.8 | 17.5 | -51.3 | -22 |

1. Part internally input matched.

(continued)

**Table 5. Electrical Characteristics** ($T_A$ = 25°C unless otherwise noted) **(continued)**

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **Typical Performances** (In Freescale Test Fixture, 50 ohm system) $V_{DD}$ = 28 Vdc, $I_{DQ1}$ = 52 mA, $I_{DQ2}$ = 134 mA, 865–895 MHz Bandwidth | | | | | |
| $P_{out}$ @ 1 dB Compression Point, CW ($V_{DD}$ = 28 Vdc, $I_{DQ1}$ = 75 mA, $I_{DQ2}$ = 100 mA) | P1dB | — | 15.5 | — | W |
| IMD Symmetry @ 16 W PEP, $P_{out}$ where IMD Third Order Intermodulation ≧ 30 dBc (Delta IMD Third Order Intermodulation between Upper and Lower Sidebands > 2 dB) | $IMD_{sym}$ | — | 45 | — | MHz |
| VBW Resonance Point (IMD Third Order Intermodulation Inflection Point) | $VBW_{res}$ | — | 180 | — | MHz |
| Quiescent Current Accuracy over Temperature [1] with 2 kΩ Gate Feed Resistors (–30 to 85°C) Stage 1<br>Stage 2 | $\Delta I_{QT}$ | —<br>— | 0.10<br>0.12 | —<br>— | % |
| Gain Flatness in 30 MHz Bandwidth @ $P_{out}$ = 1.6 W Avg. | $G_F$ | — | 0.1 | — | dB |
| Gain Variation over Temperature (–30°C to +85°C) | ΔG | — | 0.041 | — | dB/°C |
| Output Power Variation over Temperature (–30°C to +85°C) | ΔP1dB | — | 0.004 | — | dBm/°C |

**Typical Performance — 700 MHz** (In Freescale 700 MHz Test Fixture, 50 ohm system) $V_{DD}$ = 28 Vdc, $I_{DQ1}$ = 50 mA, $I_{DQ2}$ = 144 mA, $P_{out}$ = 1.6 W Avg., Single–Carrier W–CDMA, IQ Magnitude Clipping, Input Signal PAR = 7.5 dB @ 0.01% Probability on CCDF. ACPR measured in 3.84 MHz Channel Bandwidth @ ±5 MHz Offset.

| Frequency | $G_{ps}$ (dB) | PAE (%) | ACPR (dBc) | IRL (dB) |
|---|---|---|---|---|
| 728 MHz | 37.8 | 17.2 | –49.5 | –23 |
| 748 MHz | 37.8 | 17.3 | –50.5 | –22 |
| 768 MHz | 37.7 | 17.3 | –51.4 | –22 |

1. Refer to AN1977, *Quiescent Current Thermal Tracking Circuit in the RF Integrated Circuit Family* and to AN1987, *Quiescent Current Control for the RF Integrated Circuit Device Family*. Go to http://www.freescale.com/rf. Select Documentation/Application Notes – AN1977 or AN1987.

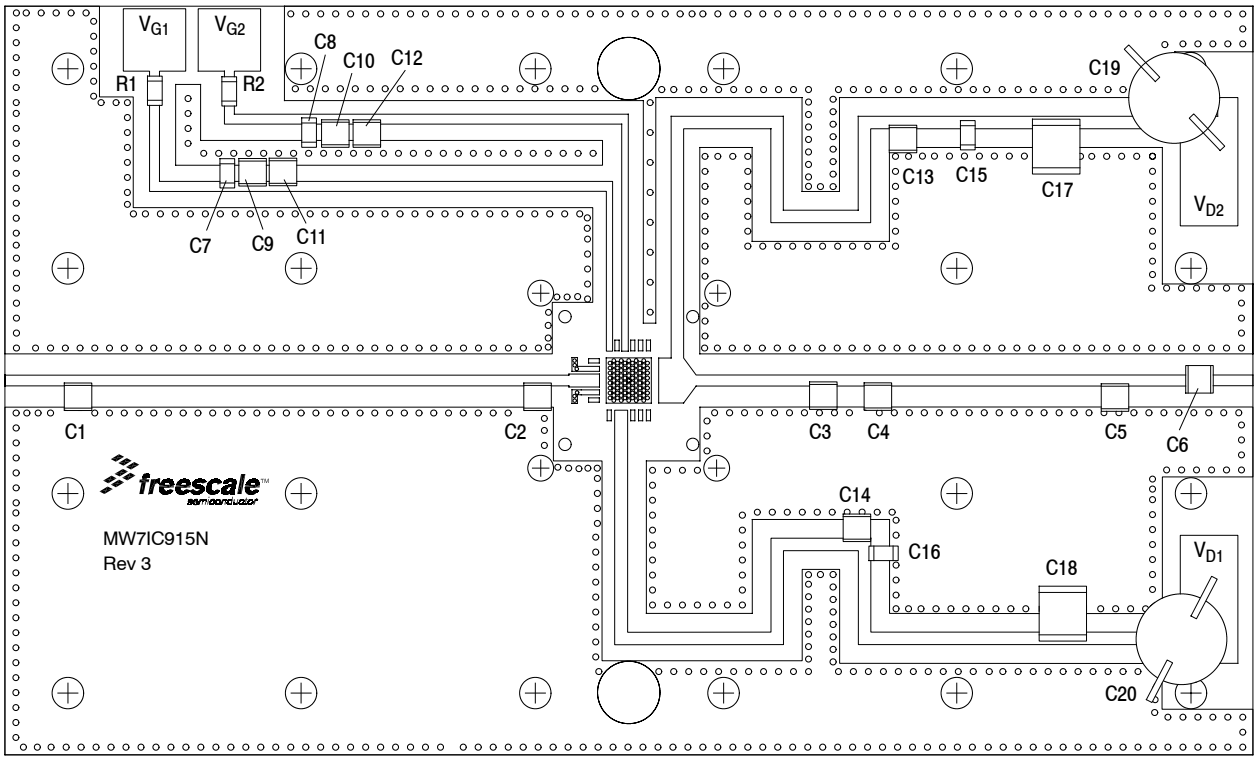



**Figure 3. MW7IC915NT1 Test Circuit Component Layout**

**Table 6. MW7IC915NT1 Test Circuit Component Designations and Values**

| Part | Description | Part Number | Manufacturer |
|---|---|---|---|
| C1 | 1.8 pF Chip Capacitor | ATC100B1R8BT500XT | ATC |
| C2, C5 | 0.8 pF Chip Capacitors | ATC100B0R8BT500XT | ATC |
| C3 | 6.2 pF Chip Capacitor | ATC100B6R2BT500XT | ATC |
| C4 | 3.3 pF Chip Capacitor | ATC100B3R3CT500XT | ATC |
| C6, C11, C12, C13, C14 | 47 pF Chip Capacitors | ATC100B470JT500XT | ATC |
| C7, C8 | 1 μF Chip Capacitors | GRM31MR71H105KA88L | Murata |
| C9, C10 | 0.1 μF Chip Capacitors | GRM32MR71H104JA01L | Murata |
| C15, C16 | 4.7 μF Chip Capacitors | GRM31CR71H475KA12L | Murata |
| C17, C18 | 10 μF, 50 V Chip Capacitors | GRM55DR61H106KA88L | Murata |
| C19, C20 | 100 μF, 50 V Electrolytic Capacitors | MCGPR50V107M8X11-RH | Multicomp |
| R1, R2 | 2 kΩ, 1/4 W Resistors | CRCW12062K00FKEA | Vishay |
| PCB | 0.020″, $\varepsilon_r$ = 3.66 | RO4350B | Rogers |

## TYPICAL CHARACTERISTICS

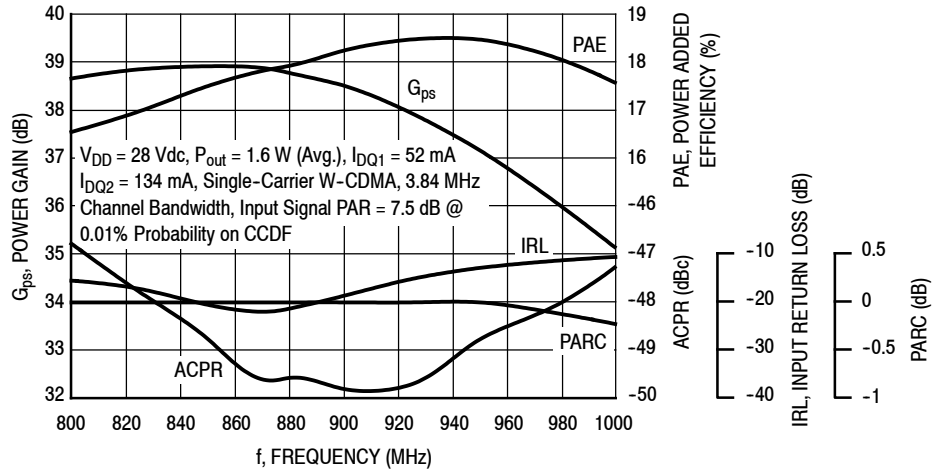



**Figure 4. Output Peak-to-Average Ratio Compression (PARC) Broadband Performance @ $P_{out}$ = 1.6 Watts Avg.**

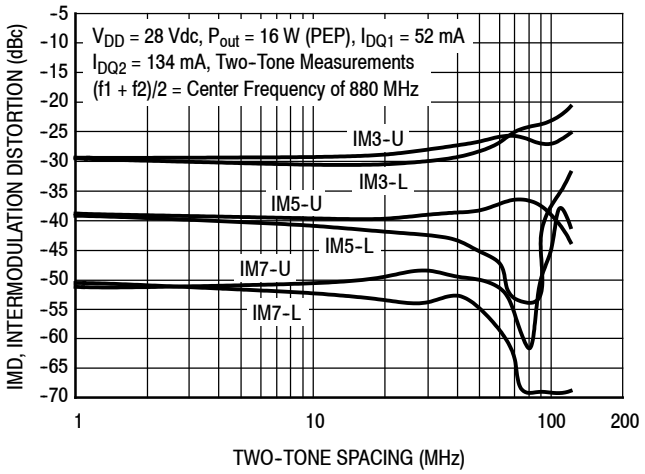



**Figure 5. Intermodulation Distortion Products versus Two-Tone Spacing**

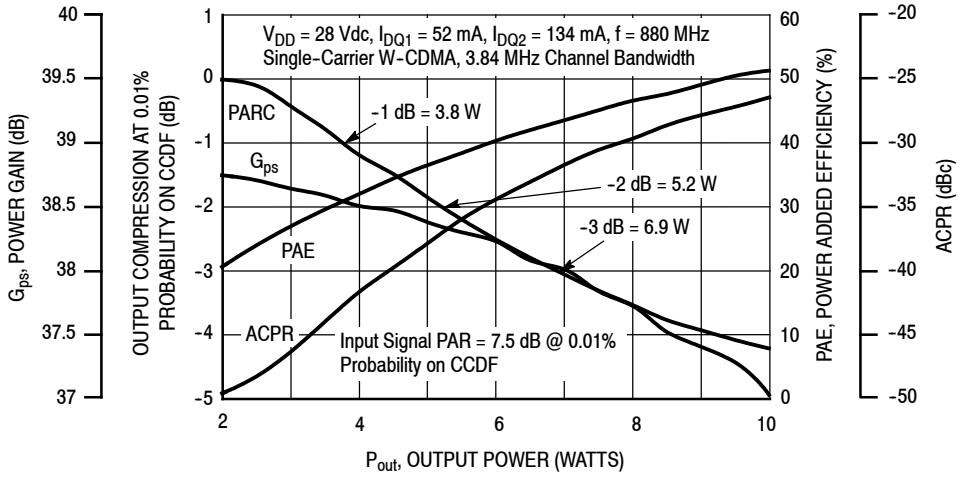



**Figure 6. Output Peak-to-Average Ratio Compression (PARC) versus Output Power**

## TYPICAL CHARACTERISTICS

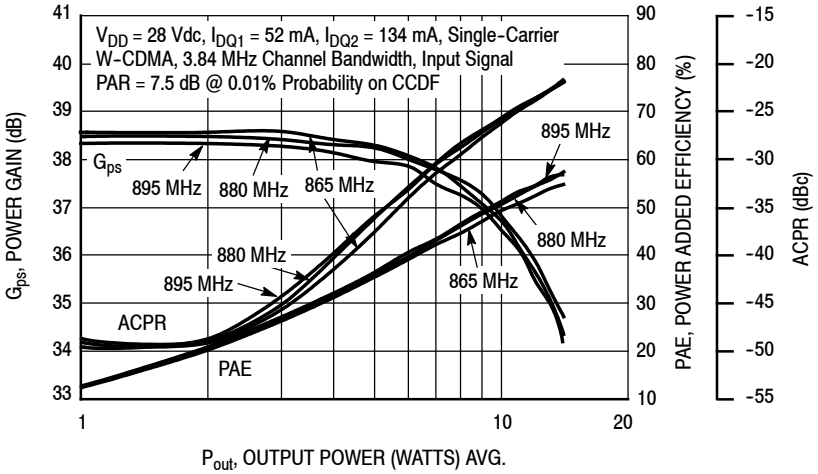



**Figure 7. Single-Carrier W-CDMA Power Gain, Power Added Efficiency and ACPR versus Output Power**

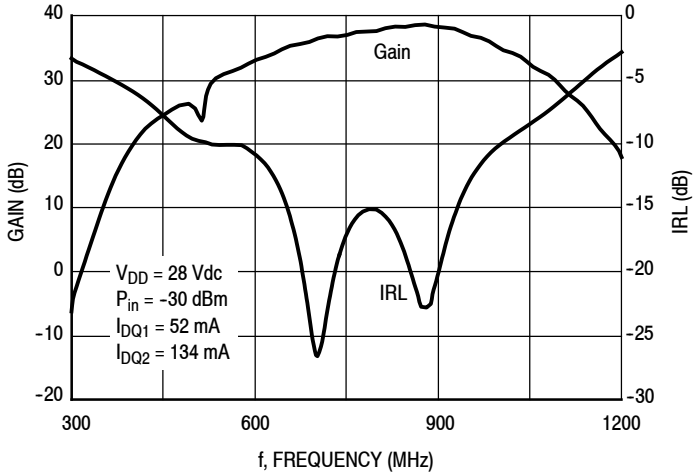



**Figure 8. Broadband Frequency Response**

## W-CDMA TEST SIGNAL

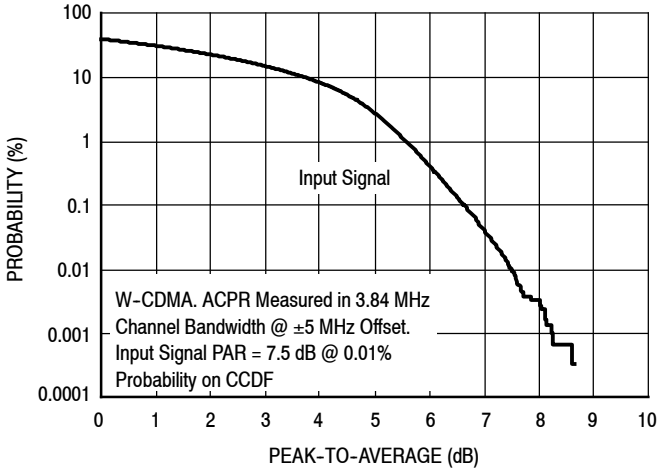



**Figure 9. CCDF W-CDMA IQ Magnitude Clipping, Single-Carrier Test Signal**

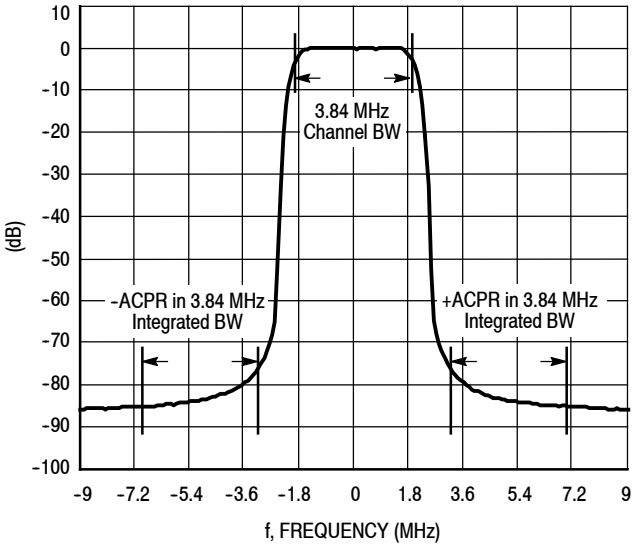



**Figure 10. Single-Carrier W-CDMA Spectrum**

$V_{DD}$ = 28 Vdc, $I_{DQ1}$ = 52 mA, $I_{DQ2}$ = 134 mA, $P_{out}$ = 1.6 W Avg.

| f<br>MHz | $Z_{in}$<br>Ω | $Z_{load}$<br>Ω |
|---|---|---|
| 820 | 52.99 – j29.47 | 7.72 + j13.96 |
| 840 | 49.35 – j27.56 | 7.34 + j14.74 |
| 860 | 46.67 – j23.60 | 7.43 + j15.55 |
| 880 | 44.88 – j17.63 | 7.94 + j16.07 |
| 900 | 43.73 – j10.46 | 7.98 + j16.74 |
| 920 | 43.12 – j2.75 | 7.80 + j17.62 |
| 940 | 43.38 + j5.01 | 8.28 + j18.33 |
| 960 | 44.07 + j12.97 | 9.07 + j19.04 |
| 980 | 43.89 + j12.61 | 9.14 + j20.02 |

$Z_{in}$ = Device input impedance as measured from gate to ground.

$Z_{load}$ = Test circuit impedance as measured from drain to ground.

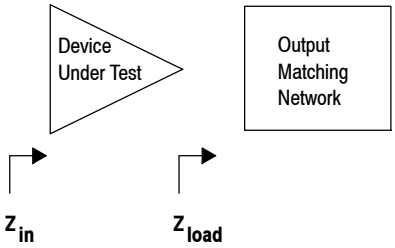
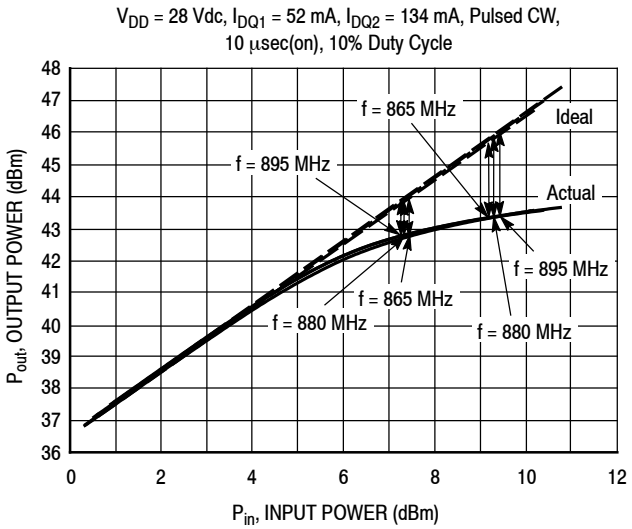



**Figure 11. Series Equivalent Input and Load Impedance**

## ALTERNATIVE PEAK TUNE LOAD PULL CHARACTERISTICS




NOTE: Load Pull Test Fixture Tuned for Peak P1dB Output Power @ 28 V

| f (MHz) | P1dB | | P3dB | |
|---|---|---|---|---|
| | Watts | dBm | Watts | dBm |
| 865 | 18.1 | 42.6 | 22.4 | 43.5 |
| 880 | 18.5 | 42.7 | 22.3 | 43.5 |
| 895 | 18.5 | 42.7 | 22.2 | 43.5 |

Test Impedances per Compression Level

| f (MHz) | | $Z_{source}$ Ω | $Z_{load}$ Ω |
|---|---|---|---|
| 865 | P1dB | 48.7 + j15.6 | 6.8 + j6.5 |
| 880 | P1dB | 52.3 + j20.8 | 6.9 + j6.7 |
| 895 | P1dB | 55.1 + j22.2 | 7.4 + j6.7 |

**Figure 12. Pulsed CW Output Power versus Input Power @ 28 V**

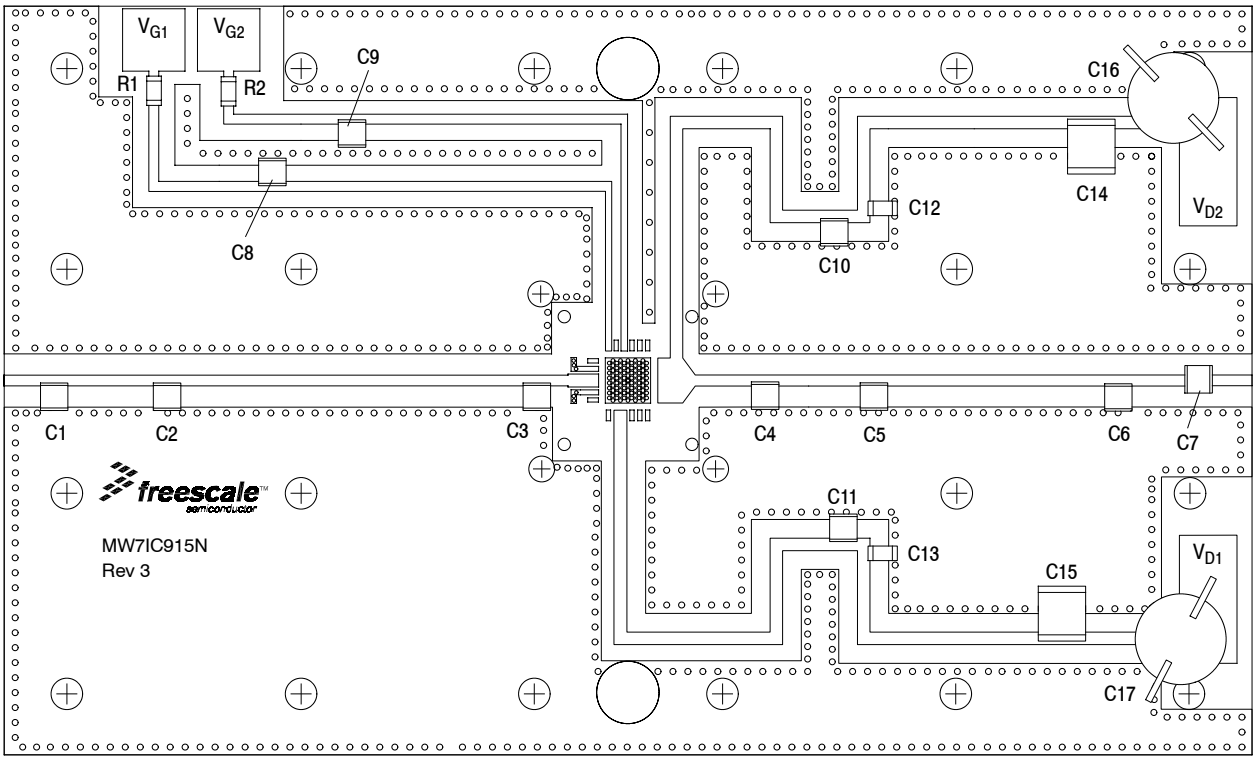



**Figure 13. MW7IC915NT1 Test Circuit Component Layout — 700 MHz**

**Table 7. MW7IC915NT1 Test Circuit Component Designations and Values — 700 MHz**

| Part | Description | Part Number | Manufacturer |
|---|---|---|---|
| C1, C3, C6 | 2.7 pF Chip Capacitors | ATC100B2R7BT500XT | ATC |
| C2 | 0.3 pF Chip Capacitor | ATC100B0R3BT500XT | ATC |
| C4 | 4.7 pF Chip Capacitor | ATC100B4R7CT500XT | ATC |
| C5 | 5.6 pF Chip Capacitor | ATC100B5R6CT500XT | ATC |
| C7, C8, C9, C10, C11 | 47 pF Chip Capacitors | ATC100B470JT500XT | ATC |
| C12, C13 | 4.7 μF Chip Capacitors | GRM31CR71H475KA12L | Murata |
| C14, C15 | 10 μF, 50 V Chip Capacitors | GRM55DR61H106KA88L | Murata |
| C16, C17 | 100 μF, 50 V Electrolytic Capacitors | MCGPR50V107M8X11-RH | Multicomp |
| R1, R2 | 2 kΩ, 1/4 W Resistors | CRCW12062K00FKEA | Vishay |
| PCB | 0.020″, $\varepsilon_r$ = 3.66 | RO4350B | Rogers |

## TYPICAL CHARACTERISTICS — 700 MHz

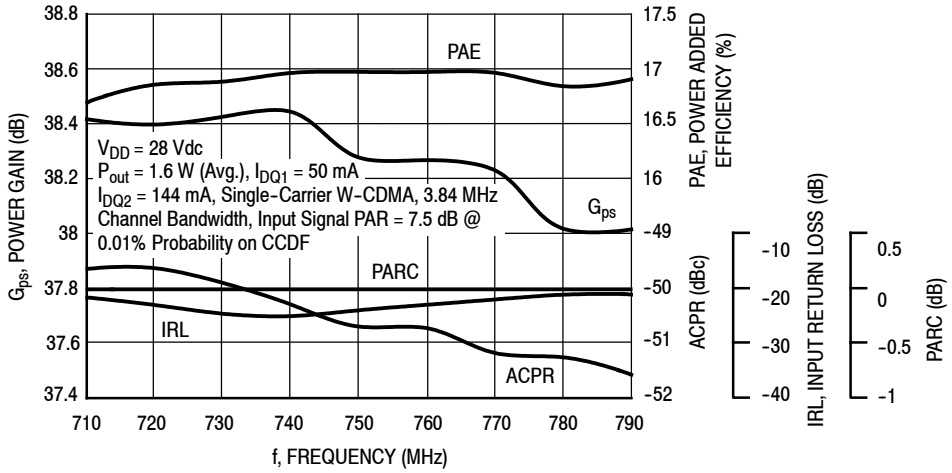



**Figure 14. Output Peak-to-Average Ratio Compression (PARC) Broadband Performance @ $P_{out}$ = 1.6 Watts Avg.**

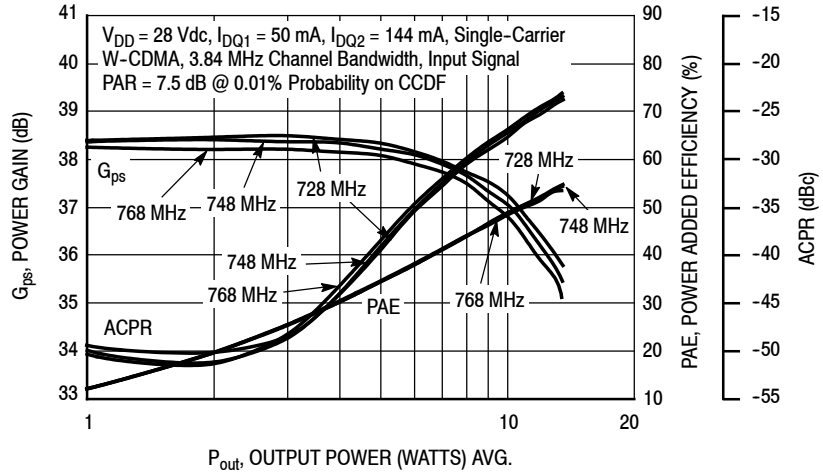



**Figure 15. Single-Carrier W-CDMA Power Gain, Power Added Efficiency and ACPR versus Output Power**

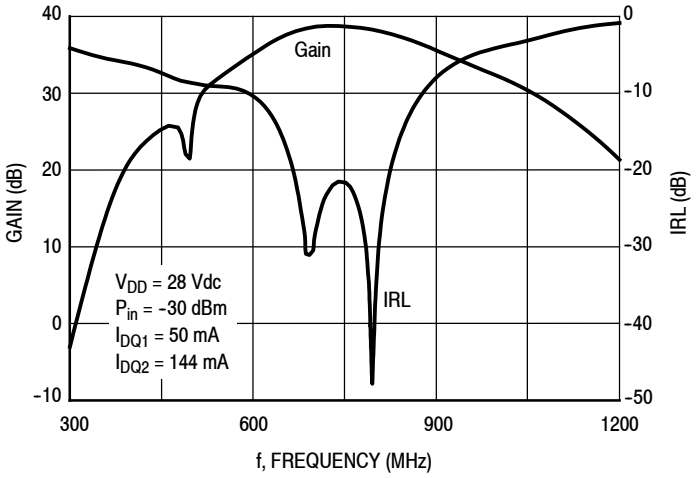



**Figure 16. Broadband Frequency Response**

$V_{DD}$ = 28 Vdc, $I_{DQ1}$ = 50 mA, $I_{DQ2}$ = 144 mA, $P_{out}$ = 1.6 W Avg.

| f<br>MHz | $Z_{in}$<br>Ω | $Z_{load}$<br>Ω |
|---|---|---|
| 710 | 54.61 – j2.01 | 9.57 + j6.52 |
| 720 | 55.46 + j0.26 | 9.95 + j7.04 |
| 730 | 56.75 + j2.12 | 10.70 + j7.79 |
| 740 | 58.35 + j3.55 | 11.39 + j8.18 |
| 750 | 60.11 + j4.65 | 11.41 + j8.07 |
| 760 | 61.83 + j5.22 | 11.00 + j7.90 |
| 770 | 63.19 + j5.31 | 10.88 + j7.88 |
| 780 | 64.01 + j4.90 | 11.41 + j7.87 |
| 790 | 64.18 + j3.91 | 12.32 + j7.61 |

$Z_{in}$ = Device input impedance as measured from gate to ground.

$Z_{load}$ = Test circuit impedance as measured from drain to ground.

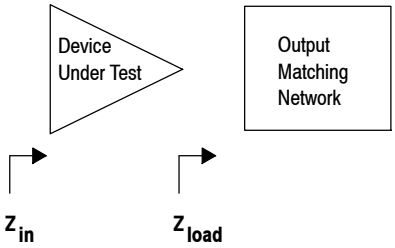
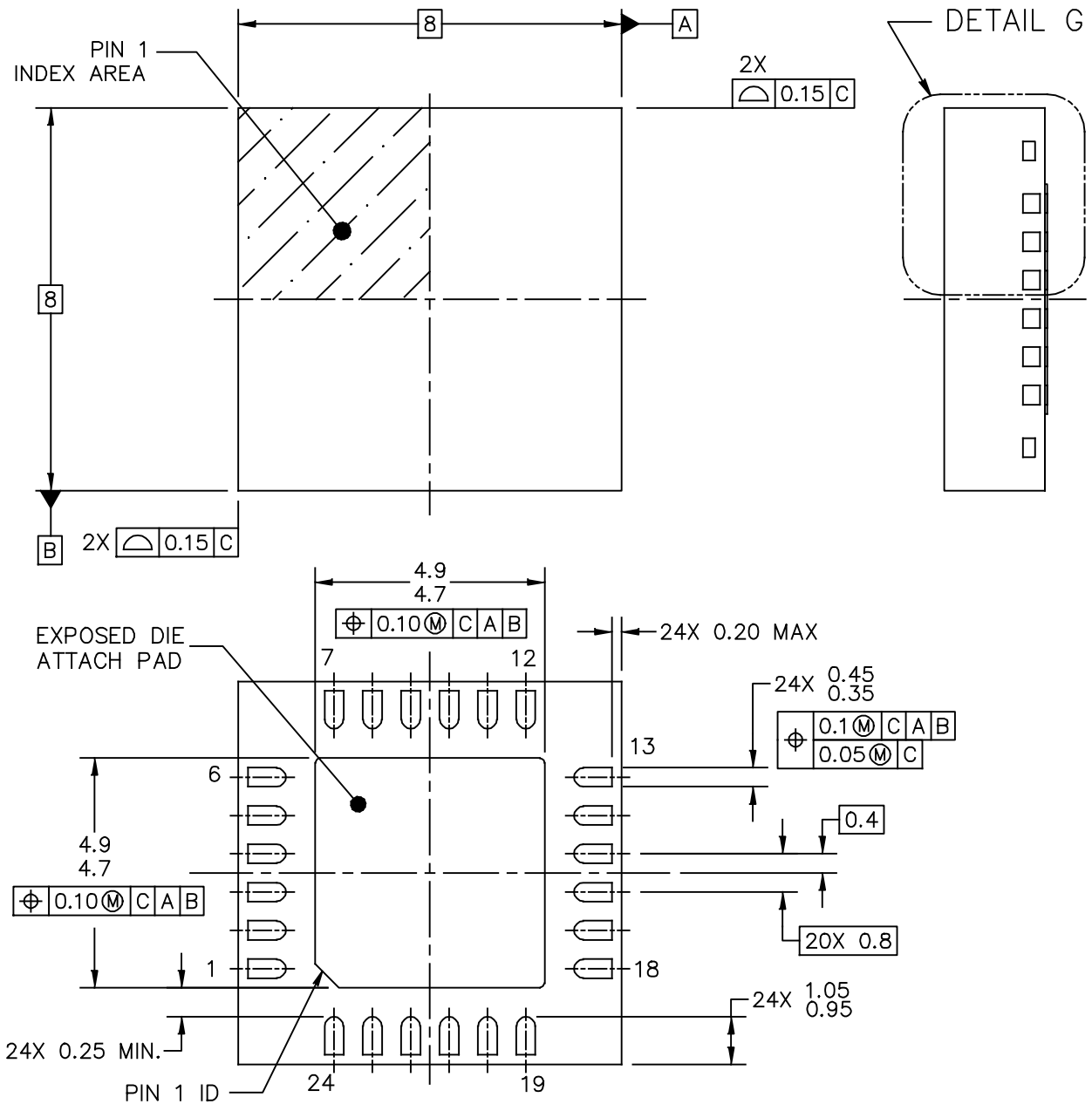
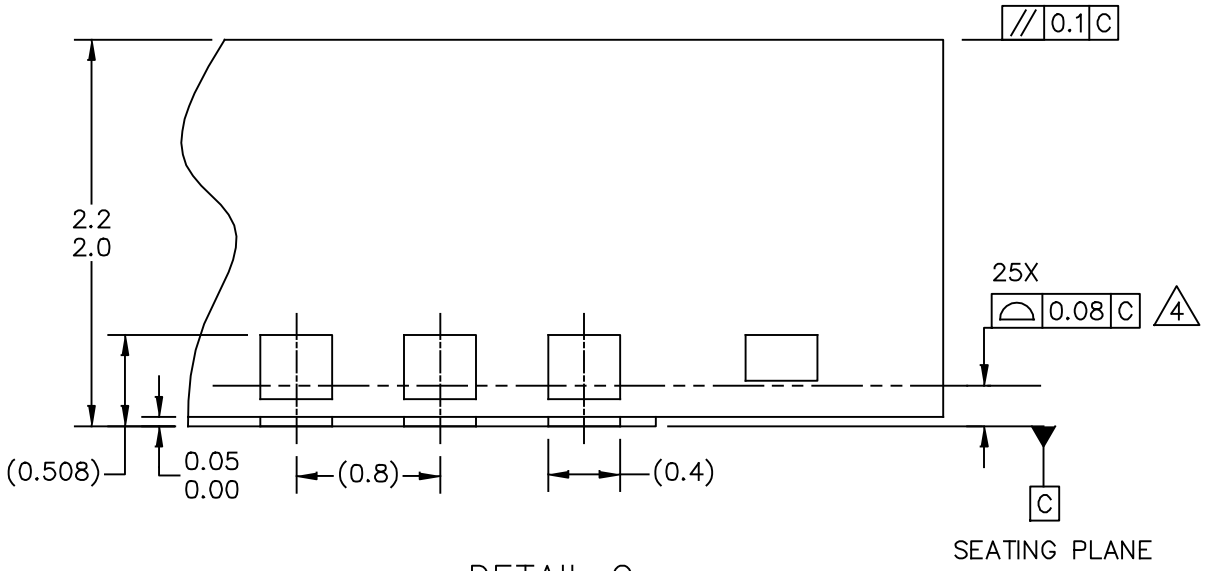



**Figure 17. Series Equivalent Input and Load Impedance — 700 MHz**

## PACKAGE DIMENSIONS




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|---|---|---|
| TITLE: PQFN (SAW), THERMALLY ENHANCED 8 X 8 X 2.1, 0.8 PITCH, 24 TERMINAL | DOCUMENT NO: 98ASA10760D | REV: A |
| | CASE NUMBER: 1894-02 | 29 MAY 2012 |
| | STANDARD: NON-JEDEC | |




DETAIL G
VIEW ROTATED 90° CW

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NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. THE COMPLETE JEDEC DESIGNATOR FOR THIS PACKAGE IS: HF–PQFN.
4. COPLANARITY APPLIES TO LEADS AND DIE ATTACH PAD.

| | | |
|---|---|---|
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## PRODUCT DOCUMENTATION, TOOLS AND SOFTWARE

Refer to the following documents to aid your design process.

**Application Notes**

- AN1955: Thermal Measurement Methodology of RF Power Amplifiers
- AN1977: Quiescent Current Thermal Tracking Circuit in the RF Integrated Circuit Family
- AN1987: Quiescent Current Control for the RF Integrated Circuit Device Family

**Engineering Bulletins**

- EB212: Using Data Sheet Impedances for RF LDMOS Devices

**Software**

- Electromigration MTTF Calculator
- RF High Power Model
- .s2p File

For Software and Tools, do a Part Number search at http://www.freescale.com, and select the “Part Number” link. Go to the Software & Tools tab on the part’s Product Summary page to download the respective tool.

## REVISION HISTORY

The following table summarizes revisions to this document.

| Revision | Date | Description |
|---|---|---|
| 0 | Sept. 2009 | • Initial Release of Data Sheet |
| 1 | Dec. 2009 | • Table 4, Moisture Sensitivity Level, corrected Package Peak Temperature to 260°C, p. 2 |
| 2 | Dec. 2013 | • Table 1, Maximum Ratings: increased input power from 4.7 dBm to 17 dBm to reflect the true capability of the device, p. 2<br>• Table 3, ESD Protection Characteristics, removed the word “Minimum” after the ESD class rating. ESD ratings are characterized during new product development but are not 100% tested during production. ESD ratings provided in the data sheet are intended to be used as a guideline when handling ESD sensitive devices, p. 2<br>• Table 6, Test Circuit Component Designations and Values: corrected C9, C10 chip capacitor description from 0.01 to 0.1 pF, p. 5. Table 6 (900 MHz component designations) and Table 7 (700 MHz component designations): added PCB material information, pp. 5, 10<br>• Replaced Case Outline 98ASA10760D, Rev. O with Rev. A, pp. 13–15. Mechanical outline drawing modified to reflect the correct lead end features. Format of the mechanical outline was also updated to the current Freescale format for Freescale mechanical outlines. |

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