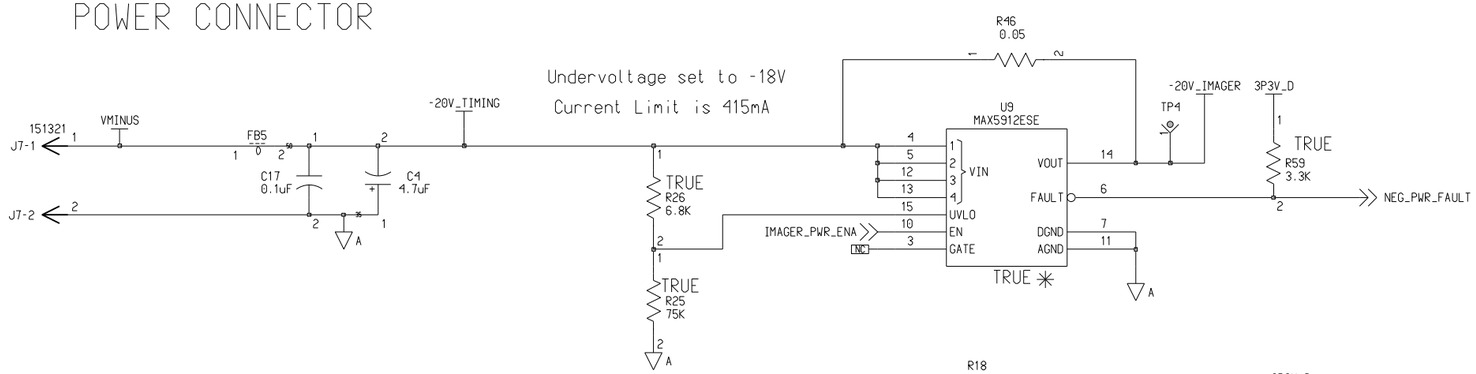
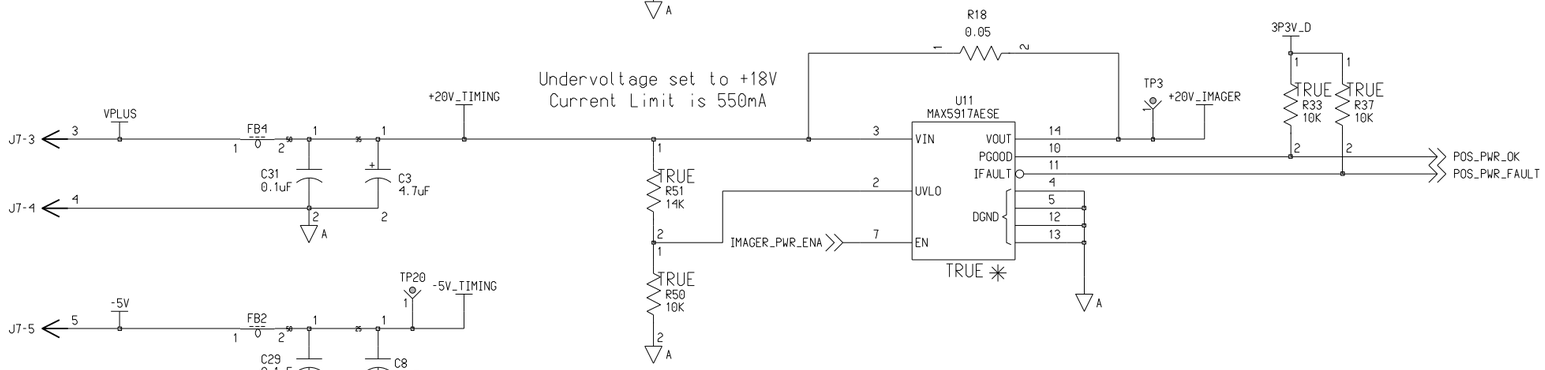
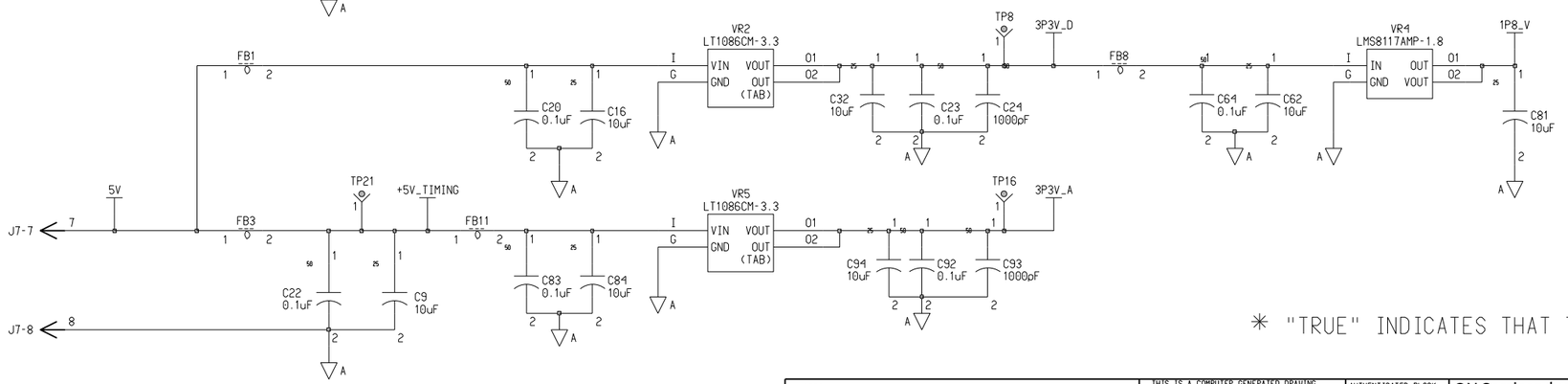
POWER CONNECTOR

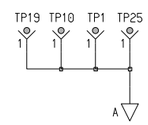


Zero Current Fault (< 8mA)
Power Not Good Fault
Undervoltage Fault (> -18V)
Thermal Fault (> 140 C)

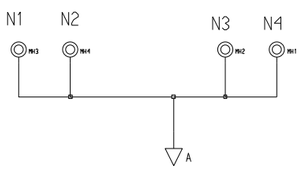


Power Not Good Fault
Zero Current Fault (< 6mA)
Undervoltage Fault (< +18V)
Thermal Fault (> 140 C)





✳ "TRUE" INDICATES THAT THIS COMPONENT IS NOT POPULATED



BOARD MOUNTING HOLES

NOTES:					
			THIS IS A COMPUTER GENERATED DRAWING. IT IS OFFICIAL WHEN THE AUTHENTICATED BLOCK IS FILLED IN. THE MASTER COPY IS AUTHENTICATED IN RED.	AUTHENTICATED BLOCK	
CHG NO DATE RLSE	REVISIONS	DWN BY APPV'D	CHG NO DATE RLSE	REVISIONS	DWN BY APPV'D

ON Semiconductor

DWN R. BROLLY	DATE 06.24.2005 at 11:05
DFTG NONE	DSGN ENGR R. BROLLY
CHK NONE	MFG ENGR NONE
ORIG CHG NO PS-0132	

FIRST USED ON EVALUATION BOARD SYSTEM

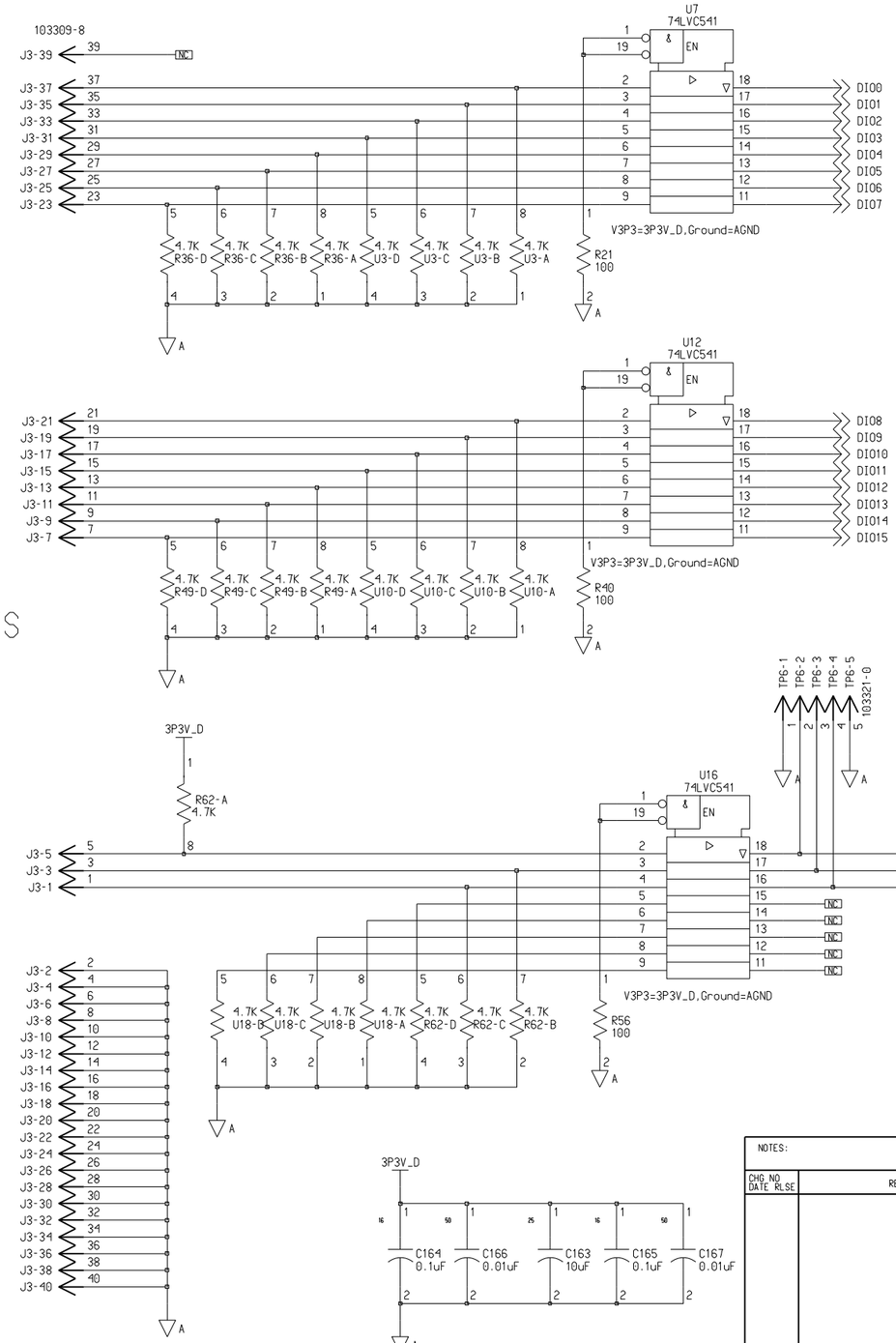
NAME AD9945 TIMING BOARD

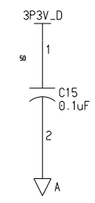
SKETCH NO. 1 DWG. SIZE D

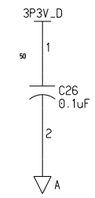
NO. 3F5592 REV1

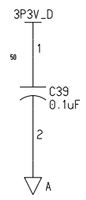
SHEET 1 OF 12

DIO INPUTS



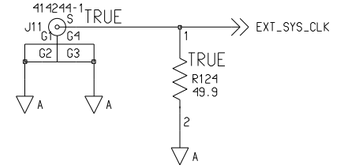




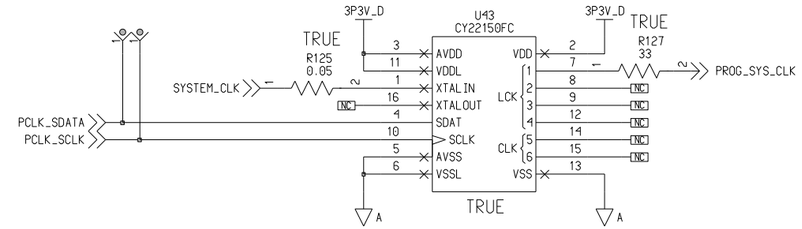


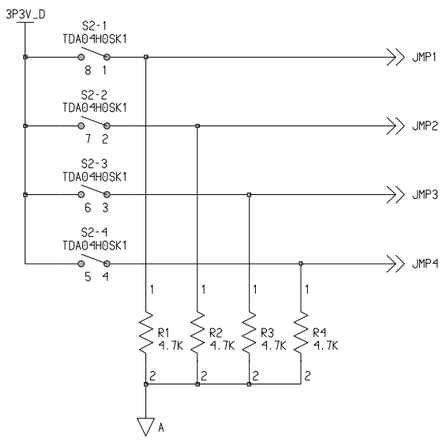
DECOUPLING CAPS

EXTERNAL SYSTEM CLOCK INPUT



PROGRAMMABLE SYSTEM CLOCK





SWITCH INPUTS

NOTES:

THIS IS A COMPUTER GENERATED DRAWING. IT IS OFFICIAL WHEN THE AUTHENTICATED BLOCK IS FILLED IN. THE MASTER COPY IS AUTHENTICATED IN RED.

AUTHENTICATED BLOCK

CHG NO DATE RLSE	REVISIONS	DWN BY APPV'D	CHG NO DATE RLSE	REVISIONS	DWN BY APPV'D

ON Semiconductor

DWN R. BROLLY	DATE 06.24.2005 at 11:07
DFTG NONE	DSGN ENGR R. BROLLY
CHK NONE	MFG ENGR NONE
ORIG CHG NO	

FIRST USED ON EVALUATION BOARD SYSTEM

NAME

AD9945 TIMING BOARD

SKETCH NO. | DWG SIZE D

NO.

3F5592 REV1

SHEET 2 OF 12

SCHEMATIC CONNECTIONS FOR FPGA PINS
MADE BY AUTO-FPGA TOOL

BOARD_RESET
SYSTEM_CLK
INTEGRATE_CLK

SDATA_INPUT
SCLOCK_INPUT
SLOAD_INPUT

JMP4
JMP3
JMP2
JMP1
DIO0
DIO1
DIO2
DIO3
DIO4
DIO5
DIO6
DIO7
DIO8
DIO9
DIO10
DIO11
DIO12
DIO13
DIO14
DIO15

POS_PWR_FAULT
POS_PWR_OK
NEG_PWR_FAULT
SCLOCK
SDATA
SLOAD_AFE_1
SLOAD_AFE_2
SLOAD_DAC
SLOAD_TG

PLD_OUT0
PLD_OUT1
PLD_OUT2
PLD_OUT3
PLD_OUT4
PLD_OUT5
PLD_OUT6
PLD_OUT7
PLD_OUT8
PLD_OUT9
PLD_OUT10
PLD_OUT11
PLD_OUT12
PLD_OUT13
PLD_OUT14

SYSTEM_CLK_TG
VD_TG
HD_TG

IMAGER_PWR_ENA
ARSTN_TG
DAC_RESET
INTEGRATE_SYNC
LED_ON

LINE_VALID_PLD
FRAME_VALID_PLD

PIXCLK_TG
INT_START_TG
AMP_ENA_TG
V6_TG
FRAME_VALID_TG
LINE_VALID_TG
V5_TG
V1_TG
V2_TG
V3_TG
V4_TG

FPGA I/O BLOCKS

U15-2
EPF10K30AFC256-IO2
V3P3=3P3V_D,Ground=AGND

U15-1
EPF10K30AFC256-IO1
V3P3=3P3V_D,Ground=AGND

FPGA POWER

U15-5
EPF10K30AFC256-POWER
VCCIO (2.5V/ 3.3V)
V3P3=3P3V_D,Ground=AGND

FPGA CONFIGURATION

U4
EPC2LC20
EPROM

U15-4
EPF10K30AFC256-JTAG
V3P3=3P3V_D,Ground=AGND

U15-3
EPF10K30AFC256-CONFIG
V3P3=3P3V_D,Ground=AGND

103309-1

TP5

NOTES:

THIS IS A COMPUTER GENERATED DRAWING. IT IS OFFICIAL WHEN THE AUTHENTICATED BLOCK IS FILLED IN. THE MASTER COPY IS AUTHENTICATED IN RED.

AUTHENTICATED BLOCK

CHG NO DATE RLSE	REVISIONS	DWN BY APPV'D

CHG NO DATE RLSE	REVISIONS	DWN BY APPV'D

ON Semiconductor

DWN R. BROLLY	DATE 06.24.2005 at 11:09
DFTG NONE	DSGN ENGR R. BROLLY
CHK NONE	MFG ENGR NONE
ORIG CHG NO	

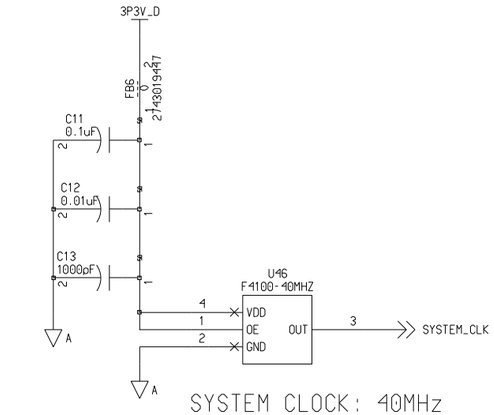
FIRST USED ON

NAME
AD9945 TIMING BOARD

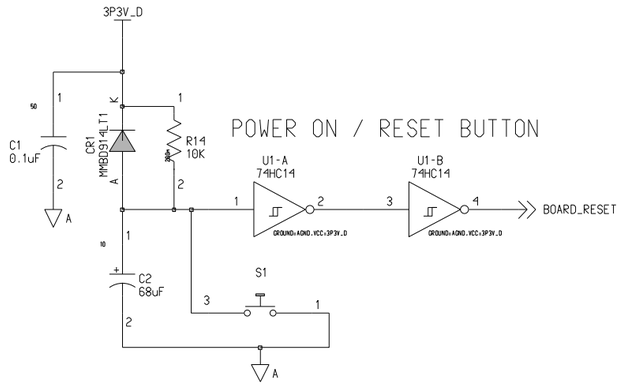
SKETCH NO. | DWG SIZE D

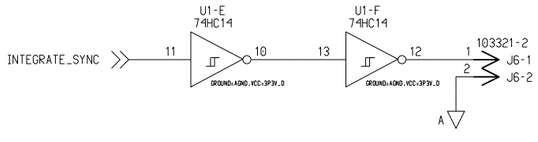
NO.
3F5592 REV1

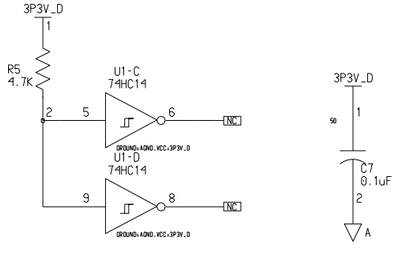
SHEET 3 OF 12

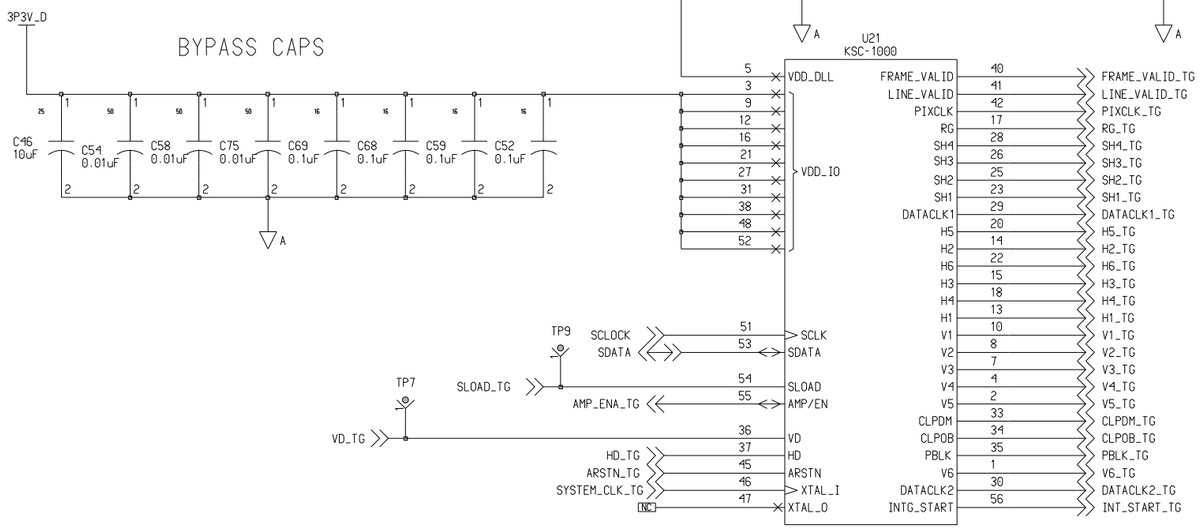


SYSTEM CLOCK: 40MHz









Ground=AGND,V1P8=1P8_V

✳ "TRUE" INDICATES THAT THIS COMPONENT IS NOT POPULATED

NOTES:							THIS IS A COMPUTER GENERATED DRAWING. IT IS OFFICIAL WHEN THE AUTHENTICATED BLOCK IS FILLED IN. THE MASTER COPY IS AUTHENTICATED IN RED.	AUTHENTICATED BLOCK
CHG NO DATE RLSE	REVISIONS	DWN BY APPV'D	CHG NO DATE RLSE	REVISIONS	DWN BY APPV'D	ON Semiconductor		
						DWN R. BROLLY	DATE 06.24.2005 at 11:09	
						DFTG NONE	DSGN ENGR R. BROLLY	
						CHK NONE	MFG ENGR NONE	
						ORIG CHG NO		

FIRST USED ON: EVALUATION BOARD SYSTEM

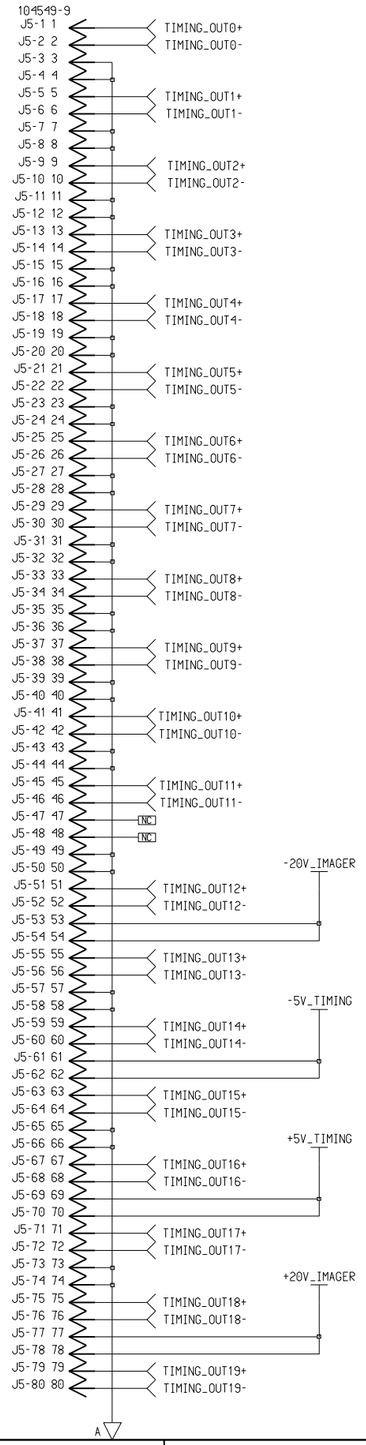
NAME: AD9945 TIMING BOARD

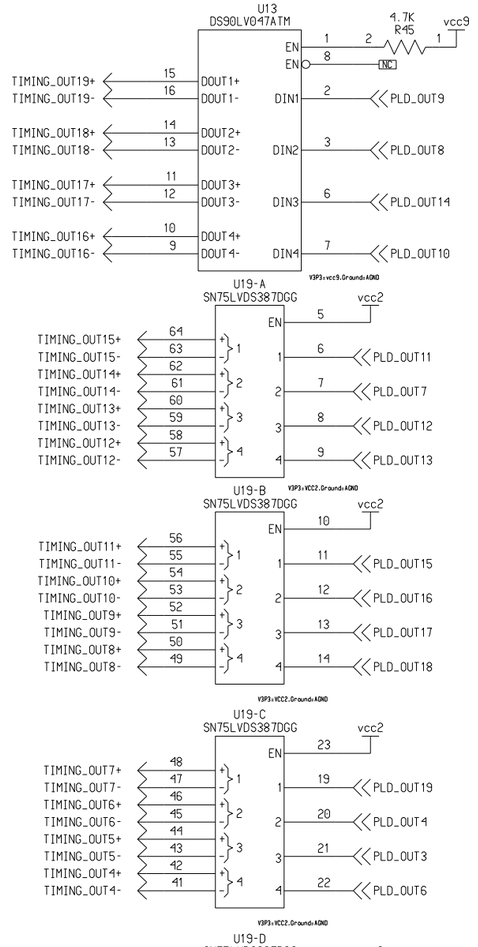
SKETCH NO. | DWG SIZE: D

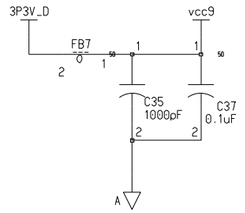
NO.: 3F5592 REV1

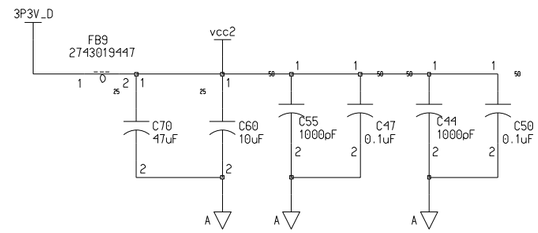
SHEET 4 OF 12

BOARD INTERFACE CONNECTOR









LVDS DRIVERS

NOTES:

THIS IS A COMPUTER GENERATED DRAWING. IT IS OFFICIAL WHEN THE AUTHENTICATED BLOCK IS FILLED IN. THE MASTER COPY IS AUTHENTICATED IN RED.

AUTHENTICATED BLOCK

CHG NO DATE RLSE	REVISIONS	DWN BY APPV'D	CHG NO DATE RLSE	REVISIONS	DWN BY APPV'D

ON Semiconductor

DWN R. BROLLY	DATE 06.24.2005 at 11:10
DFTG NONE	DSGN ENGR R. BROLLY
CHK NONE	MFG ENGR NONE
ORIG CHG NO	

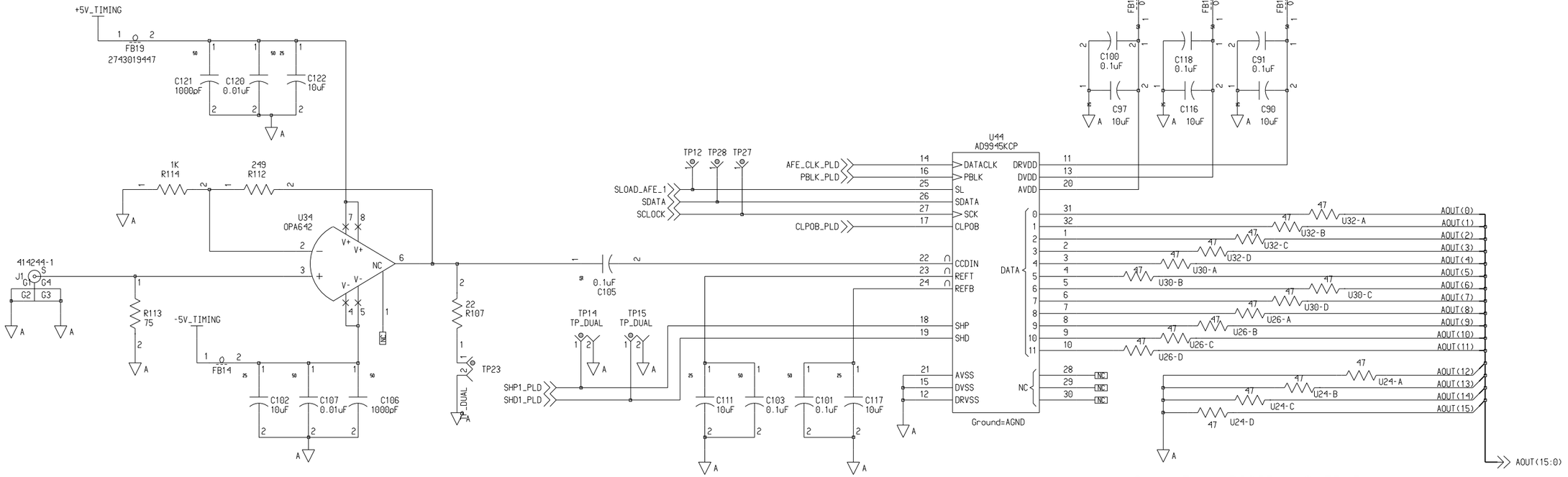
FIRST USED ON EVALUATION BOARDSYSTEM

NAME AD9945 TIMING BOARD

SKETCH NO. | DWG SIZE D

NO. 3F5592 REV1

SHEET 5 OF 12



ANALOG INPUT CHANNEL 1

CHANNEL 1 DIGITAL OUTPUT

(FRAMEGRABBER BITS 0 - 15)

NOTES:

THIS IS A COMPUTER GENERATED DRAWING. IT IS OFFICIAL WHEN THE AUTHENTICATED BLOCK IS FILLED IN. THE MASTER COPY IS AUTHENTICATED IN RED.

AUTHENTICATED BLOCK

CHG NO DATE RLSE	REVISIONS	DWN BY APPV'D

CHG NO DATE RLSE	REVISIONS	DWN BY APPV'D

ON Semiconductor

DWN R. Brolly	DATE 06.24.2005 at 11:11
DFTG	DSGN ENGR R. Brolly
CHK	MFG ENGR
ORIG CHG NO	

FIRST USED ON Evaluation Board System

NAME

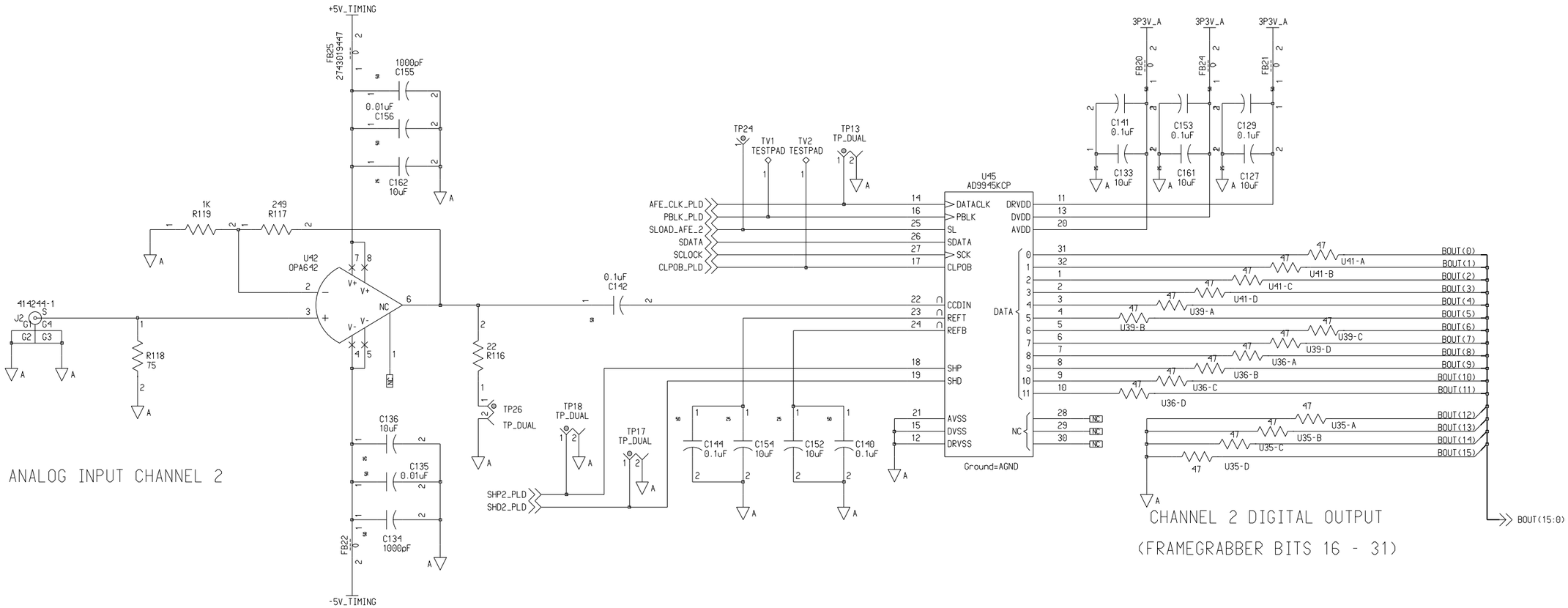
AD9945 TIMING BOARD

SKETCH NO. | DWG SIZE D

NO.

3F5592 REV1

SHEET 6 OF 12



NOTES:

THIS IS A COMPUTER GENERATED DRAWING. IT IS OFFICIAL WHEN THE AUTHENTICATED BLOCK IS FILLED IN. THE MASTER COPY IS AUTHENTICATED IN RED.

AUTHENTICATED BLOCK

CHG NO DATE RLSE	REVISIONS	DWN BY APPV'D

CHG NO DATE RLSE	REVISIONS	DWN BY APPV'D

ON Semiconductor

DWN: R. BROLLY	DATE: 06.24.2005 at 11:11
DFTG: NONE	DSGN ENGR: R. BROLLY
CHK: NONE	MFG ENGR: NONE
ORIG CHG NO	

FIRST USED ON: EVALUATION BOARD SYSTEM

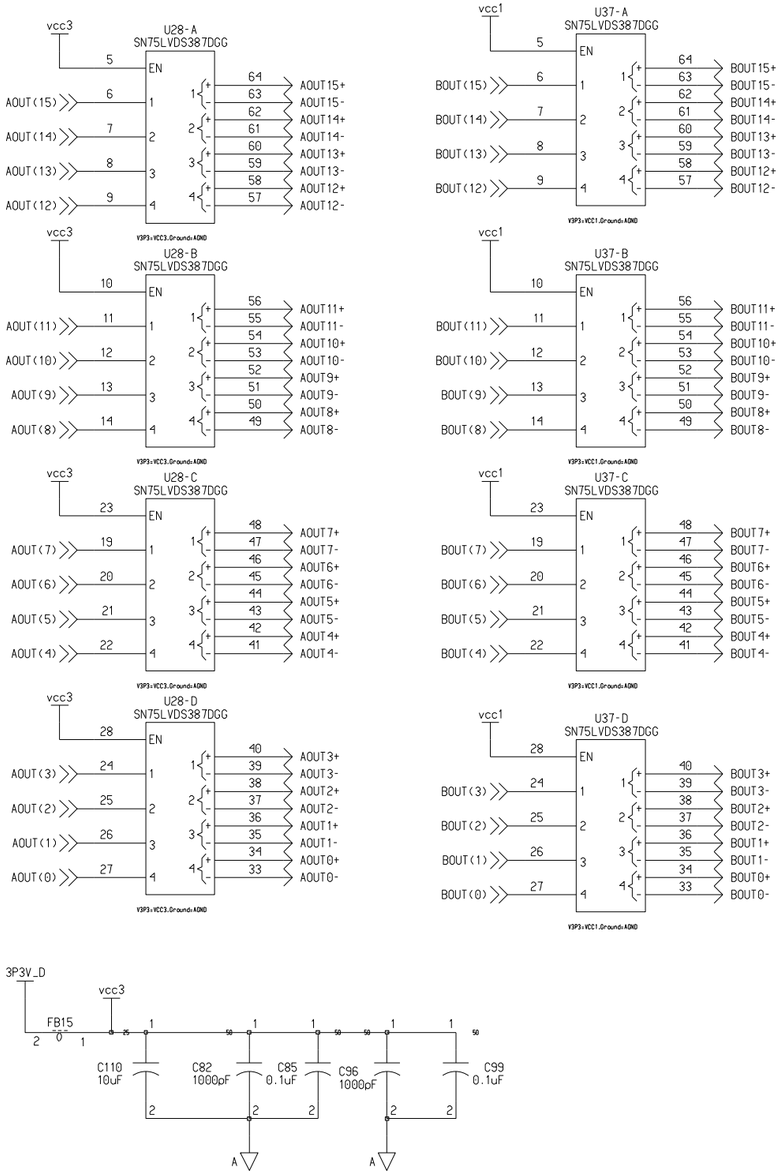
NAME: AD9945 TIMING BOARD

SKETCH NO. | DWG SIZE: D

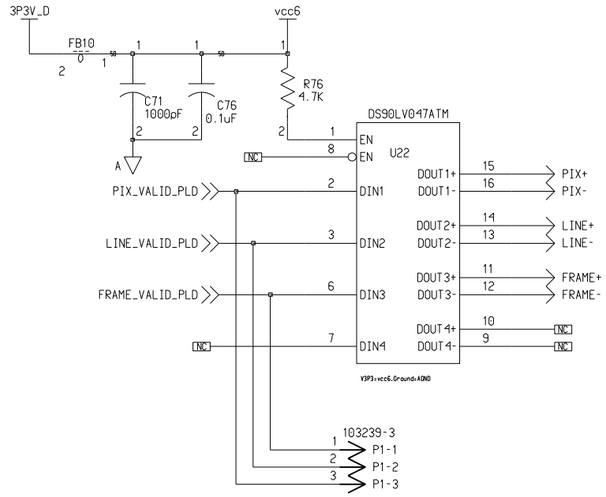
NO.: 3F5592 REV1

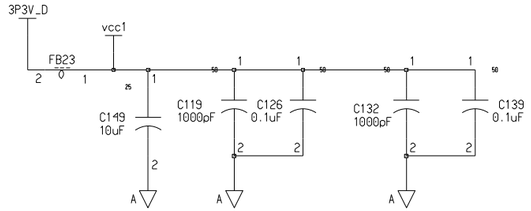
SHEET 7 OF 12

LVDS DRIVERS FOR DATA OUTPUT

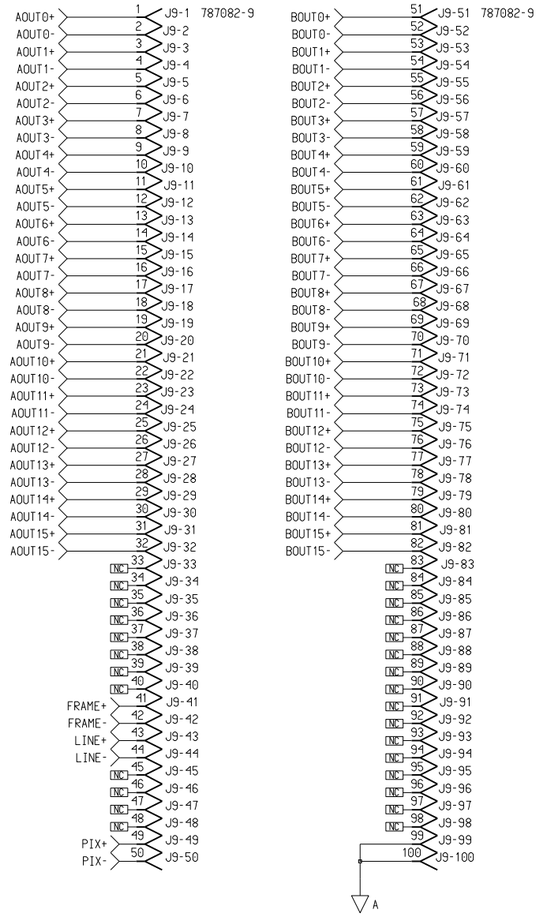


LVDS DRIVERS FOR FRAMEGRABBER SYNC





LVDS DATA OUTPUT CONNECTOR



NOTES:

THIS IS A COMPUTER GENERATED DRAWING. IT IS OFFICIAL WHEN THE AUTHENTICATED BLOCK IS FILLED IN. THE MASTER COPY IS AUTHENTICATED IN RED.

AUTHENTICATED BLOCK

CHG NO DATE RLSE	REVISIONS	DWN BY APPV'D

CHG NO DATE RLSE	REVISIONS	DWN BY APPV'D

ON Semiconductor

DWN R. BROLLY	DATE 06.24.2005 at 11:12
DFTG NONE	DSGN ENGR R. BROLLY
CHK NONE	MFG ENGR NONE
ORIG CHG NO	

FIRST USED ON EVALUATION BOARD SYSTEM

NAME

AD9945 TIMING BOARD

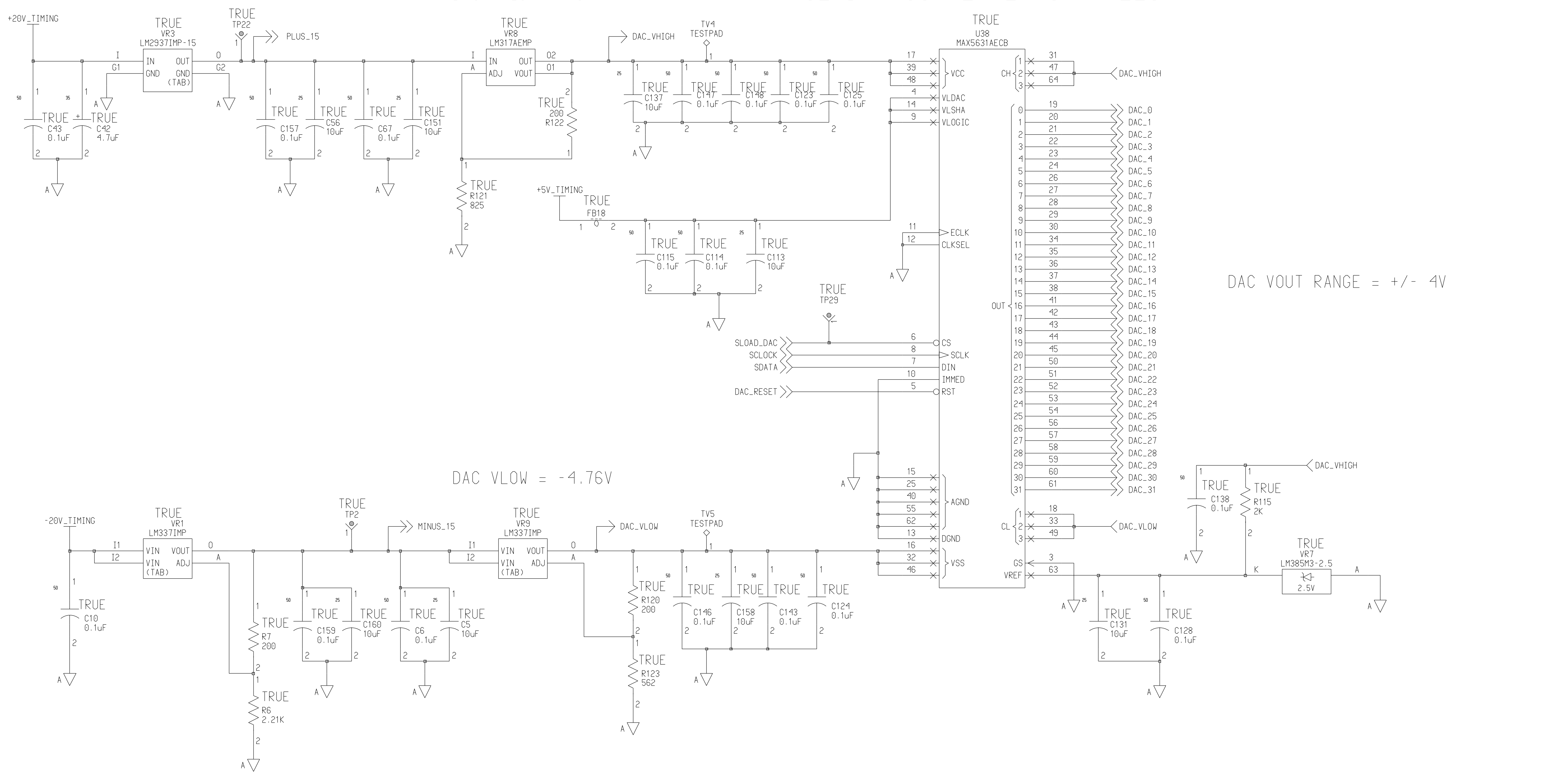
SKETCH NO. | DWG SIZE D

NO.

3F5592 REV1

SHEET 8 OF 12

32 D/A CONVERTER CHANNELS



NOTES:	THIS IS A COMPUTER GENERATED DRAWING. IT IS OFFICIAL WHEN THE AUTHENTICATED BLOCK IS FILLED IN. THE MASTER COPY IS AUTHENTICATED IN RED.	AUTHENTICATED BLOCK

CHG NO DATE RLSE	REVISIONS	DWN BY APPV'D	CHG NO DATE RLSE	REVISIONS	DWN BY APPV'D

ON Semiconductor

DWN R. BROLLY	DATE 06.24.2005 at 11:13
DFTG NONE	DSGN ENGR R. BROLLY
CHK NONE	MFG ENGR NONE
ORIG CHG NO	

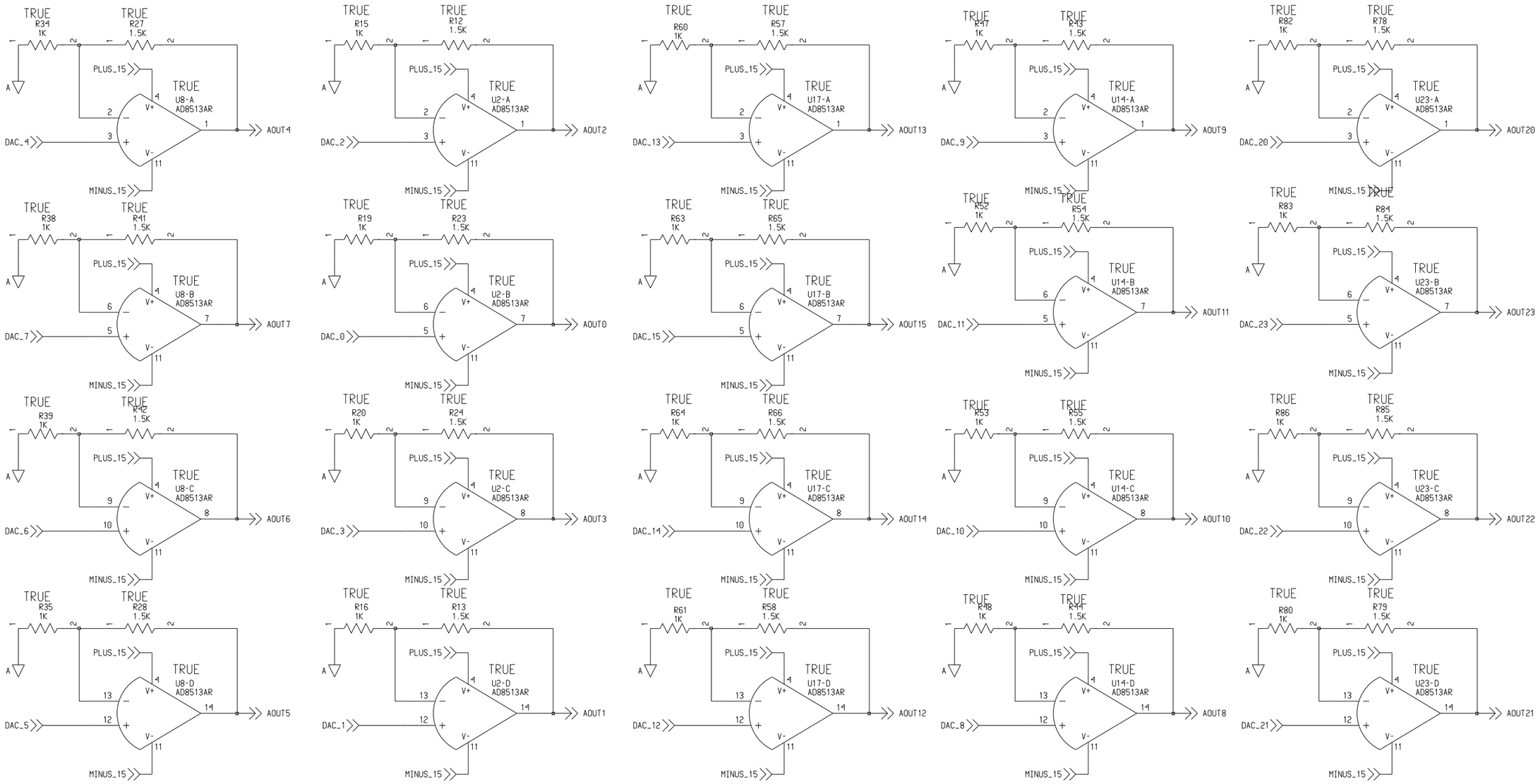
FIRST USED ON EVALUATION BOARD SYSTEM

NAME AD9945 TIMING BOARD

SKETCH NO. DWG SIZE D

NO. 3F5592 REV1

SHEET 9 OF 12



DAC VOLTAGE LEVEL SHIFTERS
D/A CONVERTER OUTPUT RANGE +/- 4V
OP-AMP VOLTAGE GAIN = 2.5
TIMING BOARD OUTPUT RANGE +/- 10V

NOTES:

THIS IS A COMPUTER GENERATED DRAWING. IT IS OFFICIAL WHEN THE AUTHENTICATED BLOCK IS FILLED IN. THE MASTER COPY IS AUTHENTICATED IN RED.

AUTHENTICATED BLOCK

CHG NO DATE RLSE	REVISIONS	DWN BY APPV'D	CHG NO DATE RLSE	REVISIONS	DWN BY APPV'D

ON Semiconductor

DWN R. BROLLY	DATE 06.24.2005 at 11:13
DFTG NONE	DSGN ENGR R. BROLLY
CHK NONE	MFG ENGR NONE
ORIG CHG NO	

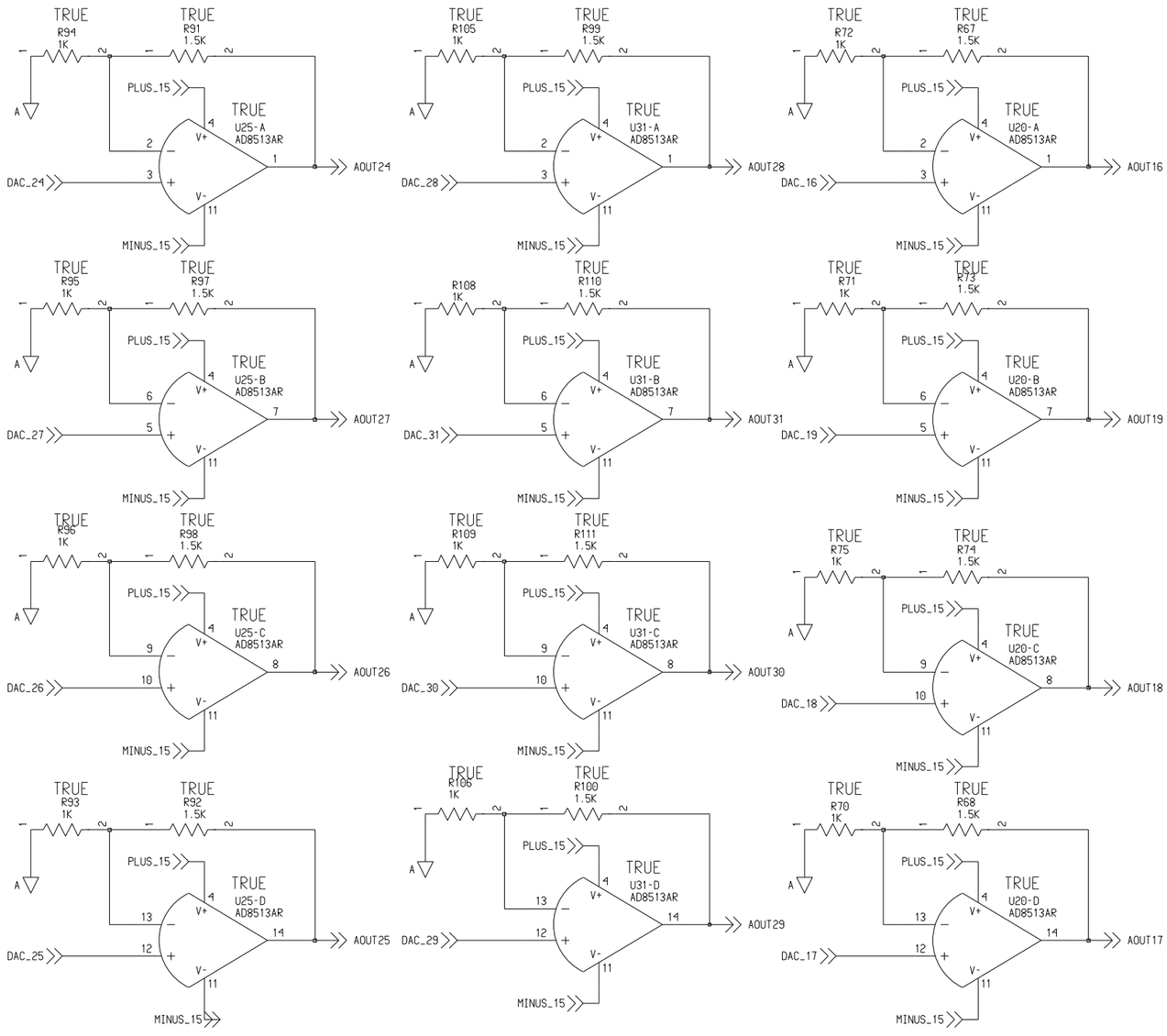
FIRST USED ON EVALUATION BOARD SYSTEM

NAME AD9945 TIMING BOARD

SKETCH NO. | DWG SIZE D

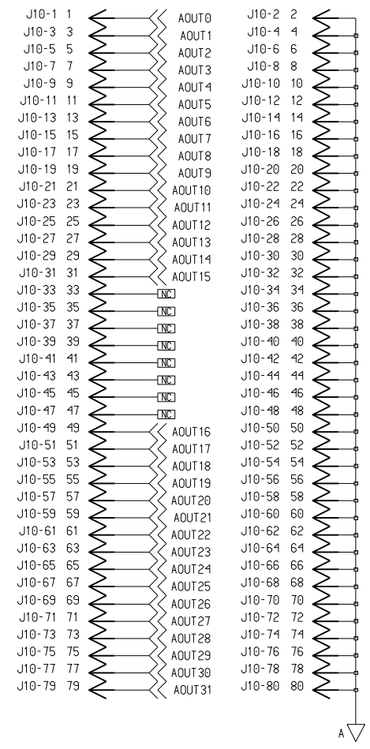
NO. 3F5592 REV1

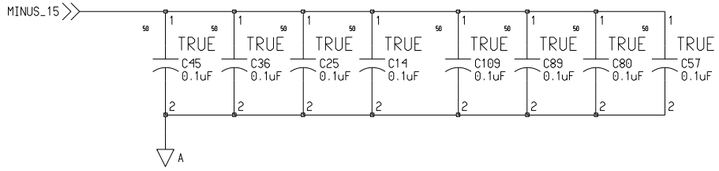
SHEET 10 OF 12

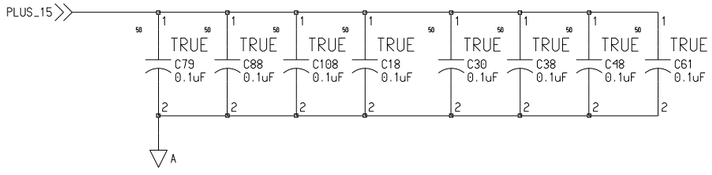


DAC OUTPUT CONNECTOR

TRUE
104549-9







NOTES:				THIS IS A COMPUTER GENERATED DRAWING. IT IS OFFICIAL WHEN THE AUTHENTICATED BLOCK IS FILLED IN. THE MASTER COPY IS AUTHENTICATED IN RED.		AUTHENTICATED BLOCK
CHG NO DATE RLSE	REVISIONS	DWN BY APPV'D	CHG NO DATE RLSE	REVISIONS	DWN BY APPV'D	

ON Semiconductor

DWN R. Brolly	DATE 06.24.2005 at 11:14
DFTG NONE	DSGN ENGR R. Brolly
CHK NONE	MFG ENGR NONE
ORIG CHG NO	

FIRST USED ON EVALUATION BOARD SYSTEM

NAME

AD9945 TIMING BOARD

SKETCH NO. | DWG SIZE D

NO.

3F5592 REV1

SHEET 11 OF 12

DAC VOLTAGE LEVEL SHIFTERS
D/A CONVERTER OUTPUT RANGE IS 0 TO +4V
OP-AMP VOLTAGE GAIN = 2.5
TIMING BOARD OUTPUT RANGE IS 0 TO +10V

VREF = 4.096V

TRUE VR6 MAX6041AEUR-T
TRUE U29 MAX5742EUB+
TRUE C86 0.1uF
TRUE TP11
TRUE C95 0.1uF
TRUE C87 0.1uF

TRUE U27-A AD8513AR
TRUE U27-B AD8513AR
TRUE U27-C AD8513AR
TRUE U27-D AD8513AR

TRUE R102 1K
TRUE R101 1.5K
TRUE R103 1K
TRUE R104 1.5K
TRUE R89 1K
TRUE R90 1.5K
TRUE R88 1K
TRUE R87 1.5K

+5V_TIMING
+20V_TIMING
-5V_TIMING
PLUS_15
MINUS_15
SDATA
SLOAD_LED_DAC
SCLOCK
DAC_32
DAC_33
DAC_34
DAC_35
RED_DAC
MISC_DAC
BLUE_DAC
GREEN_DAC
LED_ON

TRUE J8-1 J8-2 J8-3 J8-4 J8-5 J8-6 J8-7 J8-8 J8-9 J8-10
NC NC

LED BOARD CONNECTOR

NOTES:
THIS IS A COMPUTER GENERATED DRAWING. IT IS OFFICIAL WHEN THE AUTHENTICATED BLOCK IS FILLED IN. THE MASTER COPY IS AUTHENTICATED IN RED.
AUTHENTICATED BLOCK

CHG NO DATE RLSE	REVISIONS	DWN BY APPV'D	CHG NO DATE RLSE	REVISIONS	DWN BY APPV'D

ON Semiconductor

DWN R. Brolly	DATE 06.24.2005 at 11:14
DFTG	DSGN ENGR R. Brolly
CHK	MFG ENGR
ORIG CHG NO	

FIRST USED ON
NAME AD9945 TIMING BOARD
SKETCH NO. | DWG. SIZE D
NO. 3F5592 REV1
SHEET 12 OF 12

Components
For Circuit Board Assembly

NO. 3F5592
SHEET 1 NEXT SHEET 2

Item No	Part no	Assy. Side	Item Reference Designators	Qty	Package style	Notes/Comp Description
1	3F5452	HW-T-1	BRD1	1		BARE BOARD REV 1
2	7B9716	TOP-17	C1 C11 C15 C23 C26 C39 C76 C83 C85 C91 C92 C99 C118 C126 C129 C139 C153	37	0805_h.055	0.1uF_50V_.10 Ceramic Monolithic Chip
		BOT-20	C7 C17 C20 C22 C29 C31 C34 C37 C40 C47 C50 C64 C100 C101 C103 C105 C140 C141 C142 C144			
3	980646	TOP-5	C12 C107 C120 C135 C156	8	0805_h.055	0.01uF_50V_.10 MONOLITHIC, CERAMIC CHIP
		BOT-3	C21 C33 C41			
4	254471	TOP-12	C13 C24 C71 C82 C93 C96 C106 C119 C121 C132 C134 C155	16	0805_h.055	1000pF_50V_.05 MONOLITHIC, CERAMIC CHIP
		BOT-4	C35 C44 C55 C72			
5	5E6852	BOT-1	C2	1	pcap_6032_c_	68uF_10V_.20 ELECTROLYTIC TANTALUM CHIP
6	5F0628	TOP-13	C28 C84 C90 C94 C102 C110 C116 C122 C127 C136 C149 C161 C162	30	1210_h.110	10uF_25V_.20 SMD CERAMIC CHIP
		BOT-17	C8 C9 C16 C32 C46 C60 C62 C77 C78 C81 C97 C111 C117 C133 C152 C154 C163			
7	1C3731	BOT-2	C3 C4	2	pcap_6032_c_	4.7uF_35V_.10 ELECTROLYTIC, TANTALUM, CHIP
8	4B4011	BOT-8	C51 C52 C59 C68 C69 C73 C164 C165	8	0603_h.035	0.1uF_16V_.20 RECOMMENDED DECOUPLING CAP
9	4B3745	BOT-9	C53 C54 C58 C65 C66 C74 C75 C166 C167	9	0603_h.045	0.01uF_50V_.10 CERAMIC MONOLITHIC CHIP

CHG.NO DATE	REVISIONS	DR. BY APPS.
REV 1	INITIAL RELEASE	PCS

SEE SHEET FOR ADD'L REVISIONS

Notes: REFER TO CIRCUIT DIAGRAM 3F5592

PROGRAMMED PART SOFTWARE PART NUMBER IS THE PPID NUMBER WITH THE APPROPRIATE EXTENSION.

ON Semiconductor

DR. PCS	DATE 6/24/05
DES. ENG.	PKG. MATL.
CK. DFTG. PCS	MFG. ENG.
ORIG. CHG. NO. RELEASED	

FIRST USED ON
NAME CIRCUIT BOARD ASSEMBLY
AD9945 TIMING BOARD
SKETCH NO. DWG. SIZE B
3F5592
SHEET 1 NEXT SHEET 2

Components
For Circuit Board Assembly

NO. 3F5592
SHEET 2 NEXT SHEET 3

Item No	Part no	Assy. Side	Item Reference Designators	Qty	Package style	Notes/Comp Description
10	5F0627	TOP-1	C70	1	1812_h.110	47uF_25V_.20 SMD CERAMIC CHIP
11	616293	BOT-1	CR1	1	sot23_akn_sp	MMBD914LT1 DIODE, SWITCHING, 100V, 200mA
12	233152	TOP-13	FB6 FB10 FB11 FB13 FB14 FB15 FB16 FB19 FB21 FB22 FB23 FB24 FB25	23	fb_274301944	2743019447 - FERRITE, SMT BEADS
		BOT-10	FB1 FB2 FB3 FB4 FB5 FB7 FB8 FB9 FB12 FB20			
13	6C4636	TOP-2	J1 J2	2	j01s_414244-	414244-1 RF COAXIAL RECEPTACLE
14	7E7514	TOP-1	J3	1	p40s_103309-	103309-8 LOW PROFILE STRAIGHT HEADER
15	954067	TOP-1	J4	1	p10s_103309-	103309-1 LOW PROFILE STRAIGHT HEADER
16	999979	TOP-1	J5	1	p80s_104549-	104549-9 SMT, AMPMODU, SHROUDED HEADER CONNECTOR
17	7E7515	TOP-1	J6	1	p02s_103321-	103321-2 STRAIGHT HEADER CONNECTOR
18	7E7653	TOP-1	J7	1	p08ra_151321	151321 RIGHT ANGLE HEADER CONNECTOR
19	5C3152	TOP-1	J9	1	j100ra_78708	787082-9 AMPLIMITE VERTICLE RECEPTICLE CONNECTOR
20	323043	TOP-1	P1	1	p03s_103239-	103239-3 3 PIN SQ. POST HDR. CONNECTOR/JUMPER
21	255345	BOT-2	R107 R116	2	0805_h.030	22 Ohms_.100W_.05 FLAT, THICK METAL FILM, CHIP
22	2B4356	TOP-1	R108	1	0603_h.025	1K Ohms_.063W_.01 FLAT, THICK METAL FILM, CHIP
23	902504	BOT-2	R112 R117	2	0805_h.030	249 Ohms_.100W_.01 SMT CHIP FLAT THICK METAL FILM

CHG.NO DATE	REVISIONS	DR. BY APPS.
REV 1	INITIAL RELEASE	PCS

SEE SHEET FOR ADD'L REVISIONS

Notes: REFER TO CIRCUIT DIAGRAM 3F5592

PROGRAMMED PART SOFTWARE PART NUMBER IS THE PPID NUMBER WITH THE APPROPRIATE EXTENSION.

ON Semiconductor

DR. PCS	DATE 6/24/05
DES. ENG.	PKG. MATL.
CK. DFTG. PCS	MFG. ENG.
ORIG. CHG. NO. RELEASED	

FIRST USED ON
NAME CIRCUIT BOARD ASSEMBLY
AD9945 TIMING BOARD
SKETCH NO. DWG. SIZE B
3F5592
SHEET 2 NEXT SHEET 3

Components
For Circuit Board Assembly

NO. 3F5592
SHEET 3 NEXT SHEET 4

Item No	Part no	Assy. Side	Item Reference Designators	Qty	Package style	Notes/Comp Description
24	954554	TOP-2	R113 R118	2	0805_h.030	75 Ohms_.100W_.01 SMT CHIP FLAT THICK METAL FILM
25	233981	BOT-1	R14	1	0805_h.025	10K Ohms_.100W_.01 FLAT, THICK METAL FILM CHIP
26	283602	TOP-3	R21 R40 R56	3	0805_h.030	100 Ohms_.100W_.05 FLAT, THICK METAL FILM, CHIP
27	6C5175	BOT-6	R36 R49 R62 U3 U10 U18	6	cn1j4_.063_h	4.7K Ohms_.05 SURFACE MOUNT RESISTOR NETWORK
28	257516	TOP-1 BOT-1	R46 R18	2	0805_h.030	0.05 Ohms_.100W_- ZERO OHM CHIP JUMPER
29	253549	TOP-1 BOT-6	R76 R1 R2 R3 R4 R5 R45	7	0805_h.030	4.7K Ohms_.100W_.05 THICK METAL FILM
30	992865	BOT-9	R8 R9 R10 R11 R17 R22 R29 R114 R119	9	0805_h.020	1K Ohms_.100W_.001 FLAT, THIN METAL FILM, CHIP
31	2B1420	BOT-1	R81	1	0603_h.025	10 Ohms_.063W_.05 FLAT, THICK METAL FILM, CHIP
32	2E7622	BOT-1	RU4	REF	plcc20_.050_	EPC2LC20 CONFIGURATION EPROM FOR PLDS, 1.6M
33	449610	TOP-1	S1	1	sw_tpa11cgpc	TPA11CGPC0 TP/TPA SERIES PUSHBUTTON SWITCH
34	7E7503	TOP-1	S2	1	sw_tda04_h.0	TDA04H0SK1 DIP SWITCH, TOP SLIDE ACTUATED
35	901613	TOP-4	TP1 TP10 TP19 TP25	4	tp_tp104_h.2	TP-104-01-00 PRESS MOUNT TERMINAL - BLACK
36	TPDUAL	TOP-7	TP13 TP14 TP15 TP17 TP18 TP23 TP26	7	tpdual_.1_p4	TP_DUAL DUAL TEST PADS (THRU HOLE)
37	914449	TOP-11	TP3 TP4 TP5 TP7 TP9 TP12 TP24 TP27 TP28 TP30 TP31	11	p01s_146281-	146281-1 SQ POST UNSHROUDED HDR CONNECTOR

CHG.NO DATE	REVISIONS	DR. BY APPS.
REV 1	INITIAL RELEASE	PCS

SEE SHEET FOR ADD'L REVISIONS

Notes: REFER TO CIRCUIT DIAGRAM 3F5592

PROGRAMMED PART SOFTWARE PART NUMBER IS THE PPID NUMBER WITH THE APPROPRIATE EXTENSION.

ON Semiconductor

DR. PCS	DATE 6/24/05
DES. ENG.	PKG. MATL.
CK. DFTG. PCS	MFG. ENG.
ORIG. CHG. NO. RELEASED	

FIRST USED ON
NAME CIRCUIT BOARD ASSEMBLY
AD9945 TIMING BOARD
SKETCH NO. DWG. SIZE B
3F5592
SHEET 3 NEXT SHEET 4

Components
For Circuit Board Assembly

NO. 3F5592
SHEET 4 NEXT SHEET 5

Item No	Part no	Assy. Side	Item Reference Designators	Qty	Package style	Notes/Comp Description
38	7E7662	TOP-1	TP6	1	p05s_103321-	103321-0 STRAIGHT HEADER CONNECTOR
39	901614	TOP-4	TP8 TP16 TP20 TP21	4	tp_tp104_h.2	TP-104-01-02 PRESS MOUNT TERMINAL - RED
40	263526	TOP-1	U1	1	so14_.210_h.	74HC14 INVERTER, HEX, W/ SCHMITT TRIGGER
41	2E7640	TOP-1 BOT-1	U13 U22	2	so16_.210_h.	DS90LV047ATM DIFFERENTIAL LINE DRIVER, QUAD
42	7E9959	TOP-1	U15	1	bga256_.0393	EPF10K30AFC256-101 FPGA, FLEX 10KA, EPF10K30AFC256-3
43	7E7078	TOP-1 BOT-2	U19 U28 U37	3	tssop64_.294	SN75LVDS387DGG DIFFERENTIAL LINE DRIVER, 16-BIT
44	7E9108	TOP-1	U21	1	clcc56_.0197	KSC-1000 CUSTOM ASIC, CCD TIMING GENERATOR
45	7B9962	BOT-8	U24 U26 U30 U32 U35 U36 U39 U41	8	cn1j8_.048_h	47 Ohms_.05 SMT, 4 ISOLATED RESISTORS
46	5C2040	TOP-2	U34 U42	2	so08_.210_h.	OPA642 OPAMP, SINGLE, BIPOLAR, WIDEBAND, LOW-DISTORTION
47	NA	BOT-1	U4	1	plcc20_.050_	PROGRAMMED PART RAW 2E7622
48	G12337	BOT-2	U44 U45	2	clcc32_.0197	AD9945KCP CCD SIGNAL PROCESSOR, 12-BIT, 40 MSPS
49	1E5789	TOP-1	U46	1	xtal_f4100_h	F4100-40MHZ 40.000 MHz 3.3V HCMOS SMD OSC., FIXED FREQ
50	3H5151	TOP-3	U7 U12 U16	3	tssop20_.225	74LVC541 BUFFER/DRIVER, OCTAL, W/ 3-STATE OUTPUT
51	4B4595	TOP-2	VR2 VR5	2	d2pak_goio_b	LT1086CM-3.3 1.5A_4.5-20V_3.3V VOLTAGE REGULATOR, 3.3V, 1.5A, 3-T
52	6E8811	BOT-1	VR4	1	sot223_goio_	LMS8117AMP-1.8 1A_3.2-10V_1.8V VOLTAGE REGULATOR, 1.8V, 1A, 3-TER

CHG.NO DATE	REVISIONS	DR. BY APPS.
REV 1	INITIAL RELEASE	PCS

SEE SHEET FOR ADD'L REVISIONS

Notes: REFER TO CIRCUIT DIAGRAM 3F5592

PROGRAMMED PART SOFTWARE PART NUMBER IS THE PPID NUMBER WITH THE APPROPRIATE EXTENSION.

ON Semiconductor

DR. PCS	DATE 6/24/05
DES. ENG.	PKG. MATL.
CK. DFTG. PCS	MFG. ENG.
ORIG. CHG. NO. RELEASED	

FIRST USED ON
NAME CIRCUIT BOARD ASSEMBLY
AD9945 TIMING BOARD
SKETCH NO. DWG. SIZE B
3F5592
SHEET 4 NEXT SHEET 5

Components
For Circuit Board Assembly

NO. 3F5592
SHEET 5 NEXT SHEET 6

Item No	Part no	Assy. Side	Item Reference Designators	Qty	Package style	Notes/Comp Description
53	7B9716	BOT-36	C6 C10 C14 C18 C25 C30 C36 C38 C43 C45 C48 C57 C61 C67 C79 C80 C86 C87 C88 C89 C95 C108 C109 C114 C115 C123 C124 C125 C128 C138 C143 C146 C147 C148 C157 C159	36NL	0805_h.055	NO LOAD 0.1uF_50V_.10 Ceramic Monolithic Chip
54	5F0628	BOT-8	C5 C56 C113 C131 C137 C151 C158 C160	8NL	1210_h.110	NO LOAD 10uF_25V_.20 SMD CERAMIC CHIP
55	1C3731	BOT-1	C42	1NL	pcap_6032_c_	NO LOAD 4.7uF_35V_.10 ELECTROLYTIC, TANTALUM, CHIP
56	233152	BOT-1	FB18	1NL	fb_274301944	NO LOAD 2743019447 - FERRITE, SMT BEADS
57	6C4636	TOP-1	J11	1NL	j01s_414244-	NO LOAD 414244-1 RF COAXIAL RECEPTACLE
58	954067	TOP-1	J8	1NL	p10s_103309-	NO LOAD 103309-1 LOW PROFILE STRAIGHT HEADER
59	999979	TOP-1	J10	1NL	p80s_104549-	NO LOAD 104549-9 SMT, AMPMODU, SHROUDED HEADER CONNECTOR
60	2B4356	TOP-35	R15 R16 R19 R20 R34 R35 R38 R39 R47 R48 R52 R53 R60 R61 R63 R64 R70 R71 R72 R75 R80 R82 R83 R86 R88 R89 R93 R94 R95 R96 R102 R103 R105 R106 R109	35NL	0603_h.025	NO LOAD 1K Ohms_.063W_.01 FLAT, THICK METAL FILM, CHIP
61	783961	BOT-1	R115	1NL	0805_h.030	NO LOAD 2K Ohms_.100W_.01 FLAT, THICK METAL FILM, CHIP
62	8B0951	TOP-36	R12 R13 R23 R24 R27 R28 R41 R42 R43 R44 R54 R55 R57 R58 R65	36NL	0603_h.025	NO LOAD 1.5K Ohms_.063W_.01 FLAT, THICK METAL FILM, CHIP

CHG.NO DATE	REVISIONS	DR. BY APPS.
REV 1	INITIAL RELEASE	PCS

SEE SHEET FOR ADD'L REVISIONS

Notes: REFER TO CIRCUIT DIAGRAM 3F5592

PROGRAMMED PART SOFTWARE PART NUMBER IS THE PPID NUMBER WITH THE APPROPRIATE EXTENSION.

ON Semiconductor

DR. PCS	DATE 6/24/05
DES. ENG.	PKG. MATL.
CK. DFTG. PCS	MFG. ENG.
ORIG. CHG. NO. RELEASED	

FIRST USED ON
NAME CIRCUIT BOARD ASSEMBLY
AD9945 TIMING BOARD
SKETCH NO. DWG. SIZE B
3F5592
SHEET 5 NEXT SHEET 6

Components
For Circuit Board Assembly

NO. 3F5592
SHEET 6 NEXT SHEET 7

Item No	Part no	Assy. Side	Item Reference Designators	Qty	Package style	Notes/Comp Description
			R66 R67 R68 R73 R74 R78 R79 R84 R85 R87 R90 R91 R92 R97 R98 R99 R100 R101 R104 R110 R111			
63	961436	BOT-1	R121	1NL	0805_h.030	NO LOAD 825 Ohms_.100W_.01 FLAT, THICK METAL FILM, CHIP
64	9B0438	BOT-1	R123	1NL	0805_h.030	NO LOAD 562 Ohms_.100W_.01 SMT CHIP FLAT THICK METAL FILM
65	901801	BOT-1	R124	1NL	0805_h.030	NO LOAD 49.9 Ohms_.100W_.01 SMT CHIP FLAT THICK METAL FILM
66	7B8917	TOP-1	R125	1NL	0603_h.025	NO LOAD 0.05 Ohms_.063W_.05 Zero Ohm,FLAT, THICK METAL FILM, CHIP
67	6C4402	TOP-1	R127	1NL	0603_h.025	NO LOAD 33 Ohms_.063W_.05 FLAT, THICK METAL FILM, CHIP
68	233981	BOT-3	R33 R37 R50	3NL	0805_h.025	NO LOAD 10K Ohms_.100W_.01 FLAT, THICK METAL FILM CHIP
69	992867	BOT-1	R25	1NL	0805_h.030	NO LOAD 75K Ohms_.100W_.10 FLAT, THICK METAL FILM, CHIP
70	954557	BOT-1	R26	1NL	0805_h.030	NO LOAD 6.8K Ohms_.100W_.05 SMT CHIP FLAT THICK METAL FILM
71	961572	BOT-1	R51	1NL	0805_h.030	NO LOAD 14K Ohms_.100W_.01 SMT CHIP FLAT THICK METAL FILM
72	283607	BOT-1	R59	1NL	0805_h.030	NO LOAD 3.3K Ohms_.100W_.05 FLAT, THICK METAL FILM, CHIP
73	992874	BOT-1	R6	1NL	0805_h.030	NO LOAD 2.21K Ohms_.100W_.001 SMT CHIP FLAT THIN METAL FILM
74	7E8105	BOT-3	R7 R120 R122	3NL	0805_h.025	NO LOAD 200 Ohms_.100W_.001 FLAT, THIN METAL FILM, CHIP

CHG.NO DATE	REVISIONS	DR. BY APPS.
REV 1	INITIAL RELEASE	PCS

SEE SHEET FOR ADD'L REVISIONS

Notes: REFER TO CIRCUIT DIAGRAM 3F5592

PROGRAMMED PART SOFTWARE PART NUMBER IS THE PPID NUMBER WITH THE APPROPRIATE EXTENSION.

ON Semiconductor

DR. PCS	DATE 6/24/05
DES. ENG.	PKG. MATL.
CK. DFTG. PCS	MFG. ENG.
ORIG. CHG. NO. RELEASED	

FIRST USED ON
NAME CIRCUIT BOARD ASSEMBLY
AD9945 TIMING BOARD
SKETCH NO. DWG. SIZE B
3F5592
SHEET 6 NEXT SHEET 7

Components
For Circuit Board Assembly

NO. 3F5592
SHEET 7 NEXT SHEET 8

Item No	Part no	Assy. Side	Item Reference Designators	Qty	Package style	Notes/Comp Description
75	914449	TOP-2	TP11 TP29	2NL	p01s_146281-	NO LOAD 146281-1 SQ POST UNSHROUDED HDR CONNECTOR
76	901614	TOP-2	TP2 TP22	2NL	tp_tp104_h.2	NO LOAD TP-104-01-02 PRESS MOUNT TERMINAL - RED
77	7E9912	BOT-1	U11	1NL	so16_.200_h.	NO LOAD MAX5917AESE SWITCH, SIMPLE SWAPPER HOT-SWAP, 65V
78	7E8789	TOP-9	U2 U8 U14 U17 U20 U23 U25 U27 U31	9NL	so14_.200_h.	NO LOAD AD8513AR JFET OP AMP
79	5F2836	TOP-1	U29	1NL	msop10_.170_	NO LOAD 'MAX5742EUB+' D/A CONVERTER, QUAD, 12-BIT, SERIAL
80	7E9884	TOP-1	U38	1NL	qfp64_.0197_	NO LOAD MAX5631AECB D/A CONVERTER, 16-BIT, 32 CHANNEL, S/H
81	7E8536	TOP-1	U43	1NL	tssop16_.225	NO LOAD CY22150FC CLOCK GENERATOR, PLL, 6 OUTPUT, PROGRAMMABLE
82	5F0104	BOT-1	U9	1NL	so16_.200_h.	NO LOAD MAX5912ESE SWITCH, SIMPLE SWAPPER HOT-SWAP, -48V
83	6E8813	BOT-2	VR1 VR9	2NL	sot223_aioi_	NO LOAD LM337IMP 1A_3-40V_-1.2 to -37V VOLTAGE REGULATOR, NEG ADJ, 1
84	G11244	BOT-1	VR3	1NL	sot223_igog_	NO LOAD LM2937IMP-15 500mA_26V_15V 500mA LOW DROPOUT VOLTAGE REGULAT
85	5F2852	BOT-1	VR6	1NL	sot23_igo_sp	NO LOAD MAX6041AEUR-T -A_4.296-12.6V_4.096V VOLTAGE REFE
86	7E9561	BOT-1	VR7	1NL	sot23_kna_sp	NO LOAD LM385M3-2.5_20mA_-V_2.5V VOLTAGE REFERENCE, 2.5V, 2-TERMINA
87	2E5443	BOT-1	VR8	1NL	sot223_aoi_s	NO LOAD LM317AEMP

CHG.NO DATE	REVISIONS	DR. BY APPS.
REV 1	INITIAL RELEASE	PCS

SEE SHEET FOR ADD'L REVISIONS

Notes: REFER TO CIRCUIT DIAGRAM 3F5592

PROGRAMMED PART SOFTWARE PART NUMBER IS THE PPID NUMBER WITH THE APPROPRIATE EXTENSION.

ON Semiconductor

DR. PCS	DATE 6/24/05
DES. ENG.	PKG. MATL.
CK. DFTG. PCS	MFG. ENG.
ORIG. CHG. NO. RELEASED	

FIRST USED ON
NAME CIRCUIT BOARD ASSEMBLY
AD9945 TIMING BOARD
SKETCH NO. DWG. SIZE B
3F5592
SHEET 7 NEXT SHEET 8

REVISION BLOCK				
ZONE	REV.	DESCRIPTION	ENGR/DATE	APVD/DWN

NOTES:

1. MANUFACTURE BOARD IN ACCORDANCE WITH IPC-6011 & 6012, CLASS 3.

2. MATERIAL SPECIFICATIONS:
   2.1 CORE MATERIAL: POLYIMIDE LAMINATE, TYPE GIN, PER IPC-4101, HTE COPPER CLAD, SIZE AND CONSTRUCTION PER DETAIL A.
   2.2 PRE-PREG MATERIAL: POLYIMIDE, TYPE GIN, B STAGE PER IPC-4101, SIZE PER DETAIL A.
   2.3 MODIFICATIONS TO THE LAYER STACKUP AS SHOWN IN DETAIL A ARE PERMISSIBLE WITH THE FOLLOWING CONSTRAINTS:
      2.3.1 CONDUCTIVE LAYERS SHALL BE EVENLY SPACED THROUGHOUT.
      2.3.2 OVERALL THICKNESS SHALL BE UNCHANGED.

3. COPPER PLATE:
   3.1 HOLES: COPPER PLATING ON WALL OF HOLES SHALL BE 0.0015 MIN. UNLESS OTHERWISE SPECIFIED

4. SOLDER PLATE:
   4.1 SURFACE AND HOLES: EXPOSED LANDS AND LINES, EXCLUDING CONTACT FINGERS, SHALL BE TIN-LEAD COATED IN ACCORDANCE WITH THE SOLDERABILITY REQUIREMENTS OF J-STD-003.

5. CONDUCTOR WIDTH AND SPACING:
   5.1 WIDTH: 0.006 MIN
   5.2 SPACING: 0.007 MIN
   5.3 DESIGN FABRICATION ALLOWANCE IS 0.015.

6. HOLE REQUIREMENTS:
   6.1 ANNULAR RING: 0.002 MIN
   6.2 HOLE LOCATIONS TO BE 0.003 (DTP - DIAMETRICAL TRUE POSITION)
   6.3 HOLE SIZES APPLY AFTER SOLDER PLATING, REFLOW OR DEPOSITION

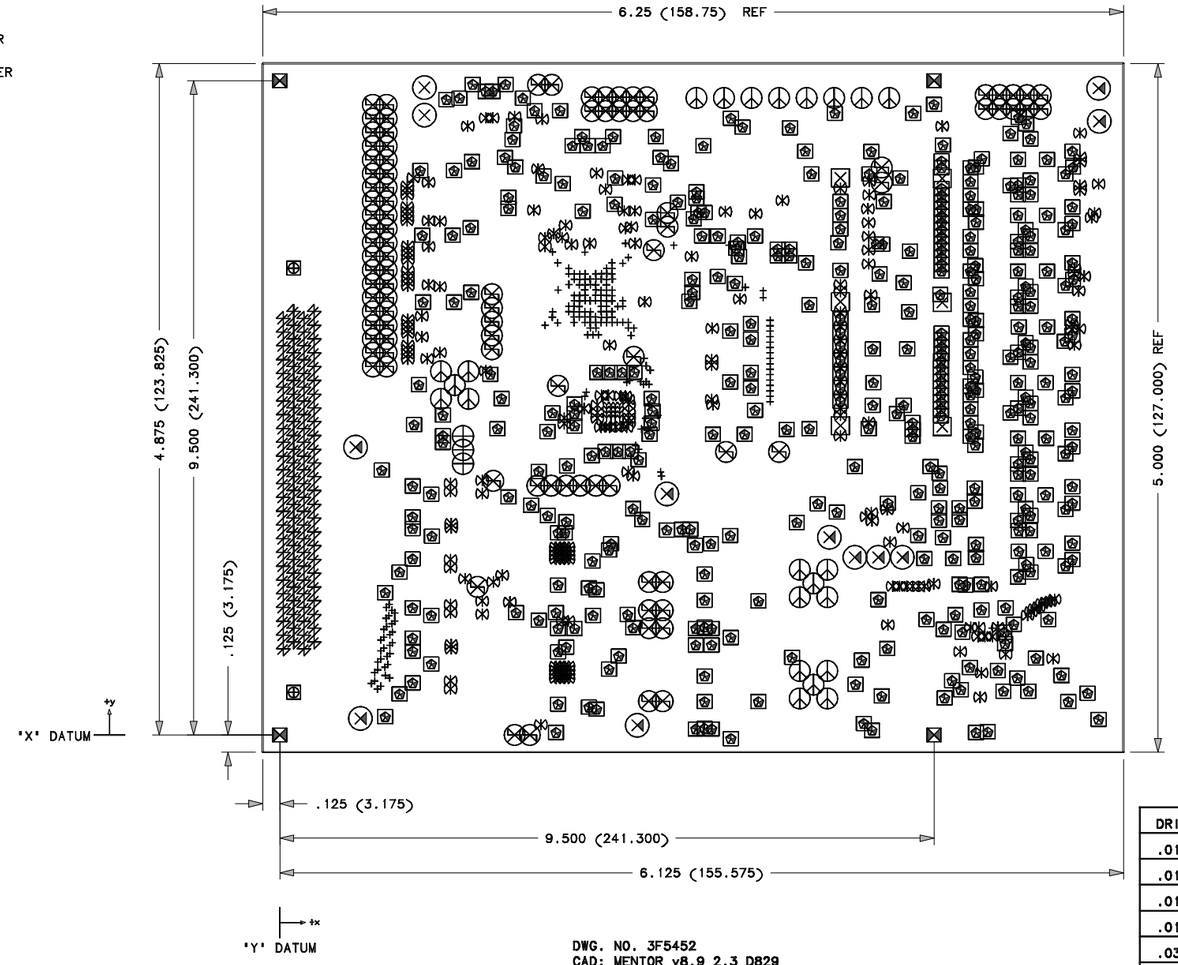
7. SOLDERMASK:
   7.1 SOLDERMASKING OF PRIMARY AND SECONDARY SIDES OF THE BOARD SHALL BE PER MASKING ARTWORK OVER BARE COPPER (SMOBC) USING PHOTOIMAGEABLE PERMANENT POLYMER FILM PER IPC-SM-840, CLASS T, 0.001 - 0.002 THICK.
   7.2 RESIZING FOR MINIMAL LAND TO MASK CLEARANCE PERMISSIBLE.

8. MARKING:
   8.1 MARKING OF PRIMARY AND SECONDARY SIDES SHALL BE PER MARKING ARTWORK USING WHITE NON-CONDUCTIVE EPOXY INK.

9. BOARD WARPAGE:
   9.1 BOARD WARPAGE 0.75% MAX.

10. TESTING:
   10.1 BOARDS SHALL BE TESTED USING CAD SUPPLIED IPC-D-356 FORMAT NET LIST. ELECTRICAL TESTING SHALL FOLLOW GUIDELINES ESTABLISHED BY IPC-ET-652.

11. MISCELLANEOUS NOTES:
   11.1 X,Y DATUMS INDICATE DRILL ORIGIN
   11.2 TEST COUPONS TO BE MADE AVAILABLE UPON REQUEST

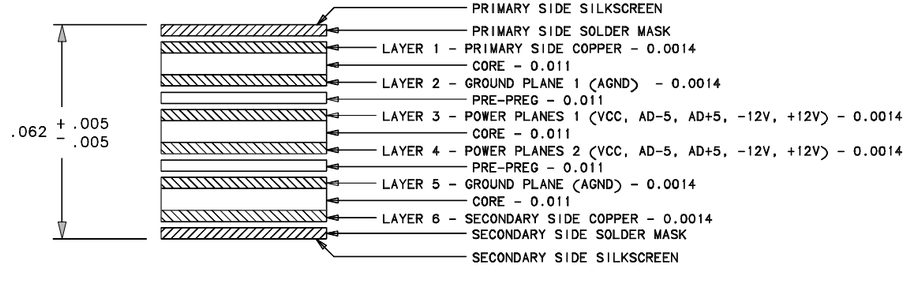


DWG. NO. 3F5452
CAD: MENTOR v8.9_2.3 D829
AD 9945 TIMING BOARD
HOLE SYMBOLOGY
REV 1
VIEWED FROM PRIMARY SIDE
Jan 28 2005

BOARD's DRILL SCHEDULE

DRILL SIZE	DRILL SYMBOL	PLATED	COUNT	
.010	+	YES	126	VIA
.012	Y	YES	16	
.013	⊠	YES	250	VIA
.015	⊡	YES	413	VIA
.034	⊹	YES	100	
.038	⊕	YES	3	
.042	⊗	YES	91	
.046	⊗	YES	2	
.050	⊠	YES	6	
.052	⊕	YES	18	
.065	⊗	YES	11	
.110	⊡	YES	2	
.125	⊠	YES	4	

TOTAL DRILL COUNT ON BOARD: 1042



DETAIL A

LAYER STACKING CONFIGURATION
SCALE = NONE

REF: DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1982.

DIMENSIONS APPLY AFTER FINISH WHERE TOTAL TOLERANCE IS .001 INCHES OR LESS AND ON ALL THREADS. IN ALL OTHER PLACES DIMENSIONS APPLY BEFORE FINISH.

DEVIATIONS FROM INTENDED SHAPE (FLATNESS, ROUNDNESS, SQUARENESS ETC.), MUST BE WITHIN STATED DIMENSIONAL TOLERANCES

3E8461 — NEXT ASSY | USED ON — APPLICATION | 1 — NEXT ASSY | FINAL ASSY — QUANTITY REQD

MATERIAL:

UNLESS OTHERWISE SPECIFIED
DATUM PRECEDENCE PRI A SEC B TER C
DIMENSIONS ARE IN INCHES (mm)
TOLERANCES
ANGLES ± 5° | 1 PL ± N/A
2 PL ± .010 | 3 PL ± .005
THIRD ANGLE PROJECTION

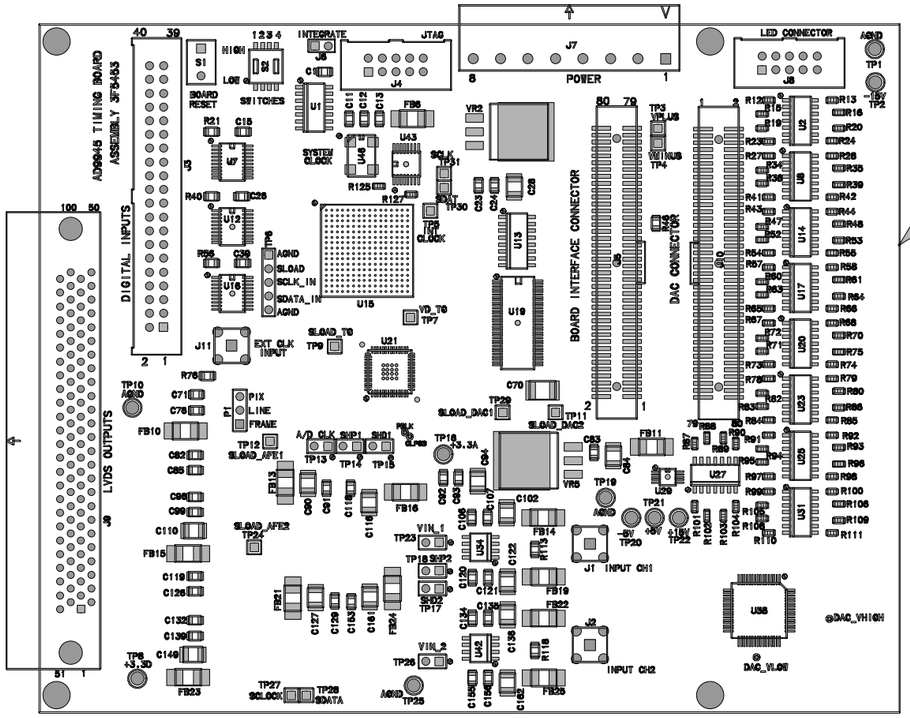
DWN	E.LEIGHT	
DFTG	R.BROLLY	
ENGR	R.BROLLY	
ENGR	X.XXXXX	XXXXXXXX
CHK	X.XXXXX	XXXXXXXX
APVD	X.XXXXX	XXXXXXXX
APVD	X.XXXXX	XXXXXXXX
APVD	X.XXXXX	XXXXXXXX
APVD	X.XXXXX	XXXXXXXX
CONTRACT #		

ON Semiconductor

TITLE: PCB, AD9945 TIMING BOARD

SIZE D | ITEM NO 3F5592 | REV 1

CODE | WT | SCALE 2X | SH 1 OF 3



1

PRIMARY SIDE VIEW

SCALE: 1X

CHG NO. DATE REL	REVISIONS	DWN BY APPS
REV 1	INITIAL DESIGN	RG

SEE SHEET FOR ADD'L REVISIONS

ON Semiconductor

FIRST USED ON

NAME CIRCUIT BOARD ASSEMBLY

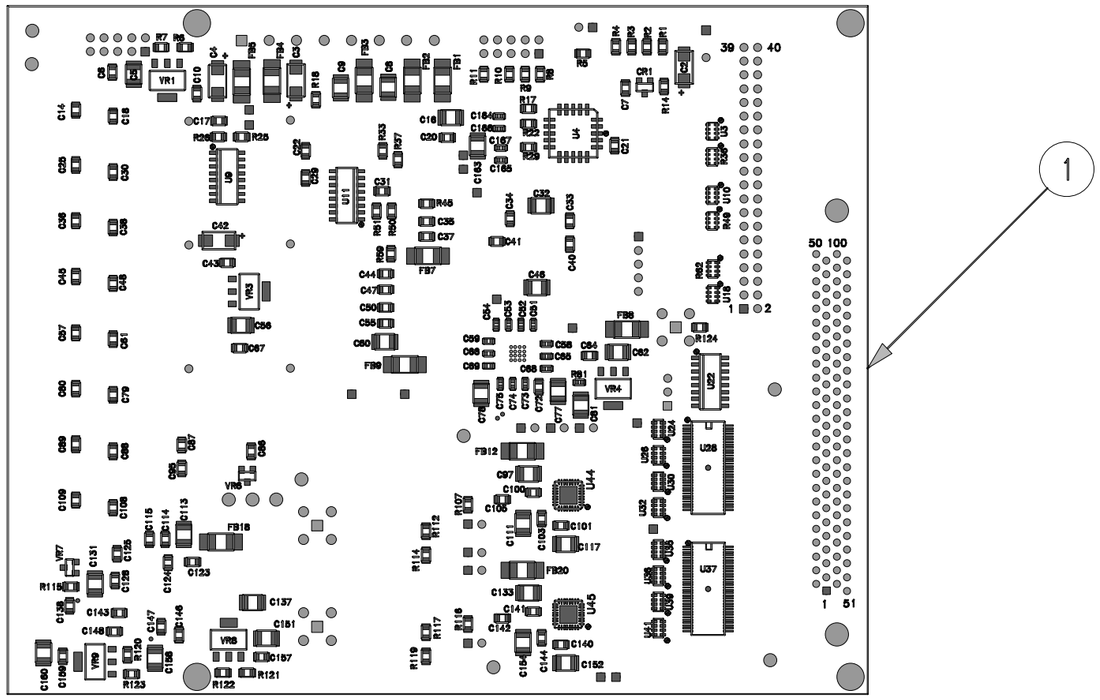
AD 9945 TIMING BOARD

DR. D829	DATE 1/26/05
DES. ENG.	PKG. MATL.
CK. DFTG. RG	MFG. ENG.
ORIG. CHG. NO. RELEASED	

SKETCH NO. | DWG. SIZE B

3F5592 REV 1

SHEET 8 NEXT SHEET 9



SECONDARY SIDE VIEW

SCALE: 1X

CHG NO. DATE REL	REVISIONS	DWN BY APPS
REV 1	INITIAL DESIGN	RG

SEE SHEET FOR ADD'L REVISIONS

ON Semiconductor

FIRST USED ON

NAME CIRCUIT BOARD ASSEMBLY

AD 9945 TIMING BOARD

DR. D829 DATE 1/26/05

DES. ENG.

PKG. MATL.

CK. DFTG. RG

MFG. ENG.

ORIG. CHG. NO. RELEASED

SKETCH NO.

DWG. SIZE B

3F5592 REV 1

SHEET 9 NEXT SHEET 0