NLPS591

Fully-Configurable Port Companion for Displays

The NLPS591 is a fully−configurable port companion for display applications. The device supports 4 externally selectable modes: (1) 4−Ch autosensing logic level translator mode, (2) CRT mode, (3) HDMI mode and (4) DisplayPort (DP) mode. The device provides switchable power to the connected display and the level shifting necessary for the different display modes. It also provides high−level ESD protection on the connector side.

Features

- Modes supported:
  - 4−Ch Logic Level Translator (LT) Mode
  - CRT Mode
  - HDMI Mode
  - DisplayPort (DP) Mode
- Wide V_{CCA} Operating Range: 1.65 V to 5.5 V
- Wide V_{IN} Range: 3.0 to 5.5 V (Power Modes)
  1.65 V to 5.5 V (Level Translator Mode)
- Low R_{DSON} Load Switch: 300 mΩ @ V_{IN} = 3.3 V
- Soft−start Control for Load Switch
- Protection Provided: Overcurrent, Overvoltage, Backdrive
- Power Consumption: < 10 mW with Load Switch On
  < 1 mW with Load Switch Off
- High Drive VESA−compliant Translator SYNC Level Translators in CRT Mode
- Integrated Pull−ups for the Autosensing Bidirectional Translators
- Low Input Capacitance for Translator Inputs: C_{IN} < 10 pF
- Small, Space Saving Package
  - 1.8 mm x 2.6 mm WQFN16
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications

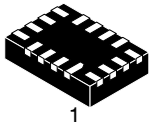
- Laptops, Desktops
- Tablets, SmartPhones

Important Information

- ESD Protection for All Pins
  - Human Body Model (HBM) > 2000 V

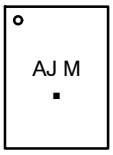
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WQFN16
CASE 488AP

MARKING DIAGRAM



AJ = Specific Device Code
M = Date Code
▪ = Pb−Free Package

ORDERING INFORMATION

Device	Package	Shipping†
NLPS591MNTWG	WQFN16 (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

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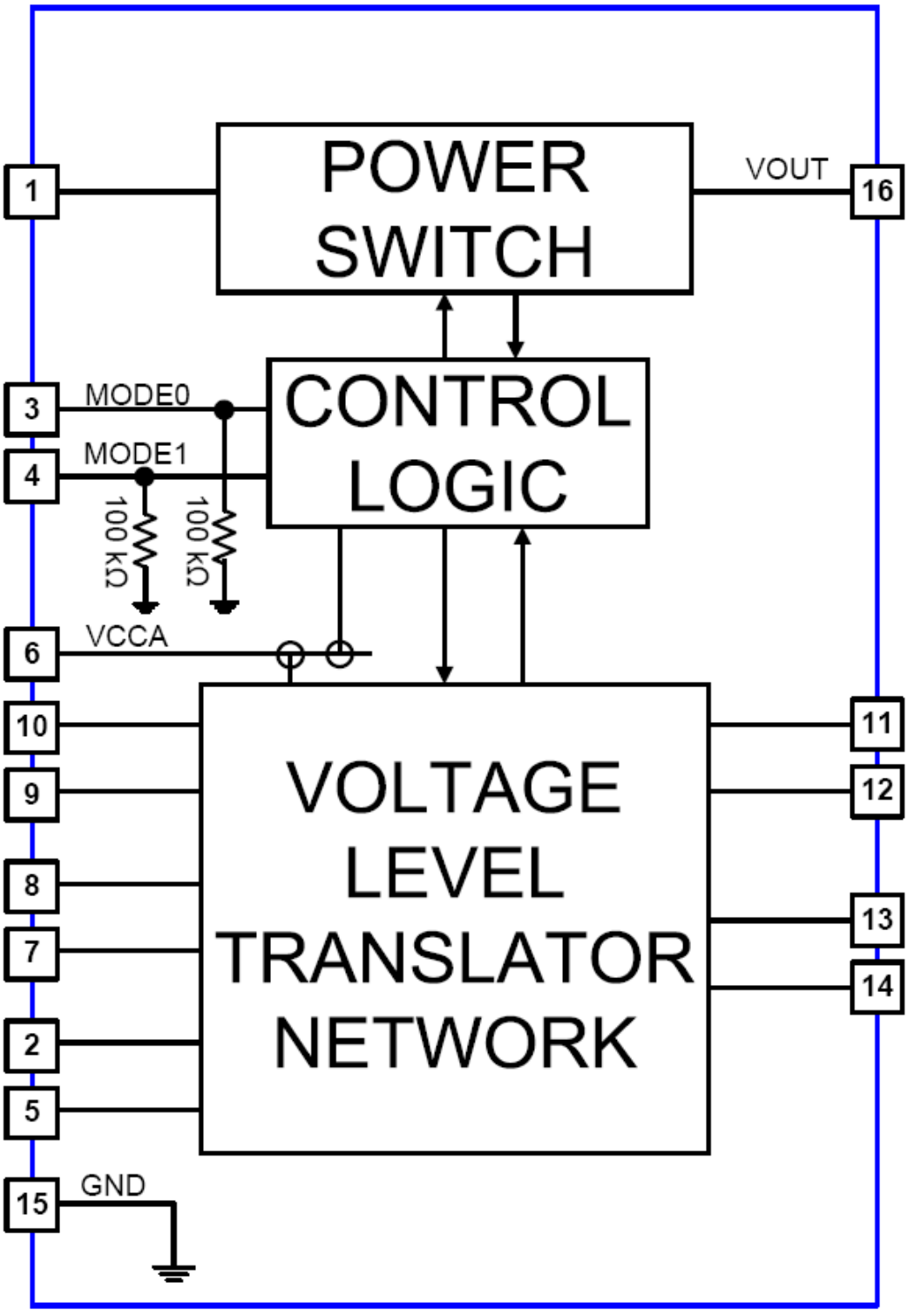


Figure 1. Function Diagram

PINOUT DIAGRAM

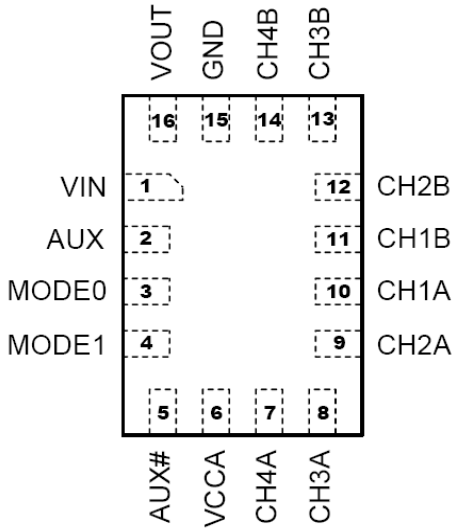


Figure 2. WQFN16 (Top−Through View)

Table 1. PIN DESCRIPTIONS

Pin		Pin Function per Mode				
Name	**Number**	**LT**	**DP0**	**DP1**	**HDMI**	**CRT**
VIN	1	VCC_I2C_1_B	VIN	VIN	VIN	VIN
AUX	2	VCC_I2C_0_B	AUX_A	–	CEC3V	–
MODE0	3	“0”	“0”	“0”	“1”	“1”
MODE1	4	“0”	“1”	“1”	“0”	“1”
AUX#	5	CH_EN	AUX_A#	–	CH_EN	CH_EN
VCCA	6	VCCA	VCCA	VCCA	VCCA	VCCA
CH4A	7	I2C_0_SDA_A	–	DDC_DATA_A	DDC_DATA_A	DDC_DATA_A
CH3A	8	I2C_0_SCL_A	–	DDC_CLK_A	DDC_CLK_A	DDC_CLK_A
CH2A	9	I2C_1_SDA_A	HPD_A	HPD_A	HPD_A	HSYNC_A
CH1A	10	I2C_1_SCL_A	–	–	CEC_A	VSYNC_A
CH1B	11	I2C_1_SCL_B	CA_DET_B = 0	CA_DET_B = 1	CEC_B	VSYNC_B
CH2B	12	I2C_1_SDA_B	HPD_B	HPD_B	HPD_B	HSYNC_B
CH3B	13	I2C_0_SCL_B	AUX_B	DDC_CLK_B	DDC_CLK_B	DDC_CLK_B
CH4B	14	I2C_0_SDA_B	AUX_B#	DDC_DATA_B	DDC_DATA_B	DDC_DATA_B
GND	15/EP*	GND	GND	GND	GND	GND
VOUT	16	–	VOUT	VOUT	VOUT	VOUT

* EP − Exposed Pad for QFN−16 Package is connected to GND.

Table 2. MODE FUNCTION TABLE

Input		Operating Mode
MODE0	**MODE1**	
0	0	Level Translator − LT (Default)
0	1	DisplayPort − DP
1	0	HDMI
1	1	CRT

OPERATING MODES

Level Translator Mode – LT (Default Mode)

When MODE0 = 0 and MODE1 = 0, the NLPS591 enters level translator mode. In this mode, the power switch is always off.

When CH_EN = 1, the device is configured as an autosensing 4−channel bidirectional logic level translator. The function diagram is shown below. The A−side I/Os are referred to VCCA (pin 6). The B−side I/Os are referred to either VCC_I2C_1_B (pin 1) or VCC_I2C_0_B (pin 2).

When CH_EN = 0, the 4−ch level translator is disabled, and the I/O pins (pins 7, 8, 9, 10, 11,12, 13, 14) go into high−impedance.

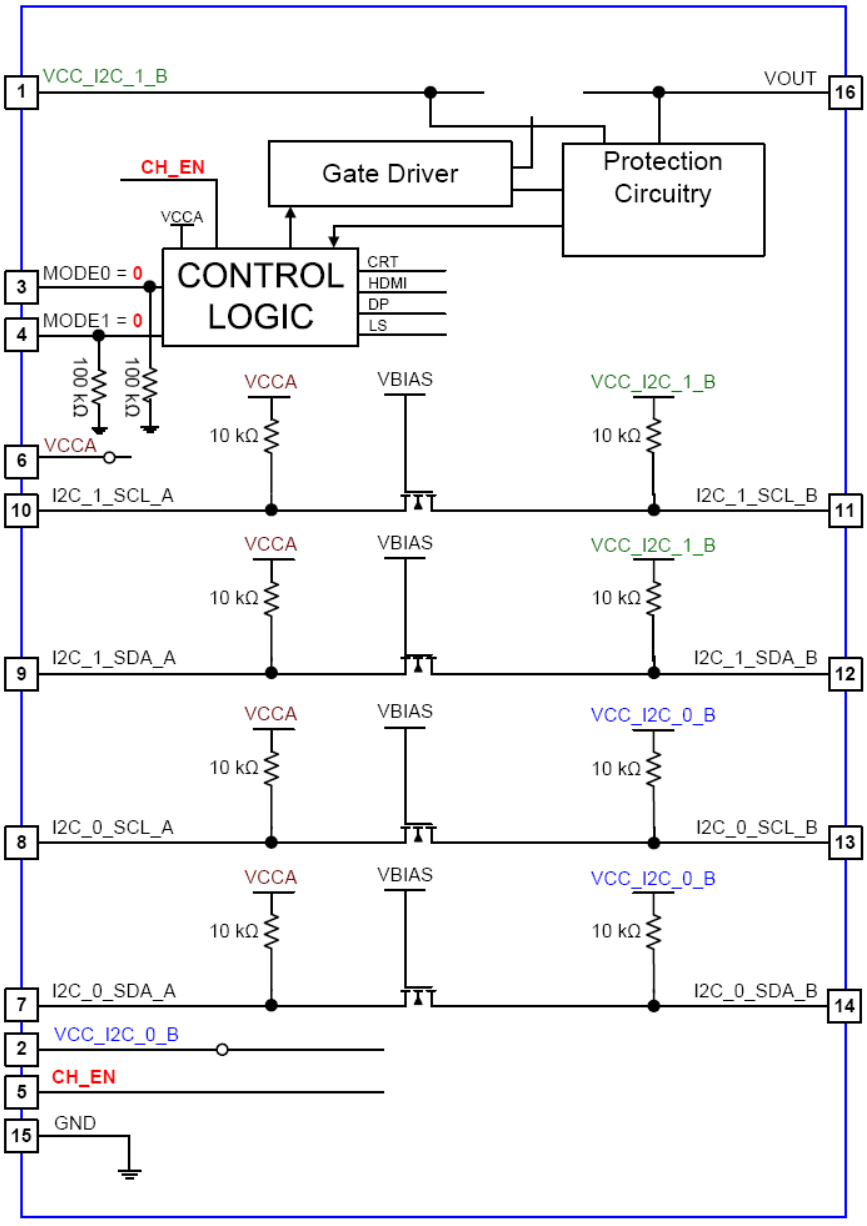


Figure 3. Function Diagram − LT Mode

DP Mode

When MODE0 = 0 and MODE1 = 1, the NLPS591 enters DP (DisplayPort) mode. The device is configured as a DP−compliant logic level translator for the control signals. A power switch provides power to the connected display. An unidirectional translator for HPD is provided.

A CA_DET_B input is provided to detect the use of an HDMI dongle. When there is no HDMI dongle attached (CA_DET_B = 0), the device goes into DP0 sub−mode, where AUX and AUX# signals are passed. The function diagram is shown below.

DP0 Sub−Mode

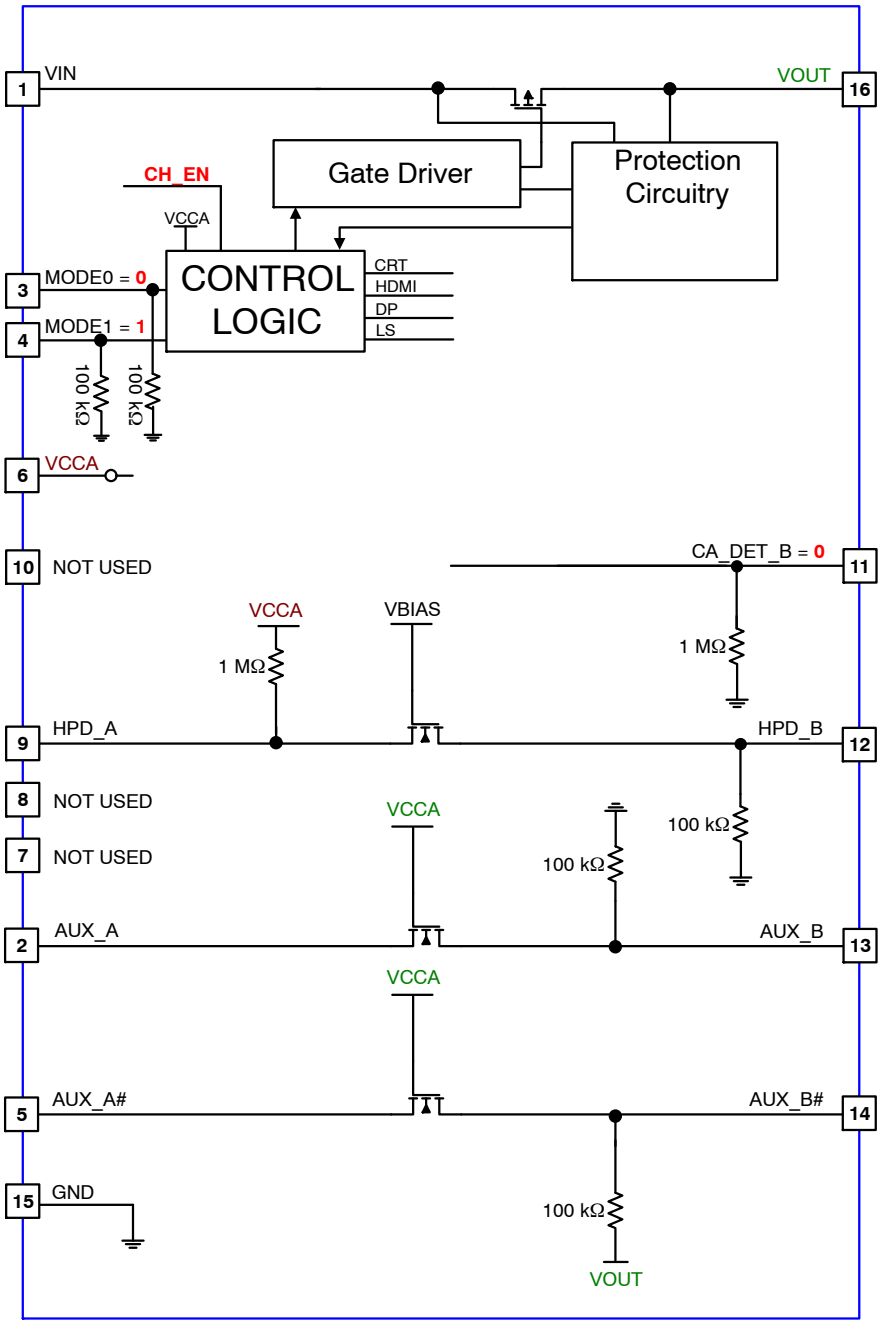


Figure 4. Function Diagram − DP0 Sub−Mode

When an HDMI dongle is attached (CA_DET_B = 1), the device enters DP1 sub−mode. Two autosensing bidirectional logic level translators for DDC signals are provided. A−side I/Os are referred to VCCA (pin 1), while B−side I/Os are referred to VOUT (pin 16). The function diagram is shown below.

DP1 Sub−Mode

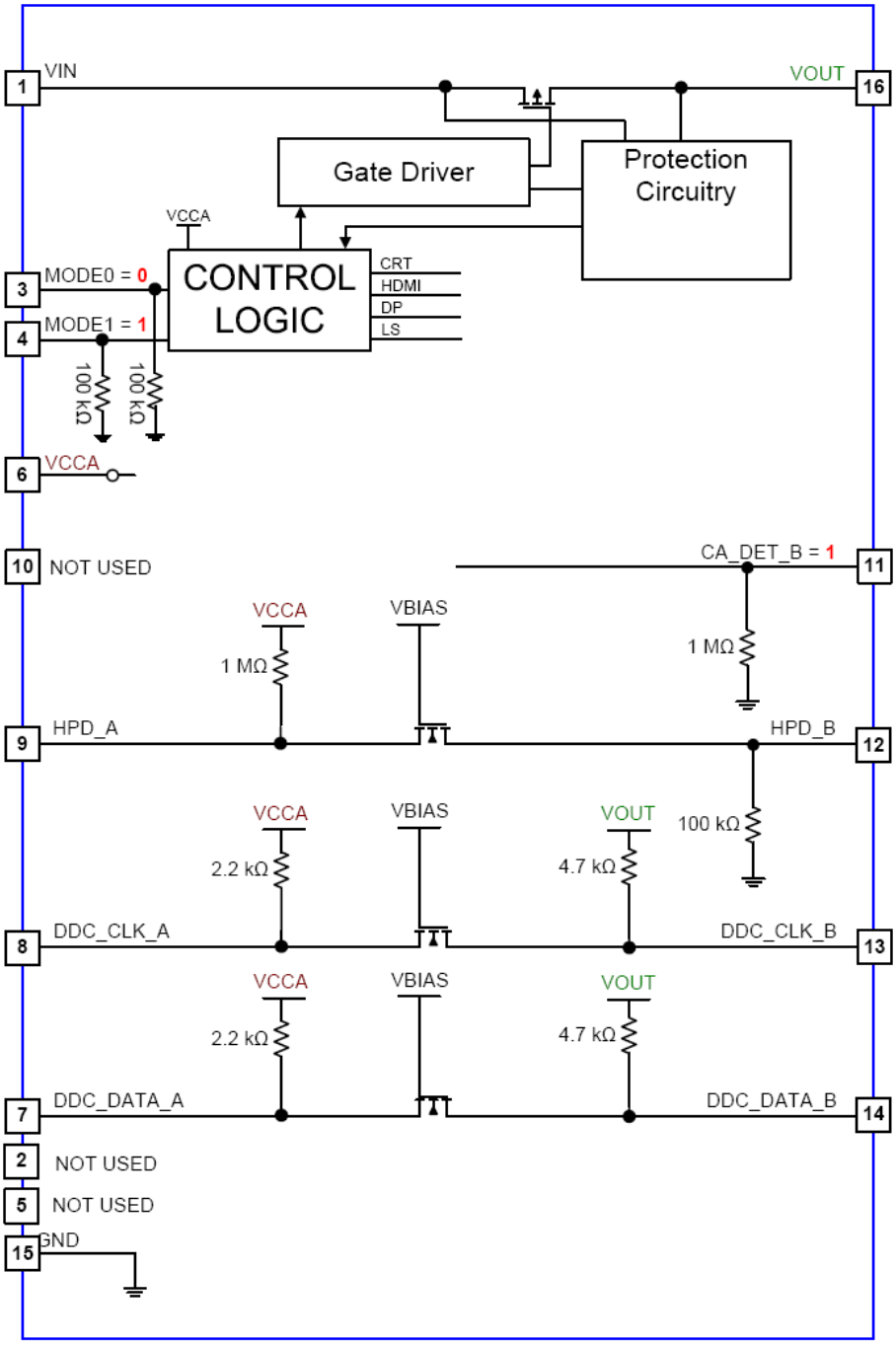


Figure 5. Function Diagram – DP1 Sub−Mode

HDMI Mode

When MODE0 = 1 and MODE1 = 0, the NLPS591 enters HDMI mode.

When CH_EN = 1, the device is configured as a HDMI−compliant logic level translator for the control signals. An unidirectional translator for HPD and three autosensing bidirectional level translators for the DDC and CEC signals are provided. A−side I/Os are referred to VCCA (pin 1), while B−side I/Os, except for CEC_B, are referred to VOUT (pin 16). A CEC3V (pin 2) input is also provided to power the connector−side pull−up of the CEC translator. A power switch provides power to the connected display. The function diagram is shown below.

When CH_EN = 0, the device is disabled. The power switch turns off, VOUT is pulled to GND, and the I/O pins (pins 7, 8, 9, 10, 11,12, 13, 14) go into high−impedance.

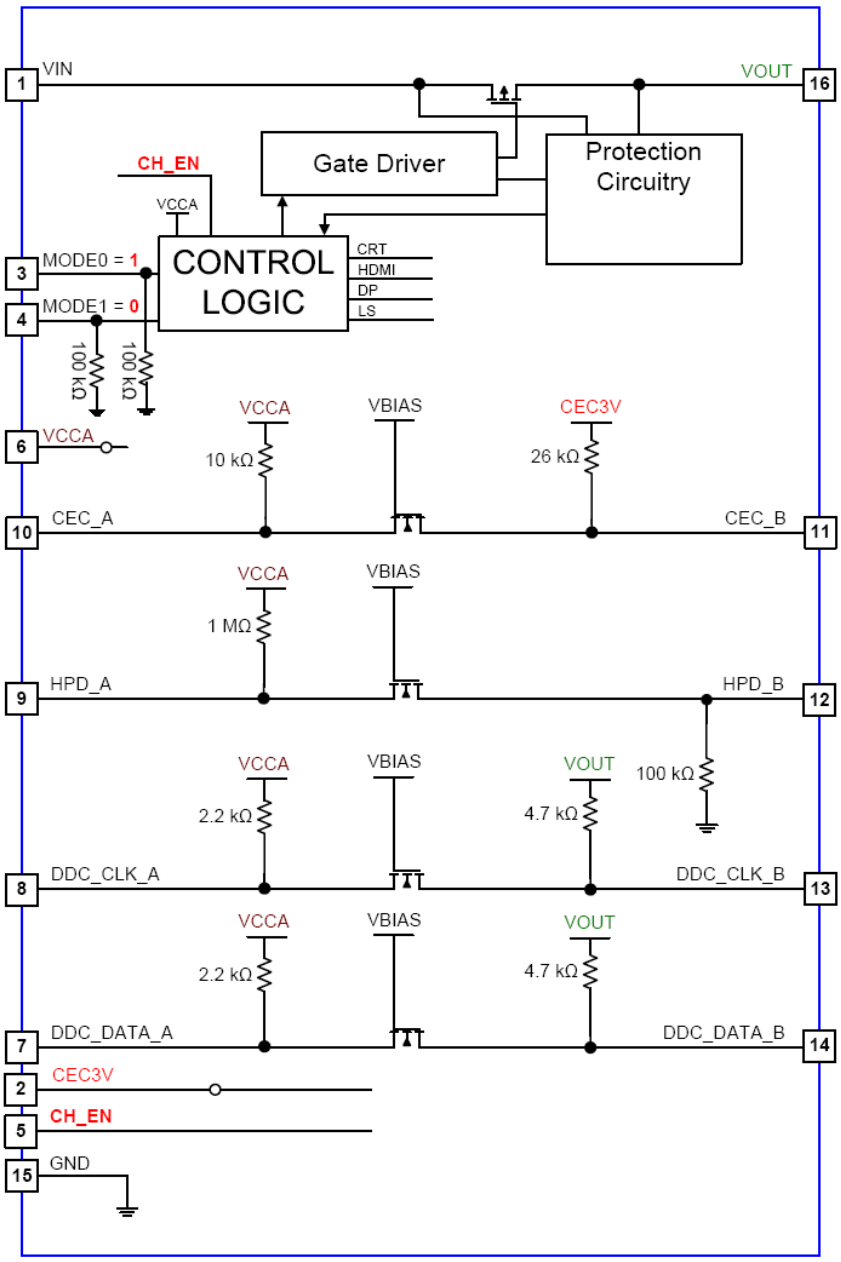


Figure 6. Function Diagram – HDMI Mode

CRT Mode

When MODE0 = 1 and MODE1 = 1, the NLPS591 enters CRT mode.

When CH_EN = 1, the device is configured as a VESA−compliant logic level translator for the CRT control signals. Two unidirectional high−drive translators for the HSYNC and VSYNC signals and two autosensing bidirectional level translators are provided for the DDC signals. A power switch provides power to the connected display. The function diagram is shown below.

When CH_EN = 0, the device is disabled. The power switch turns off, VOUT is pulled to GND and the I/O pins (pins 7, 8, 9, 10, 11,12, 13, 14) go into high−impedance.

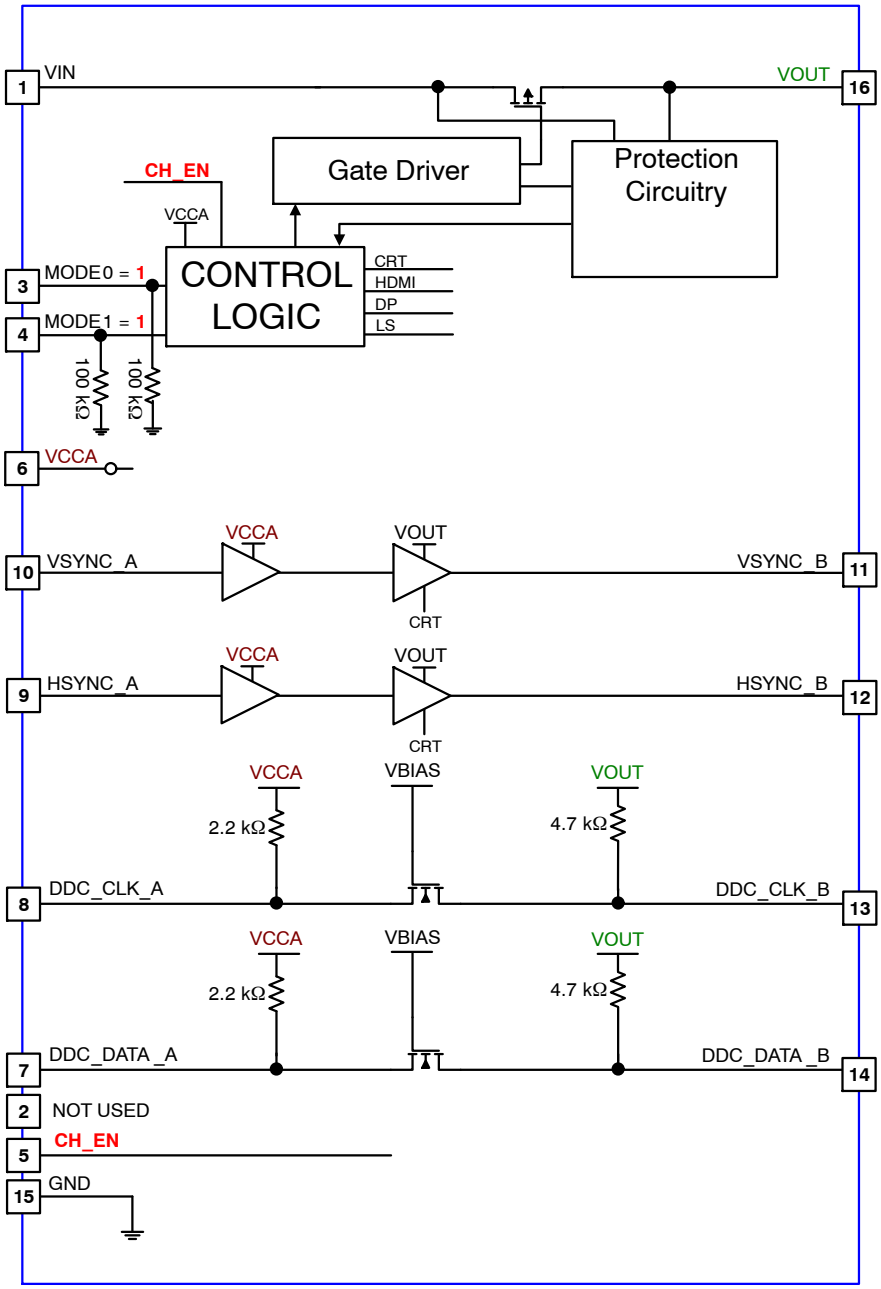


Figure 7. Function Diagram – CRT Mode

Power Switch

A power switch is provided for CRT, HDMI and DP modes, but not for LT mode. The power switch is used to provide power to a connected display. In the CRT and HDMI modes, the power may be turned on or off under user control through the CH_EN pin. When the power switch starts turning on, VOUT is held LOW momentarily before VOUT is released and follows VIN.

In the DP Mode, the CH_EN is not available, hence, the power switch is always on.

The output (VOUT) of the power switch is current−limited. The switch is protected against extended exposure to high current flows by a thermal shutdown protection circuit. The switch is back−drive protected preventing reverse current flow from VOUT to VIN.

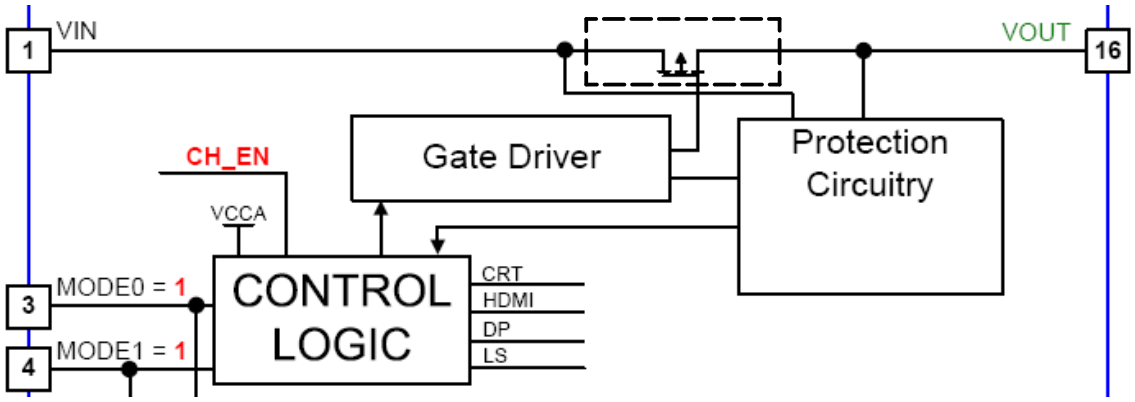


Figure 8. Function Diagram – Power Switch

Table 3. MAXIMUM RATINGS

Symbol	Parameter	Value	Condition	Unit
VIN / CEC3V / VCC_I2C_0_B / VCC_I2C_1_B	DC Supply Voltage	−0.5 to +7.0		V
V_{CCA}	Logic DC Supply Voltage	−0.5 to +7.0		V
V_{OUT}	Load Switch Output Voltage	−0.5 to +7.0		V
V_{IOA}	A−Side DC Input/Output Voltage (Power Down)	−0.5 to +7.0	V_{CCA} = 0 V	V
	(Active)	−0.5 to (V_{CCA} + 0.5)	V_{CCA} Active	
V_{IOB}	B−Side DC Input/Output Voltage (Power Down)	−0.5 to +7.0	V_{CCB} (Note 1) = 0 V	V
	(Active)	−0.5 to (V_{CCB} (Note 1) + 0.5)	V_{CCB} (Note 1) Active	
T_{STG}	Storage Temperature	−65 to +150		°C
ESD	ESD Protection Connector−Side (VOUT, CH1B, CH2B, CH3B, CH4B) All Other Pins	 8 2		kV

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Table 4. RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CCA}	Logic DC Supply Voltage	1.65	5.5	V
V_{IN}	Load Switch Input Voltage LT Mode	1.65	5.5	V
	CRT / HDMI Mode	4.5	5.5	
	DP Mode	3.0	3.6	
V_{OUT}	Load Switch Output Voltage	GND	5.5	V
V_{IOA}	A−Side DC Input/Output Voltage (Power Down)	GND	5.5	V
	(Active)	GND	V_{CCA}	
V_{IOB}	B−Side DC Input/Output Voltage (Power Down)	GND	5.5	V
	(Active)	GND	V_{CCB} (Note 1)	
$\Delta t/\Delta V$	Input Transition Rise and Fall Rate A− or B−Ports, Push−Pull Driving		100	ns/V
	Control Input		10	
T_A	Operating Temperature Range	−40	+85	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

1. V_{CCB} refers to the supply powering the translator B−side I/O pin. This supply could be VOUT, CEC3V, VCC_I2C_0_B or VCC_I2C_1_B, depending on the device function mode.

Table 5. DC ELECTRICAL CHARACTERISTICS (V_{CCA} = 1.65 V to 5.5 V, V_{CCB} (Note 2) = 1.65 V to 5.5 V, unless otherwise specified)

Symbol	Parameter	Test Conditions (Note 2)	–40°C to +85°C			Unit
			Min	Typ (Notes 2, 3)	Max	
CONTROL PINS – MODE0, MODE1						
V_{IH}	Input HIGH Voltage		2/3 * V_{CCA}			V
V_{IL}	Input LOW Voltage				1/3 * V_{CCA}	V
I_{IH}	Input HIGH Leakage	VCCA = 5.5 V		55	70	μA
I_{IL}	Input LOW Leakage	VCCA = 5.5 V			1	μA
CONTROL PIN – AUX# (CH_EN in LT, HDMI and CRT Modes)						
V_{IH}	Input HIGH Voltage		2/3 * V_{CCA}			V
V_{IL}	Input LOW Voltage				1/3 * V_{CCA}	V
I_{IL}	Input Leakage Current	VCCA = 5.5 V			±1	μA
POWER SWITCH (VIN = 3.0 V to 5.5 V)						
R_{DSON}	Static ON−State Resistance	VIN = 5 V, I_{LOAD} < 300 mA			240	mΩ
		VIN = 3.3 V, I_{LOAD} < 300 mA			300	
t_R	Output Rise Time	VIN = 5 V, I_{LOAD} = 100 mA	0.2		1.0	ms
t_F	Output Fall Time	VIN = 5 V, I_{LOAD} = 100 mA			0.01	ms
t_{ON}	Gate Turn−On Time	VIN = 5 V, From VIN applied to VOUT = 10% of fully on		0.5	1.5	ms
		VIN = 3.3 V, From VIN applied to VOUT = 10% of fully on			1.7	
I_{REV}	Reverse Current Protection	V_{CCA} ≥ 1.65 V, Switch Enabled, No Load, (VOUT − VIN) ≥ 0.5 V (Note 4)			40	μA
I_{LIM}	Current Limit Threshold	ΔV_{SW} = 400 mV (Note 5)	0.45		0.8	A
t_{DET}	Response Time to Short Circuit	(Note 6)		5		μs
T_{SHUT}	Thermal Shutdown	Shutdown Threshold, TRIP Temperature		140		°C
		Hysteresis		12		
V_{OVP}	Output Overvoltage Protection	Trip Voltage		5.9		V
		Hysteresis		0.3		
LT Mode (I^2C Translator Channels) **CRT and DP1 Modes (DDC Translator Channels)** **HDMI Mode (CEC and DDC Translator Channels)**						
V_{IHA}	A Side Input High Voltage		V_{CCA} − 0.4			V
V_{IHB}	B Side Input High Voltage		V_{CCB} − 0.4			V
V_{ILA}	A Side Input Low Voltage				0.15	V
V_{ILB}	B Side Input Low Voltage				0.15	V
V_{OHA}	A Side Output High Voltage	A Side Source Current = 20 μA	2/3 * V_{CCA}			V
V_{OHB}	B Side Output High Voltage	B Side Source Current = 20 μA	2/3 * V_{CCB}			V
V_{OLA}	A Side Output Low Voltage	A Side Sink Current = 20 μA			1/3 * V_{CCA}	V
V_{OLB}	B Side Output Low Voltage	B Side Sink Current = 20 μA			1/3 * V_{CCB}	V
I_{OZA}	Output Leakage Current on A Side in “Disabled” Modes				1	μA
I_{OZB}	Output Leakage Current on B Side in “Disabled” Modes				1	μA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. Typical values are for V_{CCB} = +3.3 V, V_{CCA} = +1.8 V and T_A = +25°C. V_{CCB} may refer to VIN, AUX or VOUT depend on the operating mode.
3. All units are production tested at T_A = +25°C. Limits over the operating temperature range are guaranteed by design.
4. Reverse current protection is activated only when a reverse current threshold of about 200 mA is reached.
5. ΔV_{SW} is the voltage difference across the power switch.
6. Guaranteed by design.

Table 6. DC ELECTRICAL CHARACTERISTICS (V_{CCA} = 1.65 V to 5.5 V, V_{CCB} (Note 7) = 3.0 V to 5.5 V, unless otherwise specified)

Symbol	Parameter	Test Conditions (Note 7)	−40°C to +85°C			Unit
			Min	Typ (Notes 7, 8)	Max	
CRT Mode (HSYNC/VSYNC Unidirectional Translator Drivers)						
V_{IH}	Input HIGH Voltage	VCCA = 4.5 to 5.5 V	2.0			V
		VCCA = 3.0 to 3.6 V	1.8			
		VCCA = 2.3 to 2.7 V	1.6			
		VCCA = 1.65 to 1.95 V	1.4			
V_{IL}	Input LOW Voltage	VCCA = 4.5 to 5.5 V			0.8	V
		VCCA = 3.0 to 3.6 V			0.7	
		VCCA = 2.3 to 2.7 V			0.5	
		VCCA = 1.65 to 1.95 V			0.3	
V_{OH}	Output HIGH Voltage	$V_I = V_{IH}$, I_{OH} = − 20 μA	V_{OUT} − 0.1			V
		I_{OH} = − 24 mA	2.0			
V_{OL}	Output LOW Voltage	$V_I = V_{IL}$, I_{OL} = 20 μA			0.1	V
		I_{OL} = 24 mA			0.8	
HPD Driver (HPD_B to HPD_A Translator for DP and HDMI Modes)						
V_{IH}	Input HIGH Voltage	VCCA ≤ 2 V; VOUT ≥ 3 V; R_{HPD_B2VOUT} ≤ 40 kΩ, HPD_A Open	2.0			V
V_{IL}	Input LOW Voltage	VCCA ≤ 2 V; VOUT ≥ 3 V; R_{HPD_B2VOUT} ≤ 40 kΩ, HPD_A Open			0.4	V
V_{OH}	Output HIGH Voltage	$V_I = V_{IH}$, I_{OH} = −0.1 μA	V_{CCA} − 0.5			V
V_{OL}	Output LOW Voltage	$V_I = V_{IL}$, I_{OL_SINK} = 20 μA			V_{IL}+0.1	V
CA_DET_B Input (CH1B for DP Modes)						
V_{IH}	Input HIGH Voltage		1.0			V
V_{IL}	Input LOW Voltage				0.35	V
I_{IH}	Input HIGH Leakage	VCCA = 5.5 V		5.5	7.0	μA
I_{IL}	Input LOW Leakage	VCCA = 5.5 V			1	μA
DP0 Mode (AUX, AUXN Level Shifters) See Figures 16 and 17.						
R_{ON}	ON−State Resistance	I_{LOAD} = 5mA, V_{CCA} = 3.0 V, VI = 1.3 V to 1.7 V		10	40	Ω
		I_{LOAD} = 5mA, V_{CCA} = 4.5 V, VI = 2.7 V to 3.1 V		4	10	

7. Typical values are for V_{CCB} = +3.3 V, V_{CCA} = +1.8 V and T_A = +25°C. V_{CCB} may refer to VIN, AUX or VOUT depend on the operating mode.
8. All units are production tested at T_A = +25°C. Limits over the operating temperature range are guaranteed by design.

Table 7. DC ELECTRICAL CHARACTERISTICS (V_{CCA} = 1.65 V to 5.5 V, V_{CCB} (Note 9) = 1.65 V to 5.5 V, unless otherwise specified)

Symbol	Parameter	Test Conditions (Note 9)	−40°C to +85°C			Unit
			Min	Typ (Notes 9, 10)	Max	
SUPPLY AND LEAKAGE CURRENTS						
I_{VCCA}	V_{CCA} Supply Current	LT Mode: VIN = 5.5 V, AUX = 5.5 V, AUX# = V_{IHA} or V_{ILA}, all other pins open			75	μA
		DP Mode: VIN = 3.3 V, all other pins left open			130	
		HDMI Mode: VIN = 5 V, AUX# = V_{IHA} or V_{ILA}, all other pins left open			130	
		CRT Mode: VIN = 5 V, AUX# = V_{IHA} or V_{ILA}, CH1A = CH2A = 0 V, all other pins left open			10	
I_{VIN}	V_{IN} Supply Current	LT Mode: VIN = 1.65 to 5.5 V, V_{CCA} = AUX = 5.5 V, AUX# = V_{IHA} or V_{ILA}, all other pins left open			60	μA
I_{OZ}	I/O Tristate Leakage Current	LT, HDMI or CRT Mode: CH_EN = L		0.1	1.0	μA
I_{OFF}	I/O Power−Off Leakage Current	All Modes: V_{CCB} = 0 V, V_{CCA} = 0 to 5.5 V, or V_{CCB} = 0 to 5.5 V, V_{CCA} = 0 V			1.0	μA

9. Typical values are for V_{CCB} = +3.3 V, V_{CCA} = +1.8 V and T_A = +25°C. V_{CCB} may refer to VIN, AUX or VOUT depend on the operating mode.
10. All units are production tested at T_A = +25°C. Limits over the operating temperature range are guaranteed by design.

Table 8. PULLUP / PULLDOWN RESISTOR CONFIGURATIONS

	Typical, T_A = +25°C (Ω)				
	Function Mode				
Pin / Mode	**LT**	**CRT**	**HDMI**	**DP0 (AUX)**	**DP1**
CH1A	10K to VCCA		10K to VCCA	Hi−Z	Hi−Z
CH2A	10K to VCCA		1M to VCCA	1M to VCCA	1M to VCCA
CH3A	10K to VCCA	2.2 K to VCCA	2.2K to VCCA	Hi−Z	2.2K to VCCA
CH4A	10K to VCCA	2.2 K to VCCA	2.2K to VCCA	Hi−Z	2.2K to VCCA
CH1B	10K to VIN		26K to CEC3V	1M to GND	1M to GND
CH2B	10K to VIN		100K to GND	100K to GND	100K to GND
CH3B	10K to AUX	4.7K to VOUT	4.7 K to VOUT	100K to GND	4.7K to VOUT
CH4B	10K to AUX	4.7K to VOUT	4.7 K to VOUT	100K to VOUT	4.7K to VOUT
AUX	Hi−Z	Hi−Z	Hi−Z		Hi−Z
AUXN	Hi−Z	Hi−Z	Hi−Z		Hi−Z

Table 9. TIMING CHARACTERISTICS in Rail−to−Rail Driving Configuration for Bidirectional Transfer Channels:
CH1, CH2, CH3, CH4 in LT Mode for VCCA = 1.65 V to 5.5 V and VCCB = 1.65 V to 5.5 V;
CH3, CH4 in DP1 Mode for VCCA = 1.65 V to 5.5 V and VCCB = 3.0 V to 3.6 V;
CH1, CH3, CH4 in HDMI Mode for VCCA = 1.65 V to 5.5 V and VCCB = 4.5 V to 5.5 V;
CH3, CH4 in CRT Mode for VCCA = 1.65 V to 5.5 V and VCCB = 4.5 V to 5.5 V.
(R_{PU_INT} = 10 kΩ, C_{LOAD} = 15 pF, driver output impedance ≤ 50 Ω, R_{LOAD} = 50 kΩ, unless otherwise specified.
See Figures 9, 10, 13, 14 and 15.)

Parameter	Symbol	Conditions	−40°C to +85°C						Unit
			V_{CCB} = 1.65 V to 1.95 V		V_{CCB} = 3.0 V to 3.6 V		V_{CCB} = 4.5 V to 5.5 V		
			Min	Max	Min	Max	Min	Max	
V_{CCA} = 1.65 V to 1.95 V									
A Side Rise Time	t_{RA}			32		25		22.6	nS
B Side Rise Time	t_{RB}			32		24		17	nS
A Side Fall Time	t_{FA}			7		6		15	nS
B Side Fall Time	t_{FB}			4.7		12.2		25	nS
A Side to B Side Propagation Delay	t_{PDA-B}			20		14		13	nS
B Side to A Side Propagation Delay	t_{PDB-A}			20		15		12	nS
Translator Enable Time (Note 11)	t_{PZH}, t_{PZL}	CH_EN = H		100		90		120	nS
Translator Disable Time (Note 11)	t_{PHZ}, t_{PLZ}	CH_EN = L		220		370		500	nS
Maximum Data Rate	MDR		20		20		20		Mbps
V_{CCA} = 3.0 V to 3.6 V									
A Side Rise Time	t_{RA}			16		13		12.3	nS
B Side Rise Time	t_{RB}			25		14		9	nS
A Side Fall Time	t_{FA}			9		4		3.5	nS
B Side Fall Time	t_{FB}			6		4		5	nS
A Side to B Side Propagation Delay	t_{PDA-B}			15		3.5		6.3	nS
B Side to A Side Propagation Delay	t_{PDB-A}			14		4		3	nS
Translator Enable Time (Note 11)	t_{PZH}, t_{PZL}	CH_EN = H		80		30		30	nS
Translator Disable Time (Note 11)	t_{PHZ}, t_{PLZ}	CH_EN = L		600		200		330	nS
Maximum Data Rate	MDR		20		20		20		Mbps
V_{CCA} = 4.5 V to 5.5 V									
A Side Rise Time	t_{RA}			17		13.5		10.5	nS
B Side Rise Time	t_{RB}			23		13.3		8	nS
A Side Fall Time	t_{FA}			13		5		3	nS
B Side Fall Time	t_{FB}			20		9.6		3	nS
A Side to B Side Propagation Delay	t_{PDA-B}			13		4		6.5	nS
B Side to A Side Propagation Delay	t_{PDB-A}			13		6		7	nS
Translator Enable Time (Note 11)	t_{PZH}, t_{PZL}	CH_EN = H		85		20		20	nS
Translator Disable Time (Note 11)	t_{PHZ}, t_{PLZ}	CH_EN = L		200		350		260	nS
Maximum Data Rate	MDR		20		20		20		Mbps

11. These parameters apply to the LT, HDMI and CRT modes only. The power switch turn−on time should be added to translator enable time for HDMI and CRT modes. Maximum CH_EN frequency is 10 kHz with minimum high pulse duration of 30 μs.

Table 10. TIMING CHARACTERISTICS in Open Drain Driving Configuration for Bidirectional Transfer Channels:
CH1, CH2, CH3, CH4 in LT Mode for VCCA = 1.65 V to 5.5 V and VCCB = 1.65 V to 5.5 V;
CH3, CH4 in DP1 Mode for VCCA = 1.65 V to 5.5 V and VCCB = 3.0 V to 3.6 V;
CH1, CH3, CH4 in HDMI Mode for VCCA = 1.65 V to 5.5 V and VCCB = 4.5 V to 5.5 V;
CH3, CH4 in CRT Mode for VCCA = 1.65 V to 5.5 V and VCCB = 4.5 V to 5.5 V.
(R_{PU_INT} = 10 kΩ, C_{LOAD} = 15 pF, driver output impedance ≤ 50 Ω, R_{LOAD} = 1 MΩ, unless otherwise specified.
See Figures 11, 12, 13, 14 and 15.)

Parameter	Symbol	Conditions	−40°C to +85°C						Unit
			V_{CCB} = 1.65 V to 1.95 V		V_{CCB} = 3.0 V to 3.6 V		V_{CCB} = 4.5 V to 5.5 V		
			Min	Max	Min	Max	Min	Max	
V_{CCA} = 1.65 V to 1.95 V									
A Side Rise Time	t_{RA}	R_{PU_INT} = 10 kΩ		145		110		200	nS
B Side Rise Time	t_{RB}			155		110		200	nS
A Side Fall Time	t_{FA}			20		15		20	nS
B Side Fall Time	t_{FB}			20		28		38	nS
A Side to B Side Propagation Delay	t_{PHLA-B}			10		15		17	nS
	t_{PLHA-B}			50		40		40	
B Side to A Side Propagation Delay	t_{PHLB-A}			10		10		14	nS
	t_{PLHB-A}			50		10		12	
Translator Enable Time (Note 12)	t_{PZH}, t_{PZL}	CH_EN = H		30		25		22	nS
Translator Disable Time (Note 12)	t_{PHZ}, t_{PLZ}	CH_EN = L		60		82		80	nS
Maximum Data Rate	MDR		2		2		2		Mbps
V_{CCA} = 3.0 V to 3.6 V									
A Side Rise Time	t_{RA}	R_{PU_INT} = 10 kΩ		105		130		105	nS
B Side Rise Time	t_{RB}			135		130		170	nS
A Side Fall Time	t_{FA}			25		20		20	nS
B Side Fall Time	t_{FB}			25		20		30	nS
A Side to B Side Propagation Delay	t_{PHLA-B}			10		10		15	nS
	t_{PLHA-B}			20		10		17	
B Side to A Side Propagation Delay	t_{PHLB-A}			15		25		15	nS
	t_{PLHB-A}			30		10		10	
Translator Enable Time (Note 12)	t_{PZH}, t_{PZL}	CH_EN = H		34		15		16	nS
Translator Disable Time (Note 12)	t_{PHZ}, t_{PLZ}	CH_EN = L		72		80		80	nS
Maximum Data Rate	MDR		2		2		2		Mbps
V_{CCA} = 4.5 V to 5.5 V									
A Side Rise Time	t_{RA}	R_{PU_INT} = 10 kΩ		85		90		125	nS
B Side Rise Time	t_{RB}			120		110		130	nS
A Side Fall Time	t_{FA}			40		30		30	nS
B Side Fall Time	t_{FB}			25		20		30	nS
A Side to B Side Propagation Delay	t_{PHLA-B}			12		11		20	nS
	t_{PLHA-B}			10		10		5	
B Side to A Side Propagation Delay	t_{PHLB-A}			25		15		20	nS
	t_{PLHB-A}			30		10		8	
Translator Enable Time (Note 12)	t_{PZH}, t_{PZL}	CH_EN = H		30		13		10	nS
Translator Disable Time (Note 12)	t_{PHZ}, t_{PLZ}	CH_EN = L		100		75		70	nS
Maximum Data Rate	MDR		2		2		2		Mbps

12. These parameters apply to the LT, HDMI and CRT modes only. The power switch turn−on time should be added to translator enable time for HDMI and CRT modes. Maximum CH_EN frequency is 10 kHz with minimum high pulse duration of 30 μs.

Table 11. TIMING CHARACTERISTICS for HSYNC/VSYNC Drivers (CH1, CH2 in CRT Mode)
(VCCA = 1.65 V to 5.5 V, VCCB = 4.5 V, C_{LOAD} = 15 pF, driver output impedance ≤ 50 Ω, R_{LOAD} = 50 kΩ, t_R ≤ 3 ns and t_F ≤ 3 ns, unless otherwise specified. See Figures 9, 13, 14 and 15.)

Parameter	Symbol	Conditions	−40°C to +85°C						Unit
			V_{CCB} = 1.65 V to 1.95 V		V_{CCB} = 3.0 V to 3.6 V		V_{CCB} = 4.5 V to 5.5 V		
			Min	Max	Min	Max	Min	Max	
V_{CCA} = 1.65 V to 1.95 V									
A Side to B Side Propagation Delay	t_{PDA-B}							13	nS
B Side Rise Time	t_{RB}							5	nS
B Side Fall Time	t_{FB}							4	nS
Output Enable Time (Note 13)	t_{PZH}, t_{PZL}	CH_EN = H						1.2	mS
Output Disable Time	t_{PHZ}, t_{PLZ}	CH_EN = L						130	nS
Maximum Data Rate	MDR						90		Mbps
V_{CCA} = 3.0 V to 3.6 V									
A Side to B Side Propagation Delay	t_{PDA-B}							6	nS
B Side Rise Time	t_{RB}							6	nS
B Side Fall Time	t_{FB}							4	nS
Output Enable Time (Note 13)	t_{PZH}, t_{PZL}	CH_EN = H						0.65	mS
Output Disable Time	t_{PHZ}, t_{PLZ}	CH_EN = L						130	nS
Maximum Data Rate	MDR						100		Mbps
V_{CCA} = 4.5 V to 5.5 V									
A Side to B Side Propagation Delay	t_{PDA-B}							6	nS
B Side Rise Time	t_{RB}							5	nS
B Side Fall Time	t_{FB}							4	nS
Output Enable Time (Note 13)	t_{PZH}, t_{PZL}	CH_EN = H						0.61	mS
Output Disable Time	t_{PHZ}, t_{PLZ}	CH_EN = L						130	nS
Maximum Data Rate	MDR						120		Mbps

13. Output Enable Time takes into account turn−on time of the power switch. Maximum CH_EN frequency is 10 kHz with minimum high pulse duration of 30 μs.

Table 12. TIMING CHARACTERISTICS for AUX_A/AUX#_A to AUX_B/AUX#_B (AUX−CH3B [AUX_A−AUX_B], AUX#−CH4B [AUX_A#−AUX_B#] in DP0 Mode) (VCCA = 1.65 V to 5.5 V and VOUT = 3.0 V to 3.6 V. See Figures 16 and 17.)

Parameter	Symbol	Conditions	−40°C to +85°C						Unit
			V_{OUT} = 1.65 V to 1.95 V		V_{OUT} = 3.0 V to 3.6 V		V_{OUT} = 4.5 V to 5.5 V		
			Min	Max	Min	Max	Min	Max	
V_{CCA} = 1.65 V to 1.95 V									
B Side Rise Time	t_{RB}	V_{IH} = 0.65 V, V_{IL} = 0.25 V				2.5			nS
B Side Fall Time	t_{FB}					2.5			nS
A Side to B Side Propagation Delay	t_{PDA-B}					0.2			nS
Maximum Data Rate	MDR				100				Mbps
V_{CCA} = 3.0 V to 3.6 V									
B Side Rise Time	t_{RB}	V_{IH} = 2.0 V, V_{IL} = 1.6 V				2.5			nS
B Side Fall Time	t_{FB}					2.5			nS
A Side to B Side Propagation Delay	t_{PDA-B}					0.1			nS
Maximum Data Rate	MDR				100				Mbps
V_{CCA} = 4.5 V to 5.5 V									
B Side Rise Time	t_{RB}	V_{IH} = 3.5 V, V_{IL} = 3.1 V				2.5			nS
B Side Fall Time	t_{FB}					2.5			nS
A Side to B Side Propagation Delay	t_{PDA-B}					0.05			nS
Maximum Data Rate	MDR				100				Mbps

Test Setups

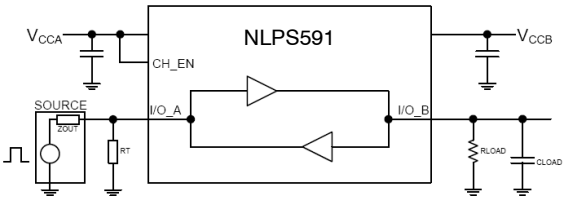


Figure 9. Rail−to−Rail Driving A−side I/O

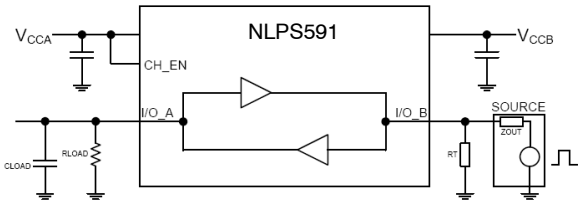


Figure 10. Rail−to−Rail Driving B−side I/O

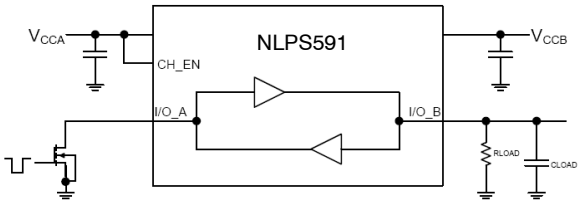


Figure 11. Open−Drain Driving A−side I/O

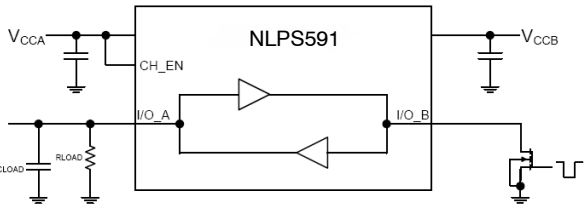


Figure 12. Open−Drain Driving B−side I/O

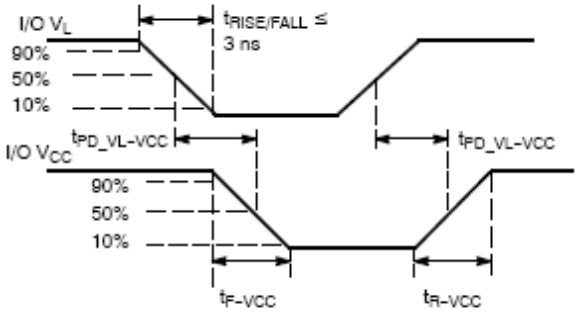
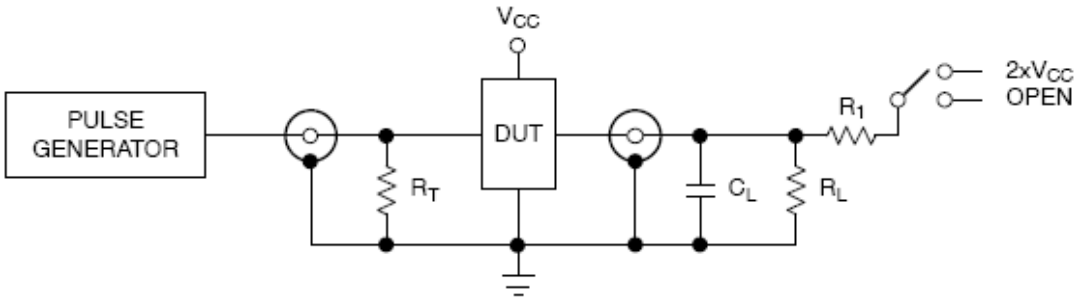


Figure 13. Definition of Timing Specification Parameters



Test	Switch
t_{PZH}, t_{PHZ}	Open
t_{PZL}, t_{PLZ}	2 x V_{CC}

C_L = 15 pF or equivalent (Includes jig and probe capacitance)
R_L = R_1 = 50 kΩ or equivalent
R_T = Z_{OUT} of pulse generator (typically 50 Ω)

Figure 14. Test Circuit for Translator Enable/Disable Time Measurements

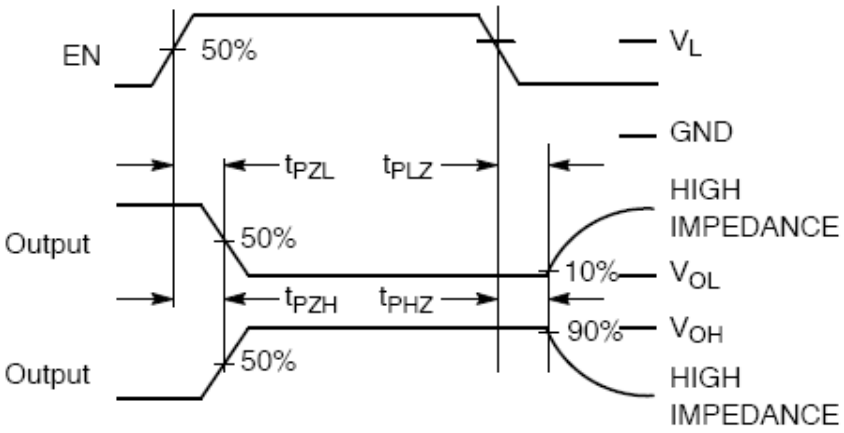


Figure 15. LT, HDMI, CRT Mode Translator Enable/Disable Time Definition

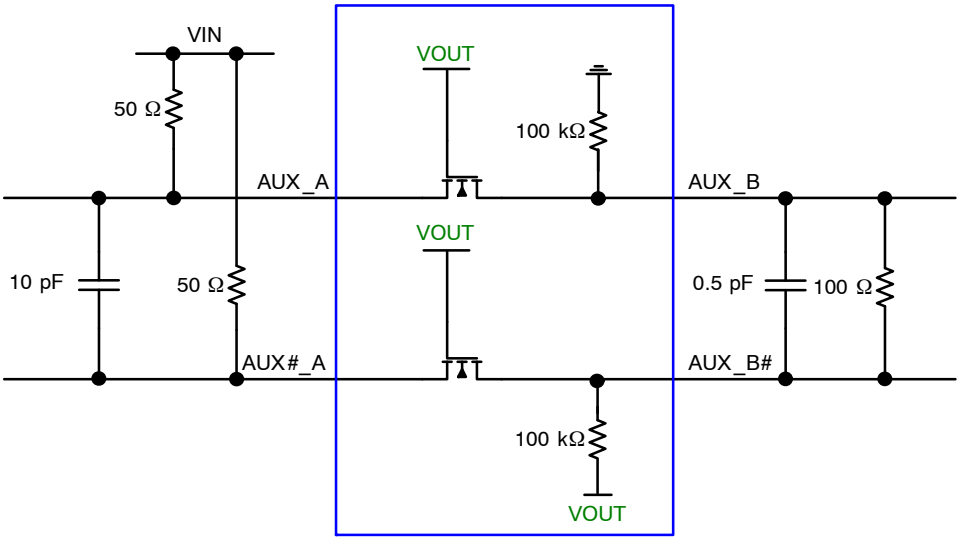


Figure 16. DP0 Mode AUX Channels Test Circuit

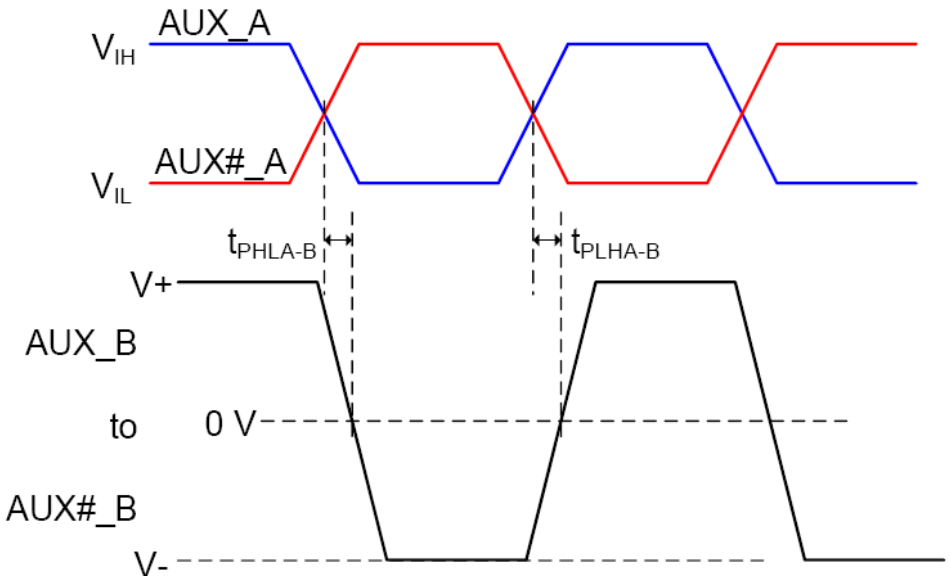
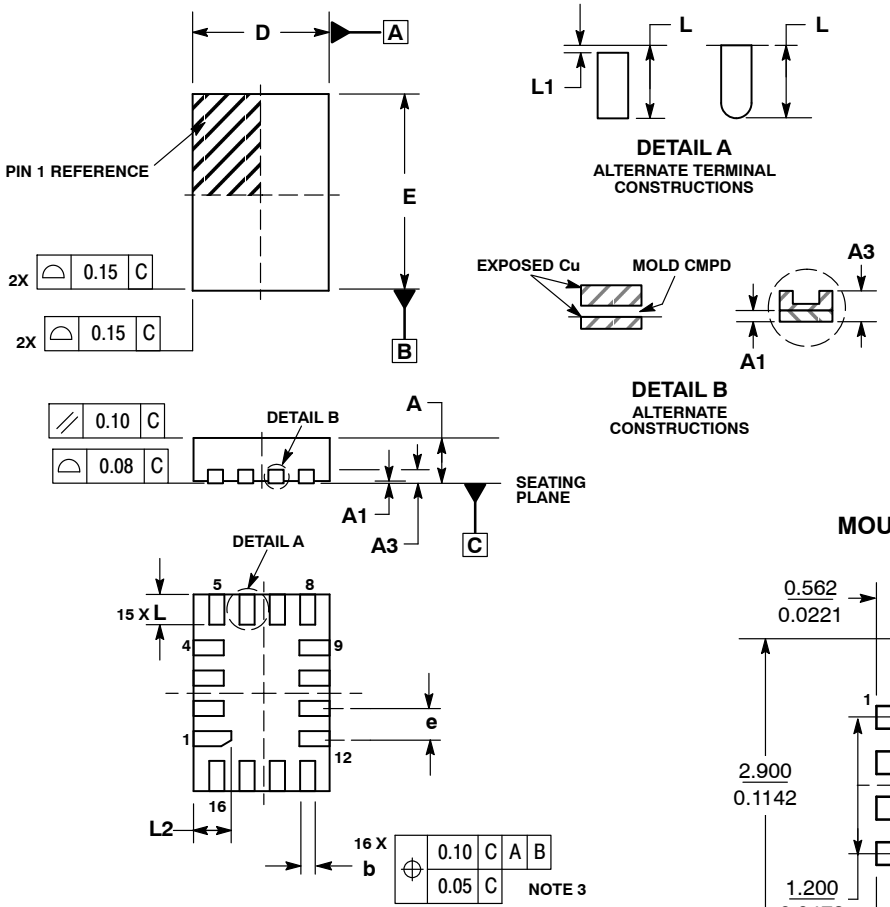


Figure 17. DP0 Mode AUX Channels Propagation Delay Definition

PACKAGE DIMENSIONS

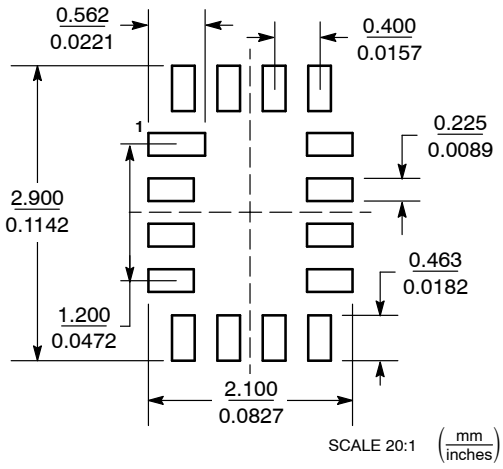
WQFN16, 1.8x2.6, 0.4P
CASE 488AP
ISSUE B



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. EXPOSED PADS CONNECTED TO DIE FLAG. USED AS TEST CONTACTS.

DIM	MILLIMETERS MIN	MAX
A	0.70	0.80
A1	0.00	0.050
A3	0.20 REF	
b	0.15	0.25
D	1.80 BSC	
E	2.60 BSC	
e	0.40 BSC	
L	0.30	0.50
L1	0.00	0.15
L2	0.40	0.60

MOUNTING FOOTPRINT*



For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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