ANALOG DEVICES

Circuit Note
CN-0383

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Devices Connected/Referenced	
AD7124-4/ AD7124-8	4-Channel/8-Channel, Low Noise, Low Power, 24-Bit, Sigma-Delta ADCs with PGA and Reference
ADP1720	50 mA, High Voltage, Micropower Linear Regulator

Completely Integrated 3-Wire RTD Measurement System Using a Low Power, Precision, 24-Bit Sigma-Delta ADC

EVALUATION AND DESIGN SUPPORT

Circuit Evaluation Boards

AD7124-4 Evaluation Board (EVAL-AD7124-4SDZ) or AD7124-8 Evaluation Board (EVAL-AD7124-8SDZ)
System Demonstration Platform (EVAL-SDP-CB1Z)

Design and Integration Files

Schematics, Layout Files, Bill of Materials

CIRCUIT FUNCTION AND BENEFITS

The circuit shown in Figure 1 is an integrated 3-wire resistance temperature detector (RTD) system based on the AD7124-4/ AD7124-8 low power, low noise, 24-bit Σ-Δ analog-to-digital converter (ADC) optimized for high precision measurement applications. With a two-point calibration and linearization, the overall 3-wire system accuracy is better than ±1°C over a temperature range of −50°C to +200°C. Typical noise free code resolution of the system is 17.9 bits for full power mode, $sinc^4$ filter selected, at an output data rate of 50 SPS, and 16.8 bits for low power mode, post filter selected, at an output data rate of 25 SPS.

The AD7124-4 can be configured for 4 differential or 7 pseudo differential input channels, while the AD7124-8 can be configured for 8 differential or 15 pseudo differential channels. The on-chip programmable gain array (PGA) ensures that signals of small amplitude can be interfaced directly to the ADC.

The AD7124-4/AD7124-8 establishes the highest degree of signal chain integration, which includes programmable low drift excitation current sources. Therefore, the design of an RTD system is greatly simplified because most of the required RTD measurement system building blocks are included on-chip.

The AD7124-4/AD7124-8 gives the user the flexibility to employ one of three integrated power modes, where the current consumption, range of output data rates, and rms noise are tailored with the power mode selected. The current consumed by the AD7124-4/AD7124-8 is only 255 µA in low power mode and 930 µA in full power mode. The power options make the device suitable for non-power critical applications, such as input/output modules, and also for low power applications, such as loop-powered smart transmitters where the complete transmitter must consume less than 4 mA.

The device also has a power down option. In power-down mode, the complete ADC along with its auxiliary functions are powered down so that the device consumes 1 µA typical. The AD7124-4/ AD7124-8 also has extensive diagnostic functionality integrated as part of its comprehensive feature set.

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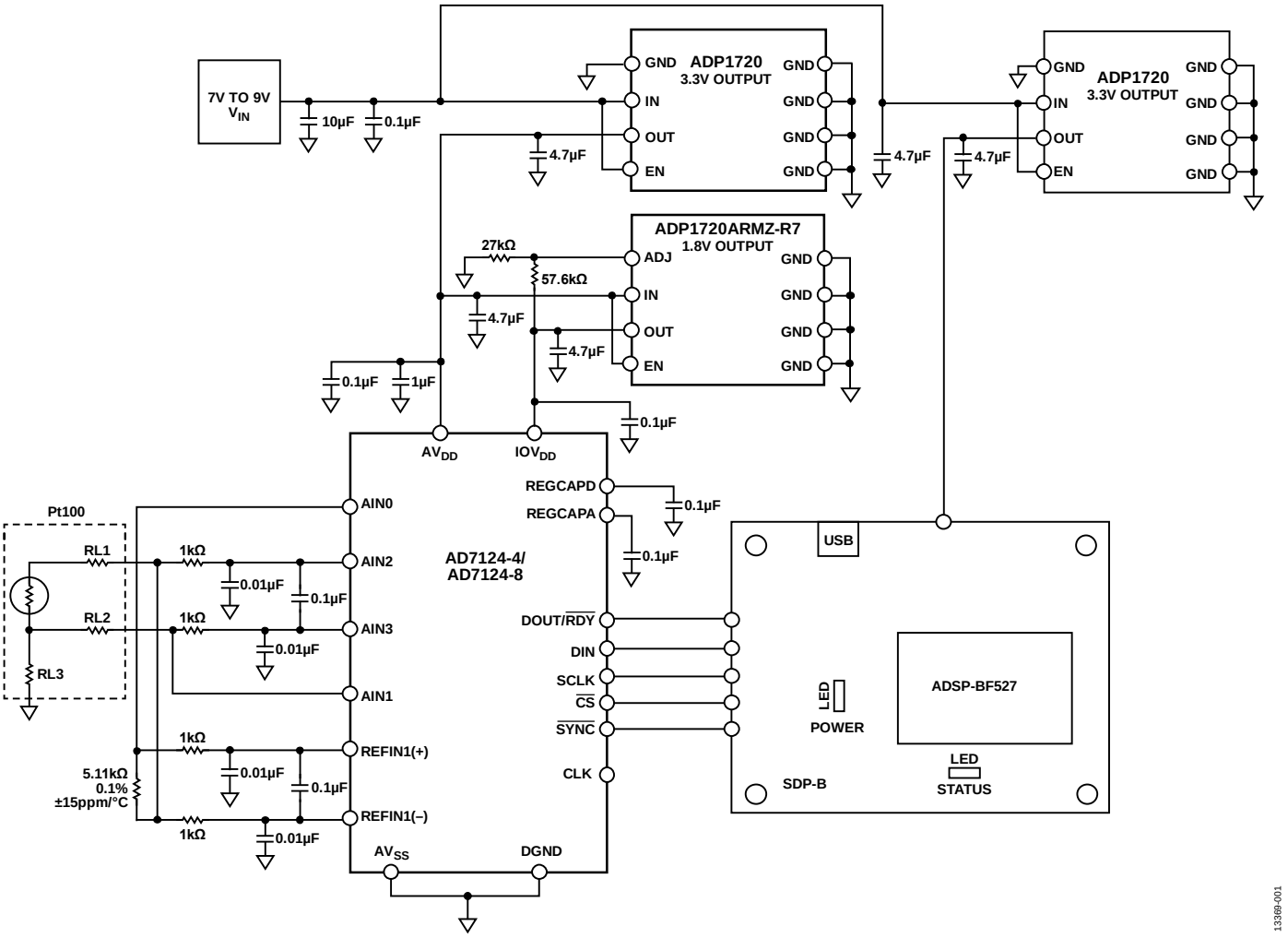

Figure 1. 3-Wire RTD Measurement Configuration

CIRCUIT DESCRIPTION

RTD Temperature Measurement Introduction

RTDs are frequently used sensors for temperature measurements in industrial applications. An RTD is made from a pure metal (examples include platinum, nickel, or copper), which has a predictable change in resistance as the temperature changes. The most widely used RTDs are platinum Pt100 and Pt1000. RTDs are capable of high accuracy and good stability when compared with other types of temperature sensors. The resistance of long wire lengths can be compensated for with a 3-wire connection.

To accurately measure the resistance, a voltage is generated across the RTD by a constant current source. The AD7124-4/AD7124-8 offers two such excitation current sources that are register programmable from 50 µA to 1 mA. Errors in the current source can be easily cancelled by referring the measurement to the voltage across a precision reference resistor that is driven with the same current source, thereby resulting in a ratiometric measurement result.

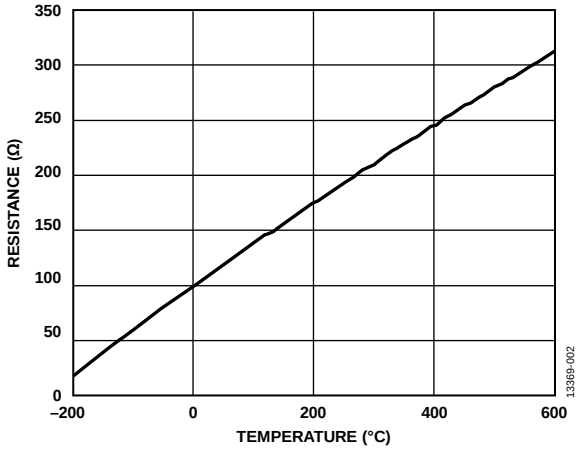

Figure 2. RTD Resistance vs. Temperature

For the circuit in Figure 1, a Class B Pt100 RTD sensor was used. Pt100 RTDs measure temperature from −200°C to +600°C. The resistance of a Class B RTD is typically 100 Ω at 0°C and has a typical temperature coefficient of ~0.385 Ω/°C (see Figure 2). Using this information, the voltage generated across the Pt100 RTD can easily be calculated based on the current source selected.

How the Circuit Works

The AD7124-4/AD7124-8 provides an integrated solution for RTD measurement. It can achieve high resolution, low non-linearity and low noise performance as well as very high 50 Hz and 60 Hz rejection. The AD7124-4/AD7124-8 consists of an on-chip, low noise PGA that amplifies the small signal from the RTD with a gain programmable from 1 to 128, thus allowing direct interface with the sensor. The gain stage has high input impedance and limits the input leakage current to 3.3 nA typical for full power mode and 1 nA typical for low power mode. The following section explain the different elements that make up the 3-wire RTD temperature measurement system.

Power Supplies

The AD7124-4/AD7124-8 has separate analog and digital power supplies. The digital power supply, IOV_{DD}, is independent of the analog power supply and can be from 1.65 V to 3.6 V referenced to DGND. The analog power supply, AV_{DD}, is referred to AV_{SS} and has a range of 2.7 V to 3.6 V for low and mid power modes, and 2.9 V to 3.6 V for full power mode. The circuit shown in Figure 1 operates from a single supply; therefore, AV_{SS} and DGND are connected together, and only one ground plane is used. The AV_{DD} and IOV_{DD} voltage are generated separately using ADP1720 voltage regulators. The AV_{DD} voltage is set to 3.3 V and the IOV_{DD} voltage is set to 1.8 V using the ADP1720 regulators. Using separate regulators ensures the lowest noise.

Serial Peripheral Interface (SPI)

SPI communications to the AD7124-4/AD7124-8 is handled by the Blackfin® ADSP-BF527 on the EVAL-SDP-CB1Z, as shown in Figure 1. To access the registers of the AD7124-4/AD7124-8, use the AD7124_Eval+ Software. Figure 3 shows the main window of this software. Clicking **3-WIRE RTD** configures the software for the 3-wire RTD measurement.

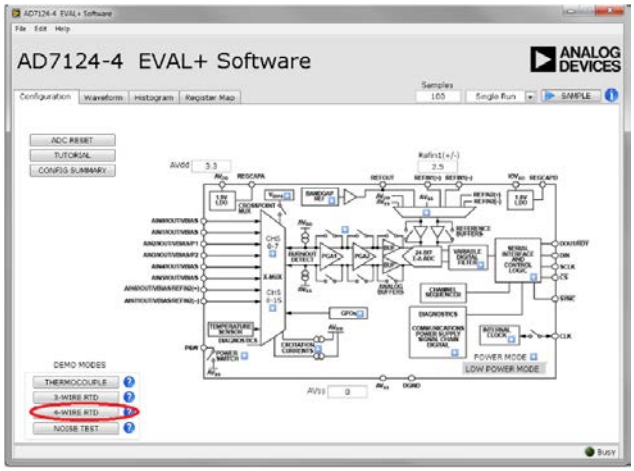

Figure 3. AD7124_Eval+ Software Configuration Screen

The AD7124-4/AD7124-8 has diagnostic functions on-chip that can be used to detect faults in the SPI communication. These diagnostics include checks on the SPI read and write operations, ensuring that only valid registers are accessed. An SCLK counter ensures that the correct number of SCLK pulses are used, while the CRC functionality checks for changes in bit values during transmission. When any of these SPI communication diagnostic functions are enabled and an associated error occurs, the corresponding flag is set in the error register. All enabled flags are OR'ed together and control the ERR flag in the status register. This functionality is particularly useful if the status bits are appended to the ADC conversions.

Analog Inputs and Reference

The AD7124-4 can be configured for 4 differential or 7 pseudo differential channels, while the AD7124-8 can be configured for 8 differential or 15 pseudo differential channels.

The AD7124-4/AD7124-8 has on-chip diagnostics that can be used to check that the voltage level on the analog pins are within the specified operating range. The positive (AINP) and negative (AINM) analog inputs can be separately checked for overvoltages and undervoltages, as well as ADC saturation. An overvoltage is flagged when the voltage on the analog input exceeds AV_{DD}, while an undervoltage is flagged when the voltage on the analog input goes below AV_{SS}.

For the circuit shown in Figure 1, four analog pins of the AD7124-4/AD7124-8 are used to implement the 3-wire measurement: AIN0, AIN1, AIN2, and AIN3. AIN2 and AIN3 are configured as a fully differential input channel and are used for sensing the voltage across the Pt100. The excitation current source used to excite the RTD is generated from AV_{DD} and is directed to AIN0. An identical current is directed to AIN1 and flows through the RL2 lead resistance, thereby generating a voltage that cancels the voltage dropped across the RL1 lead resistance. The analog pins and their configuration are shown in greater detail in Figure 4.

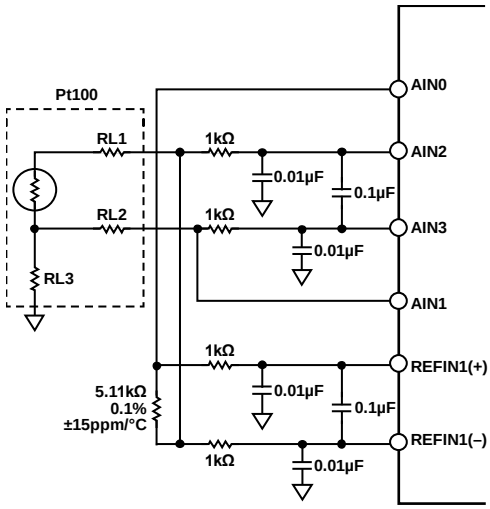

Figure 4. Analog Inputs for 3-Wire RTD Measurement

With the PGA enabled, the analog input buffers are automatically enabled. The PGA allows voltages on the input pins to be as low as AV_{SS}; therefore, headroom resistors are not required for the analog input pins. The reference buffers are also enabled. These buffers require headroom. Because the reference resistor is on the high side, the headroom requirements for the reference resistor

are met; therefore, additional headroom resistors are not required for this measurement configuration .

For the circuit shown in Figure 1, the reference input used is REFIN1(±). The current through the Pt100 also flows through the precision reference resistor that generates the reference voltage. The voltage generated across this precision reference resistor is ratiometric to the voltage across the Pt100; therefore, any errors because of variations in the excitation current are removed.

Digital and Analog Filtering

Differential (~800 Hz cutoff) and common-mode (~16 kHz cutoff) filters are implemented at the analog inputs as well as at the reference inputs. This filtering is required to reject any interference at the modulator frequency and also any multiples of this frequency.

The AD7124-4/AD7124-8 offers a great deal of on-chip digital filtering flexibility. Several filter options are available; the filter option selected has an effect on the output data rate, settling time, as well as 50 Hz and 60 Hz rejection. For this circuit note, the sinc^4 filter and the post filter are implemented. The sinc^4 filter is used because it has excellent noise performance across the range of output data rates, as well as excellent 50 Hz and 60 Hz rejection. The post filter is used to provide simultaneous 50 Hz and 60 Hz rejection with a 40 ms settling time.

Calibration

The AD7124-4/AD7124-8 provides different calibration modes that can be used to eliminate offset and gain errors. For this circuit note, internal zero-scale calibration as well as internal full-scale calibration were used. Note that these calibrations remove only the ADC gain and offset errors, not gain and offset errors created by the external circuitry.

3-Wire RTD Configuration

The circuit shown in Figure 1 is designed for precision 3-wire RTD measurement using the AD7124-4/AD7124-8. For the 3-wire RTD measurement, two precision excitation current sources are required that provide an easy way to cancel the lead resistance errors produced by RL1 and RL2. Note that the RL3 lead resistance does not affect the measurement accuracy. For the 3-wire RTD configuration shown in Figure 1, the reference resistor is placed on the high side of the RTD. For this setup, one excitation current flows through both the reference resistor and the RTD; the second current flows through lead-resistance RL2 and develops a voltage that cancels the voltage dropped across RL1. Because only one excitation current generates the reference voltage to REFIN1±, and also generates the voltage across the RTD, the current source accuracy, mismatch, and mismatch drift has a minimal effect on the ADC transfer function.

A low level voltage is generated across the Pt100 RTD by the excitation current. This low level voltage can then be amplified by the on-board PGA of the AD7124-4/AD7124-8, and is then converted to a precision digital representation using the 24-bit Σ-Δ ADC. For this 3-wire RTD configuration, both excitation currents are programmed to 500 µA. For a maximum RTD temperature of 600°C, the voltage generated across the RTD using the 500 µA excitation current is approximately 156.85 mV. To ensure that the maximum range of the AD7124-4/AD7124-8 is used, the PGA gain is programmed to 16, which amplifies the maximum RTD sensor output voltage to 2.5096 V. To ensure a true ratiometric configuration for this 3-wire circuit, the reference voltage to the ADC is generated using an external precision resistor using the same excitation current as that used for the Pt100. Using this configuration means that any deviation in the value of the excitation current is seen across the Pt100 as well as the reference resistor, and therefore does not alter the accuracy of the system.

Using the excitation current of 500 µA and the amplified voltage of the ADC, the reference resistor value is

$$V_{RTD\,MAX}/I_{EXC} = 2.51\text{ V}/500\text{ µA} = 5020\ \Omega$$

Therefore, a 5.11 kΩ resistor is chosen, which gives a reference voltage of

$$V_{REF} = R_{REF} \times I_{EXC} = 5.11\text{ kΩ} \times 500\text{ µA} = 2.555\text{ V}$$

The output compliance of the excitation current source must also be considered when making 3-wire RTD measurements using the AD7124-4/AD7124-8. The output compliance is dependent on the excitation current selected. For this circuit, 500 µA is selected, which has an output compliance voltage of AV_{DD} − 0.37 V. The AV_{DD} supply voltage for this circuit is 3.3 V, which means that the output compliance level for the excitation current source must be less than 2.93 V. From the previous calculations, this specification is met because the maximum voltage on the AIN0 pin is the voltage across the precision reference resistor plus the voltage across the RTD:

$$V_{REF} + V_{RTD} = 2.555\text{ V} + 156.85\text{ mV} = 2.71185\text{ V}$$

The AD7124-4/AD7124-8 configuration for the 3-wire RTD measurement is as follows:

- Differential input: AINP = AIN2, AINM = AIN3
- Excitation current: IOUT0 = AIN0 = 500 µA
- Excitation current: IOUT1 = AIN1 = 500 µA
- Gain = 16
- 5.11 kΩ precision reference resistor
- Digital filtering (sinc^4 and post filter)

The general expression to calculate the RTD resistance (R), where the ADC is operating in bipolar mode, is given by

$$R_{RTD} = \frac{(CODE - 2^{N-1}) \times R_{REF}}{G \times 2^{N-1}} \quad (1)$$

where:
CODE is the ADC code.
N is the resolution of the ADC (24, in this case).
R_{REF} is the reference resistor.
G is the selected gain.

From the specification of the Class B RTD, the resistance changes by approximately 0.385 Ω/°C. This relationship can be used as a quick method to get an approximate temperature of the RTD. This

method has inaccuracies due to the temperature coefficient of the RTD changing slightly over the temperature range; however, it can be a useful method to quickly check the temperature.

To calculate the approximate temperature, use Equation 2, where the resistance of the RTD is 100 Ω at 0°C.

$$Temperature\ (°C) = \frac{R_{RTD} - 100}{0.385} \quad (2)$$

The RTD transfer function known as the Callender-Van Dusen equation is made up of two distinct polynomial equations. Equation 3 is used for temperatures less than 0°C, and Equation 4 for temperatures greater than 0°C.

The equation for temperature t ≤ 0°C is

$$R_{RTD}(t) = R_0[1 + At + Bt^2 + C(t - 100°C)t^3] \quad (3)$$

The equation for temperature t ≥ 0°C is

$$R_{RTD}(t) = R_0(1 + At + Bt^2) \quad (4)$$

where:
t is the RTD temperature (°C).
$R_{RTD}(t)$ is the RTD resistance at temperature (t).
R_0 is the RTD resistance at 0°C (in this case, R_0 = 100 Ω).
$A = 3.9083 \times 10^{-3}$.
$B = -5.775 \times 10^{-7}$.
$C = -4.183 \times 10^{-12}$.

There are many different ways to determine the temperature as a function of the RTD resistance given the transfer function in Equation 3 and Equation 4. For this circuit note, the direct mathematical method is chosen because of its accuracy. Using Equation 3, the temperature can be calculated as

$$T_{RTD}\ (°C) = \frac{-A + \sqrt{A^2 - 4B\left(1 - \frac{r}{R_0}\right)}}{2B} \quad (5)$$

where r is the RTD resistance, and the other variables are as defined previously.

This method works well for temperatures greater than or equal to 0°C. To calculate the RTD temperature for temperatures below 0°C, a best fit polynomial expression is required. The polynomial used in this note is a fifth-order polynomial, shown in Equation 6.

$$T_{RTD}\ (°C) = -242.02 + 2.2228 \times r + (2.5859 \times 10^{-3})r^2 - (-4.8260 \times 10^{-6})r^3 - (2.8183 \times 10^{-3})r^4 + (1.5243 \times 10^{-10})r^5 \quad (6)$$

As an example, the code read back from the AD7124-4/AD7124-8 for the temperature set to 25°C is 11270065. Converting this code to a resistance using Equation 1 gives

$$R_{RTD} = \frac{(11270065 - 2^{23}) \times R_{REF}}{G \times 2^{23}} = 109.704\ \Omega$$

Linearization using Equation 5 gives a temperature of 24.921°C.

As a second example, the code read back from the AD7124-4/AD7124-8 for the temperature set to −25°C is 10757779. Converting this code to a resistance gives

$$R_{RTD} = \frac{(10757779 - 2^{23}) \times R_{REF}}{G \times 2^{23}} = 90.200\ \Omega$$

Linearization using Equation 6 gives a temperature of −24.982°C.

3-Wire RTD Measurements and Results

For the circuit shown in Figure 1, data was gathered for different digital filter and power mode configurations of the AD7124-4/AD7124-8, namely the sinc⁴ filter operating in full power mode and the post filter operating in low power mode.

Choosing the configuration for sinc⁴ filter, full power mode for an output data rate of 50 SPS allows the user to operate the AD7124-4/AD7124-8 for best performance in relation to speed and noise. Figure 5 shows the noise distribution when a 3-wire RTD is connected as shown in Figure 1 at ambient temperature. The corresponding rms noise is typically 199.37 nV rms equating to approximately 17.9 noise free bits. The noise performance of the AD7124-4/AD7124-8 for inputs shorted when the same filter, gain, and output data rate are selected is typically 100 nV rms or 18.7 noise free bits. The increase in the noise comes directly from the RTD connected across the input channel (AIN2, AIN3).

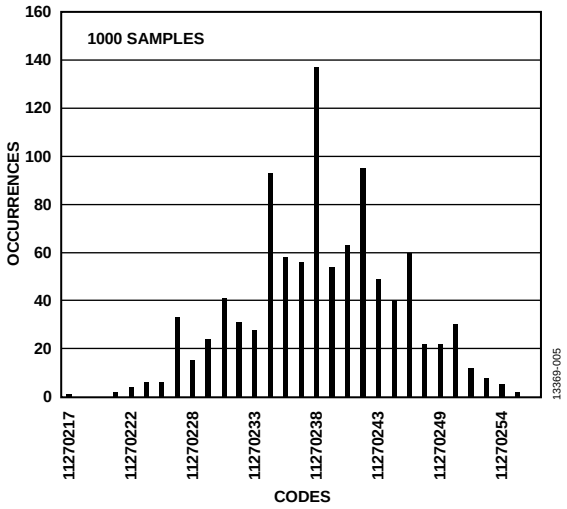

Figure 5. Histogram of Codes for RTD at Ambient, Sinc⁴ Filter, Full Power Mode, 50 SPS

For the 3-wire RTD configuration where the sinc⁴ filter and full power mode were selected, the temperature of the RTD was swept from −50°C to +200°C. For each temperature, the corresponding voltage across the RTD was measured using the AD7124-4/AD7124-8 as outlined previously. This voltage was then converted to a resistance, linearized, and converted to a temperature as outlined in the 3-Wire RTD Configuration section. Figure 6 shows the resulting error between the set temperature and the measured system temperature of the RTD after linearization. For each RTD temperature setting, the AD7124-4/AD7124-8 is kept at 25°C. As shown in Figure 6, the error of the RTD temperature measured is well within the error window of the Pt100 Class B RTD. Figure 6 also shows the deviation of the RTD error across different AD7124-4/AD7124-8

temperature settings. For each AD7124-4/AD7124-8 temperature setting, an internal zero-scale and full-scale calibration is carried out. As shown in Figure 6, the error of the RTD is well within the expected error of the Class B RTD for all temperature settings of the AD7124-4/AD7124-8.

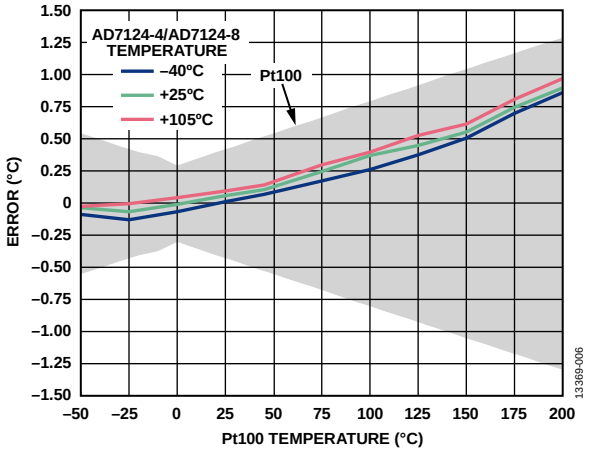

Figure 6. Temperature Accuracy Measurement, Sinc⁴ Filter, Full Power Mode, 50 SPS

Figure 7 shows the error in measured RTD temperature for a one time, internal zero-scale and full-scale calibrations carried out at 25°C. The plot shows that carrying out a one time calibration at 25°C or calibrating at each individual temperature of the AD7124-4/AD7124-8 gives similar performances.

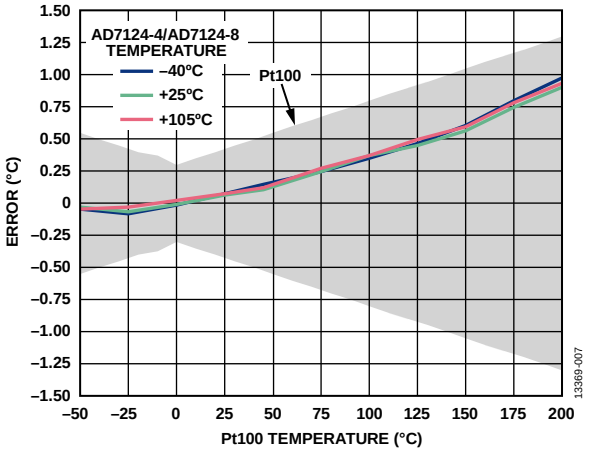

Figure 7. Temperature Accuracy Measurement, Sinc⁴ Filter, Full Power Mode, 50 SPS, One Time 25°C Calibration Only

The second AD7124-4/AD7124-8 configuration tested was the low power mode, where the post filter and 25 SPS output data rate were selected. The 25 SPS filter gives simultaneous 50 Hz and 60 Hz rejection and allows the user to trade off settling time with power supply rejection. Figure 8 shows the resulting noise distribution when a 3-wire RTD is connected as shown in Figure 1 at ambient temperature. The corresponding rms noise is typically 774 nV rms equating to approximately 16.8 noise free bits. The noise performance of the AD7124-4/AD7124-8 for inputs shorted with the same filter, gain, power mode, and output data rate is typically 360 nV rms or 17.3 noise free bits. The increase in the noise between the two measurements comes directly from the RTD connection across the input channel (AIN2, AIN3).

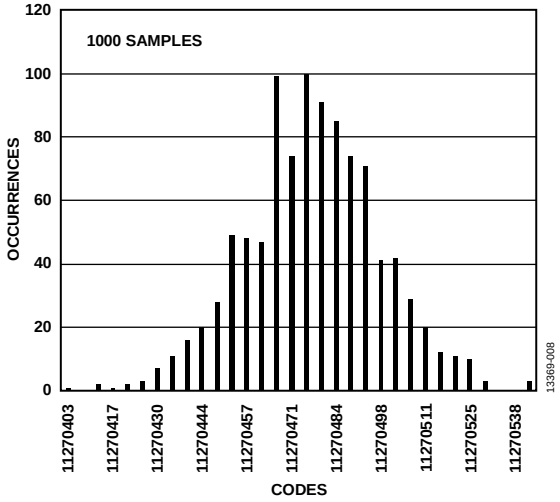

Figure 8. Histogram of Codes for RTD at Ambient, Post Filter, Low Power Mode, 25 SPS

For this AD7124-4/AD7124-8 configuration where the post filter and low power mode were selected, the temperature of the RTD was swept from −50°C to +200°C. For each of the set RTD temperatures, the corresponding voltage across the RTD was measured using the AD7124-4/AD7124-8 as outlined previously. This voltage was then converted to a resistance, which was then linearized and converted to a temperature as outlined in the 3-Wire RTD Configuration section. Figure 9 shows the resulting error between the set and measured temperatures of the RTD after linearization. For each RTD temperature setting, the AD7124-4/AD7124-8 is kept at 25°C. As shown in Figure 9, the error of the RTD temperature measured is well within the error window of the Pt100 Class B RTD. Figure 9 also shows the deviation of the RTD error across different AD7124-4/AD7124-8 temperature settings. For each AD7124-4/AD7124-8 temperature setting, an internal zero-scale and full-scale calibration is carried out. Figure 9 shows that the error of the RTD is well within the expected error of the Class B RTD for all temperature settings of the AD7124-4/AD7124-8.

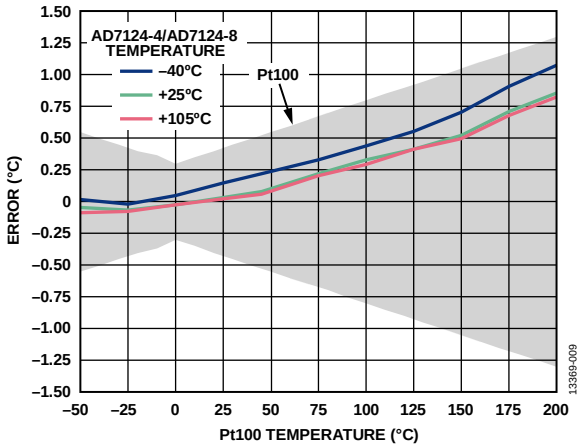

Figure 9. Temperature Accuracy Measurement, Post Filter, Low Power Mode, 25 SPS

Figure 10 shows the error in measured RTD temperature for a one time, internal zero-scale and full-scale calibration carried out at 25°C. The plot shows that carrying out a one time calibration at 25°C or calibrating at each individual temperature of the AD7124-4/AD7124-8 gives similar performances.

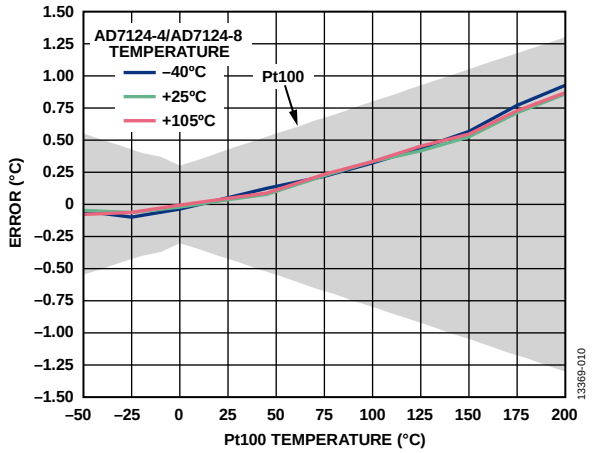

Figure 10. Temperature Accuracy Measurement, Post Filter, Low Power Mode, 25 SPS, 25°C One Time Calibration Only

COMMON VARIATIONS

Current Source Mismatch and Mismatch Drift

In the Figure 1 circuit, the precision reference resistor was placed on the high side. The high-side configuration works well for systems using a single RTD. When multiple RTDs are used, it is better to place the precision resistor on the low side because only a single reference resistor is required. With the reference resistor on the low side, better excitation current matching is required. Two different techniques can be used to minimize the errors due to mismatches in the currents:

- Chopping the excitation currents
- Calibration by measuring the excitation currents

Chopping the Excitation Currents

The crosspoint multiplexer on the AD7124-4/AD7124-8 allows easy implementation of the chopping configuration. Figure 11 shows the 3-wire RTD configuration with the precision 5.11 kΩ reference resistor connected to the low side of the Pt100 RTD. For this configuration, the current source used as well as the gain must be reconsidered. Both IOUT0 and IOUT1 are set to 250 µA. Selecting this current ensures that the circuit complies with the output compliance of the current sources as well as the reference voltage generated across the precision resistor. To ensure that the full range of the ADC is used, the gain of the PGA was set to 32. A resistor is required on the low side of the reference resistor because the reference buffers are enabled and require headroom (100 mV).

To chop the currents, a measurement of the RTD voltage is taken when IOUT0 is connected to AIN0, and IOUT1 is connected to AIN1, as shown in Figure 11. A second measurement of the voltage across the RTD is then taken when the currents are swapped, that is, when IOUT1 is connected to AIN0, and IOUT1 is connected to AIN1. The average of these two voltage measurements is then used in the overall calculation of the RTD resistance, and subsequently the temperature is calculated using Equation 1 through Equation 6. The chopping method greatly reduces any effects of excitation current mismatch and mismatch drift. However, there is an impact on the throughput rate since two measurements are required.

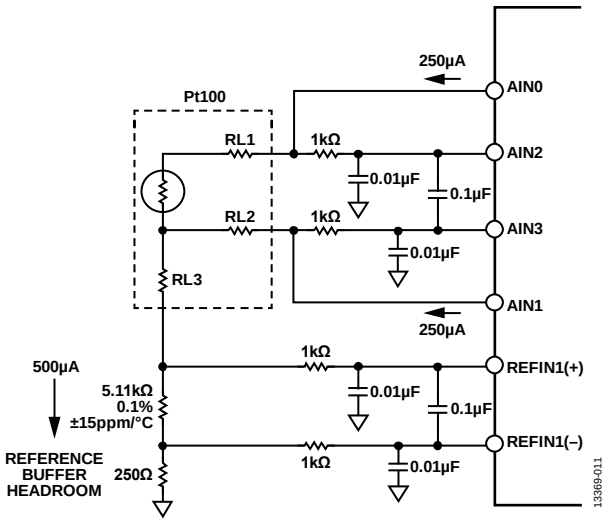

Figure 11. AD7124-4/AD7124-8 Configuration for 3-Wire RTD Measurement Using the Current Chopping Measurement Technique

Measurement data using the excitation current chopping method was gathered, and the corresponding Pt100 temperature error recorded as shown in Figure 12. For all RTD temperatures measured, the temperature error is within the error band of the Pt100 RTD for different ambient temperatures of the AD7124-4/AD7124-8. These results show that chopping the excitation current gives results that are comparable to the data gathered with the high-side precision reference resistor configuration.

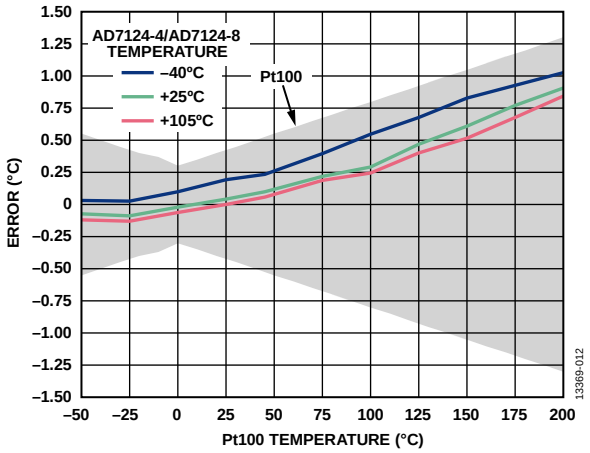

Figure 12. Temperature Accuracy Measurement for Chopping Configuration, Sinc⁴ Filter, Full Power Mode, Calibration at Each Temperature

Calibration by Measuring the Excitation Currents

The configuration for calibrating the 3-wire system by measuring the excitation currents is shown in Figure 13. For this configuration, the precision reference resistor is connected

to the low side of the RTD. This configuration is similar to that used for chopping the currents, where both the currents are set to 250 µA, and the PGA gain is set to 32. However, the main difference is that an additional differential input channel is required. The additional input channel enables the measurement of the two excitation currents. The measurement is implemented by measuring the voltage drop across the precision reference resistor with respect to the internal reference when each of the excitation currents is individually enabled. The measured voltage is then converted to a current based on the value of the precision reference resistor value, which is subsequently used to calculate the ratio of the currents, and then used to calibrate the mismatch.

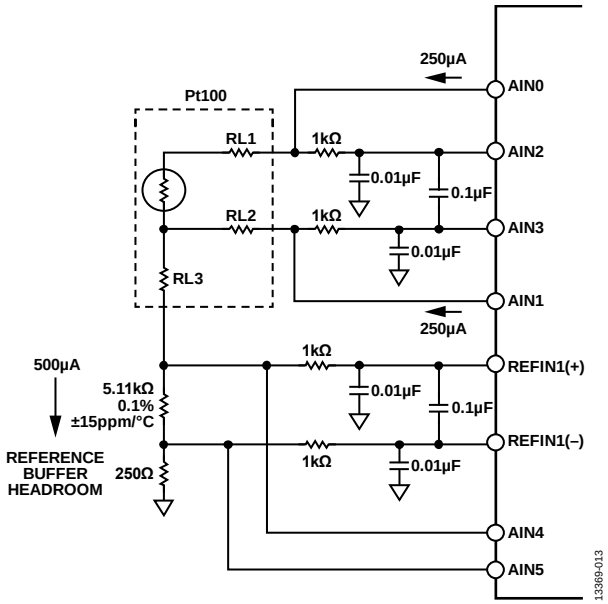

Figure 13. AD7124-4/AD7124-8 Configuration for 3-Wire RTD Measurement Calibration by Measuring the Excitation Currents

Figure 14 shows the calibrated temperature error in the RTD measurements. The results show that the RTD error is within the expected error band of the RTD, where the error in measurement is close to the error profile of the RTD itself. To ensure accurate results, calibration of the currents must take place at regular intervals over time.

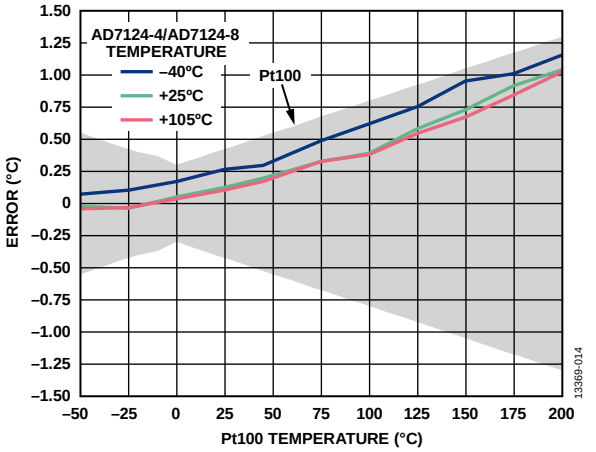

Figure 14. Temperature Accuracy Measurement for Excitation Current Calibration, Sinc⁴ Filter, Full Power Mode, Calibration at Each Temperature

Lead Resistance Considerations

For the 3-wire RTD measurement, the accuracy of the lead resistance compensation depends on the resistance of each of the leads being equal (specifically, RL1 = RL2). The voltage dropped across RL3 does not affect the voltage measured across the RTD element; therefore, RL3 does not introduce error in the measurement for the circuits described in this circuit note.

The nominal resistance of 24 AWG copper wire is 0.026 Ω/foot. A 50 foot length has a 1.3 Ω lead resistance. A 10% error in matching produces a 0.13 Ω error in the RTD measurement, assuming perfectly matched compensation and excitation currents. The RTD temperature coefficient is approximately 0.385 Ω/°C; therefore, the 0.13 Ω lead resistance mismatch measurement error translates into approximately (0.13 Ω) ÷ (0.385 Ω/°C) = 0.337°C error due to lead resistance mismatch. Therefore, for accurate 3-wire measurements, the matching characteristics of the connecting cables must be known precisely.

Assuming perfect lead resistance matching, mismatches in the excitation currents (IOUT0 and IOUT1) produce an error that is proportional to the total lead resistance. For instance, a 0.5% mismatch in the excitation currents (typical specification for the AD7124-4/AD7124-8) produces a corresponding 0.5% error in the RTD resistance measurement. The nominal Pt100 RTD resistance temperature coefficient is 0.385 Ω/°C, which is equivalent to a temperature change of 2.6°C/Ω. A 0.5% error in the resistance measurement gives an RTD measurement error of 0.005 × 2.6°C/Ω = 0.013°C/Ω. For a lead resistance of 10 Ω (~400 feet of 24 AWG copper wire), the error due to the mismatch in currents is only 0.13°C.

The previous discussion illustrates that, in most practical applications, the mismatch in the lead resistances creates much more error than the 0.5% mismatch in excitation currents. As previously mentioned, the mismatch error in the excitation currents can be minimized by using either the chopping mode or by measuring the individual excitation currents.

CIRCUIT EVALUATION AND TEST

Equipment Needed

The following equipment is required for the 3-wire RTD measurement system:

- The EVAL–AD7124-4SDZ or EVAL-AD7124-8SDZ evaluation board
- The EVAL-SDP-CB1Z System Demonstration Platform (SDP)
- AD7124_Eval+ Software
- Power supply: 7 V or 9 V wall wart
- Class B Pt100 3-wire RTD
- A PC running Windows® XP (SP2), Windows Vista, or Windows 7 (32-bit or 64-bit)

Software Installation

A complete software user guide for the AD7124-4/AD7124-8 and the SDP board can be found in the EVAL-AD7124-4SDZ/ EVAL-AD7124-8SDZ user guide and the SDP User Guide.

Software is required to interface with the hardware. This software can be downloaded from ftp://ftp.analog.com/pub/evalcd/AD7124. If the setup file does not run automatically, double-click **setup.exe** from the file. Install the evaluation software before connecting the evaluation board and SDP board to the USB port of the PC to ensure that the evaluation system is correctly recognized when connected to the PC.

After the evaluation software installation is complete, connect the SDP board (via Connector A) to the EVAL-AD7124-4SDZ/ EVAL-AD7124-8SDZ and then connect the SDP board to the USB port of the PC using the supplied cable. When the evaluation system is detected, proceed through any dialog boxes that appear to complete the installation.

Setup and Test

Figure 15 shows a functional block diagram of the test setup for the 3-wire RTD configuration.

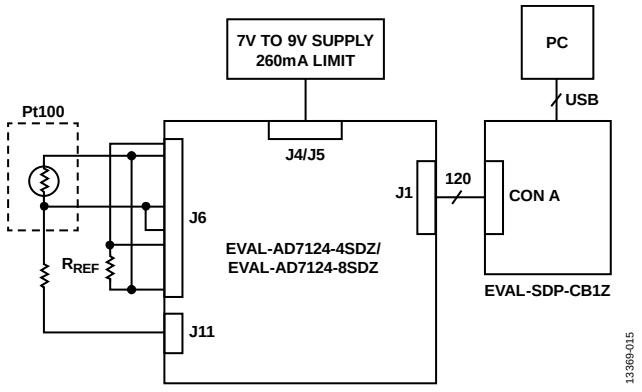

Figure 15. Test Setup Functional Diagram

The EVAL-AD7124-4SDZ/EVAL-AD7124-8SDZ evaluation board is required to test the circuit. In addition, the following sensor and resistors are required for proper operation:

- 3-wire Pt100 RTD, Class B
- 5.11 kΩ precision resistor
- 250 Ω resistor for buffer headroom (not needed for this configuration, but included for completeness because it may be required if a Pt1000 RTD is used with a gain of 1)

To configure the hardware, take the following steps:

- Set all links on the EVAL-AD7124-4SDZ/EVAL-AD7124-8SDZ to the default board positions as outlined in the EVAL-AD7124-4SDZ/EVAL-AD7124-8SDZ user guide.
- Power the board with a 7 V or 9 V power source connected to J5.
- Connect the RTD, precision reference resistor, and resistor for headroom as shown in Figure 16.

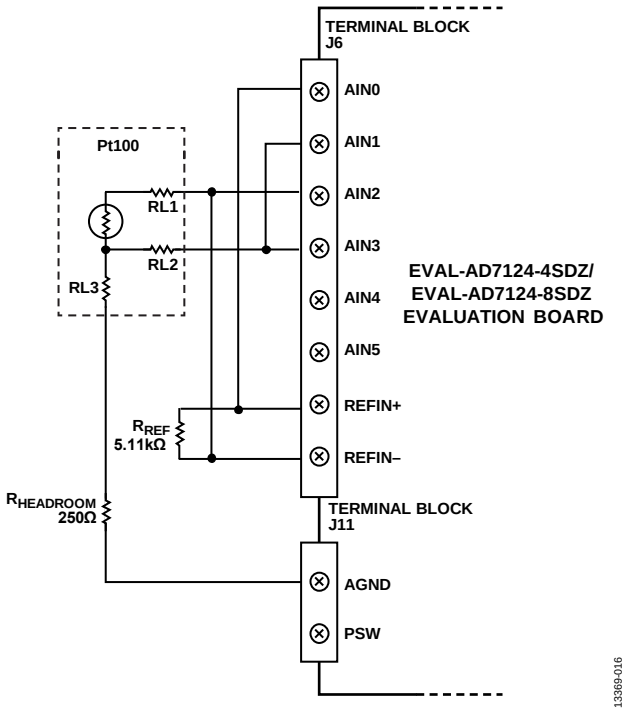

Figure 16. EVAL-AD7124-4SDZ/EVAL-AD7124-8SDZ Evaluation Board Connector for 3-Wire RTD Measurement

Run the AD7124-4/AD7124-8 EVAL+ Software. Figure 17 shows a screenshot of the main window of the software.

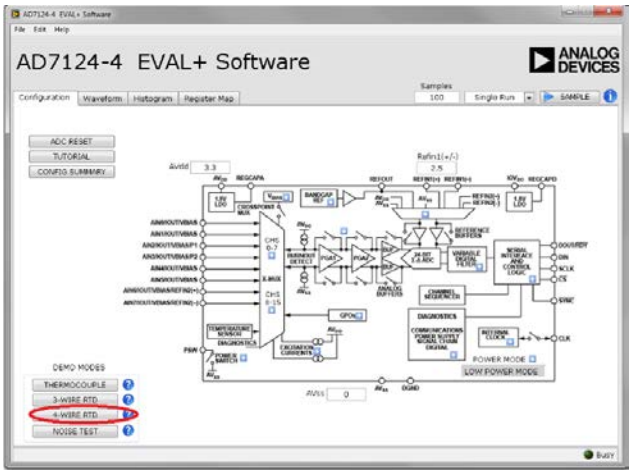

Figure 17. AD7124_Eval+ Software Main Window

To configure the AD7124-4/AD7124-8 for 3-wire RTD measurements, click the **3-WIRE RTD** demo mode button (see Figure 17). Clicking this button configures the ADC software for optimized performance. Some of the register settings are as follows:

1. Channel_0
   a. AINP_0 = AIN2
   b. AINM_0 = AIN3
   c. Setup0
   d. Enabled = TRUE
2. Setup_0
   a. PGA_0 = 16
   b. AIN_BUFP, AIN_BUFM both = ENABLED
   c. BIPOLAR = ENABLED
   d. FS_0 = 384
   e. FILTER_MODE_0 = SINC4
3. ADC_Control
   a. MODE = Continuous Conversion
   b. POWER_MODE = FULL
4. IO_CONTROL_1
   a. IOUT0 Channel Enable = AIN0
   b. IOUT0 Select = 500 µA
   c. IOUT1 Channel Enable = AIN1
   d. IOUT1 Select = 500 µA

One additional step is required before the AD7124-4/AD7124-8 is configured for 3-wire RTD measurements: an internal full-scale and zero-scale calibration of the AD7124-4/AD7124-8. This calibration can be performed via the **Register Map** tab, as shown in Figure 18.

1. From the register tree, select the **ADC_Control** register.
2. Select **Low Power** mode.
3. Perform an internal full-scale calibration.
   a. Click the **Mode** bitfield of the ADC control register.
   b. In the **Mode** bitfield, select the internal full-scale calibration option.
   c. Check that the calibration performed by selecting the **Gain0** register from the register tree, and check that the coefficients have changed.
4. Perform an internal zero-scale calibration.
   a. Click the **Mode** bitfield of the ADC control register.
   b. In the **Mode** bitfield, select the internal zero-scale calibration option.
   c. Check that the calibration performed by selecting the **Offset0** register from the register tree, and check that the coefficients have changed.
5. When calibrations are complete, change the power mode to the required mode of operation, and ensure that the ADC is set to continuous conversion mode by selecting **Continuous** from the drop-down box in the **Mode** bitfield of the **ADC_Control** register.

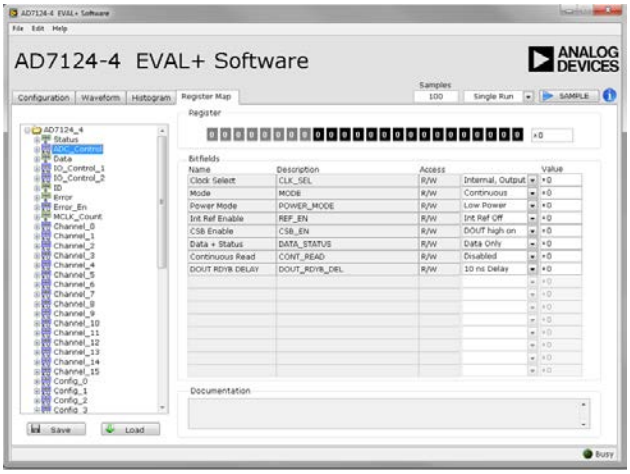

Figure 18. Register Map Internal Full-Scale and Zero-Scale Calibration

The board and device are now configured for 3-wire RTD measurements. Click **SAMPLE** to start gathering samples from the AD7124-4/AD7124-8. The **Waveform** tab and the **Histogram** tab show the data gathered from the AD7124-4/AD7124-8.

LEARN MORE

CN-0383 Design Support Package: www.analog.com/CN0383-DesignSupport

SDP User Guide

EVAL-AD7124-4 User Guide (UG-855)

EVAL-AD7124-8 User Guide (UG-856)

AN-892 Application Note. *Temperature Measurement Theory and Practical Techniques*. Analog Devices.

Kester, Walt. "Temperature Sensors," Chapter 7 in *Sensor Signal Conditioning.* Analog Devices, 1999.

McCarthy, Mary. AN-615 Application Note. *Peak-to-Peak Resolution Versus Effective Resolution*. Analog Devices.

MT-031 Tutorial. *Grounding Data Converters and Solving the Mystery of "AGND" and "DGND"*. Analog Devices.

MT-101 Tutorial. *Decoupling Techniques*. Analog Devices.

Circuit Note CN-0376. *Channel-to-Channel Isolated Temperature Input (Thermocouple/RTD) for PLC/DCS Applications.* Analog Devices.

Circuit Note CN-0381. *Completely Integrated 4-Wire RTD Measurement System Using a Low Power, Precision, 24-Bit, Sigma-Delta ADC*. Analog Devices.

Circuit Note CN-0382. *Ultralow Power Industrial Temperature and Pressure 4 mA to 20mA/HART Transmitter*. Analog Devices.

Circuit Note CN-0384. *Completely Integrated Thermocouple Measurement System Using a Low Power, Precision, 24-Bit, Sigma-Delta ADC*. Analog Devices.

Data Sheets and Evaluation Boards

EVAL-AD7124-4SDZ

EVAL-AD7124-8SDZ

System Demonstration Platform (EVAL-SDP-CB1Z)

AD7124-4 Data Sheet

AD7124-8 Data Sheet

ADP1720 Data Sheet

REVISION HISTORY

10/2019—Rev. A to Rev. B

Changes to Serial Peripheral Interface (SPI) Section and Analog Inputs and Reference Section 3
Change to Digital and Analog Filtering Section 4
Change to 3-Wire RTD Configuration 5
Change to Equipment Needed Section 9
Change to Figure 17 Caption 10

9/2017—Rev. 0 to Rev. A

Changes to 3-Wire RTD Configuration Section 5

7/2015—Revision 0: Initial Version