TLC5941-Q1 16-Channel LED Driver With Dot Correction and Grayscale PWM Control

1 Features

- Qualified for Automotive Applications
- AEC-Q100 Qualified With the Following Results:
  - Device Temperature Grade 1: –40°C to 125°C Ambient Operating Temperature Range
  - Device HBM ESD Classification Level 2
  - Device CDM ESD Classification Level C4B
- 16 Channels
- 12-Bit (4096 Steps) Grayscale PWM Control
- Dot Correction: 6 Bit (64 Steps)
- Drive Capability (Constant-Current Sink): 0 mA to 60 mA
- LED Power Supply Voltage up to 17 V
- V_{CC} = 3.0 V to 5.5 V
- Serial Data Interface
- Controlled In-Rush Current
- 30-MHz Data Transfer Rate
- CMOS Level I/O
- Error Information
  - LOD: LED Open Detection
  - TEF: Thermal Error Flag

2 Applications

- Monocolor, Multicolor, Full-Color LED Displays
- LED Signboards
- Display Back-Lighting

3 Description

The TLC5941-Q1 device is a 16-channel, constant-current sink, LED driver. Each channel has an individually adjustable 4096-step grayscale PWM brightness control and a 64-step constant-current sink (dot correction), which both are accessible via a serial interface. This device features two fault diagnostic circuits. The LED open detection (LOD) indicates a broken or disconnected LED at an output terminal. The thermal error flag (TEF) indicates an over temperature condition.

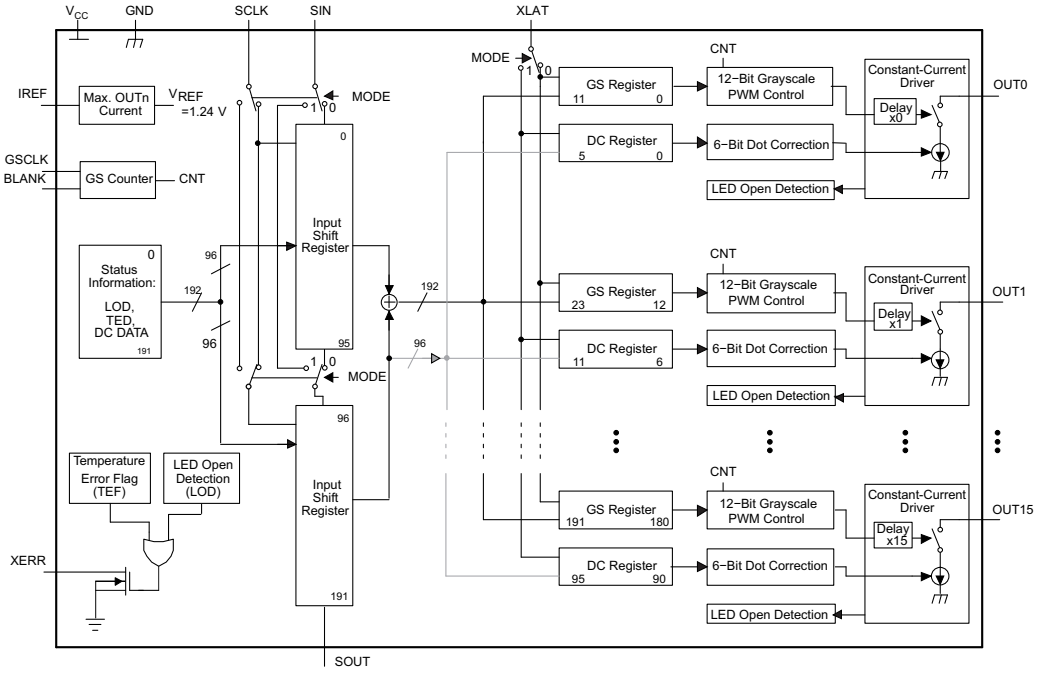
The TLC5941-Q1 features two error information circuits. The LED open detection (LOD) indicates a broken or disconnected LED at an output terminal. The thermal error flag (TEF) indicates an overtemperature condition.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TLC5941-Q1	HTSSOP (28)	9.70 mm × 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Functional Block Diagram



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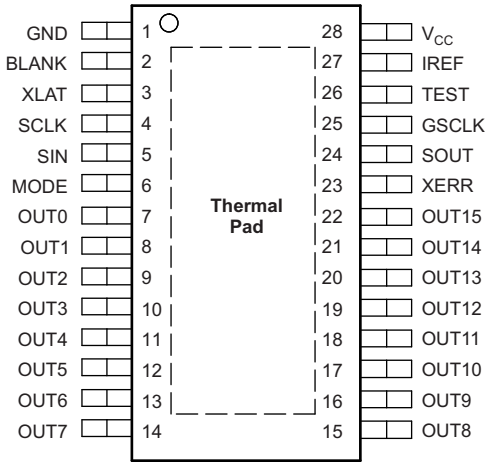
4 Revision History

Changes from Original (December 2008) to Revision A **Page**

- Added the *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 4

5 Pin Configuration and Functions

PWP Package
28-Pin HSSOP With Thermal Pad
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
BLANK	2	I	Blank all outputs. When BLANK = H, all OUTn outputs are forced OFF. GS counter is also reset. When BLANK = L, OUTn are controlled by grayscale PWM control. This pin should be pull up to high before micro-controller or digital signal processor sending control signal to device. A pull-up resistor to VCC is needed.
GND	1	G	Ground
GSCLK	25	I	Reference clock for grayscale PWM control
IREF	27	I/O	Reference current terminal
MODE	6	I	Input mode-change pin. When MODE = GND, the device is in GS mode. When MODE = V_{CC}, the device is in DC mode.
OUT0	7	O	Constant-current output
OUT1	8	O	Constant-current output
OUT2	9	O	Constant-current output
OUT3	10	O	Constant-current output
OUT4	11	O	Constant-current output
OUT5	12	O	Constant-current output
OUT6	13	O	Constant-current output
OUT7	14	O	Constant-current output
OUT8	15	O	Constant-current output
OUT9	16	O	Constant-current output
OUT10	17	O	Constant-current output
OUT11	18	O	Constant-current output
OUT12	19	O	Constant-current output
OUT13	20	O	Constant-current output
OUT14	21	O	Constant-current output
OUT15	22	O	Constant-current output
SCLK	4	I	Serial data shift clock
SIN	5	I	Serial data input
SOUT	24	O	Serial data output
TEST	26	I	Test. Must be connected to VCC.
V_{CC}	28	I	Power supply voltage. This pin should be powered up before micro-controller or digital signal processor sending control signal to device.
XERR	23	O	Error output. Open-drain. Goes L when LOD or TEF is detected.

Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
XLAT	3	I	Level triggered latch signal. When XLAT = high, the TLC5941-Q1 writes data from the input shift register to either GS register (MODE = low) or DC register (MODE = high). When XLAT = low, the data in the GS or DC registers is held constant and does not change.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Input voltage, V_I(2)	V_{CC}	–0.3	6	V
	$V_{(BLANK)}$, $V_{(SCLK)}$, $V_{(XLAT)}$, $V_{(MODE)}$, $V_{(SIN)}$, $V_{(GSCLK)}$, $V_{(IREF)}$, $V_{(TEST)}$	–0.3	V_{CC} + 0.3	
Output voltage, V_O	$V_{(SOUT)}$, $V_{(XERR)}$	–0.3	V_{CC} + 0.3	V
	$V_{(OUT0)}$ to $V_{(OUT15)}$	–0.3	18	
Output current (DC), I_O			90	mA
Operating junction temperature, $T_{J(max)}$			150	°C
Storage temperature, T_{stg}		–55	150	

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1)		±2000	V
		Charged device model (CDM), per AEC Q100-011	Corner pins (1, 14, 15, and 28)	±750	
			Other pins	±500	

(1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

			MIN	MAX	UNIT
DC CHARACTERISTICS					
V_{CC}	Supply voltage		3	5.5	V
V_O	Voltage applied to output (OUT0–OUT15)			17	V
V_{IH}	High-level input voltage		0.8 V_{CC}	V_{CC}	V
V_{IL}	Low-level input voltage		GND	0.2 V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 5 V at SOUT		–1	mA
I_{OL}	Low-level output current	V_{CC} = 5 V at SOUT, XERR		1	mA
I_{OLC}	Constant output current	OUT0 to OUT15		60	mA
T_J	Operating junction temperature		–40	125	°C
AC CHARACTERISTICS					
$f_{(SCLK)}$	Data shift clock frequency	SCLK		30	MHz
$f_{(GSCLK)}$	Grayscale clock frequency	GSCLK		30	MHz
t_{wh0}/t_{wl0}	SCLK pulse duration	SCLK = H/L (see Figure 12)	16		ns
t_{wh1}/t_{wl1}	GSCLK pulse duration	GSCLK = H/L (see Figure 12)	16		ns
t_{wh2}	XLAT pulse duration	XLAT = H (see Figure 12)	20		ns
t_{wh3}	BLANK pulse duration	BLANK = H (see Figure 12)	20		ns
t_{su0}	Setup time	SIN to SCLK↑ (see Figure 12)	5		ns
t_{su1}	Setup time	SCLK↓ to XLAT↑ (see Figure 12)	10		ns

Recommended Operating Conditions (continued)

			MIN	MAX	UNIT
t_{su2}	Setup time	MODE↑↓ to SCLK↑ (see Figure 12)	10		ns
t_{su3}	Setup time	MODE↑↓ to XLAT↑ (see Figure 12)	10		ns
t_{su4}	Setup time	BLANK↓ to GSCLK↑ (see Figure 12)	10		ns
t_{su5}	Setup time	XLAT↑ to GSCLK↑ (see Figure 12)	30		ns
t_{h0}	Hold time	SCLK↑ to SIN (see Figure 12)	3		ns
t_{h1}	Hold time	XLAT↓ to SCLK↑ (see Figure 12)	10		ns
t_{h2}	Hold time	SCLK↑ to MODE↑↓ (see Figure 12)	10		ns
t_{h3}	Hold time	XLAT↓ to MODE↑↓ (see Figure 12)	10		ns
t_{h4}	Hold time	GSCLK↑ to BLANK↑ (see Figure 12)	10		ns

6.4 Thermal Information

THERMAL METRIC(1)		TLC5941-Q1 PWP 28 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance(2)(3)	36.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	18.9	
$R_{\theta JB}$	Junction-to-board thermal resistance	15.9	
ψ_{JT}	Junction-to-top characterization parameter	0.6	
ψ_{JB}	Junction-to-board characterization parameter	15.8	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	2.3	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The package thermal impedance is calculated in accordance with JESD 51-7.
(3) With PowerPAD soldered on PCB with 2-oz trace of copper. For further information see the TI application report, *PowerPAD™ Thermally Enhanced Package*, SLMA002.

6.5 Electrical Characteristics

V_{CC} = 3 V to 5.5 V, T_J = –40°C to 125°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –1 mA, SOUT	V_{CC} – 0.5			V
V_{OL}	Low-level output voltage	I_{OL} = 1 mA, SOUT			0.5	V
I_I	Input current	V_I = V_{CC} or GND, BLANK, TEST, GSCLK, SCLK, SIN, XLAT	–1		1	µA
		V_I = GND, MODE pin	–1		1	
		V_I = V_{CC}, MODE pin			50	
I_{CC}	Supply current	No data transfer, all output OFF, V_O = 1 V, $R_{(IREF)}$ = 10 kΩ		0.9	6	mA
		No data transfer, all output OFF, V_O = 1 V, $R_{(IREF)}$ = 1.3 kΩ		5.2	12	
		Data transfer 30 MHz, all output ON, V_O = 1 V, $R_{(IREF)}$ = 1.3 kΩ		16	25	
		Data transfer 30 MHz, all output ON, V_O = 1 V, $R_{(IREF)}$ = 640 Ω		30	60	
$I_{O(LC)}$	Constant output current	All output ON, V_O = 1 V, $R_{(IREF)}$ = 640 Ω	54	61	69	mA
I_{lkg}	Leakage output current	All output OFF, V_O = 15 V, $R_{(IREF)}$ = 640 Ω, OUT0 to OUT15			0.1	µA
$\Delta I_{O(LC0)}$	Constant sink current error	All output ON, V_O = 1 V, $R_{(IREF)}$ = 640 Ω, OUT0 to OUT15, T_A = –20°C to 85°C(1)		±1%	±4%	
		All output ON, V_O = 1 V, $R_{(IREF)}$ = 640 Ω, OUT0 to OUT15(1)		±1%	±8%	

(1) The deviation of each output from the average of OUT0-15 constant current. It is calculated by Equation 1 in Test Parameter Equations.

Electrical Characteristics (continued)

V_{CC} = 3 V to 5.5 V, T_J = –40°C to 125°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$\Delta I_{O(LC1)}$	Constant sink current error	Device to device, averaged current from OUT0 to OUT15, $R_{(IREF)}$ = 1920 Ω (20 mA)(2)		0.4%	±4%	
$\Delta I_{O(LC2)}$	Line regulation	All output ON, V_O = 1 V, $R_{(IREF)}$ = 640 Ω, OUT0 to OUT15, V_{CC} = 3 V to 5.5 V(3)		±1	±4	%/V
$\Delta I_{O(LC3)}$	Load regulation	All output ON, V_O = 1 V to 3 V, $R_{(IREF)}$ = 640 Ω, OUT0 to OUT15(4)		±2	±6	%/V
$T_{(TEF)}$	Thermal error flag threshold	Junction temperature(5)	150		170	°C
$V_{(LED)}$	LED open detection threshold			0.3	0.4	V
$V_{(IREF)}$	Reference voltage output	$R_{I(REF)}$ = 640 Ω	1.20	1.25	1.29	V

(2) The deviation of average of OUT0–OUT15 constant current from the ideal constant-current value. It is calculated by Equation 2 in *Test Parameter Equations*. The ideal current is calculated by Equation 3 in *Test Parameter Equations*.
(3) The line regulation is calculated by Equation 4 in *Test Parameter Equations*.
(4) The load regulation is calculated by Equation 5 in *Test Parameter Equations*.
(5) Not tested. Specified by design.

6.6 Switching Characteristics

V_{CC} = 3 V to 5.5 V, C_L = 15 pF, T_J = –40°C to 125°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{r0}	Rise time	SOUT			16	ns
t_{r1}	Rise time	OUTn, V_{CC} = 5 V, T_A = 60°C, DCn = 3Fh		10	30	ns
t_{f0}	Fall time	SOUT			16	ns
t_{f1}	Fall time	OUTn, V_{CC} = 5 V, T_A = 60°C, DCn = 3Fh		10	30	ns
t_{pd0}	Propagation delay time	SCLK to SOUT (see Figure 12)			30	ns
t_{pd1}	Propagation delay time	BLANK to OUT0 (see Figure 12)			60	ns
t_{pd2}	Propagation delay time	OUTn to XERR (see Figure 12)			1000	ns
t_{pd3}	Propagation delay time	GSCLK to OUT0 (see Figure 12)			60	ns
t_{pd4}	Propagation delay time	XLAT to I_{OUT} (dot correction) (see Figure 12)			1000	ns
t_d	Output delay time	OUTn to OUT(n+1) (see Figure 12)		20	30	ns
t_{on_err}	Output on-time error	t_{outon} – t_{gsclk} (see Figure 12), GSn = 01h, GSCLK = 11 MHz	10	–50	–90	ns

6.7 Typical Characteristics

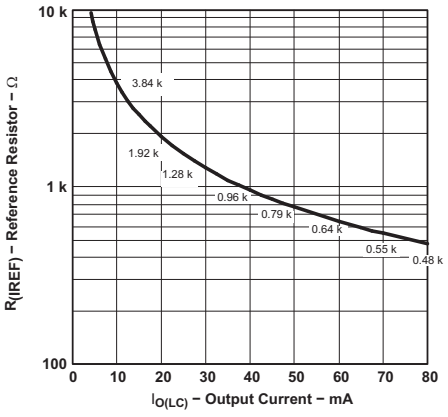


Figure 1. Reference Resistor vs Output Current

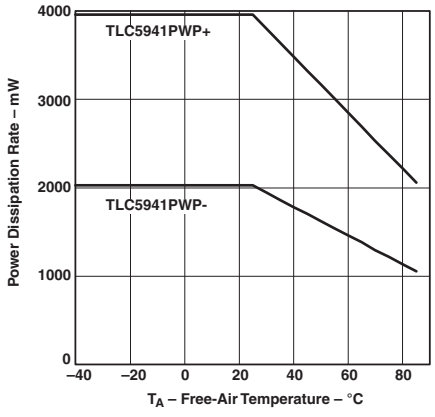


Figure 2. Power Dissipation Rate vs Free-Air Temperature

Typical Characteristics (continued)

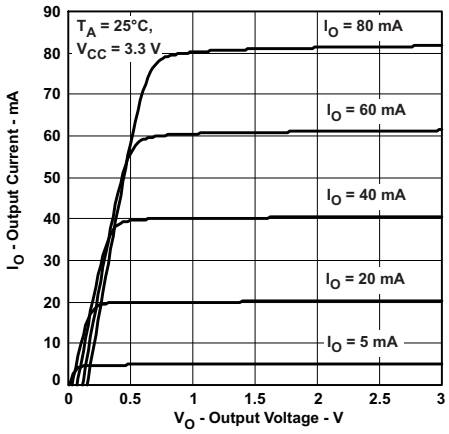


Figure 3. Output Current vs Output Voltage

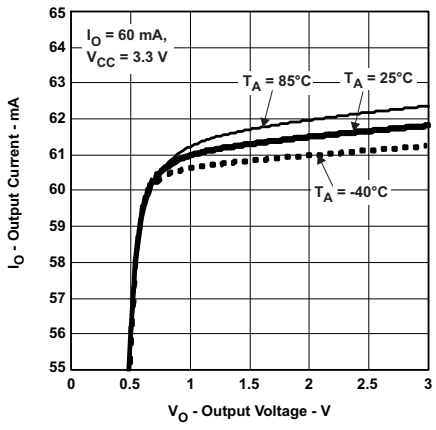


Figure 4. Output Current vs Output Voltage

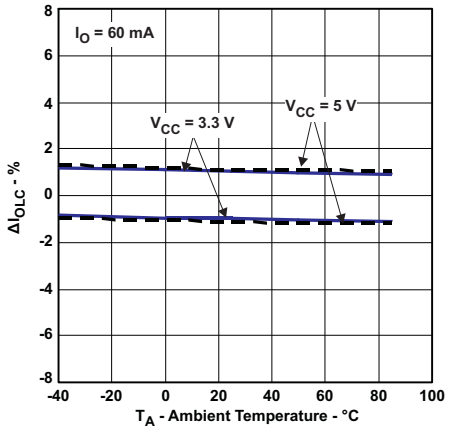


Figure 5. Delta Output Current vs Free-Air Temperature

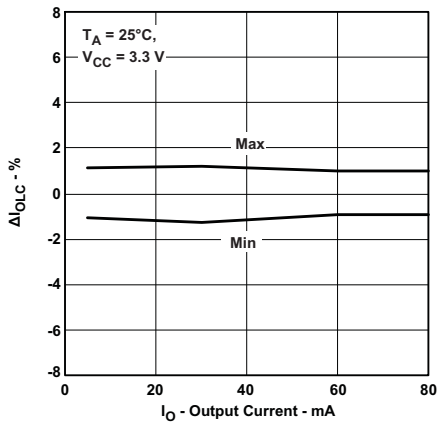


Figure 6. Delta Output Current vs Output Current

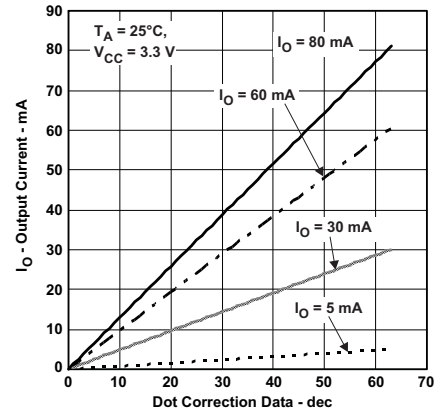


Figure 7. Dot Correction Linearity (ABS Value)

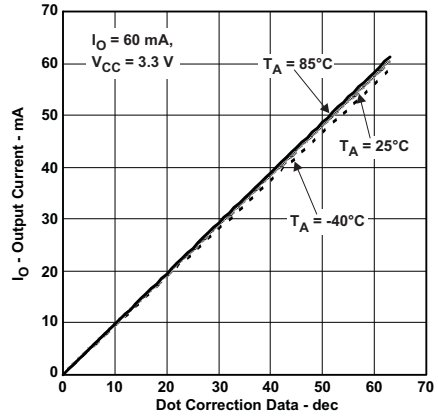


Figure 8. Dot Correction Linearity (ABS Value)

Typical Characteristics (continued)

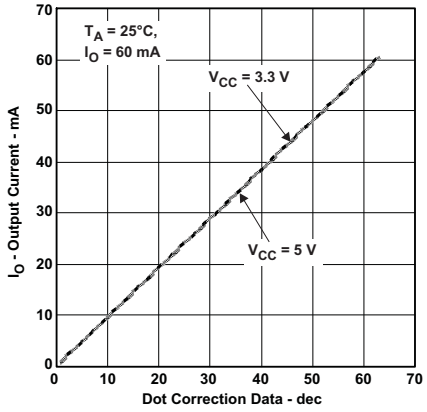


Figure 9. Dot Correction Linearity (ABS Value)

7 Parameter Measurement Information

7.1 Pin Equivalent Input and Output Schematic Diagrams

Resistor values are equivalent resistance and not tested.

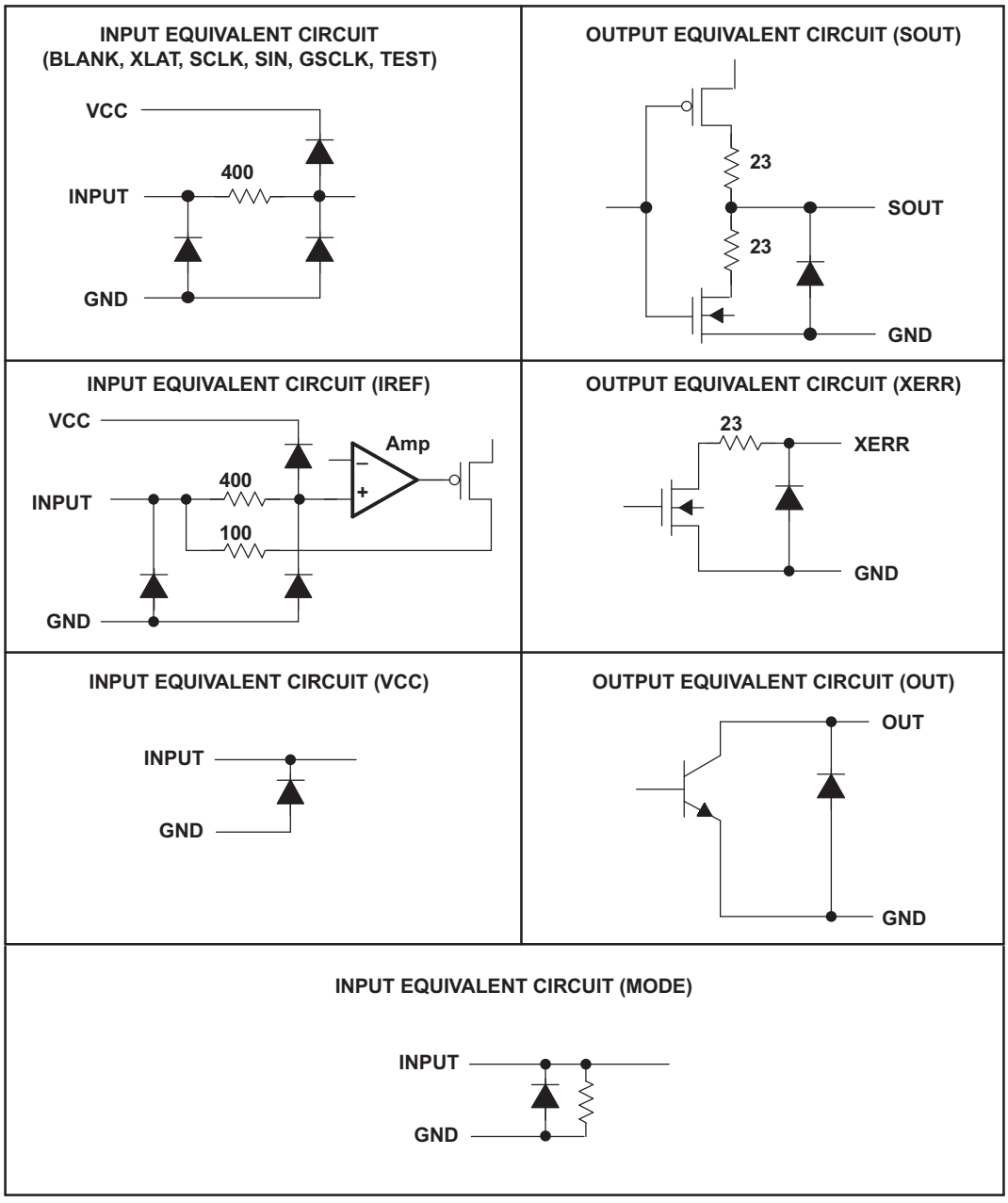


Figure 10. Input and Output Equivalent Circuits

Pin Equivalent Input and Output Schematic Diagrams (continued)

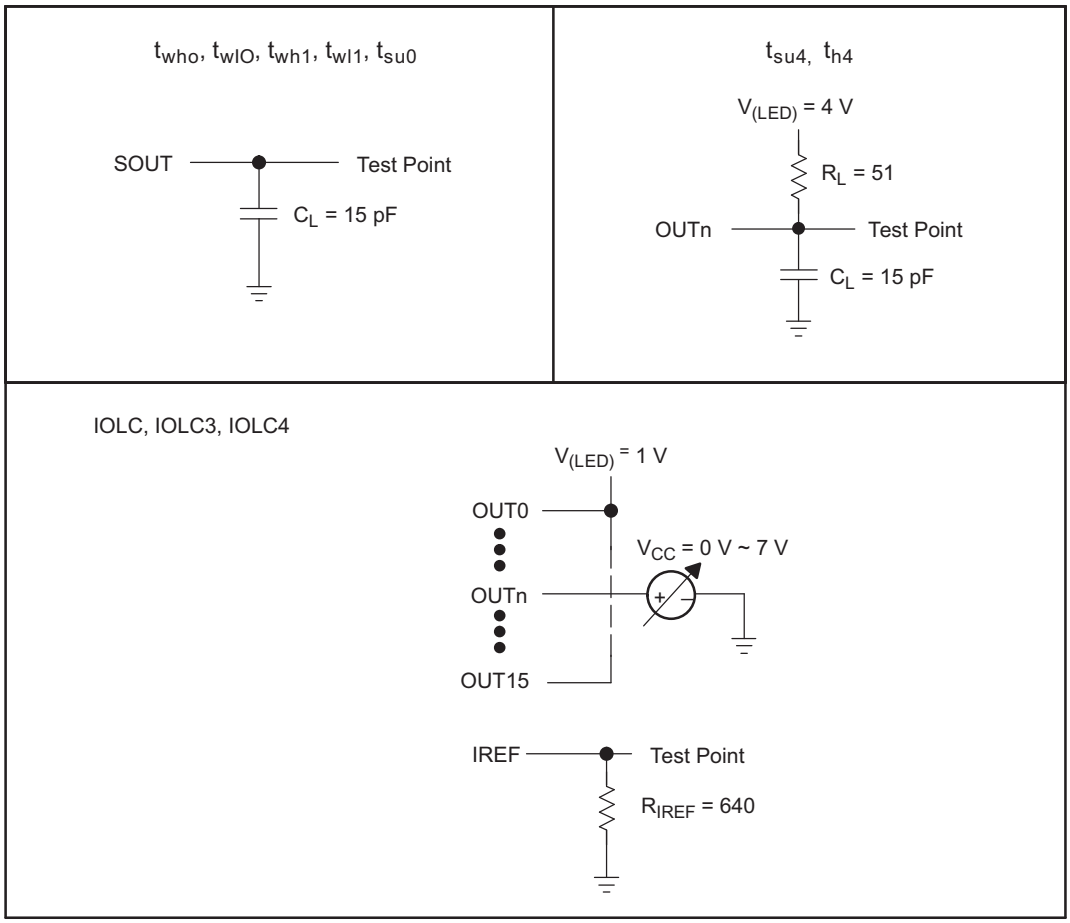


Figure 11. Parameter Measurement Circuits

7.2 Test Parameter Equations

$$\Delta(\%) = \frac{I_{OUTn} - I_{OUTavg\_0-15}}{I_{OUTavg\_0-15}} \times 100 \quad (1)$$

$$\Delta(\%) = \frac{I_{OUTavg} - I_{OUT(IDEAL)}}{I_{OUT(IDEAL)}} \times 100 \quad (2)$$

$$I_{OUT(IDEAL)} = 31.5 \times \left(\frac{1.24V}{R_{IREF}}\right) \quad (3)$$

$$\Delta(\%/V) = \frac{(I_{OUTn} \text{ at } V_{CC} = 5.5V) - (I_{OUTn} \text{ at } V_{CC} = 3.0V)}{(I_{OUTn} \text{ at } V_{CC} = 3.0V)} \times \frac{100}{2.5} \quad (4)$$

$$\Delta(\%/V) = \frac{(I_{OUTn} \text{ at } V_{OUTn} = 3.0V) - (I_{OUTn} \text{ at } V_{OUTn} = 1.0V)}{(I_{OUTn} \text{ at } V_{OUTn} = 1.0V)} \times \frac{100}{2.0} \quad (5)$$

8 Detailed Description

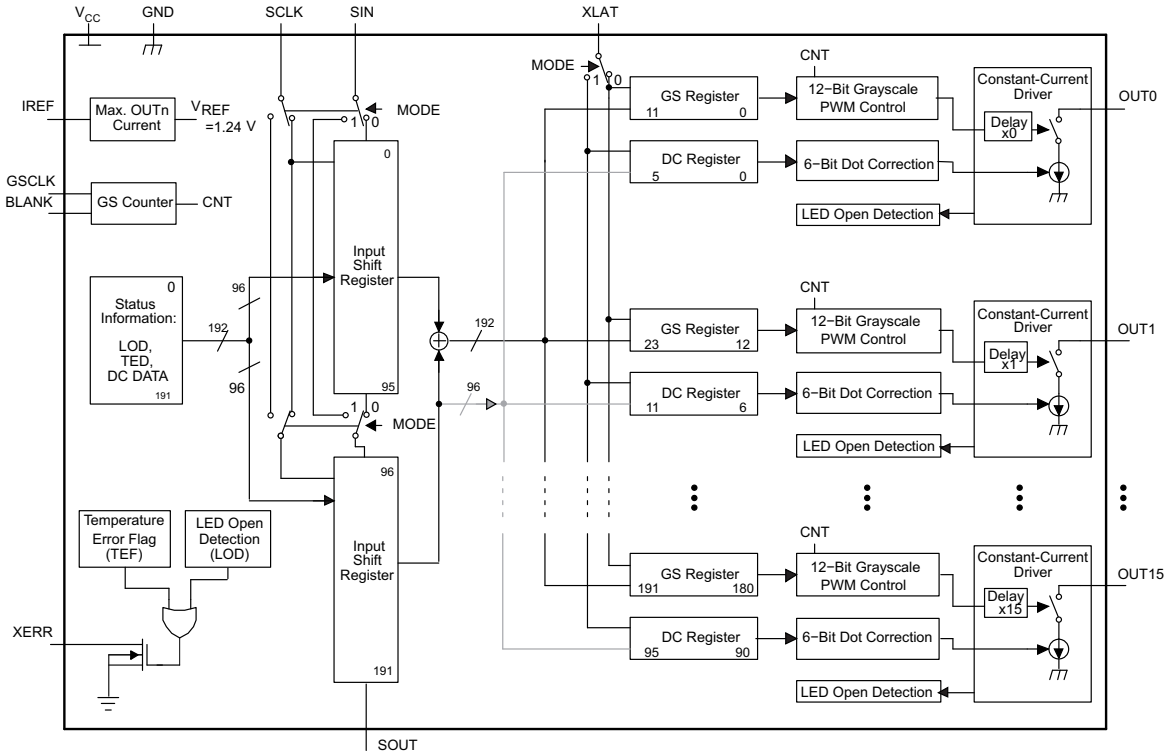
8.1 Overview

The TLC5941-Q1 device is a 16-channel constant-current sink LED driver with individual PWM dimming and dot correction, designed for LEDs in automotive indicator application. Each channel has up to 60-mA capability, giving a combined 960-mA current capability when paralleled. A single external resistor sets the maximum current value of all 16 channels.

The TLC5941-Q1 device can adjust 4096-step grayscale brightness of each channel OUTn individually, using a PWM control scheme. As well, the TLC5941-Q1 device has the capability to fine-adjust 64-step the output current of each channel independently. The dot correction adjusts the brightness variations between LED channels and other LED drivers. Both grayscale control and dot correction are accessible via a serial interface, which can be connected to microcontrollers or digital signal processors in various ways.

The integrated diagnostic circuit is used to detect device working condition, normal operation, LOD or TEF. The LED open detection (LOD) indicates a broken or disconnected LED at an output terminal. The thermal error flag (TEF) indicates an over temperature condition.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Serial Interface

The TLC5941-Q1 device has a flexible serial interface, which can be connected to microcontrollers or digital signal processors in various ways. Only 3 pins are needed to input data into the device. The rising edge of SCLK signal shifts the data from the SIN pin to the internal register. After all data is clocked in, a high-level pulse of XLAT signal latches the serial data to the internal registers. The internal registers are level-triggered latches of XLAT signal. All data are clocked in with the MSB first. The length of serial data is 96 bit or 192 bit, depending on the programming mode. Grayscale data and dot correction data can be entered during a grayscale cycle. Although new grayscale data can be clocked in during a grayscale cycle, the XLAT signal should only latch the

Feature Description (continued)

grayscale data at the end of the grayscale cycle. Latching in new grayscale data immediately overwrites the existing grayscale data. Figure 12 shows the timing chart. More than two TLC5941-Q1 devices can be connected in series by connecting an SOUT pin from one device to the SIN pin of the next device. An example of cascading two TLC5941-Q1 devices is shown in Figure 13. The SOUT pin can also be connected to the controller to receive status information from TLC5941-Q1 device as shown in Figure 18.

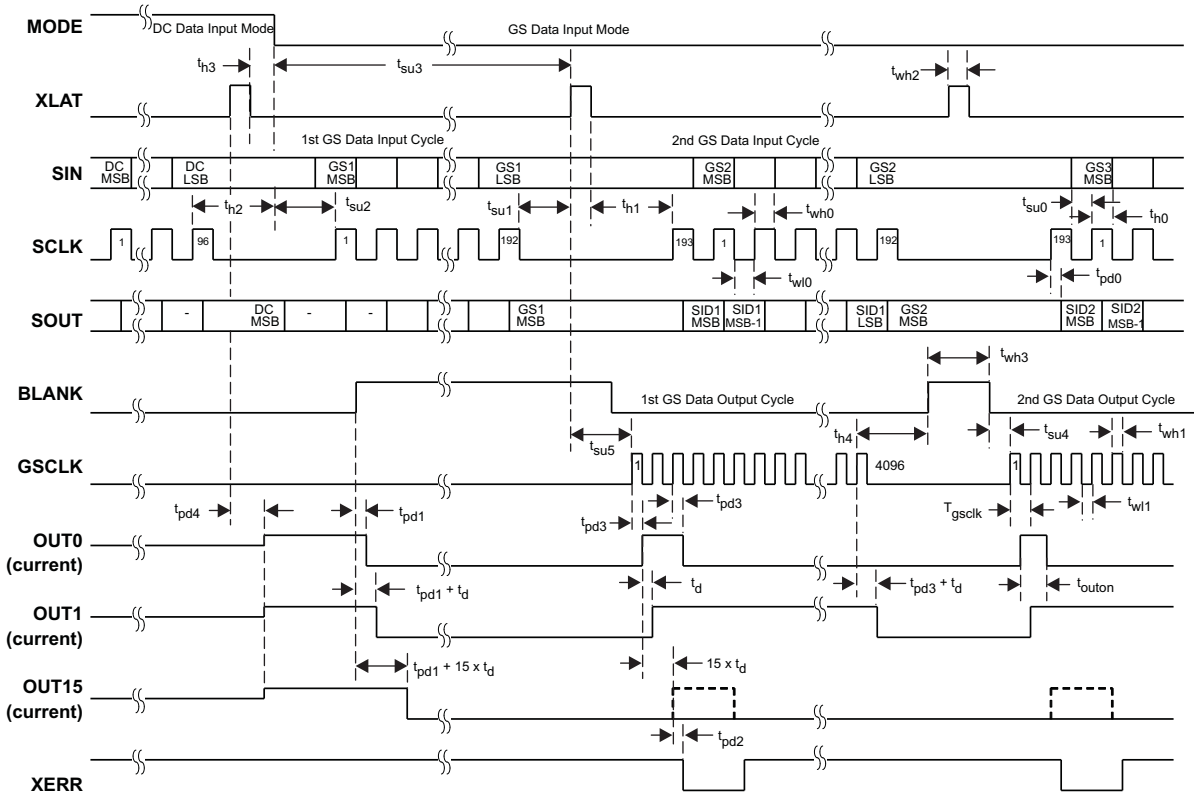


Figure 12. Serial Data Input Timing Chart

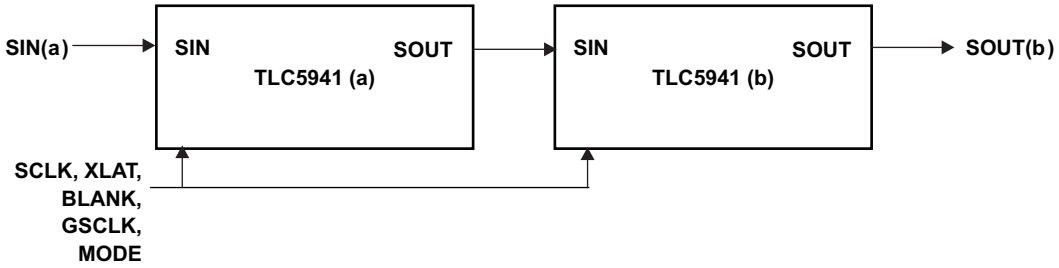


Figure 13. Cascading Two TLC5941-Q1 Devices

Feature Description (continued)

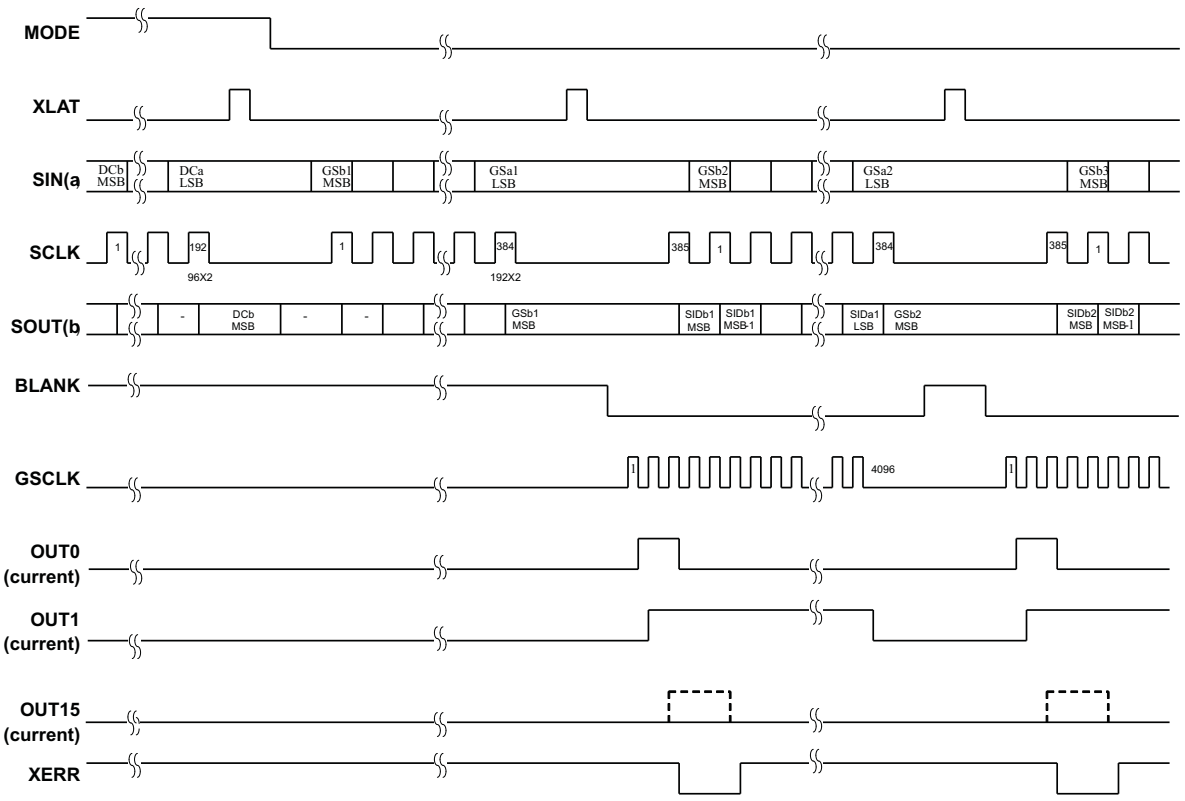


Figure 14. Timing Chart for Two Cascaded TLC5941-Q1 Devices

8.3.2 Error Information Output

The open-drain output XERR is used to report both of the TLC5941-Q1 error flags, TEF and LOD. During normal operating conditions, the internal transistor connected to the XERR pin is turned off. The voltage on XERR is pulled up to V_{CC} through an external pullup resistor. If TEF or LOD is detected, the internal transistor is turned on, and XERR is pulled to GND. Because XERR is an open-drain output, multiple ICs can be ORed together and pulled up to V_{CC} with a single pullup resistor which reduces the number of signals needed to report a system error (see Figure 18).

To differentiate LOD and TEF signal from XERR pin, LOD can be masked out with BLANK = HIGH.

Table 1. XERR Truth Table

ERROR CONDITION		ERROR INFORMATION		SIGNALS	
TEMPERATURE	OUTn VOLTAGE	TEF	LOD	BLANK	XERR
$T_J < T_{(TEF)}$	Don't Care	L	X	H	H
$T_J > T_{(TEF)}$	Don't Care	H	X		L
$T_J < T_{(TEF)}$	OUTn > $V_{(LED)}$	L	L	L	H
	OUTn < $V_{(LED)}$	L	H		L
$T_J > T_{(TEF)}$	OUTn > $V_{(LED)}$	H	L		L
	OUTn < $V_{(LED)}$	H	H		L

8.3.3 TEF: Thermal Error Flag

The TLC5941-Q1 device provides a temperature error flag (TEF) circuit to indicate an overtemperature condition of the IC. If the junction temperature exceeds the threshold temperature (160°C typical), the TEF flag becomes H and XERR pin goes to low level. When the junction temperature becomes lower than the threshold temperature, the TEF flag becomes L and the XERR pin becomes high impedance. The TEF status can also be read out from the TLC5941-Q1 status register.

8.3.4 LOD: LED Open Detection

The TLC5941-Q1 device has an LED-open detection circuit that detects broken or disconnected LEDs. The LED open detector pulls the XERR pin to GND when an open LED is detected. The XERR pin and the corresponding error bit in the Status Information Data is only active under the following open LED conditions:

1. OUTn is on and the time tpd2 (1 µs typical) has passed.
2. The voltage of OUTn is < 0.3V (typical)

The LOD status of each output can be also read out from the SOUT pin. See the *Status Information Output* section for details. The LOD error bits are latched into the Status Information Data when the XLAT pin returns to a low after a high. Therefore, the XLAT pin must be pulsed high then low while the XERR pin is active in order to latch the LOD error into the Status Information Data for subsequent reading via the serial shift register.

8.3.5 Delay Between Outputs

The TLC5941-Q1 device has graduated delay circuits between outputs. These circuits can be found in the constant current driver block of the device (see the functional block diagram). The fixed-delay time is 20 ns (typical), the OUT0 output has no delay, the OUT1 output has 20-ns delay, the OUT2 output has 40-ns delay, and so on. The maximum delay is 300 ns from the OUT0 output to the OUT15 output. The delay works during switch on and switch off of each output channel. These delays prevent large inrush currents which reduces the bypass capacitors when the outputs turn on.

8.3.6 Output Enable

All OUTn channels of the TLC5941-Q1 device can be switched off with one signal. When the BLANK signal is set high, all OUTn channels are disabled, regardless of logic operations of the device. The grayscale counter is also reset. When the BLANK signal is set low, all OUTn channels work under normal conditions. If BLANK goes low and then back high again in less than 300 ns, all outputs programmed to turn on still turn on for either the programmed number of grayscale clocks, or the length of time that the BLANK signal was low, which ever is lower. For example, if all outputs are programmed to turn on for 1 ms, but the BLANK signal is only low for 200 ns, all outputs still turn on for 200 ns, even though some outputs are turning on after the BLANK signal has already gone high.

Table 2. BLANK Signal Truth Table

BLANK	OUT0 to OUT15
LOW	Normal condition
HIGH	Disabled

8.3.7 Status Information Output

The TLC5941-Q1 device does have a status information register, which can be accessed in grayscale mode (MODE = GND). After the XLAT signal latches the data into the GS register, the input shift register data is replaced with status information data (SID) of the device (see Figure 22). The LOD, TEF, and dot-correction register data can be read out at the SOUT pin. The status information data packet is 192 bits wide. Bits 0 through 15 contain the LOD status of each channel. Bit 16 contains the TEF status. Bits 24 through 119 contain the data of the dot-correction register. The remaining bits are reserved. The complete status information data packet is shown in Figure 15.

The SOUT pin outputs the MSB of the SID at the same time the SID are stored in the SID register, as shown in Figure 16. The next SCLK pulse, which is the clock for receiving the MSB of the next grayscale data, transmits MSB-1 of SID. If output voltage is < 0.3 V (typical) when the output sink current turns on, the LOD status flag becomes active. The LOD status flag is an internal signal which pulls the XERR pin down to low when the LOD status flag becomes active. The delay time, t_{pd2} (1 µs, maximum), is from the time of turning on the output sink

current to the time the LOD status flag becomes valid. The timing for each channels LOD status to become valid is shifted by the 30-ns (maximum), channel-to-channel turn-on time. After the first GSCLK pin goes high, the OUT0 LOD status is valid; $t_{pd3} + t_{pd2}$ = 60 ns + 1 µs = 1.06 µs. The OUT1 LOD status is valid; $t_{pd3} + t_d + t_{pd2}$ = 60 ns + 30 ns + 1 µs = 1.09 µs. The OUT2 LOD status is valid; $t_{pd3} + 2^{td} + t_{pd2}$ = 1.12 µs, and so on. The total time from the first GSCLK rising edge until all LOD become valid is about 1.51 µs maximum ($t_{pd3} + 15^{td} + t_{pd2}$); t_{suLOD} must be > 1.51 µs (see Figure 16) to ensure that all LOD data are valid.

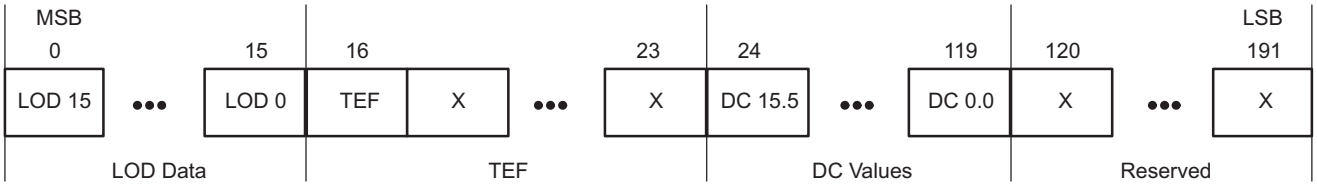


Figure 15. Status Information Data Packet Format

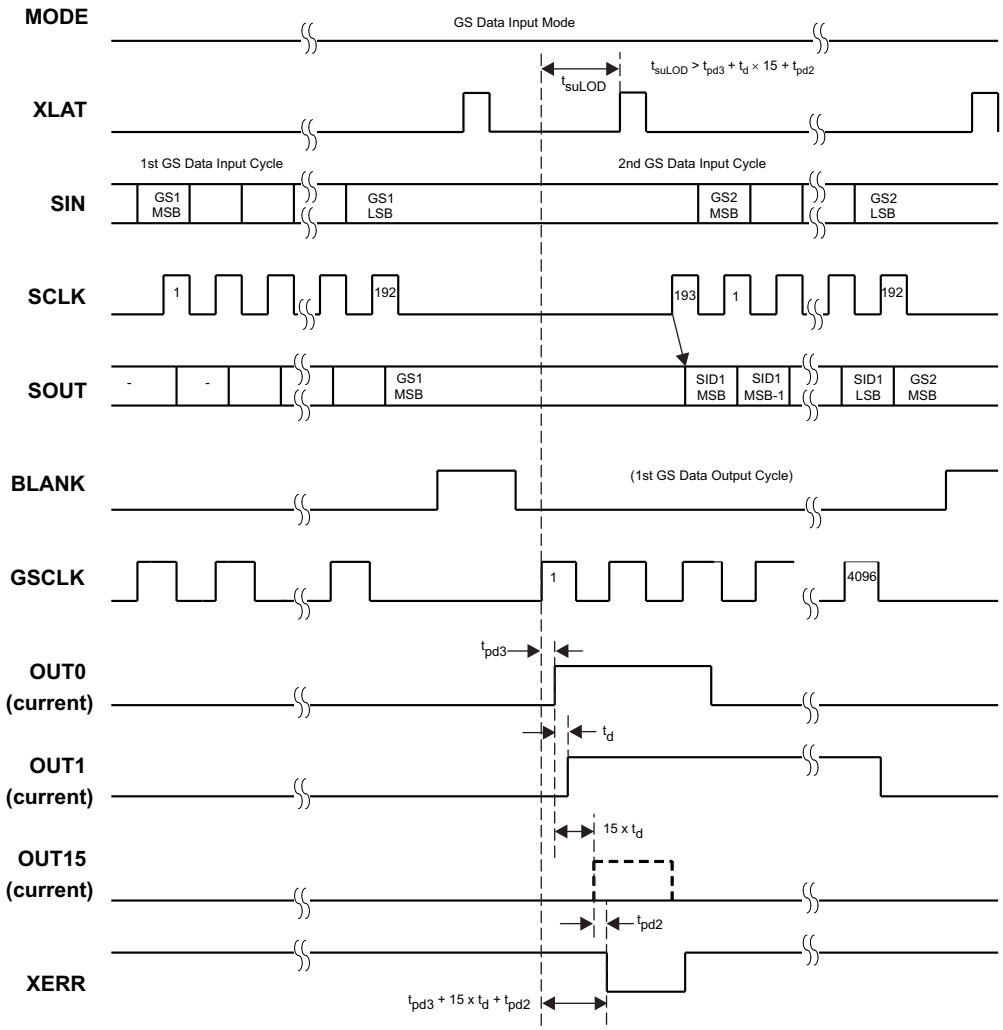


Figure 16. Readout Status Information Data (SID) Timing Chart

The LOD status of each output can be read out from the SOUT pin. The LOD error bits are latched into the Status Information Data when the XLAT pin returns to a low after a high. Therefore, the XLAT pin must be pulsed high then low while the XERR pin is active in order to latch the LOD error into the Status Information Data for subsequent reading through the serial shift register.

8.3.8 Grayscale PWM Operation

The grayscale PWM cycle begins with the falling edge of BLANK. The first GSCLK pulse after the BLANK pin goes low increases the grayscale counter by one and switches on all OUTn pins with grayscale value not zero. Each following rising edge of the GSCLK pin increases the grayscale counter by one. The TLC5941-Q1 device compares the grayscale value of each output, OUTn, with the grayscale counter value. All OUTn pins with grayscale values equal to the counter values are switched off. A BLANK = H signal after 4096 GSCLK pulses resets the grayscale counter to zero and completes the grayscale PWM cycle (see Figure 17). When the counter reaches a count of FFFh, the counter stops counting and all outputs turn off. Pulling the BLANK pin high before the counter reaches FFFh immediately resets the counter to zero.

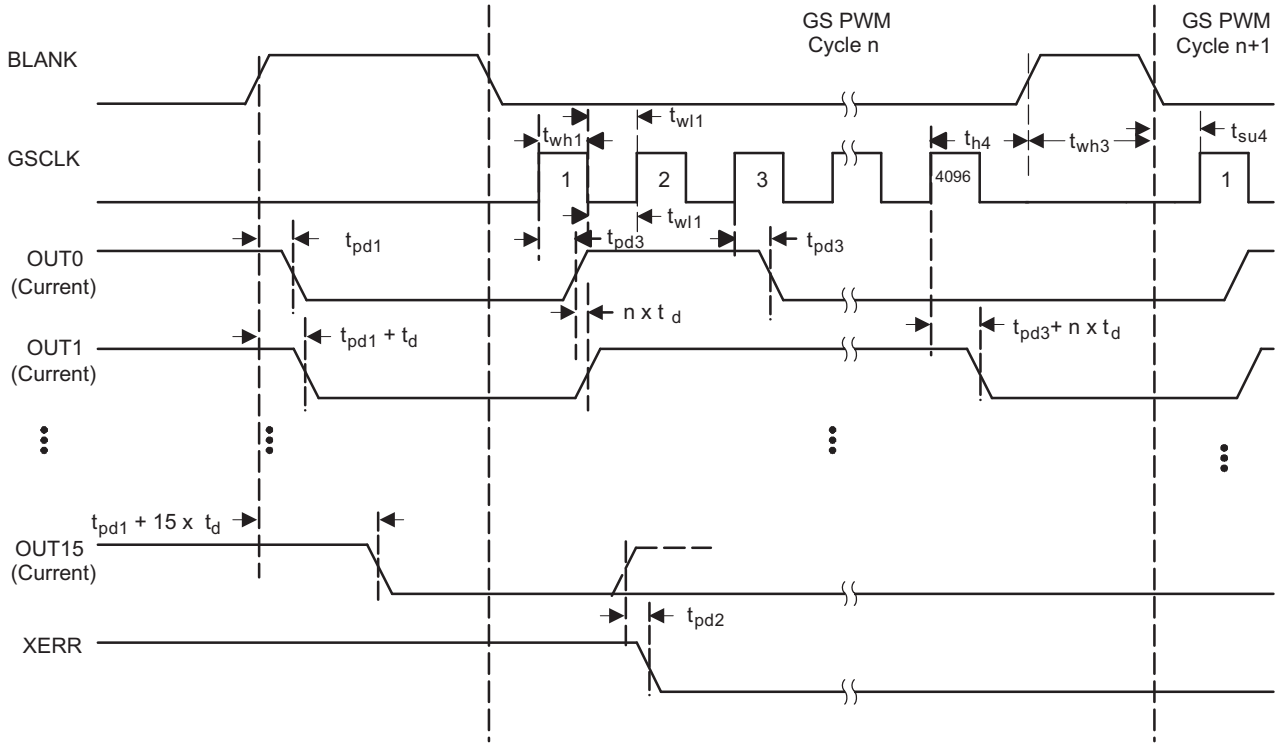


Figure 17. Grayscale PWM Cycle Timing Chart

8.3.8.1 Output On Time

The amount of time that each output is turned on is a function of the grayscale clock frequency and the programmed grayscale PWM value. The on-time of each output can be calculated using Equation 6.

$$T\_on_n = \frac{GSn}{f_{(GSCLK)}} + t_{on\_err} \quad (6)$$

where

- T_on_n is the time that the OUTn pin turns on and sinks current
- GSn is the programmed grayscale PWM value of the OUTn pin between 0 and 4095
- t_{on_err} is the output on time error defined in the *Switching Characteristics* table
-

When using Equation 6 with very high GSCLK frequencies and very low grayscale PWM values, the resulting T_on time may be negative. If T_on is negative, the output does not turn on. For example, using f(GSCLK) = 30 MHz, GSn = 1, and the typical t_{on_err} = 50 nS, Equation 6 calculates that OUTn turns on for –16.6 ns. This output may not turn on under these conditions. Increasing the PWM value or reducing the GSCLK clock frequency ensures turn-on.

8.4 Device Functional Modes

8.4.1 Operating Modes

The TLC5941-Q1 device has two operating modes defined by MODE as shown in Table 3. The GS and DC registers are set to random values that are not known just after power on. The GS and DC values must be programmed before turning on the outputs.

NOTE

When initially setting GS and DC data after power on, the GS data must be set before the DC data is set. Failure to set GS data before DC data may result in the first bit of GS data being lost. The XLAT pin must be low when the MODE pin goes high-to-low or low-to-high to change back and forth between GS mode and DC mode.

Table 3. TLC5941-Q1 Operating Modes Truth Table

MODE	INPUT SHIFT REGISTER	OPERATING MODE
GND	192 bit	Grayscale PWM Mode
V_{CC}	96 bit	Dot Correction Data Input Mode

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TLC5941-Q1 device can be used for LED lighting, such as signboards and automotive dashboard back-lighting.

9.2 Typical Application

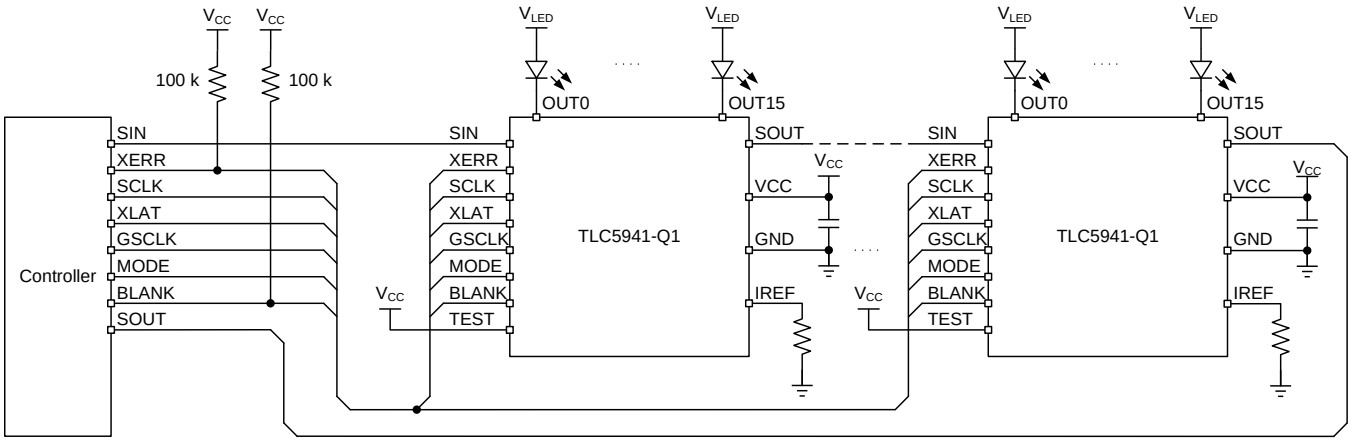


Figure 18. Cascading Devices

9.2.1 Design Requirements

For the design example, use the following as the input parameter.

- V_{CC} = 5 V
- V_{LED} = 5 V – 16 V
- I_{MAX} = 30 mA

9.2.2 Detailed Design Procedure

9.2.2.1 Setting Maximum Channel Current

The maximum output current per channel is programmed by a single resistor, $R_{(IREF)}$, which is placed between the IREF pin and the GND pin. The voltage on the IREF pin is set by an internal band gap $V_{(IREF)}$ with a typical value of 1.24 V. The maximum channel current is equivalent to the current flowing through $R_{(IREF)}$ multiplied by a factor of 31.5. The maximum output current can be calculated by Equation 7.

$$I_{max} = \frac{V_{(IREF)}}{R_{(IREF)}} \times 31.5 \quad (7)$$

where

- $V_{(IREF)}$ = 1.24 V
- $R_{(IREF)}$ = User-selected external resistor.

The value of I_{max} must be set between 5 mA and 60 mA. The output current may be unstable if I_{max} is set lower than 5 mA. Output currents lower than 5 mA can be achieved by setting I_{max} to 5 mA or higher and then using dot correction.

Typical Application (continued)

Figure 1 shows the maximum output current I_O versus $R_{(IREF)}$. $R_{(IREF)}$ is the value of the resistor between IREF terminal to GND, and I_O is the constant output current of OUT0 to OUT15. A variable power supply may be connected to the IREF pin through a resistor to change the maximum output current per channel. The maximum output current per channel is 31.5 times the current flowing out of the IREF pin.

9.2.2.2 Power Dissipation Calculation

The device power dissipation must be below the power dissipation rate of the device package to ensure correct operation. Equation 8 calculates the power dissipation of device.

$$P_D = \left(V_{CC} \times I_{CC}\right) + \left(V_{OUT} \times I_{MAX} \times N \times \frac{DC_n}{63} \times d_{PWM}\right)$$

where

- V_{CC}: device supply voltage
- I_{CC}: device supply current
- V_{OUT}: TLC5941-Q1 OUTn voltage when driving LED current
- I_{MAX}: LED current adjusted by $R_{(IREF)}$ resistor
- DC_n: maximum dot correction value for OUTn
- N: number of OUTn driving LED at the same time
- d_{PWM}: duty cycle defined by BLANK pin or GS PWM value (8)

9.2.2.3 Setting Dot Correction

The TLC5941-Q1 device has the capability to fine-adjust the output current of each channel (OUT0 to OUT15) independently which is also called dot correction. This feature is used to adjust the brightness deviations of LEDs connected to the output channels OUT0 to OUT15. Each of the 16 channels can be programmed with a 6-bit word. The channel output can be adjusted in 64 steps from 0% to 100% of the maximum output current I_{max}. The TEST pin must be connected to V_{CC} to ensure proper operation of the dot correction circuitry. Equation 9 calculates the output current for each output n.

$$I_{OUTn} = I_{max} \times \frac{DCn}{63}$$

where

- I_{max} = the maximum programmable output current for each output.
- DCn = the programmed dot correction value for output n (DCn = 0 to 63)
- n = 0 to 15 (9)

Figure 19 shows the dot correction data packet format which consists of 6 bits x 16 channel, total 96 bits. The format is Big-Endian format. This means that the MSB is transmitted first, followed by the MSB-1 and so on. The DC 15.5 in Figure 19 stands for the 5th-most significant bit for output 15.

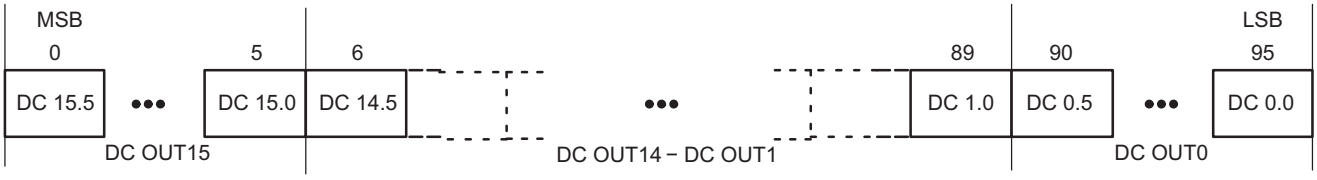


Figure 19. Dot Correction Data Packet Format

Typical Application (continued)

When the MODE pin is set to V_{CC}, the TLC5941-Q1 device enters the dot correction data input mode. The length of input shift register becomes 96bits. After all serial data are shifted in, the TLC5941-Q1 device writes the data in the input shift register to DC register when the XLAT pin is high, and holds the data in the DC register when the XLAT pin is low. The DC register is a level triggered latch of the XLAT signal. Because the XLAT pin is a level-triggered signal, SCLK and SIN must not be changed while the XLAT pin is high. After the XLAT pin goes low, data in the DC register is latched and does not change. The BLANK signal does not need to be high to latch in new data. When the XLAT pin goes high, the new dot-correction data immediately becomes valid and changes the output currents if the BLANK pin is low. the XLAT pin has setup time (t_{su1}) and hold time (t_{h1}) to SCLK as shown in Figure 12.

To input data into the dot correction register, the MODE pin must be set to V_{CC}. The internal input shift register is then set to 96-bit width. After all serial data are clocked in, a rising edge of the XLAT pin is used to latch the data into the dot correction register. Figure 20 shows the DC-data input-timing chart.

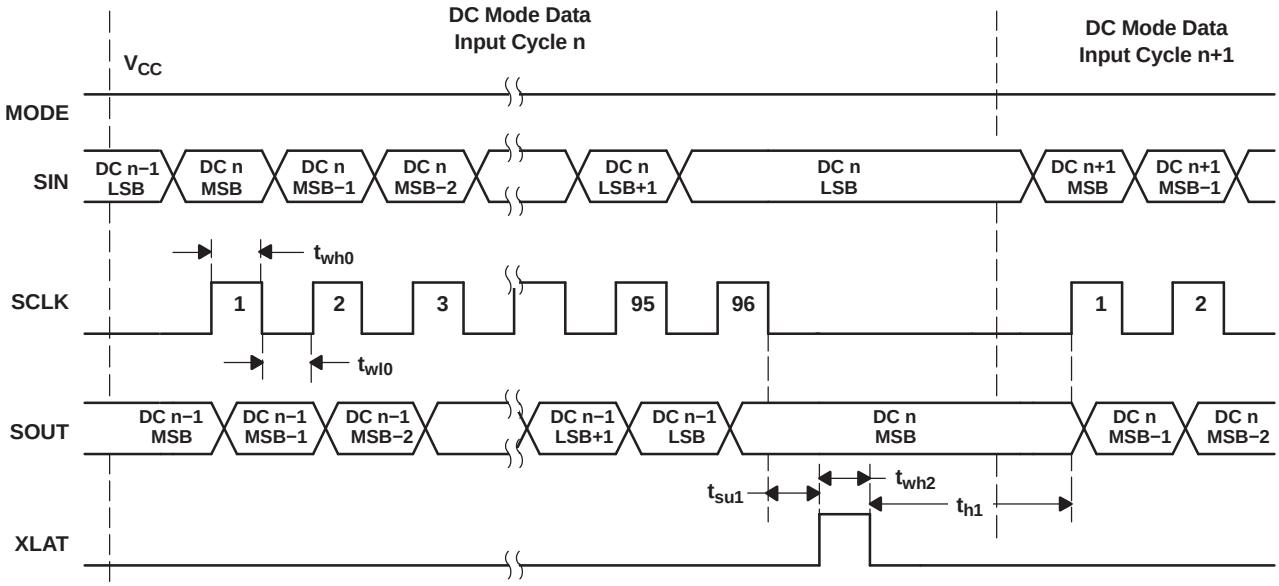


Figure 20. Dot-Correction Data Input-Timing Chart

9.2.2.4 Setting Grayscale

The TLC5941-Q1 device can adjust the brightness of each channel, OUTn, using a PWM control scheme. The use of 12 bits per channel results in 4096 different brightness steps, from 0% to 100% brightness. Equation 10 calculates the brightness level for each output n.

$$\text{Brightness in \%} = \frac{GSn}{4095} \times 100 \quad (10)$$

where

- GSn = the programmed grayscale value for output n (GSn = 0 to 4095)
- n = 0 to 15
- Grayscale data for all OUTn

The input shift register enters grayscale data into the grayscale register for all channels simultaneously. The complete grayscale data format consists of 16 × 12 bit words, which forms a 192-bit wide data packet (see Figure 21). The data packet must be clocked in with the MSB first.

Typical Application (continued)

Figure 21. Grayscale Data Packet Format

When the MODE pin is set to GND, the TLC5941-Q1 device enters the grayscale data input mode. The device switches the input shift register to 192-bit width. After all data is clocked in, a rising edge of the XLAT signal latches the data into the grayscale register (see Figure 22). New grayscale data immediately becomes valid at the rising edge of the XLAT signal; therefore, new grayscale data should be latched at the end of a grayscale cycle when BLANK is high. The first GS data input cycle after dot correction requires an additional SCLK pulse after the XLAT signal to complete the grayscale update cycle. All GS data in the input shift register is replaced with status information data (SID) after updating the grayscale register.

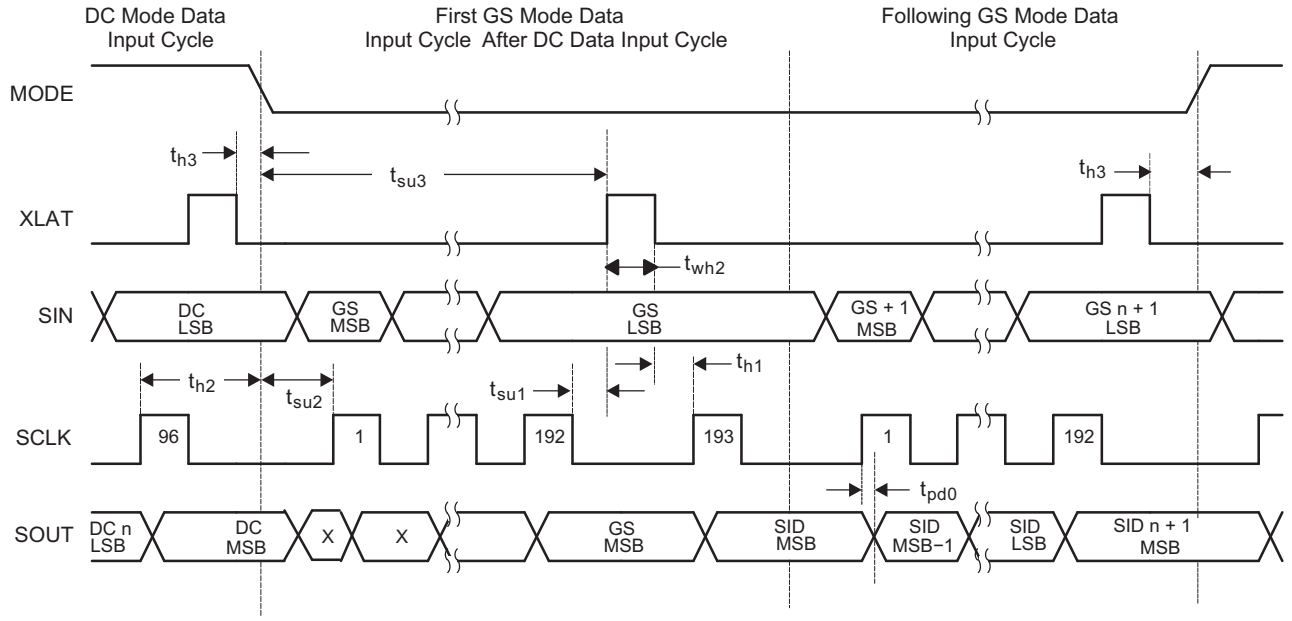


Figure 22. Grayscale Data Input Timing Chart

9.2.2.5 Serial Data Transfer Rate

Figure 18 shows a cascading connection of *n* TLC5941-Q1 devices connected to a controller, building a basic module of an LED display system. The TLC5941-Q1 device has no limit to the maximum number of ICs that can be cascaded. The maximum number of cascading TLC5941-Q1 devices depends on the application system and is in the range of 40 devices. Equation 11 calculates the minimum frequency needed:

$$f_{(GSCLK)} = 4096 \times f_{(update)}$$

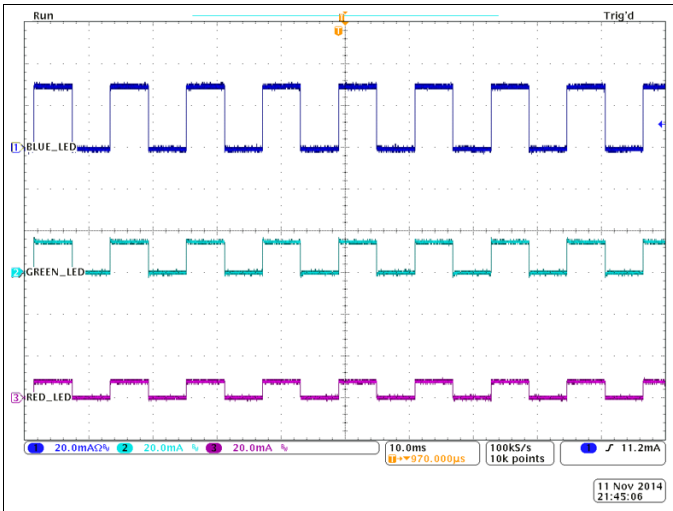
$$f_{(SCLK)} = 193 \times f_{(update)} \times n \quad (11)$$

where

- $f_{(GSCLK)}$: minimum frequency needed for GSCLK
- $f_{(SCLK)}$: minimum frequency needed for SCLK and SIN
- $f_{(update)}$: update rate of whole cascading system
- n: number cascaded of TLC5941-Q1 device

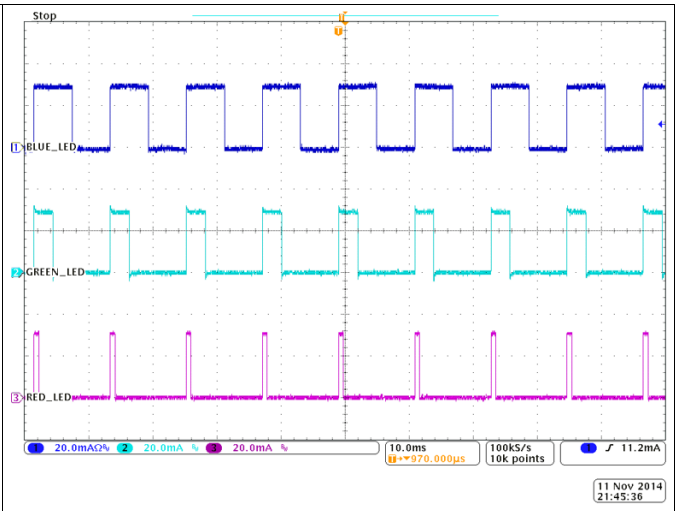
Typical Application (continued)

9.2.3 Application Curves



CH1 DC=63 CH2 DC=31 CH3 DC=15

Figure 23. Current with Dot Correction



CH1 GS=512 CH2 GS=256 CH3 GS=64

Figure 24. Current with Grayscale PWM Brightness Control

10 Power Supply Recommendations

The TLC5941-Q1 devices is qualified for automotive applications. The normal power supply connection is therefore an automotive electrical system that provides a voltage within the range specified in the *Recommended Operating Conditions*.

VCC pin and BLANK pin should be powered up before micro-controller or digital signal processor sends the control signal to the device.

11 Layout

11.1 Layout Guidelines

In order to prevent thermal shutdown, T_J must be less than 150ºC. If the input voltage is very high, the power dissipation might be large. Currently there is the HTSSOP package which has good thermal impedance, but at the same time, the PCB layout is also very important. Good PCB design can optimize heat transfer, which is absolutely essential for the long-term reliability of the device.

- Maximize the copper coverage on the PCB to increase the thermal conductivity of the board, because the major heat-flow path from the package to the ambient is through the copper on the PCB. Maximum copper is extremely important when there are not any heat sinks attached to the PCB on the other side of the package.
- Add as many thermal vias as possible directly under the package ground pad to optimize the thermal conductivity of the board.
- All thermal vias should be either plated shut or plugged and capped on both sides of the board to prevent solder voids. To ensure reliability and performance, the solder coverage should be at least 85 percent.

11.2 Layout Example

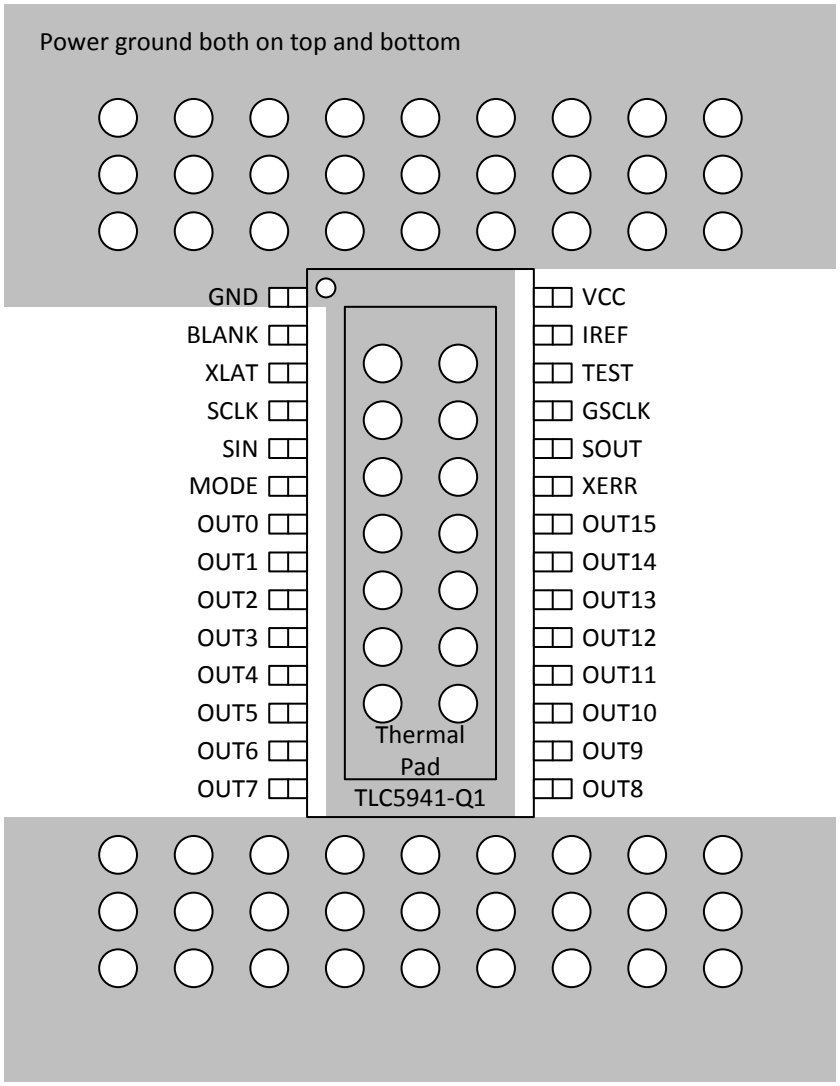


Figure 25. PCB Layout Example

12 Device and Documentation Support

12.1 Trademarks

All trademarks are the property of their respective owners.

12.2 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.3 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLC5941QPWPRQ1	ACTIVE	HTSSOP	PWP	28	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-3-260C-168 HR	-40 to 125	TLC5941Q	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF TLC5941-Q1 :

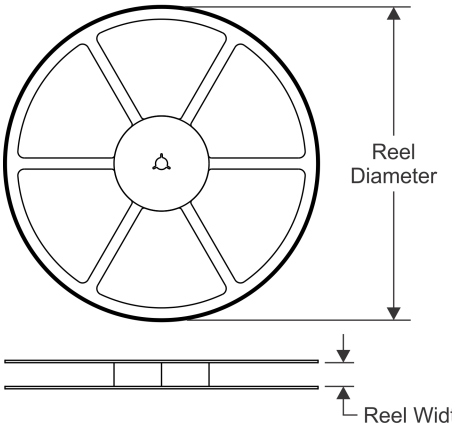
- Catalog: TLC5941

NOTE: Qualified Version Definitions:

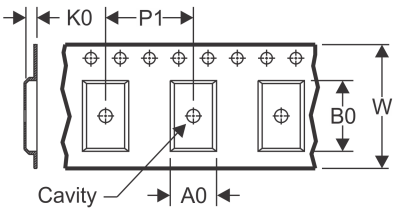
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

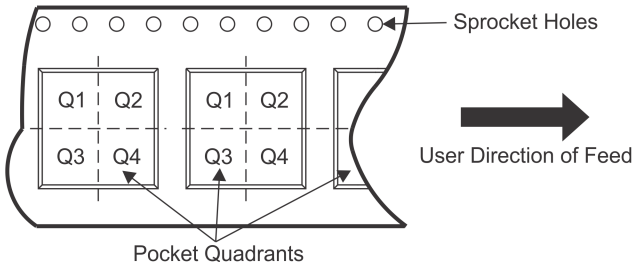


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

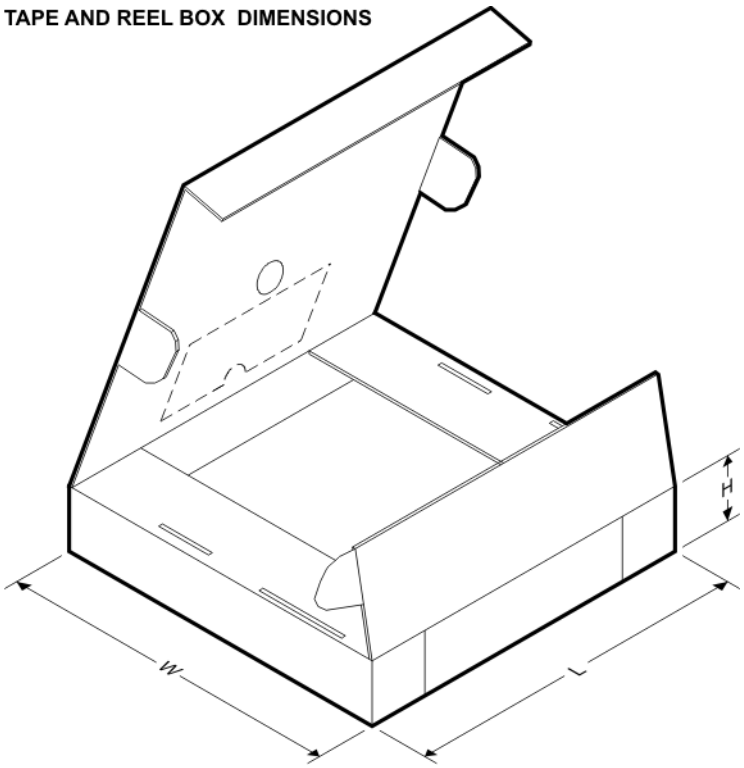
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLC5941QPWPRQ1	HTSSOP	PWP	28	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLC5941QPWPRQ1	HTSSOP	PWP	28	2000	350.0	350.0	43.0

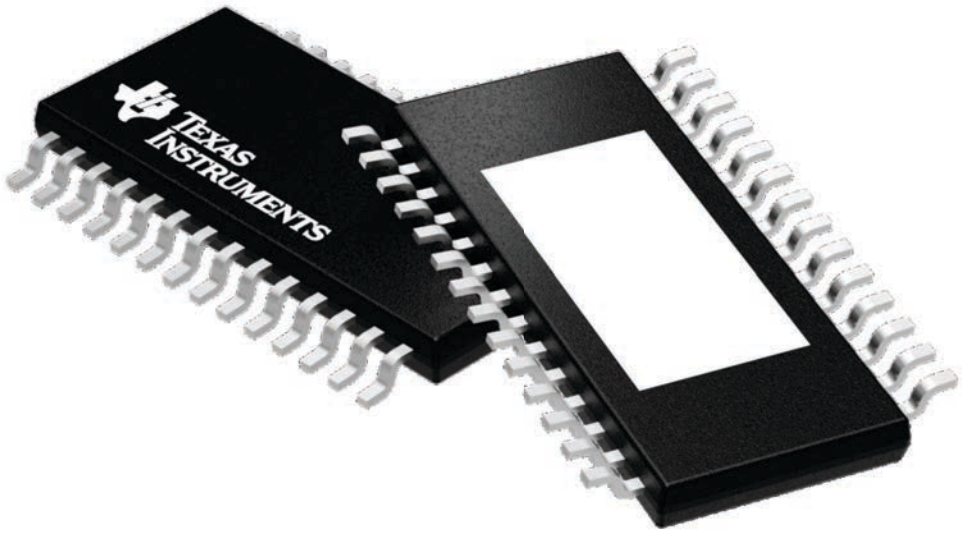
GENERIC PACKAGE VIEW

PWP 28

PowerPAD™ TSSOP - 1.2 mm max height

4.4 x 9.7, 0.65 mm pitch

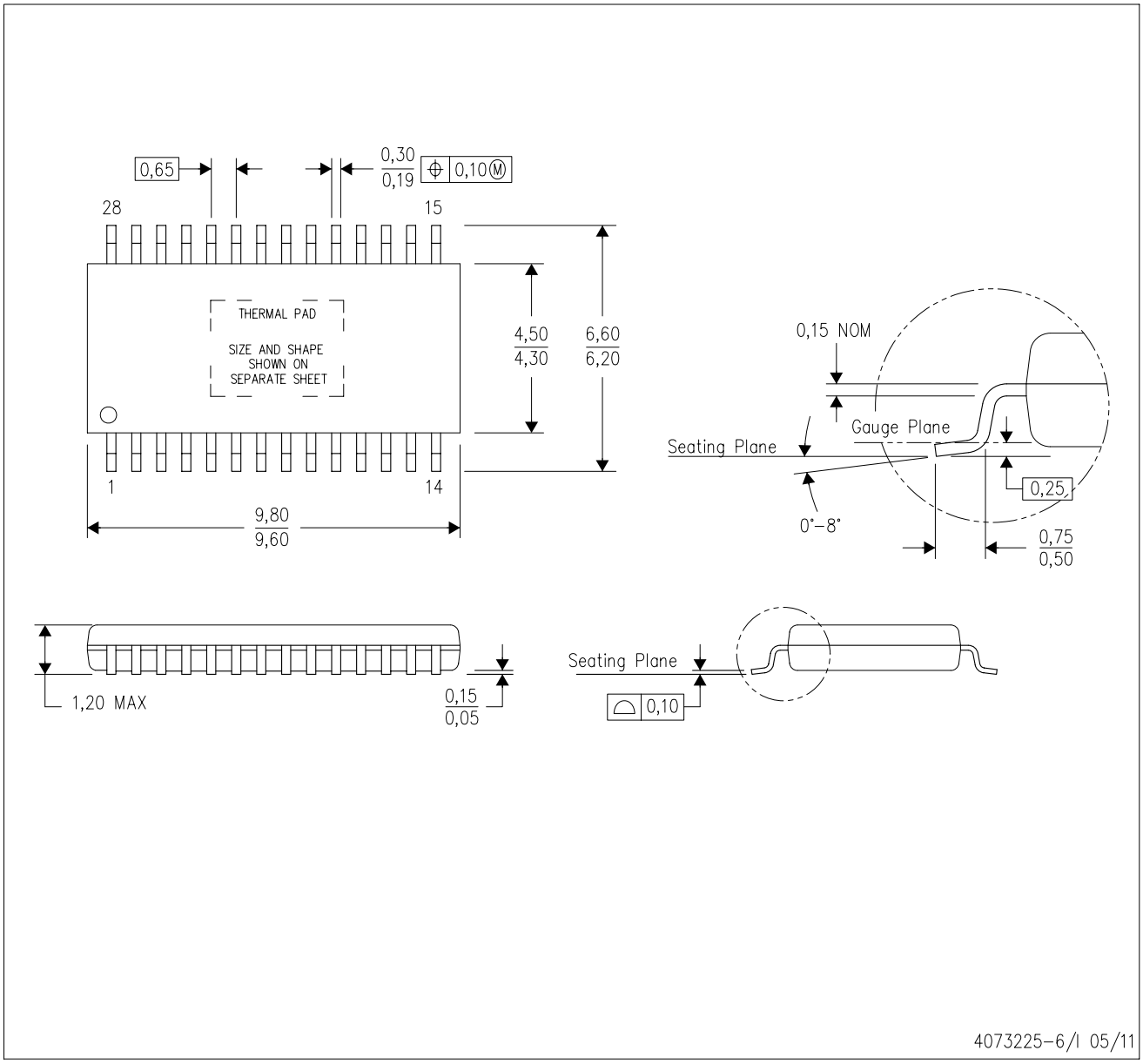
SMALL OUTLINE PACKAGE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4224765/A

PWP (R–PDSO–G28) PowerPAD™ PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
E. Falls within JEDEC MO–153

PowerPAD is a trademark of Texas Instruments.

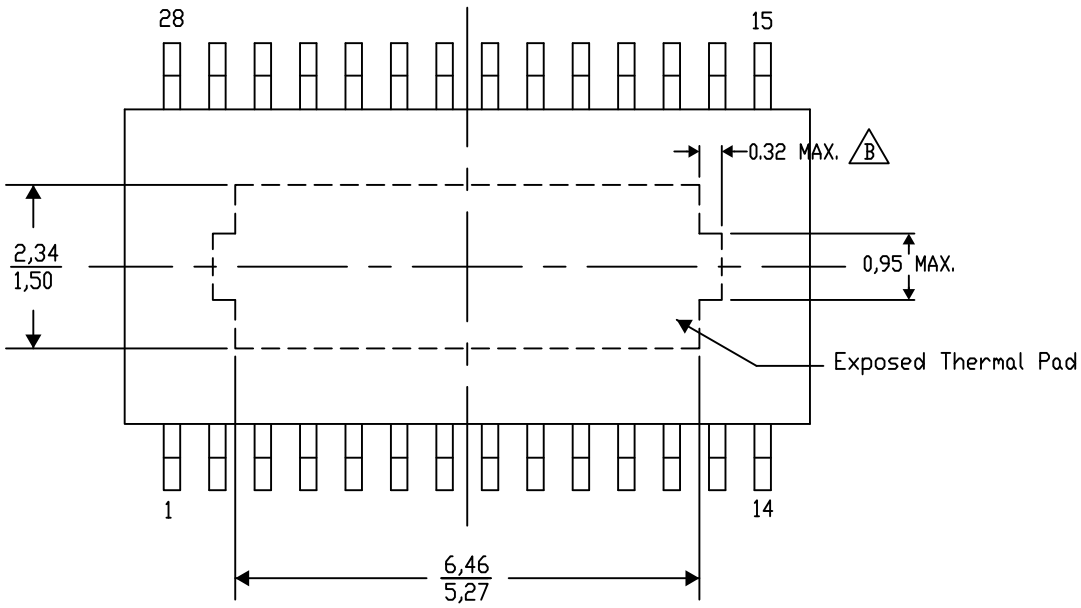
PWP (R–PDSO–G28) PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

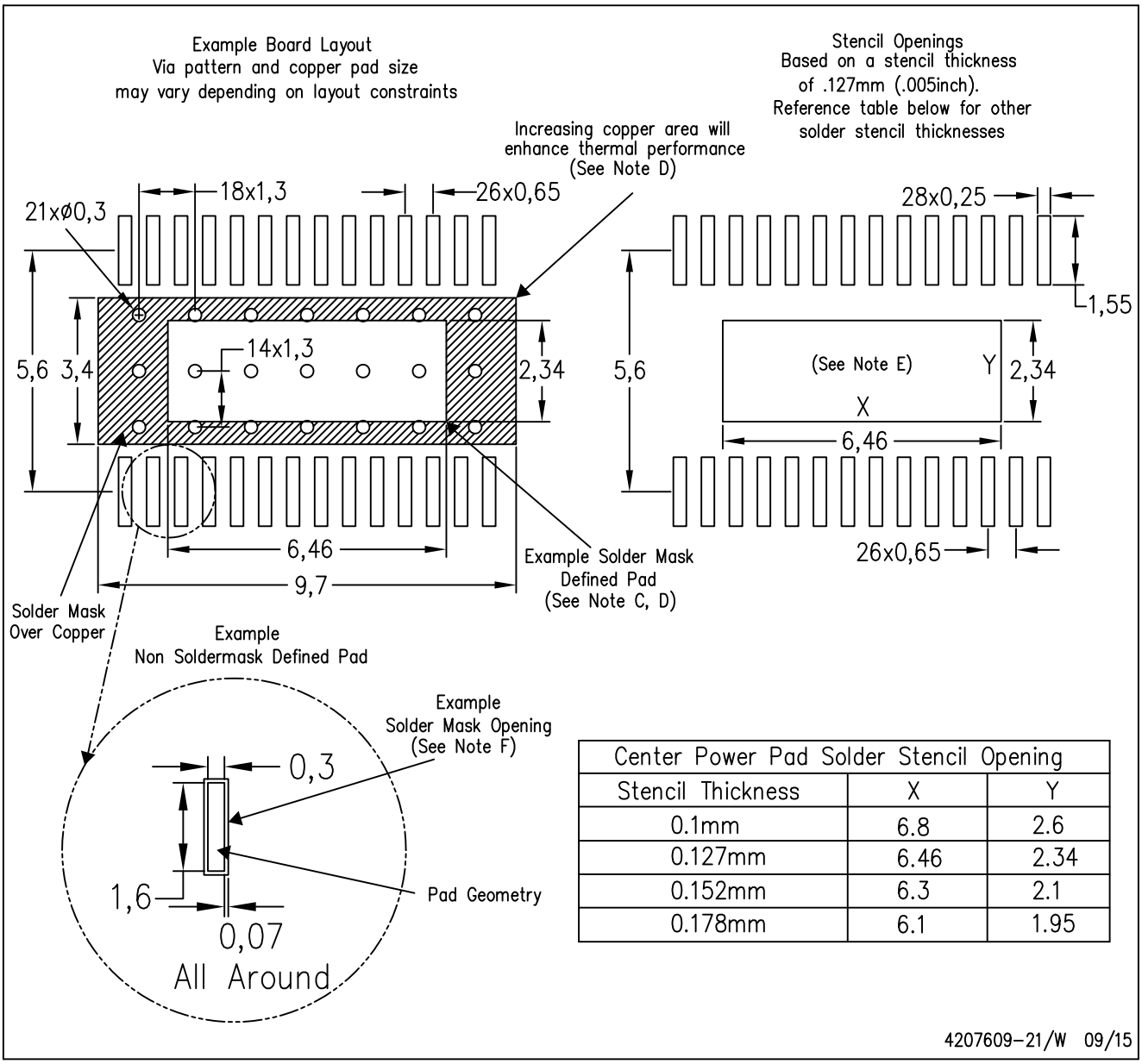
4206332–36/AO 01/16

NOTE: A. All linear dimensions are in millimeters

B. Exposed tie strap features may not be present.

PowerPAD is a trademark of Texas Instruments

PWP (R–PDSO–G28) PowerPAD™ PLASTIC SMALL OUTLINE



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	6.8	2.6
0.127mm	6.46	2.34
0.152mm	6.3	2.1
0.178mm	6.1	1.95

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NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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