SN65HVD62 AISG On-Off Keying Modem Evaluation Module (EVM)

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1 Introduction

This user's guide details the evaluation module (EVM) operation of factory installed SN65HVD62 AISG On Off Keying Coax Modem Transceivers. The EVM may be configured to evaluate one SN65HVD62 IC in a stand-alone configuration or to hook up two EVMS in a system scenario with one acting as a transmitter while the other acts as the receiver and vice-versa.

1.1 Overview

SN65HVD62 is an integrated AISG transceiver designed to be compliant with the Antenna Interface Standards Group v2.0 specification.

The receive channel integrates an active bandpass filter to enable demodulation of signals even in the presence of spurious frequency components.

The transmitter supports adjustable output power levels varying from 0dBm to +6dBm delivered to the 50Ω coax cable.

A direction output is provided which facilitates bus arbitration for an RS-485 interface. These devices integrate an oscillator input for a crystal and also accept standard clock inputs to the oscillator.

The pinout of the SN65HVD62 device is shown in Figure 1.

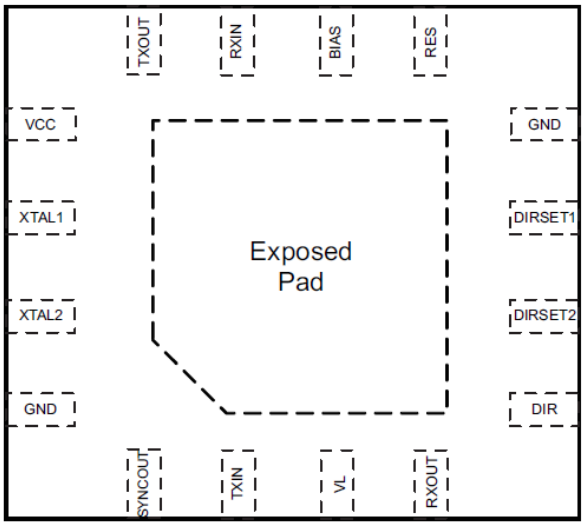


Figure 1. SN65HVD62 Pinout

1.2 SN65HVD62EVM Kit Contents

1. SN65HVD62EVM Circuit Board (PWB P/N 6559756).
2. SN65HVD62EVM User's Guide (SLLU152)
3. SN65HVD62 Datasheet (SLLSE94)

2 EVM Description

A picture of the EVM is shown in Figure 2. The EVM comes with two SN65HVD62 devices installed at locations U1 and U2.

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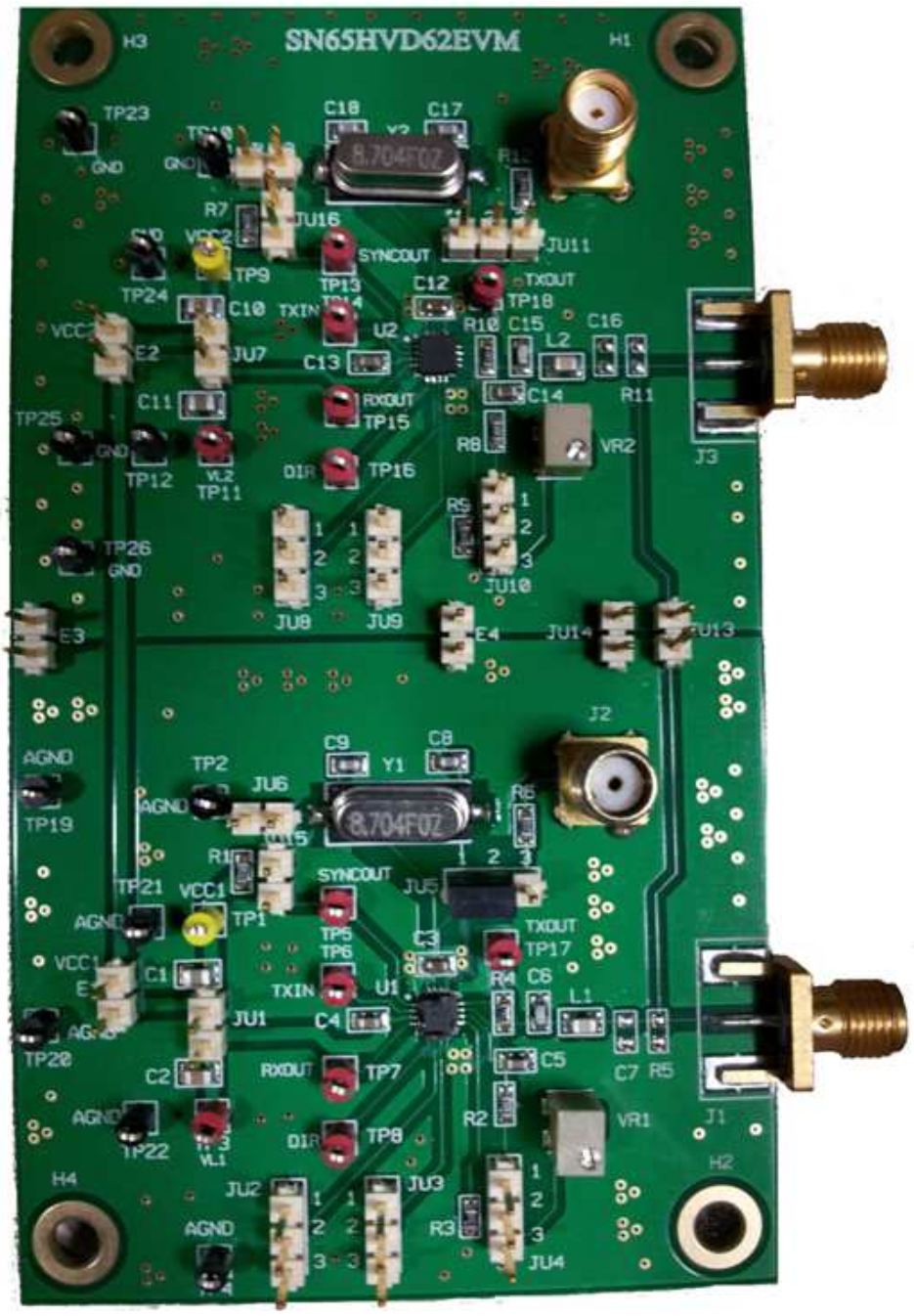


Figure 2. SN65HVD62 EVM

The two edge mounted SMA connectors, J1 and J3, are the coax interface to the SN65HVD62 devices, U1 and U2 respectively. The two devices have their own independent ground planes which may be shorted together using jumpers E3, E4, and JU14 to provide a common ground plane for the entire EVM.

Jumper JU13 can be shorted to provide a communication path between the two SN65HVD62 devices at the coax interface without requiring an external cable.

2.1 EVM Schematic

A schematic diagram for the SN65HVD62 EVM is presented in Figure 3.

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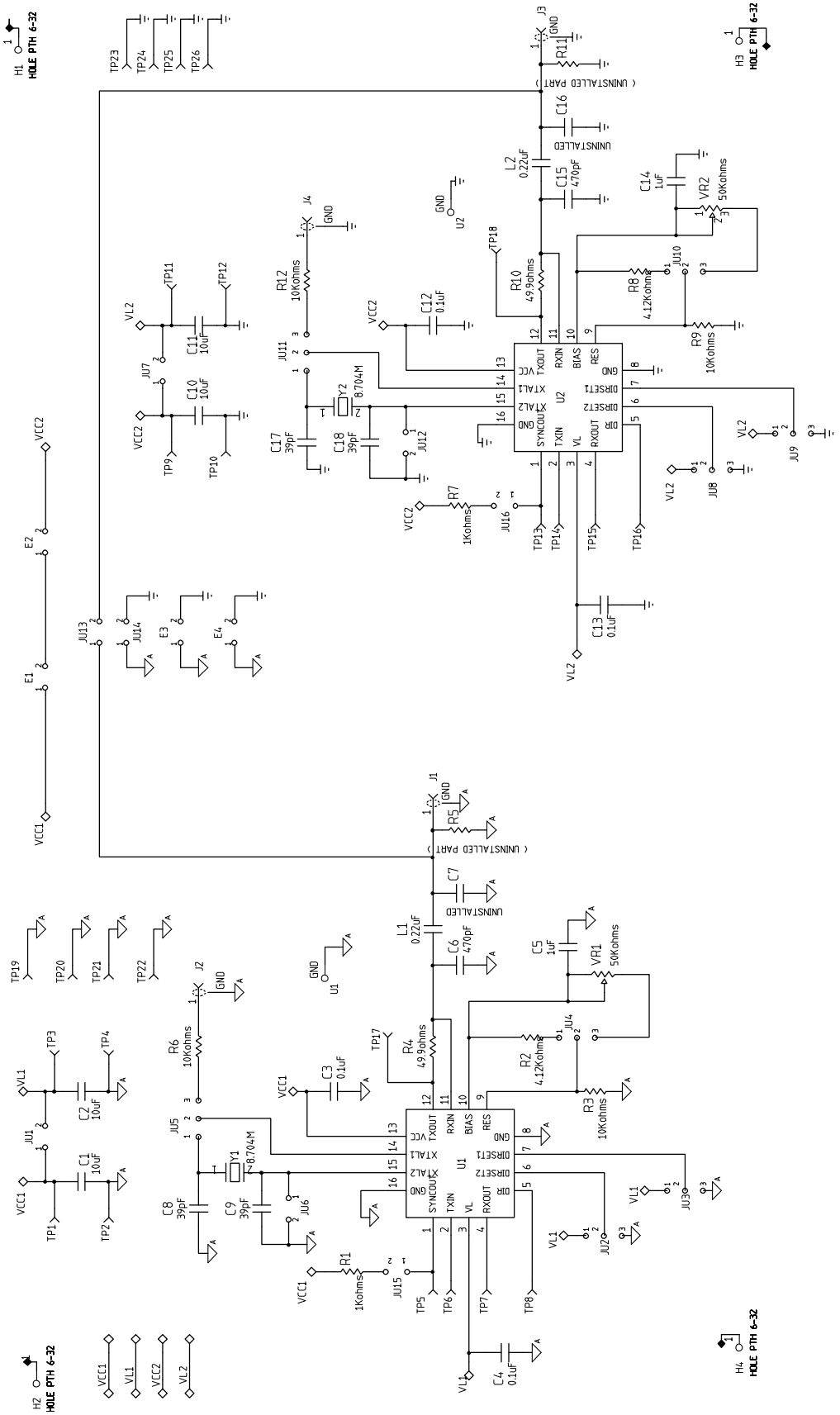


Figure 3. SN65HVD62EVM Schematics

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The various EVM components and their functions are described in Table 1.

Table 1. SN65HVD62EVM Description

Label	Description
U1, U2	SN65HVD62 AISG Device
TP5, TP13	Test point to access SYNCOUT pin of U1 and U2, respectively
JU15, JU16	Jumpers to pull-up SYNCOUT to VCC for U1, U2 respectively. **Default: these jumpers are shorted.**
R1, R7	1kΩ pull-up on SYNCOUT pin for U1, U2 respectively
TP6, TP14	Test point to access TXIN pin of U1, U2 respectively
TP7, TP15	Test point to access RXOUT pin of U1, U2 respectively
TP8, TP16	Test point to access DIR pin of U1, U2 respectively
JU2, JU8	Jumper provision for connecting DIRSET2 pin to either VL or GND for U1, U2 respectively. **By default, pins 1 and 2 of these jumpers are shorted. See Table 4 for data rate control settings.**
JU3, JU9	Jumper provision for connecting DIRSET1 pin to either VL or GND for U1, U2 respectively. **By default, pins 2 and 3 of these jumpers are shorted. See Table 4 for data rate control settings.**
R3, R9	10kΩ resistor to ground from RES pin of U1, U2 respectively
JU4, JU10	Jumper option for selecting between a fixed 4.1kΩ - 10kΩ voltage divider from BIAS pin to RES pin or a variable potentiometer to 10kΩ voltage divider between these two pins for U1, U2 respectively. **By default, pins 1 and 2 of these jumpers are shorted** to provide a fixed 4.1kΩ -10kΩ voltage divider output to RES pin, that is, 1.064V.
VR1, VR2	Potentiometer to provide variable voltage to RES pin if JU4, JU10 pins 2 and 3 are shorted for U1, U2 respectively
C5, C14	1µF capacitor to ground for BIAS pin of U1, U2 respectively
R4, R10	50Ω resistor between TXOUT and RXIN pins of U1, U2 respectively
C6, C15	470pF filter capacitor to ground at TXOUT of U1, U2 respectively
L1, L2	220nF AC coupling cap between RXIN and coax for U1, U2 respectively
C7, R5, C16, R11	Uninstalled components
TP17, TP18	Test point to access TXOUT pin of U1, U2 respectively
JU5, JU11	Jumper option to provide crystal clock or external clock on XTAL1 pin for U1, U2 respectively. **By default, short pins 1 and 2 of these jumpers** to provide clock from the on-board crystal.
J2, J4	SMA connectors using which external clock can be applied on XTAL1 pins of U1, U2 respectively if pins 2 and 3 of jumpers JU5 and JU11 are shorted
R6, R12	Series 10kΩ resistor through which external clock will be applied on XTAL1 pins for U1, U2 respectively
Y1, Y2	On board crystal clock source for U1, U2 respectively
C8, C17	39pF capacitor to ground from on-board crystal pin connected to XTAL1 of U1, U2 respectively
C9, C18	39pF capacitor to ground from on-board crystal pin connected to XTAL2 of U1, U2 respectively
JU6, JU12	Jumper option to connect XTAL2 pin to ground for U1, U2 respectively. By default, when using on-board crystal clock source, these jumpers are open. If external clock source is used through J2, J4, then these jumpers must be shorted.
TP1, TP9	Test point to access VCC pin of U1, U2 respectively
TP3, TP11	Test point to access VL pin of U1, U2 respectively
JU1, JU7	Jumper option to short VCC and VL supplies for U1, U2 respectively. **By default, jumpers are shorted** to allow use of a single supply source per device.
C3, C12	0.1uF decoupling capacitor on VCC pin of U1, U2 respectively
C4, C13	0.1uF decoupling capacitor on VL pin of U1, U2 respectively
C1, C10	10uF decoupling capacitor on VCC supply of U1, U2 respectively
C2, C11	10uF decoupling capacitor on VL supply of U1, U2 respectively
JU13	Jumper option to connect coax interface of U1 and U2. **By default, this jumper is shorted** to allow the system evaluation of two devices without the need for an external cable.
TP2, TP4, TP19, TP20, TP21, TP22	Test points to access GND pins of U1
TP10, TP12, TP23, TP24, TP25, TP26	Test points to access GND pins of U2
E1, E2	Jumper option to short VCC supply of U1 to VCC supply of U2. Both jumpers should be shorted to exercise this option. **By default, these jumpers are shorted.**
E3, E4, JU14	Jumper option to short GND planes of devices U1 and U2. **By default, these jumpers are shorted.**

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2.2 EVM Configuration: Jumpers and Test Points

Table 2 summarizes the jumper settings. An asterisk (*) indicates the default setting of the jumpers.

Table 2. Jumper Settings Description

Jumper	Shunt Position	Description
Jumper settings for U1		
JU1	Short*	U1 VL pin connected to U1 VCC pin (single supply)
	Open	U1 VLpin disconnected from U1 VCC pin
JU2	1-2*	Direction Control Settings for U1. Default setting is for 115.2kbps data rate. See Table 4
	2-3	
JU3	1-2	
	2-3*	
JU4	1-2*	U1 output level at TXOUT is set at +3dBm
	2-3	U1 output level at TXOUT is adjustable by VR1
JU5	1-2*	U1 uses on-board crystal
	2-3	U1 uses external clock applied on SMA J2
JU6	Open*	U1 uses on-board crystal
	Short	U1 uses external clock applied on SMA J2
JU15	Short*	U1 SYNCOUT pulled up to VCC through a 1kΩ resistor
	Open	U1 SYNCOUT not pulled up to VCC
Jumper settings for U2		
JU7	Short*	U2 VL pin connected to U2 VCC pin
	Open	U2 VL pin disconnected from U2 VCC pin
JU8	1-2*	Direction Control Settings for U1. Default setting is for 115.2kbps data rate. See Table 4
	2-3	
JU9	1-2	
	2-3*	
JU10	1-2*	U2 output level at TXOUT is set at +3dBm
	2-3	U2 output level at TXOUT is adjustable by VR2
JU11	1-2*	U2 uses on-board crystal
	2-3	U2 uses external clock applied on SMA J4
JU12	Open*	U2 uses on-board crystal
	Short	U2 uses external clock applied on SMA J4
JU16	Short*	U2 SYNCOUT pulled up to VCC through a 1kΩ resistor
	Open	U2 SYNCOUT not pulled up to VCC
Jumper settings for U1 to U2 connections		
JU13	Short*	SMA J1 and J3 signals connected by a PCB trace (loopback)
	Open	SMA J1 and J3 signals not connected (requires external cable)
JU14, E3, E4	Short*	U1 and U2 grounds connected
	Open	U1 and U2 grounds disconnected
E1, E2	Short*	U1 VCC connected to U2 VCC
	Open	U1 VCC not connected to U2 VCC
* indicates the default jumper configuration		

Table 3 summarizes the list of test points available on the EVM and their functionality.

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Table 3. Test Point Description

Test Point	Description
TP1	VCC1, Supply for U1
TP2	AGND, Ground plane for U1
TP3	VL1, Logic supply for U1
TP4	AGND – Analog GND
TP5	SYNCOUT1, Syncout for U1
TP6	TXIN1, Transmitter input for U1
TP7	RXOUT1, Receiver output for U1
TP8	DIR1, Direction output for U1
TP9	VCC2, Supply for U2
TP10	GND, Ground plane for U2
TP11	VL2, Logic supply for U2
TP12	GND
TP13	SYNCOUT2, Syncout output for U2
TP14	TXIN2, Transmitter input for U2
TP15	RXOUT2, Receiver output for U2
TP16	DIR2, Direction output for U2
TP17	TXOUT1, Transmitter output for U1
TP18	TXOUT2, Transmitter output for U2
TP19	AGND
TP20	AGND
TP21	AGND
TP22	AGND
TP23	GND
TP24	GND
TP25	GND
TP26	GND

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3 EVM Setup and Operation

This section describes the EVM configuration(s) required to set-up the EVM for device evaluation. The EVM can be configured to evaluate one SN65HVD62 device individually or evaluate two of devices simultaneously, one device acting as the transmitter and the other as the receiver. Table 4 describes the jumper settings required for setting up U1 and U2 for various data rates during this evaluation.

Table 4. Data Rate Settings

Data Rate	DIRSET2 Logic Level	DIRSET1 Logic Level	U1 Jumper setting		U2 Jumper setting	
			JU2 for DIRSET2	JU3 for DIRSET1	JU8 for DIRSET2	JU9 for DIRSET1
9.6kbps	0	0	Short pins 2-3	Short pins 2-3	Short pins 2- 3	Short pins 2-3
38.4kbps	0	1	Short pins 2-3	Short pins 1-2	Short pins 2-3	Short pins 1-2
115.2kbps	1	0	Short pins 1-2	Short pins 2-3	Short pins 1-2	Short pins 2-3
Standby Mode (Receive only)	1	1	Short pins 1-2	Short pins 1-2	Short pins 1-2	Short pins 1-2

If these jumpers are left OPEN, then the internal pull-down on the DIRSET1 and DIRSET2 pins of the device will set the open pins to logic ‘0’ level.

3.1 Equipment

The following equipment is required to perform the evaluation described in this section:

1. SN65HVD62EVM
2. Arbitrary Function Generator
3. DC Power Supply
4. Four channel Oscilloscope

3.2 Standalone Evaluation

This section covers the board configuration required to evaluate either U1 or U2 individually for either Transmit or Receive channel parameters.

To set-up the board for standalone evaluation, refer to Table 2 for the default settings of the jumpers.

NOTE: OPEN JU13 FOR STANDALONE EVALUATION.

Table 1 indicates how each of the device pins may be accessed depending on whether U1 or U2 is selected for evaluation. The remaining section describe the connections to required for evaluation of U1. See Table 1 for the corresponding component connections necessary for the standalone alone evaluation of U2.

3.2.1 Tx Channel Evaluation

This section describes the evaluation of the transmit channel of the SN65HVD62 transceiver. Adjusting the transmit output power using different voltage settings at the RES pin is also explained.

1. From the default jumper positions as described in Table 2, open Jumper JU13 for standalone evaluation of either U1 or U2.
2. Set the DC power supply to source 5V with 80mA current limit and connect it between TP1 (U1_VCC) and TP2 (GND).
3. Since JU1 is shorted by default, this means that VL supply will also get 5V. In case a different supply is required for VL, open JU1 and connect the second supply between TP3 (U1_VL) and TP4 (GND).
4. See Table 4 for data-rate settings. The board is configured by default for 115.2kbps data rate.
5. Set the waveform generator to output a square wave. Set the high and low levels to 5V (= V_L) and 0V respectively into a high-impedance load, frequency to half of the data-rate setting and duty cycle to 50%.

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6. Connect the waveform-generator output between TP6 (TXIN) and TP2 (GND).
7. Connect the oscilloscope channel 1 to TP6 (TXIN).
8. Connect the oscilloscope channel 2 to TP17 (TXOUT).
9. Connect the oscilloscope channel 3 to JU4, pin2 (RES).
10. Example waveforms for a 115.2kbps setting are shown in Figure 4.

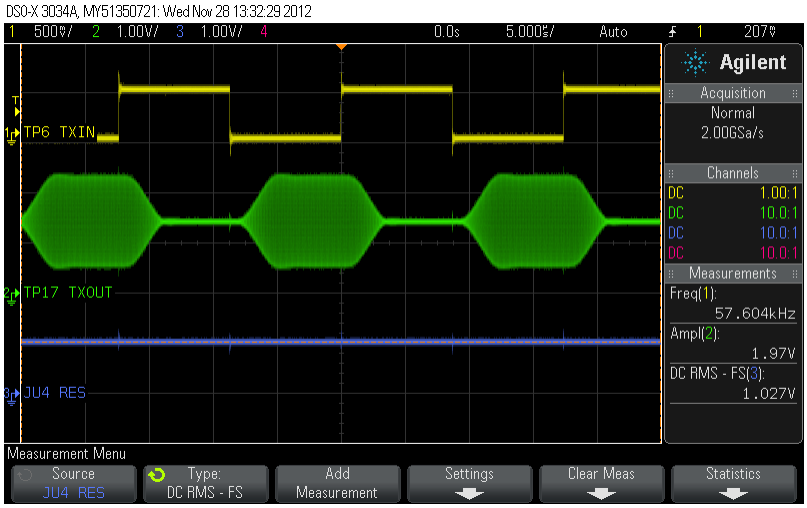


Figure 4. Time Domain Waveforms for 115.2kbps Transmission

11. Now look at the output spectrum of the transmitter by connecting a spectrum analyzer to J1. Example output spectrum up to 30MHz for 115.2kbps setting is shown in Figure 5.

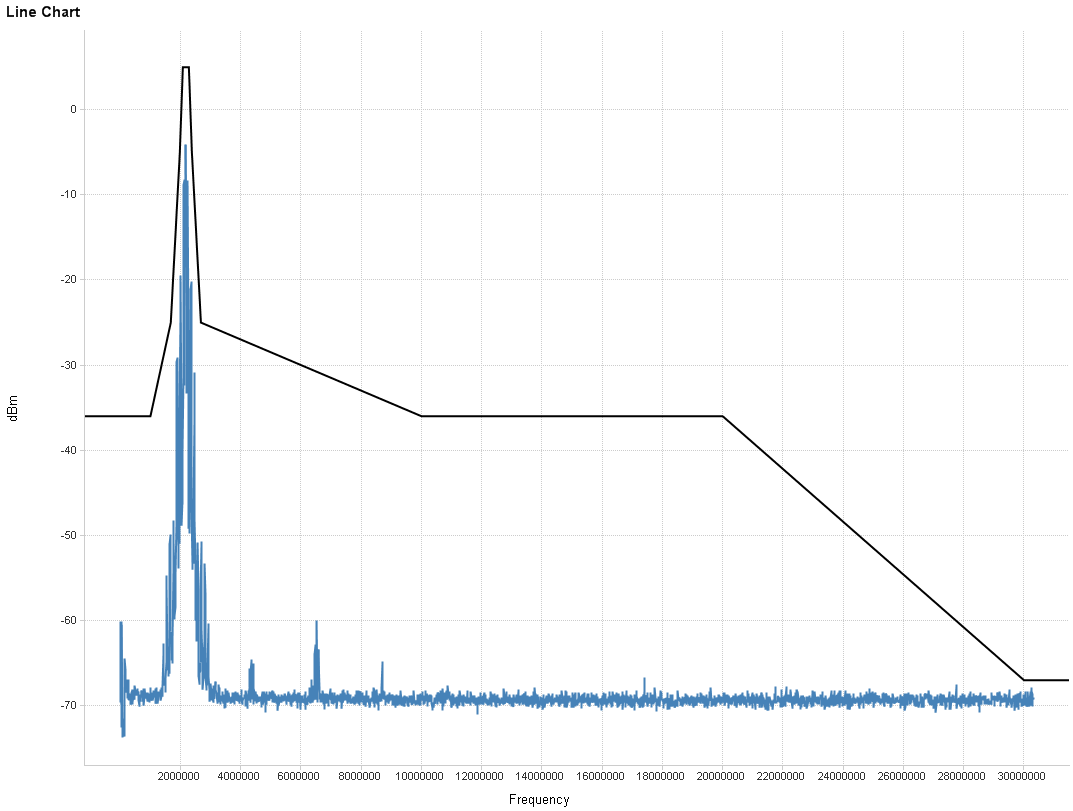


Figure 5. Emission Spectrum for 115.2kbps Transmission: up to 30MHz

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12. A spectrum for higher frequency ranges can be checked. If the signal is captured then the dynamic range of the spectrum analyzer will limit the noise floor performance. To improve the measurement a high pass filter has been used to remove the signal content while leaving the emissions content unaffected in the emission spectrum plot from 30MHz to 400MHz shown in Figure 6.

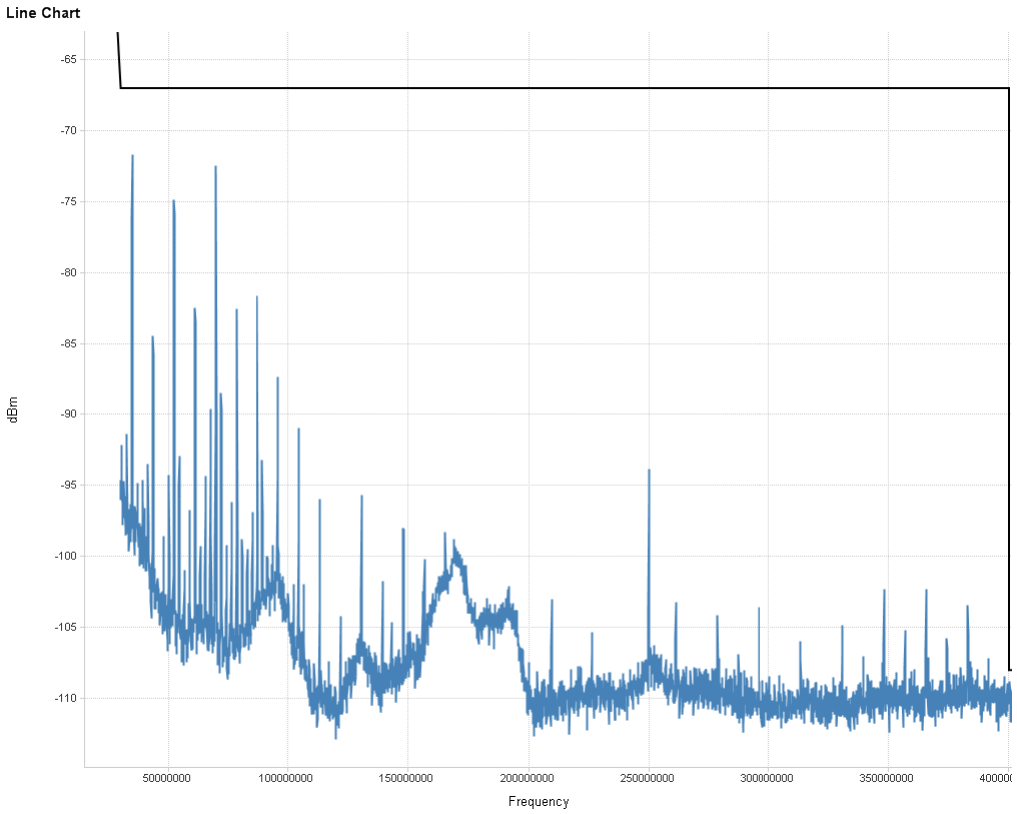


Figure 6. Emission Spectrum for 115.2kbps Transmission: 30MHz to 400MHz

13. To evaluate the effect of the voltage on the RES pin on the Tx output power, change the jumper JU4 default setting and short pins 2 and 3.
14. Change the VR1 setting to apply between 0.7V and 1.5V on the RES pin and observe the oscilloscope and spectrum analyzer plots.

3.2.2 Rx Channel Evaluation

1. From the default jumper positions as described in Table 2, open Jumper JU13 for standalone evaluation of either U1 or U2.
2. Set the DC power supply to source 5V with 80mA current limit and connect it between TP1 (U1_VCC) and TP2 (GND).
3. Since JU1 is shorted by default, this means that VL supply will also get 5V. If a different supply is required for V_L, open JU1 and connect the second supply between TP3 (U1_VL) and TP4 (GND).
4. Leave TP6 (TXIN) floating or short it to TP3 (VL).
5. Set the waveform generator to output a 160mV p-p sine wave into a 50-Ω load with common mode of 1.5V.
6. Connect the waveform generator to J1.
7. Connect the oscilloscope channel 1 to JU13 pin on U1 side (RXIN).
8. Connect the oscilloscope channel 2 to TP7 (RXOUT).
9. Connect the oscilloscope channel 3 to TP8 (DIR).
10. Example waveforms with a 160mVpp sine wave input at J1 are shown in Figure 7. RXOUT is low and DIR is high indicating that the device is in Receive mode.

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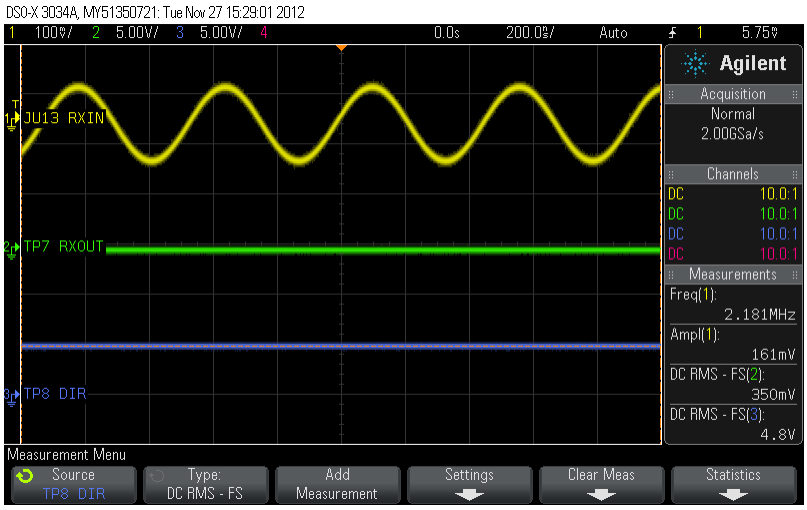


Figure 7. Rx Channel Evaluation: 160mVpp input at RXIN

11. Change the input amplitude to 80mVpp.
12. Example waveforms with an 80mVpp sine wave input at J1 are shown in Figure 8. RXOUT is high and DIR is low indicating the device is not in Receive mode.

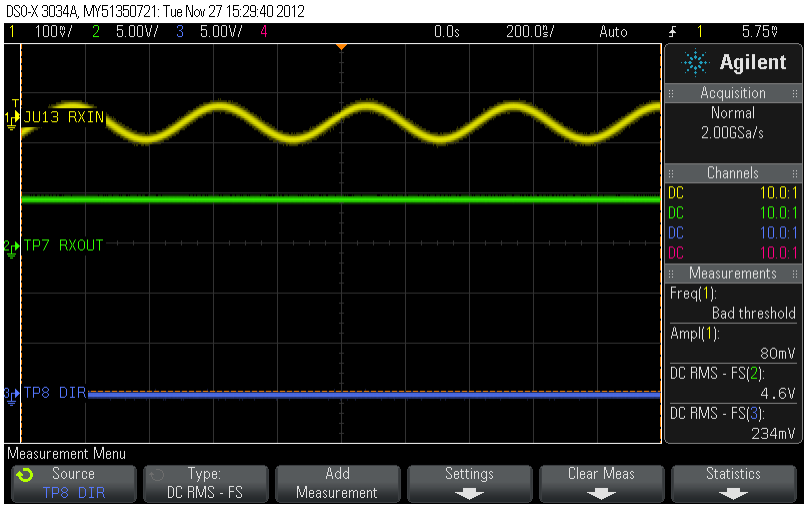


Figure 8. Rx Channel Evaluation: 80mVpp input at RXIN

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3.3 System Evaluation

This section covers the board configuration required to evaluate U1 and U2 in communication with one another. Figure 9 illustrates the device configuration in this mode.

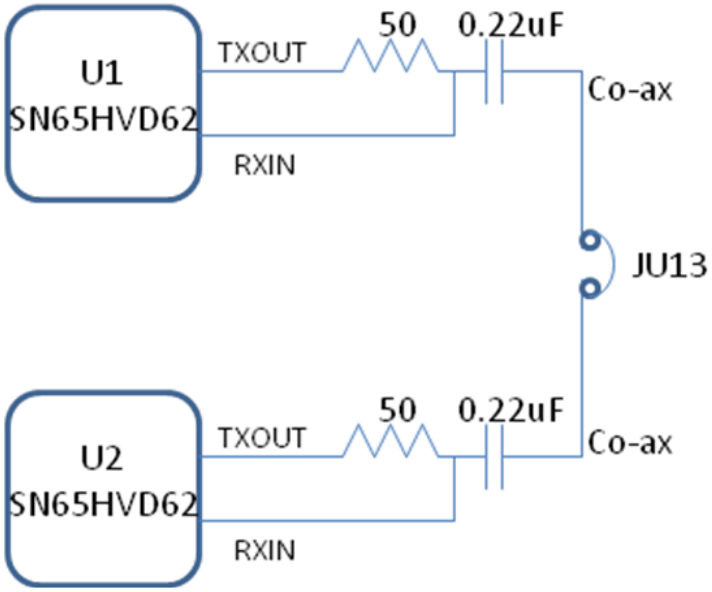


Figure 9. EVM System Evaluation Block Diagram

1. Retain the default jumper settings as described in Table 2.
2. Set the DC power supply to source 5V with 80mA current limit and connect it between TP1 (U1_VCC) and TP2 (GND).
3. Since jumpers E1 and E2 are shorted by default, both U1 and U2 will get powered up.
4. Since jumpers JU14, E3 and E4 are shorted by default, the board has a common ground plane.
5. Since JU1 and JU7 are shorted by default, this means that V_L supplies will also get 5V. If different supply is required for V_L, open JU1 and connect the second supply between TP3 (U1_VL) and TP4 (GND) and also between TP11 (U2_VL) and TP12 (GND).
6. Jumpers JU2 and JU3 for U1 and jumpers JU8 and JU9 for U2 are by default set to 115.2kbps data rate settings (see Table 4).
7. Set the waveform generator to output a square wave. Set the high and low levels to 5V (= V_L) and 0V respectively into a high-impedance load, with frequency 6.4kHz and duty-cycle 94.44%. This corresponds to 1-bit on period and 17-bit off period for a 115.2kbps data-rate.
8. To use U1 and transmitter and U2 as receiver, leave TP14 (U2 TXIN) floating connect the waveform-generator output between TP6 (U1 TXIN) and TP2 (GND).
9. Since JU13 is shorted by default, the TXOUT from U1 is received by the RXIN of U2.
10. Connect the oscilloscope channel 1 to TP6 (U1 TXIN).
11. Connect the oscilloscope channel 2 to TP5 (U1 SYNCOUT).
12. Connect the oscilloscope channel 3 to TP15 (U2 RXOUT).
13. Connect the oscilloscope channel 4 to TP16 (U2 DIR).
14. Example waveforms for U1 acting as transmitter and U2 acting as receiver at 115.2kbps data transmission rate are shown in Figure 10.

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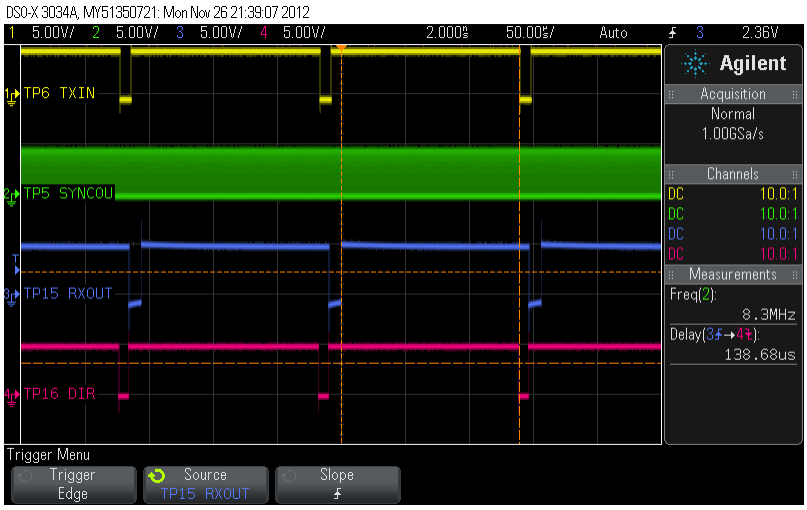


Figure 10. System Evaluation with U1 as Transmitter and U2 as Receiver at 115.2kbps

3.4 External Clock Input

The default setting for the clock source at the XTAL1 pin of U1 and U2 is the on-board crystal, Y1 and Y2 respectively. The SN65HVD62EVM also provides an option to use an external clock source on the XTAL1 pin. The following steps must be followed to enable this option for U1. Corresponding jumpers need to be used to enable this option for U2.

1. Short pins 2 and 3 of jumper JU5.
2. Short jumper JU6 to connect the XTAL2 pin to GND.
3. Apply an external clock source of 8.704MHz at the SMA connector J2.

3.5 Standby Mode

Table 4 describes settings for putting the device into “stand-by” mode by making DIRSET1 = DIRSET2 = 1.

In this mode, the Transmit channel of the device is disabled and it acts as a pure receiver. With the device in stand-by mode, the current consumption is significantly reduced. If a logic low is applied at the TXIN pin of the device in this mode, the device will not transmit since the transmit channel is disabled.

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4 Bill Of Materials (BOM)

Table 5 shows the parts list for the SN65HVD62EVM.

Table 5. SN65HVD62EVM Bill Of Materials

ITEM	QTY	REFERENCE DESIGNATOR	PART DESCRIPTION	MFG
1	4	C1,C2,C10,C11	CAPACITOR,SMT,0805,CERAMIC,10uF,10V,10%,X5R,LOW ESR	TAIYO YUDEN/ANY
2	4	C3,C4,C12,C13	CAPACITOR,SMT,0603,CERAMIC,0.1uF,16V,10%,X7R	AVX/ANY
3	2	C5,C14	CAPACITOR,SMT,0603,CERAMIC,1.0uF,16V,10%,X7R	TDK/ANY
4	2	C6,C15	CAPACITOR,SMT,0603,CERAMIC,470pF,50V,5%,C0G(NP0)	AVX/ANY
5	2	C7,C16	CAPACITOR,SMT,0603,CERAMIC,UNINSTALLED	UNINSTALLED
6	4	C8,C9,C17,C18	CAPACITOR,SMT,0603,CERAMIC,39pF,50V,5%,C0G(NP0)	AVX/ANY
7	12	E1,E2,E3,E4,JU1,JU6,JU7,JU12,JU13,JU14,JU15,JU16	2-PIN JUMPER	ANY
8	2	U1,U2	AISG Modem	TEXAS INSTRUMENTS
9	8	JU2,JU3,JU4,JU5,JU8,JU9,JU10,JU11	3-PIN JUMPER	ANY
10	2	J1,J3	SMA JACK RECEPTACLE, END LAUNCH	JOHNSON part # 142-0701-801
11	2	J2,J4	SMA, FEM, VERT, THREAD	AMPHENOL part # 901-144-8RFX
12	2	L1,L2	CAPACITOR,SMT,0805,CERAMIC,0.22uF,25V,5%,X7R	AVX/ANY
13	2	R1,R7	RESISTOR,SMT,0603,1%,1/10W,1.00K	VISHAY/ANY
14	2	R2,R8	RESISTOR,SMT,0603,1%,1/10W,4.12K	VISHAY/ANY
15	2	R3,R9	RESISTOR,SMT,0603,THICK FILM,10K,1%,1/10W	YAGEO/ANY
16	2	R4,R10	RESISTOR,SMT,0603,1%,1/10W,49.9	PANASONIC/ANY
17	2	R5,R11	RESISTOR,SMT,0603,UNINSTALLED	UNINSTALLED
18	2	R6,R12	RESISTOR,SMT,0603,5%,1/10W,10K	PANASONIC/ANY
19	2	TP1,TP9	TEST POINTS,THU,SMALL,TL-70,YELLOW	COMPONENTS CORP part # TP105-01-04
20	12	TP2,TP4,TP10,TP12,TP19,TP20,TP21,TP22,TP23,TP24,TP25,TP26	TEST POINTS,THU,SMALL,TL-70,BLACK	COMPONENTS CORP part # TP105-01-00
21	12	TP3,TP5,TP6,TP7,TP8,TP11,TP13,TP14,TP15,TP16,TP17,TP18	TEST POINTS,THU,SMALL,TL-70,RED	COMPONENTS CORP part # TP105-01-02
22	2	VR1,VR2	TRIMPOT,50K,10%,11T,100ppm,200CY,SEALED	BOURNS part # 3224W-1-503
23	2	Y1,Y2	1500 PIECE MIN 5 WEEK LEAD	HONGKONG CRYSTALS part # SSL8704018AEHFF0
24	4		BUMPON HEMISPHERE .44X.20 CLEAR	3M part # SJ5303
25	20		SHUNT LP W/HANDLE 2 POS 30AU	Tyco/ANY
Assembly Instructions:				
1.	Short the following jumpers using the 881545-2 shunts: JU1, JU7, JU15, JU16, JU13, JU14, E1, E2, E3, E4			
2.	Short positions 1 and 2 of the following 3-pin jumpers using the 881545-2 shunts: JU2, JU8, JU4, JU10, JU5, JU11			
3.	Short positions 2 and 3 of the following 3-pin jumpers using the 881545-2 shunts: JU3, JU9			
4.	Install the SJ5303 bumpon hemisphere at the 4 corners of the board on the bottom side.			

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5 SN65HVD62EVM Layout

Figure 11 shows the top layer routing of the SN65HVD62EVM.

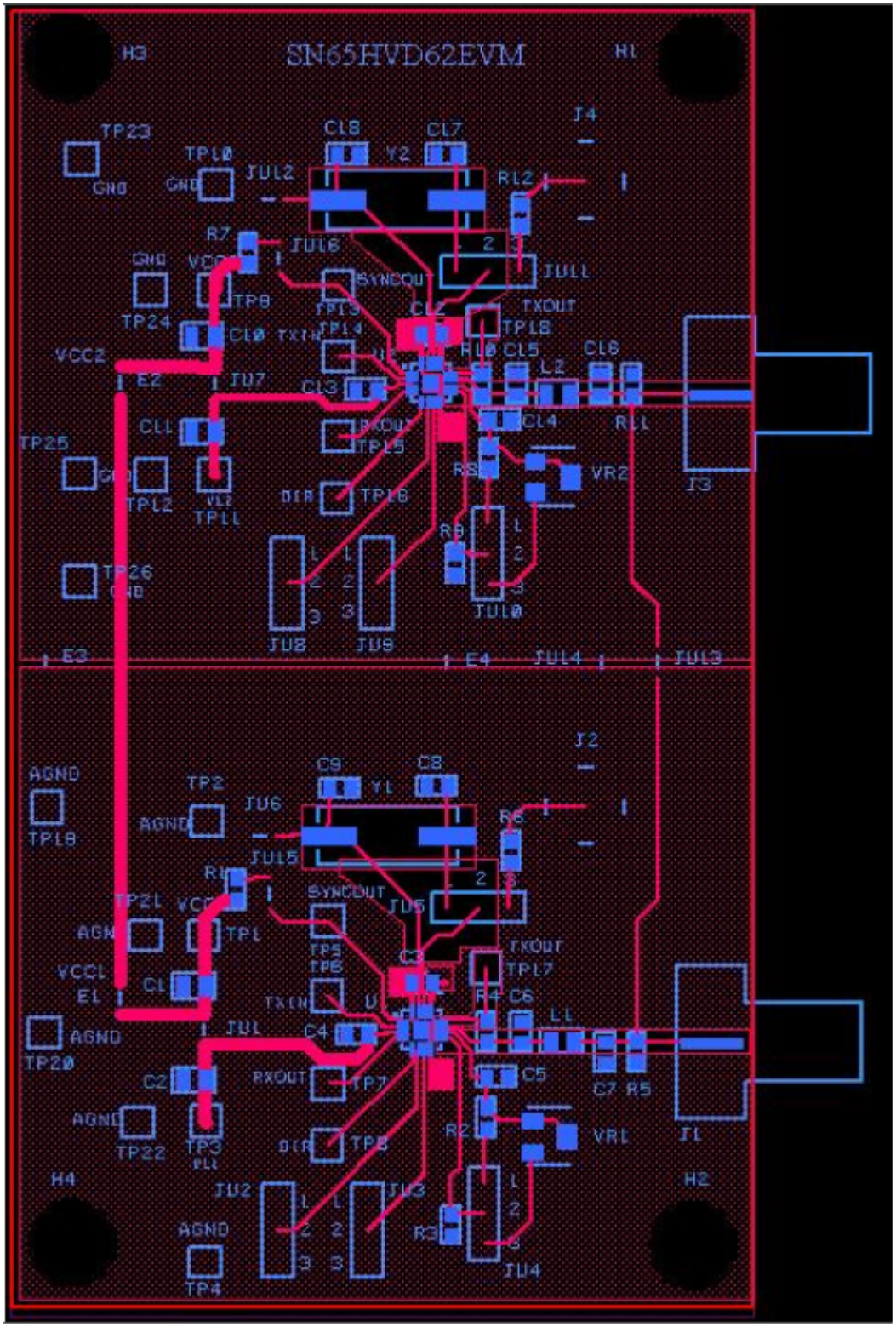


Figure 11. SN65HVD62EVM Top Layer Routing

Figure 12 shows the bottom layer routing and ground planes.

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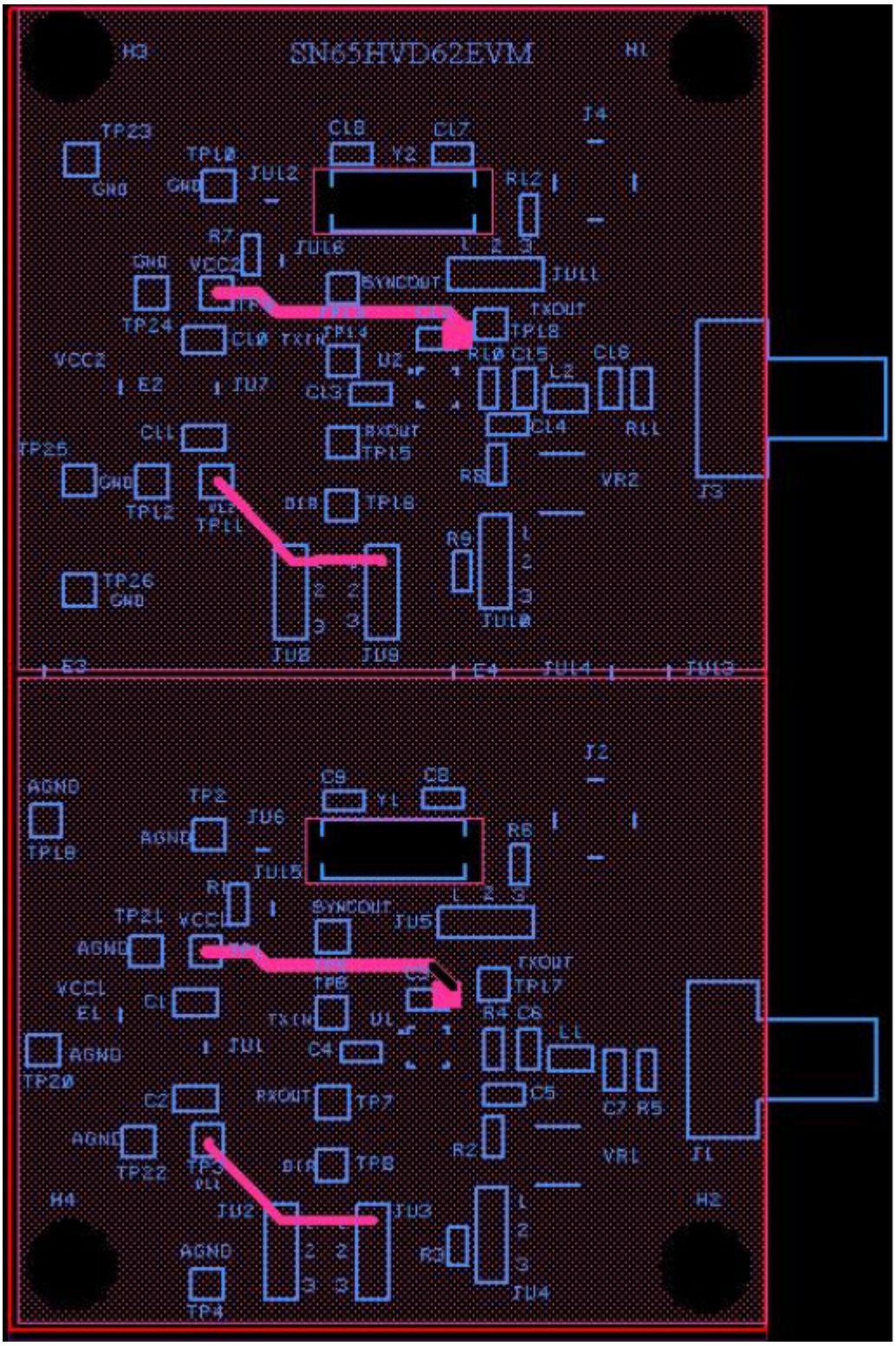


Figure 12. SN65HVD62EVM Bottom Layer Routing

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As noted in the EVM User's Guide and/or EVM itself, this EVM and/or accompanying hardware may or may not be subject to the Federal Communications Commission (FCC) and Industry Canada (IC) rules.

For EVMs **not** subject to the above rules, this evaluation board/kit/module is intended for use for ENGINEERING DEVELOPMENT, DEMONSTRATION OR EVALUATION PURPOSES ONLY and is not considered by TI to be a finished end product fit for general consumer use. It generates, uses, and can radiate radio frequency energy and has not been tested for compliance with the limits of computing devices pursuant to part 15 of FCC or ICES-003 rules, which are designed to provide reasonable protection against radio frequency interference. Operation of the equipment may cause interference with radio communications, in which case the user at his own expense will be required to take whatever measures may be required to correct this interference.

General Statement for EVMs including a radio

User Power/Frequency Use Obligations: This radio is intended for development/professional use only in legally allocated frequency and power limits. Any use of radio frequencies and/or power availability of this EVM and its development application(s) must comply with local laws governing radio spectrum allocation and power limits for this evaluation module. It is the user's sole responsibility to only operate this radio in legally acceptable frequency space and within legally mandated power limitations. Any exceptions to this are strictly prohibited and unauthorized by Texas Instruments unless user has obtained appropriate experimental/development licenses from local regulatory authorities, which is responsibility of user including its acceptable authorization.

For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant

Caution

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

FCC Interference Statement for Class A EVM devices

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC Interference Statement for Class B EVM devices

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

For EVMs annotated as IC – INDUSTRY CANADA Compliant

This Class A or B digital apparatus complies with Canadian ICES-003.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

Concerning EVMs including radio transmitters

This device complies with Industry Canada licence-exempt RSS standard(s). Operation is subject to the following two conditions: (1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concerning EVMs including detachable antennas

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication.

This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Cet appareil numérique de la classe A ou B est conforme à la norme NMB-003 du Canada.

Les changements ou les modifications pas expressément approuvés par la partie responsable de la conformité ont pu vider l'autorité de l'utilisateur pour actionner l'équipement.

Concernant les EVMs avec appareils radio

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes : (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante.

Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur.

【Important Notice for Users of this Product in Japan】

This development kit is NOT certified as Confirming to Technical Regulations of Radio Law of Japan

If you use this product in Japan, you are required by Radio Law of Japan to follow the instructions below with respect to this product:

1. Use this product in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use this product only after you obtained the license of Test Radio Station as provided in Radio Law of Japan with respect to this product, or
3. Use of this product only after you obtained the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to this product. Also, please do not transfer this product, unless you give the same notice above to the transferee. Please note that if you could not follow the instructions above, you will be subject to penalties of Radio Law of Japan.

Texas Instruments Japan Limited
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Your Sole Responsibility and Risk. You acknowledge, represent and agree that:

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Certain Instructions. It is important to operate this EVM within TI's recommended specifications and environmental considerations per the user guidelines. Exceeding the specified EVM ratings (including but not limited to input and output voltage, current, power, and environmental ranges) may cause property damage, personal injury or death. If there are questions concerning these ratings please contact a TI field representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may result in unintended and/or inaccurate operation and/or possible permanent damage to the EVM and/or interface electronics. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative. During normal operation, some circuit components may have case temperatures greater than 60°C as long as the input and output are maintained at a normal ambient operating temperature. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors which can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during normal operation, please be aware that these devices may be very warm to the touch. As with all electronic evaluation tools, only qualified personnel knowledgeable in electronic measurement and diagnostics normally found in development environments should use these EVMs.

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