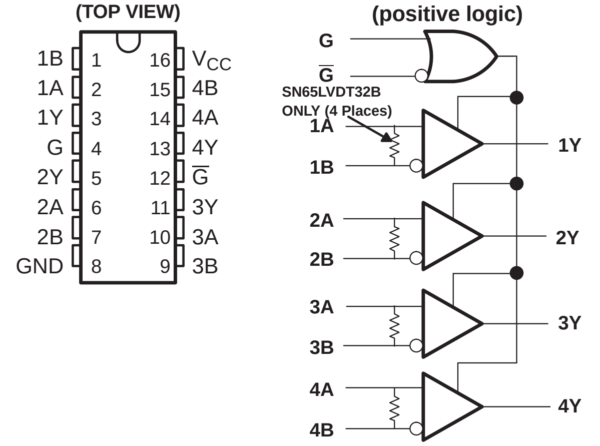
HIGH-SPEED DIFFERENTIAL RECEIVERS

FEATURES

- **Meets or Exceeds the Requirements of ANSI EIA/TIA-644 Standard for Signaling Rates (1) up to 400 Mbps**
- **Operates With a Single 3.3-V Supply**
- **–2-V to 4.4-V Common-Mode Input Voltage Range**
- **Differential Input Thresholds <50 mV With 50 mV of Hysteresis Over Entire Common-Mode Input Voltage Range**
- **Integrated 110-Ω Line Termination Resistors Offered With the LVDT Series**
- **Propagation Delay Times 4 ns (typ)**
- **Active Fail Safe Assures a High-Level Output With No Input**
- **Bus-Pin ESD Protection Exceeds 15 kV HBM**
- **Inputs Remain High-Impedance on Power Down**
- **Recommended Maximum Parallel Rate of 200 M-Transfer/s**
- **Available in Small-Outline Package With 1,27-mm Terminal Pitch**
- **Pin-Compatible With the AM26LS32, MC3486, or µA9637**

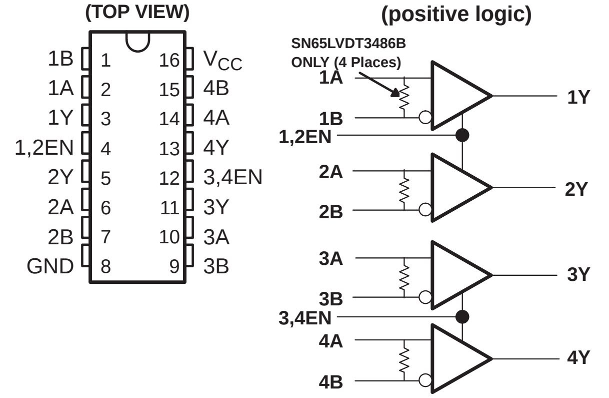
SN65LVDS32B
SN65LVDT32B

D PACKAGE (TOP VIEW) **Logic Diagram (positive logic)**



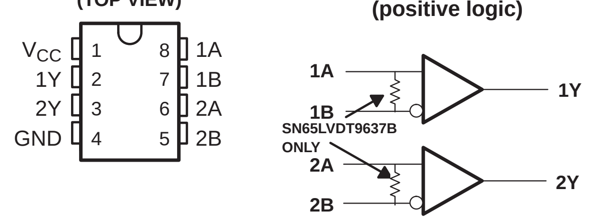
SN65LVDS3486B
SN65LVDT3486B

D PACKAGE (TOP VIEW) **Logic Diagram (positive logic)**



SN65LVDS9637B
SN65LVDT9637B

D PACKAGE (TOP VIEW) **Logic Diagram (positive logic)**



DESCRIPTION

This family of differential line receivers offers improved performance and features that implement the electrical characteristics of low-voltage differential signaling (LVDS). LVDS is defined in the TIA/EIA-644 standard. This improved performance represents the second generation of receiver products for this standard, providing a better overall solution for the cabled environment. This generation of products is an extension to TI's overall product portfolio and is not necessarily a replacement for older LVDS receivers.

(1) Signaling rate, 1/t, where t is the minimum unit interval and is expressed in the units bit/s (bits per second).

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

DESCRIPTION (CONTINUED)

Improved features include an input common-mode voltage range 2 V wider than the minimum required by the standard. This will allow longer cable lengths by tripling the allowable ground noise tolerance to 3 V between a driver and receiver. TI has additionally introduced an even wider input common-mode voltage range of –4 to 5 V in their SN65LVDS/T33 and SN65LVDS/T34.

Precise control of the differential input voltage thresholds now allows for inclusion of 50 mV of input voltage hysteresis to improve noise rejection on slowly changing input signals. The input thresholds are still no more than ±50 mV over the full input common-mode voltage range.

The high-speed switching of LVDS signals almost always necessitates the use of a line impedance matching resistor at the receiving-end of the cable or transmission media. The SN65LVDT series of receivers eliminates this external resistor by integrating it with the receiver. The non-terminated SN65LVDS series is also available for multidrop or other termination circuits.

The receivers can withstand ±15-kV human-body model (HBM) and ±600 V-machine model (MM) electrostatic discharges to the receiver input pins with respect to ground without damage. This provides reliability in cabled and other connections where potentially damaging noise is always a threat.

The receivers also include a (patent pending) fail-safe circuit that will provide a high-level output within 600 ns after loss of the input signal. The most common causes of signal loss are disconnected cables, shorted lines, or powered-down transmitters. This prevents noise from being received as valid data under these fault conditions. This feature may also be used for wired-OR bus signaling.

The intended application of these devices and signaling technique is for point-to-point baseband data transmission over controlled impedance media of approximately 100 Ω. The transmission media may be printed-circuit board traces, backplanes, or cables. The ultimate rate and distance of data transfer is dependent upon the attenuation characteristics of the media and the noise coupling to the environment.

The SN65LVDS32B, SN65LVDT32B, SN65LVDS3486B, SN65LVDT3486B, SN65LVDS9637B, and SN65LVDT9637B are characterized for operation from –40°C to 85°C.

AVAILABLE OPTIONS

PART NUMBER(1)	NUMBER OF RECEIVERS	TERMINATION RESISTOR	SYMBOLIZATION
SN65LVDS32BD	4	No	LVDS32B
SN65LVDT32BD	4	Yes	LVDT32B
SN65LVDS3486BD	4	No	LVDS3486
SN65LVDT3486BD	4	Yes	LVDT3486
SN65LVDS9637BD	2	No	DK637B
SN65LVDT9637BD	2	Yes	DR637B

(1) Add the suffix R for taped and reeled carrier.

FUNCTION TABLES

SN65LVDS32B and SN65LVDT32B

DIFFERENTIAL INPUT	ENABLES(1)		OUTPUT(1)
A-B	G	$\overline{G}$	Y
V_{ID} ≥ –32 mV	H X	X L	H H
–100 mV < V_{ID} ≤ –32 mV	H X	X L	? ?
V_{ID} ≤ –100 mV	H X	X L	L L
X	L	H	Z
Open	H X	X L	H H

(1) H = high level, L = low level, X = irrelevant, Z = high impedance (off), ? = indeterminate

SN65LVDS3486B and SN65LVDT3486B

DIFFERENTIAL INPUT	ENABLES(1)	OUTPUT(1)
A-B	EN	Y
V_{ID} ≥ –32 mV	H	H
–100 mV < V_{ID} ≤ –32 mV	H	?
V_{ID} ≤ –100 mV	H	L
X	L	Z
Open	H	H

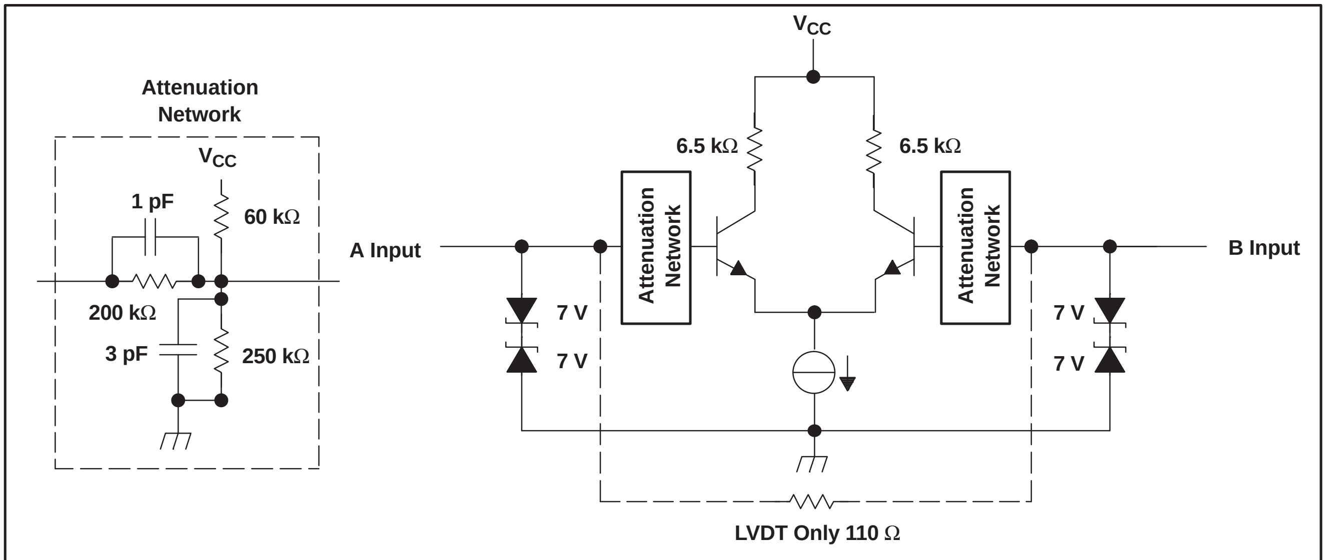
(1) H = high level, L = low level, X = irrelevant, Z = high impedance (off), ? = indeterminate

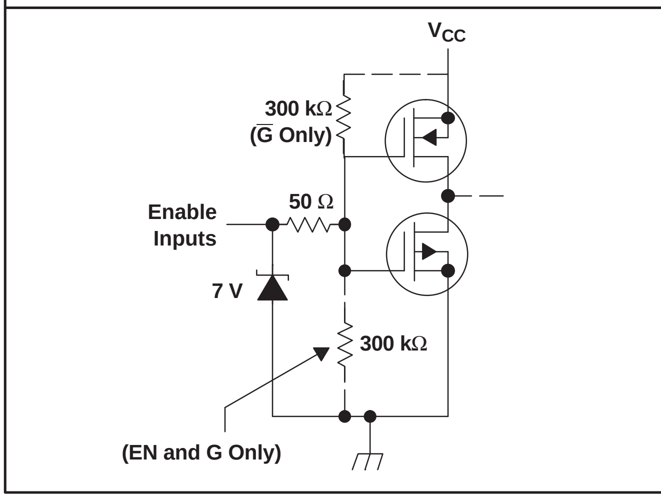
SN65LVDS9637B and SN65LVDT9637B

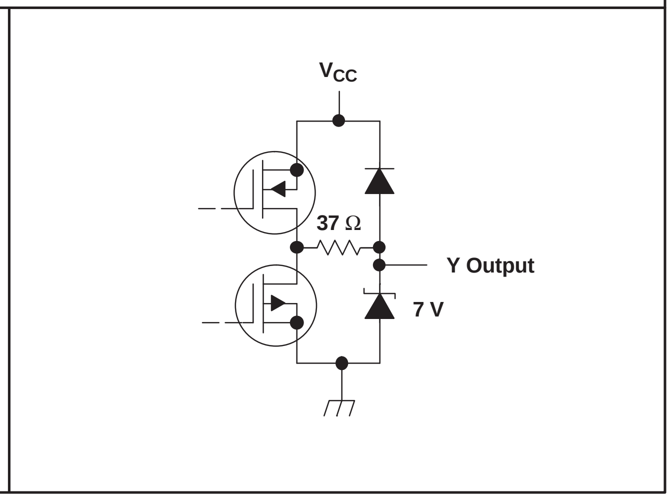
DIFFERENTIAL INPUT	OUTPUT(1)
A-B	Y
V_{ID}≥ -32 mV	H
–100 mV < V_{ID}≤ -32 mV	?
V_{ID}≤ -100 mV	L
Open	H

(1) H = high level, L = low level, ? = indeterminate

EQUIVALENT INPUT AND OUTPUT SCHEMATIC DIAGRAMS







ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)[(1)]

			UNIT
V_{CC}	Supply voltage range[(2)]		–0.5 V to 4 V
	Voltage range	Enables or Y	–0.5 V to V_{CC} + 3 V
		A or B	–4 V to 6 V
		$\|V_A – V_B\|$ (LVDT)	1 V
	Electrostatic discharge:	A, B, and GND[(3)]	Class 3, A: 15 kV, B: 600 V
	Continuous power dissipation		See Dissipation Rating Table
	Storage temperature range		–65°C to 150°C
	Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds		260°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.
(3) Tested in accordance with MIL-STD-883C Method 3015.7.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	OPERATING FACTOR[(1)] ABOVE $T_A = 25°C$	$T_A = 85°C$ POWER RATING
D8	725 mW	5.8 mW/°C	377 mW
D16	950 mW	7.6 mW/°C	494 mW

(1) This is the inverse of the junction-to-ambient thermal resistance when board-mounted and with no air flow.

RECOMMENDED OPERATING CONDITIONS

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		3	3.3	3.6	V
V_{IH}	High-level input voltage	Enables	2			V
V_{IL}	Low-level input voltage	Enables			0.8	V
$\|V_{ID}\|$	Magnitude of differential input voltage	LVDS	0.1		3	V
		LVDT			0.8	V
V_I or V_{IC}	Voltage at any bus terminal (separately or common-mode)		–2		4.4	V
T_A	Operating free-air temperature		–40		85	°C

ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
V_{IT1}	Positive-going differential input voltage threshold		V_{IB} = -2 V or 4.4 V, See Figure 1 and Figure 2			50	mV
V_{IT2}	Negative-going differential input voltage threshold			–50			mV
V_{IT3}	Differential input fail-safe voltage threshold		See Table 1 and Figure 5	–32		–100	mV
$V_{ID(HYS)}$	Differential input voltage hysteresis, $V_{IT1}– V_{IT2}$				50		mV
V_{OH}	High-level output voltage		I_{OH} = –4 mA	2.4			V
V_{OL}	Low-level output voltage		I_{OL} = 4 mA			0.4	V
I_{CC}	Supply current	'32B or '3486B	G or EN at V_{CC}, No load, Steady-state		16	23	mA
			G or EN at GND		1.1	5	
		'9637B	No load, Steady-state		8	12	
I_I	Input current (A or B inputs)	SN65LVDS	V_I = 0 V, Other input open			±20	µA
			V_I = 2.4 V, Other input open			±20	
			V_I = –2 V, Other input open			±40	
			V_I = 4.4 V, Other input open			±40	
		SN65LVDT	V_I = 0 V, Other input open			±40	µA
			V_I = 2.4 V, Other input open			±40	
			V_I = –2 V, Other input open			±80	
			V_I = 4.4 V, Other input open			±80	
I_{ID}	Differential input current (I_{IA} - I_{IB})	SN65LVDS	V_{ID} = 100 mV, V_{IC}= –2 V or 4.4 V, See Figure 1			±3	µA
		SN65LVDT	V_{ID} = 0.2 V, V_{IC} = –2 V or 4.4 V	1.55		2.22	mA
$I_{I(OFF)}$	Power-off input current (A or B inputs)	SN65LVDS	V_A or V_B = 0 V or 2.4 V, V_{CC} = 0 V			±20	µA
			V_A or V_B = –2 V or 4.4 V, V_{CC} = 0 V			±35	
		SN65LVDT	V_A or V_B = 0 V or 2.4 V, V_{CC} = 0 V			±30	
			V_A or V_B = –2 V or 4.4 V, V_{CC} = 0 V			±50	
I_{IH}	High-level input current (enables)		V_{IH} = 2 V			10	µA
I_{IL}	Low-level input current (enables)		V_{IL} = 0.8 V			10	µA
I_{OZ}	High-impedance output current					±10	µA
C_I	Input capacitance, A or B input to GND		V_I = 0.4 sin (4E6πt) + 0.5 V		5		pF

(1) All typical values are at 25°C and with a 3.3 V supply.

SWITCHING CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP [(1)]	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	See Figure 3	2.5	4	6	ns
t_{PHL}	Propagation delay time, high-to-low-level output		2.5	4	6	ns
t_{d1}	Delay time, fail-safe deactivate time	See Figure 3 and Figure 6			9	ns
t_{d2}	Delay time, fail-safe activate time		0.3		1.5	µs
$t_{sk(p)}$	Pulse skew ($\|t_{PHL1}$ - $t_{PLH1}\|$)	C_L = 10 pF, See Figure 3		200		ps
$t_{sk(o)}$	Output skew [(2)]			150		ps
$t_{sk(pp)}$	Part-to-part skew [(3)]				1	ns
t_r	Output signal rise time			0.8		ns
t_f	Output signal fall time			0.8		ns
t_{PHZ}	Propagation delay time, high-level-to-high-impedance output	See Figure 4		5.5	9	ns
t_{PLZ}	Propagation delay time, low-level-to-high-impedance output			4.4	9	ns
t_{PZH}	Propagation delay time, high-impedance -to-high-level output			3.8	9	ns
t_{PZL}	Propagation delay time, high-impedance-to-low-level output			7	9	ns

(1) All typical values are at 25°C and with a 3.3-V supply.
(2) $t_{sk(o)}$ is the magnitude of the time difference between the t_{PLH} or t_{PHL} of all receivers of a single device with all of their inputs driven together.
(3) $t_{sk(pp)}$ is the magnitude of the time difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.

PARAMETER MEASUREMENT INFORMATION

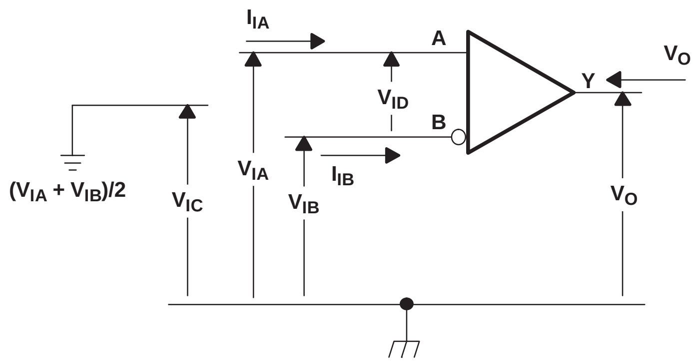
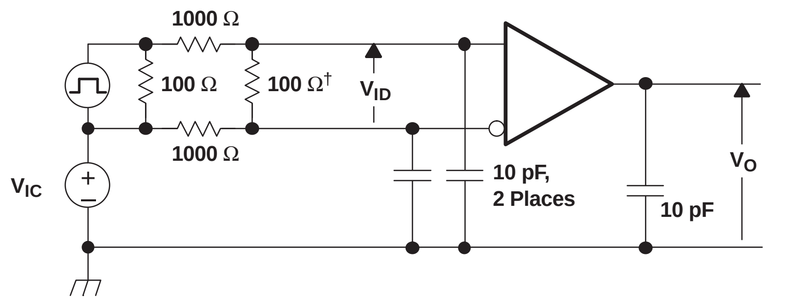
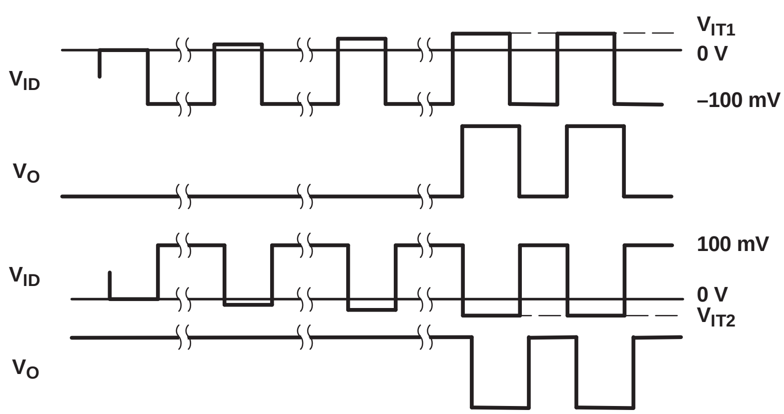


Figure 1. Voltage and Current Definitions



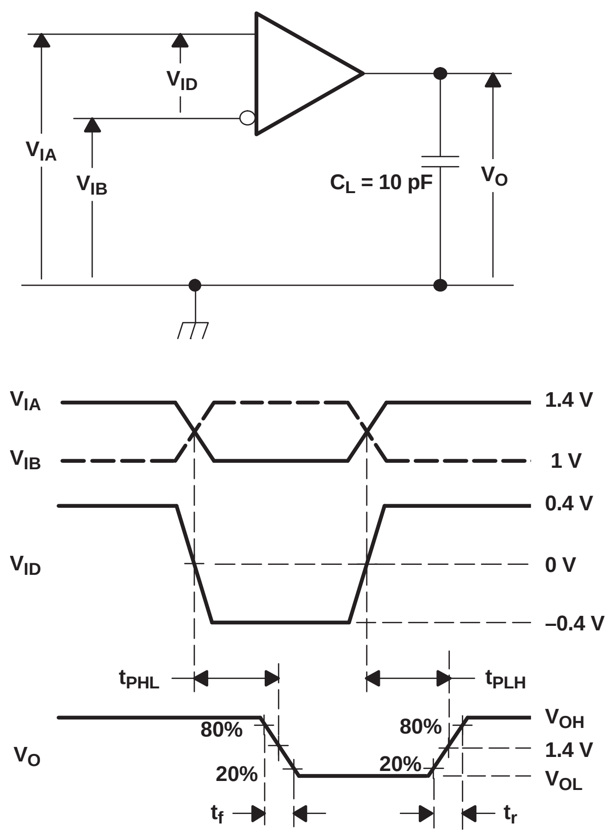
† Removed for testing the LVDT device



NOTE: Input signal of 3 Mpps, duration of 167 ns, and transition time of <1 ns.

Figure 2. V_{IT1} and V_{IT2} Input Voltage Threshold Test Circuit and Definitions

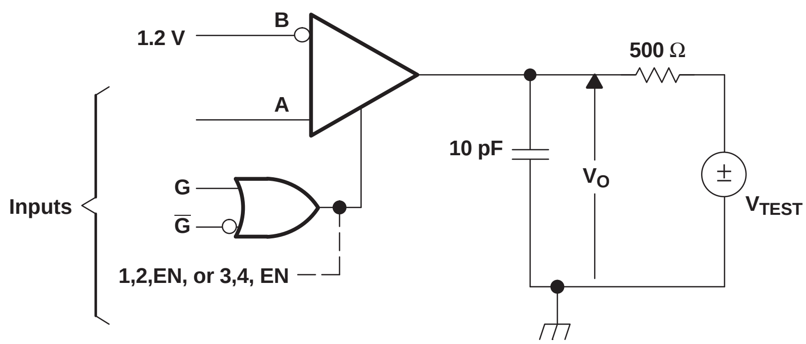
PARAMETER MEASUREMENT INFORMATION (continued)



A. All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq$ 1 ns, pulse repetition rate (PRR) = 50 Mpps, Pulsewidth = 10 ±0.2 ns . C_L includes instrumentation and fixture capacitance within 0,06 mm of the D.U.T.

Figure 3. Timing Test Circuit and Waveforms

PARAMETER MEASUREMENT INFORMATION (continued)



NOTE: All input pulses are supplied by a generator having the following characteristics: t_r or t_f ≤ 1 ns, pulse repetition rate (PRR) = 0.5 Mpps, Pulsewidth = 500 ±10 ns . C_L includes instrumentation and fixture capacitance within 0,06 mm of the D.U.T.

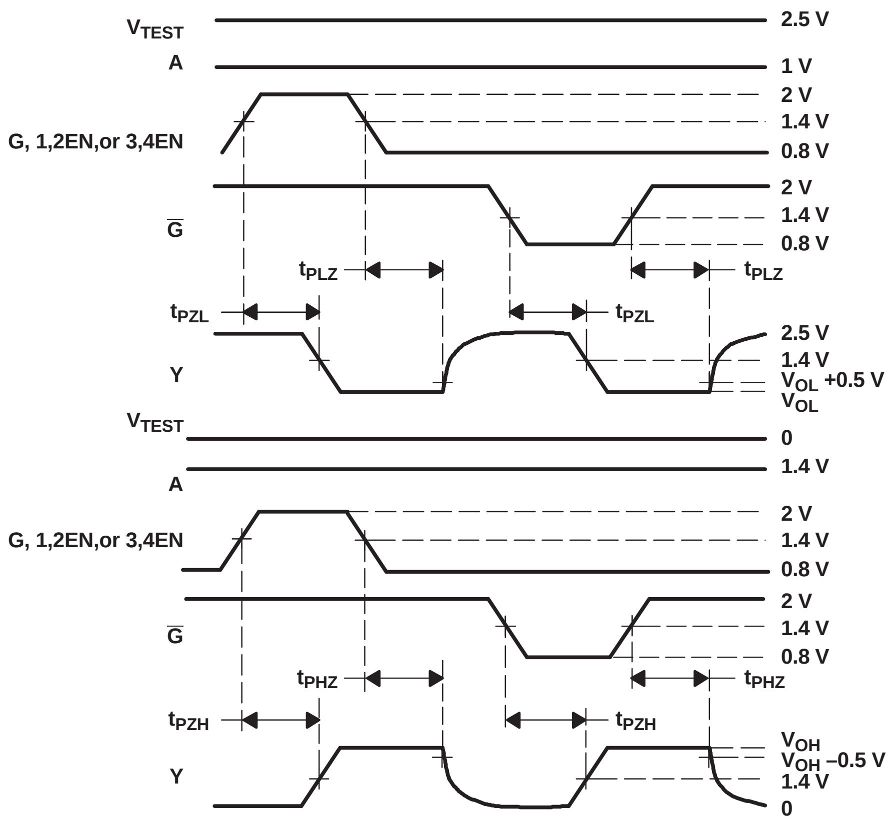


Figure 4. Enable/Disable Time Test Circuit and Waveforms

Table 1. Receiver Minimum and Maximum V_{IT3} Input Threshold Test Voltages

APPLIED VOLTAGES(1)		RESULTANT INPUTS		
V_{IA} (mV)	V_{IB} (mV)	V_{ID} (mV)	V_{IC} (mV)	Output
–2000	–1900	–100	–1950	L
–2000	–1968	–32	–1984	H
4300	4400	–100	4350	L
4368	4400	–32	4384	H

(1) These voltages are applied for a minimum of 1.5 µs.

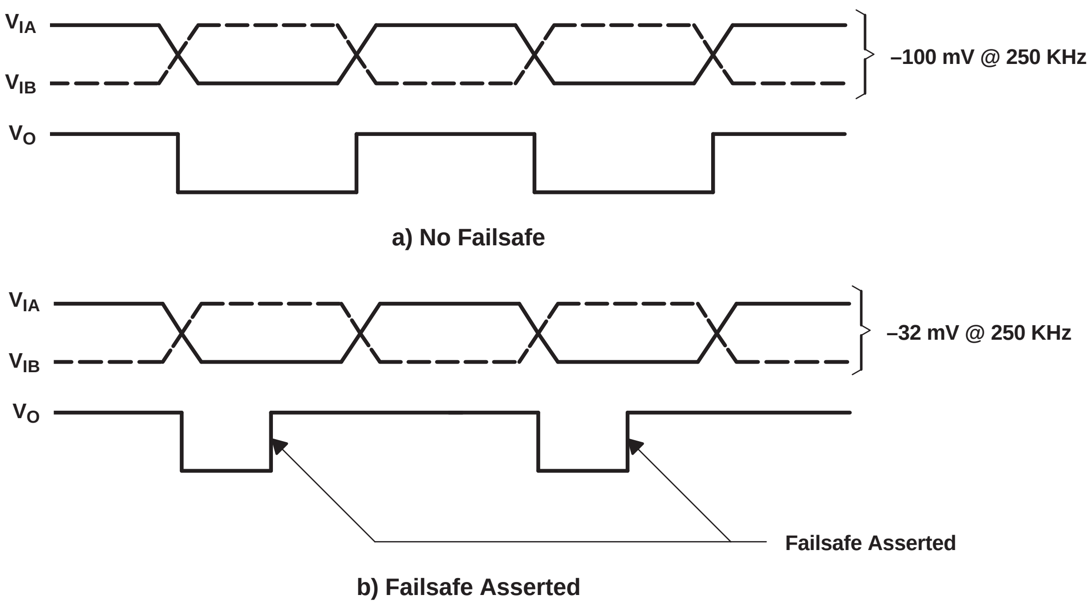


Figure 5. V_{IT3} Failsafe Threshold Test

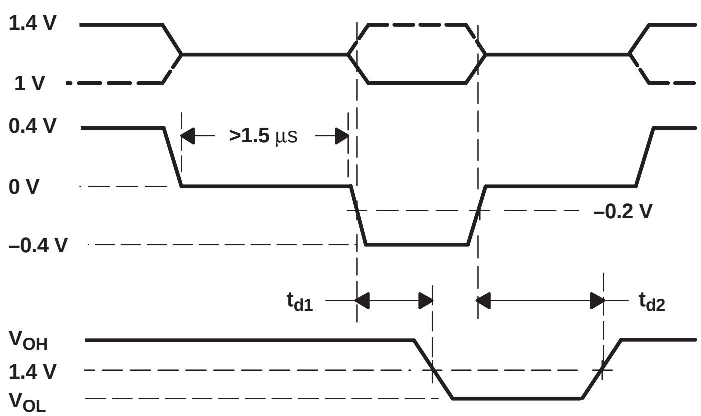


Figure 6. Waveforms for Failsafe Activate and Deactivate

TYPICAL CHARACTERISTICS

LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT

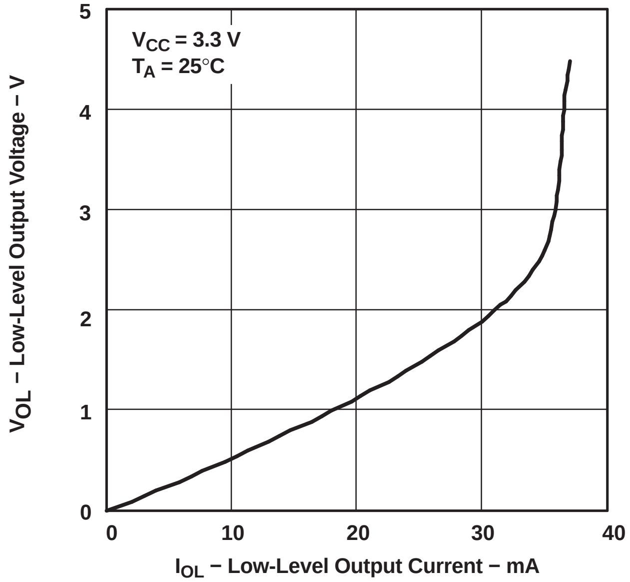


Figure 7.

HIGH-LEVEL OUTPUT VOLTAGE vs HIGH-LEVEL OUTPUT CURRENT

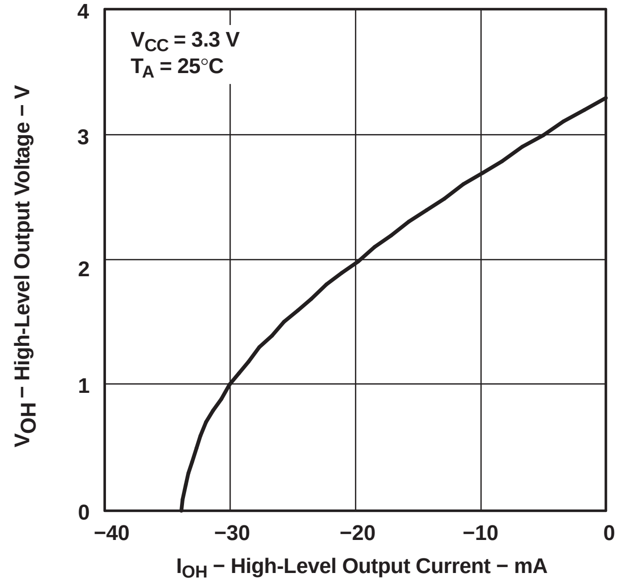


Figure 8.

LOW-TO-HIGH PROPAGATION DELAY TIME vs FREE-AIR TEMPERATURE

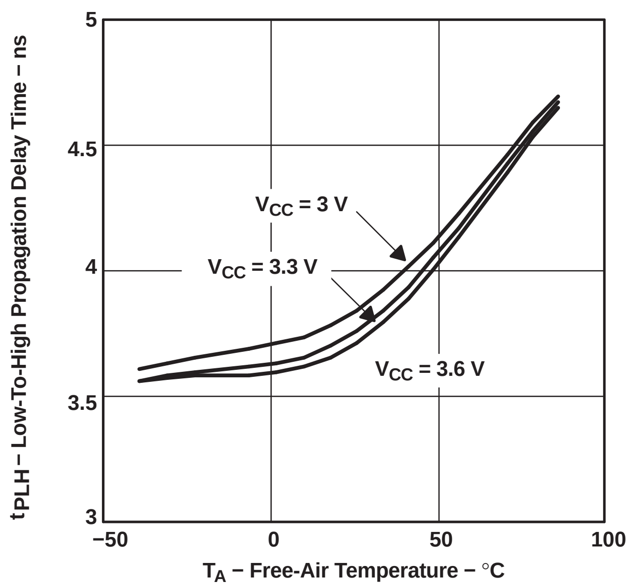


Figure 9.

HIGH-TO-LOW PROPAGATION DELAY TIME vs FREE-AIR TEMPERATURE

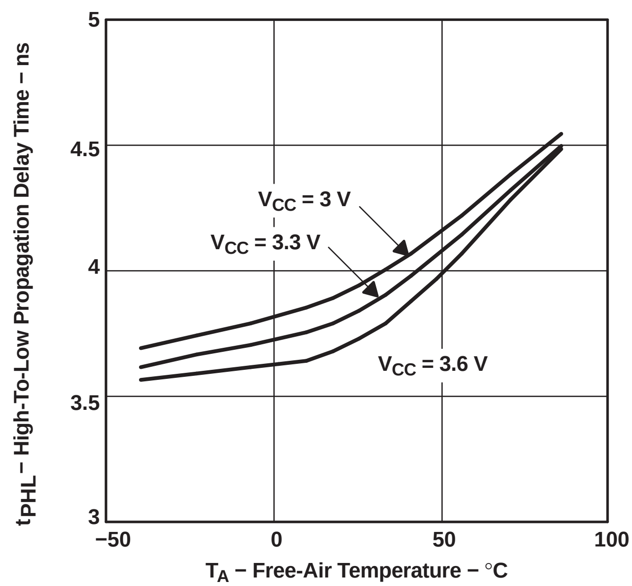


Figure 10.

TYPICAL CHARACTERISTICS (continued)

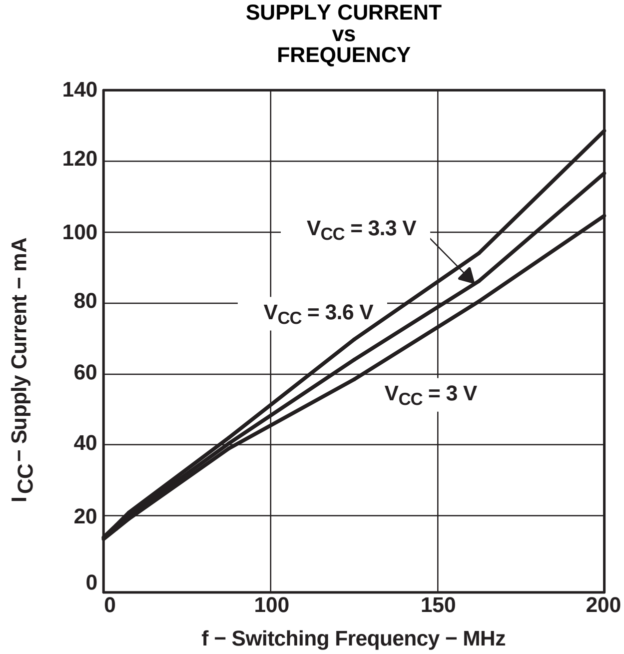
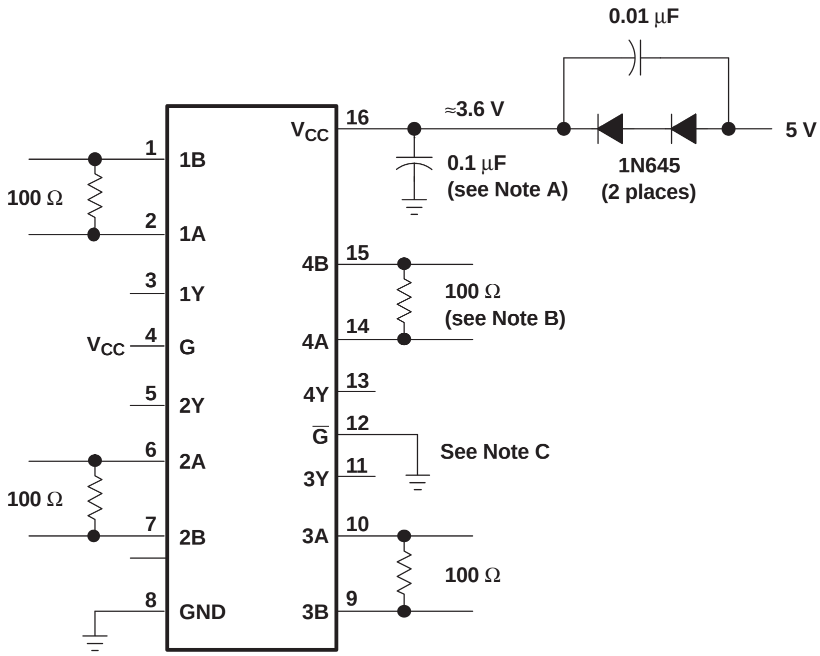


Figure 11.

APPLICATION INFORMATION



A. Place a 0.1-µF Z5U ceramic, mica or polystyrene dielectric, 0805 size, chip capacitor between V_{CC} and the ground plane. The capacitor should be located as close as possible to the device terminals.

B. The termination resistance value should match the nominal characteristic impedance of the transmission media with ±10%.

C. Unused enable inputs should be tied to V_{CC} or GND as appropriate.

Figure 12. Operation with 5-V Supply

RELATED INFORMATION

IBIS modeling is available for this device. contact the local TI sales office or the TI Web site at *www.ti.com* for more information.

For more application guidelines, see the following documents:

- *Low-Voltage Differential Signaling Design Notes* (SLLA014)
- *Interface Circuits for TIA/EIA-644* (LVDS) (SLLA038)
- *Reducing EMI With LVDS* (SLLA030)
- *Slew Rate Control of LVDS Circuits* (SLLA034)
- *Using an LVDS Receiver With RS-422 Data* (SLLA031)
- *Evaluating the LVDS EVM* (SLLA033)

TERMINATED FAILSAFE

A differential line receiver commonly has a fail-safe circuit to prevent it from switching on input noise. Current LVDS fail-safe solutions require either external components with subsequent reduction in signal quality or integrated solutions with limited application. This family of receivers has a new integrated fail-safe that solves the limitations seen in present solutions. A detailed theory of operation is presented in application note *The Active Fail-Safe Feature of the SN65LVDS32A* (SLLA082).

Figure 13 shows one receiver channel with active fail-safe. It consists of a main receiver that can respond to a high-speed input differential signal. Also connected to the input pair are two fail-safe receivers that form a window comparator. The window comparator has a much slower response than the main receiver and detects when the input differential falls below 80 mV. A 600-ns fail-safe timer filters the window comparator outputs. When fail-safe is asserted, the fail-safe logic drives the main receiver output to logic high.

APPLICATION INFORMATION (continued)

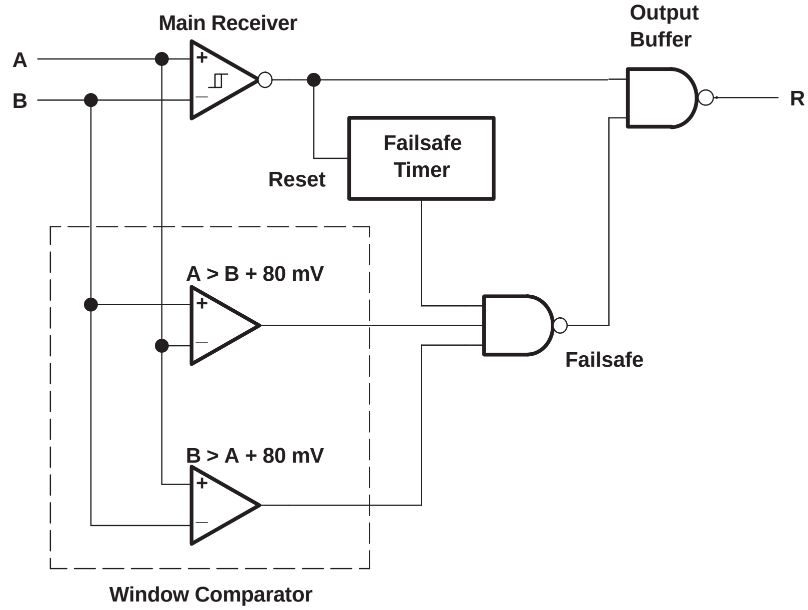


Figure 13. Receiver With Terminated Failsafe

ECL/PECL-to-LVTTL CONVERSION WITH TI's LVDS RECEIVER

The various versions of emitter-coupled logic (i.e., ECL, PECL and LVPECL) are often the physical layer of choice for system designers. Designers know of the established technology and that it is capable of high-speed data transmission. In the past, system requirements often forced the selection of ECL. Now technologies like LVDS provide designers with another alternative. While the total exchange of ECL for LVDS may not be a design option, designers have been able to take advantage of LVDS by implementing a small resistor divider network at the input of the LVDS receiver. TI has taken the next step by introducing a wide common-mode LVDS receiver (no divider network required) which can be connected directly to an ECL driver with only the termination bias voltage required for ECL termination (V_{CC} – 2 V).

Figure 14 and Figure 15 show the use of an LV/PECL driver driving 5 meters of CAT-5 cable and being received by TI's wide common-mode receiver and the resulting eye pattern. The values for R3 are required in order to provide a resistor path to ground for the LV/PECL driver. With no resistor divider, R1 simply needs to match the characteristic load impedance of 50 Ω. The R2 resistor is a small value and is intended to minimize any possible common-mode current reflections.

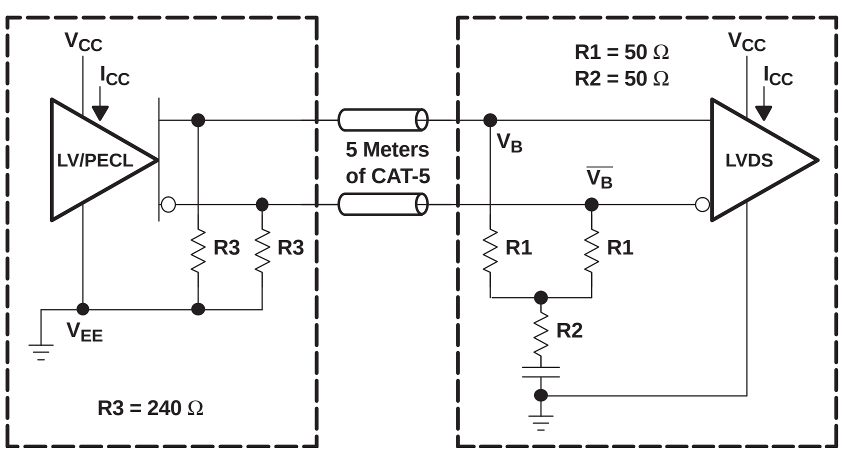


Figure 14. LVPECL or PECL to Remote Wide Common-Mode LVDS Receiver

APPLICATION INFORMATION (continued)

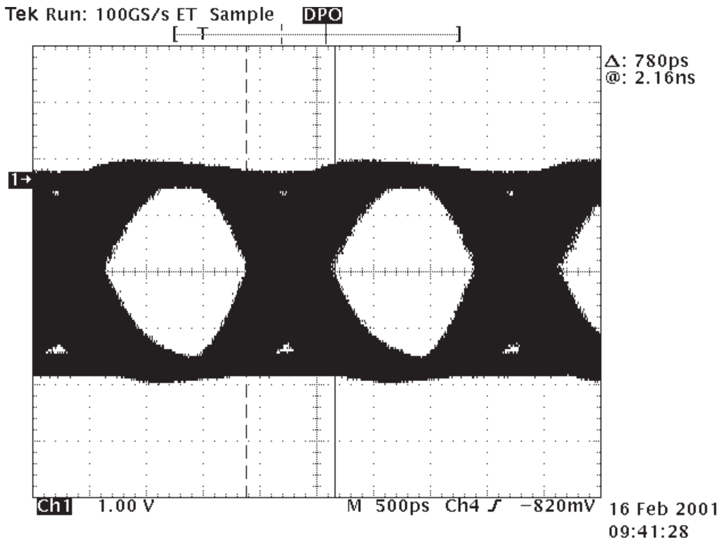


Figure 15. LV/PECL to Remote SN65LVDS32B at 500 Mbps Receiver Output (CH1)

TEST CONDITIONS

- V_{CC} = 3.3 V
- T_A = 25°C (ambient temperature)
- All four channels switching simultaneously with NRZ data. Scope is pulse-triggered simultaneously with NRZ data.

EQUIPMENT

- Tektronix PS25216 programmable power supply
- Tektronix HFS 9003 stimulus system
- Tektronix TDS 784D 4-channel digital phosphor oscilloscope – DPO

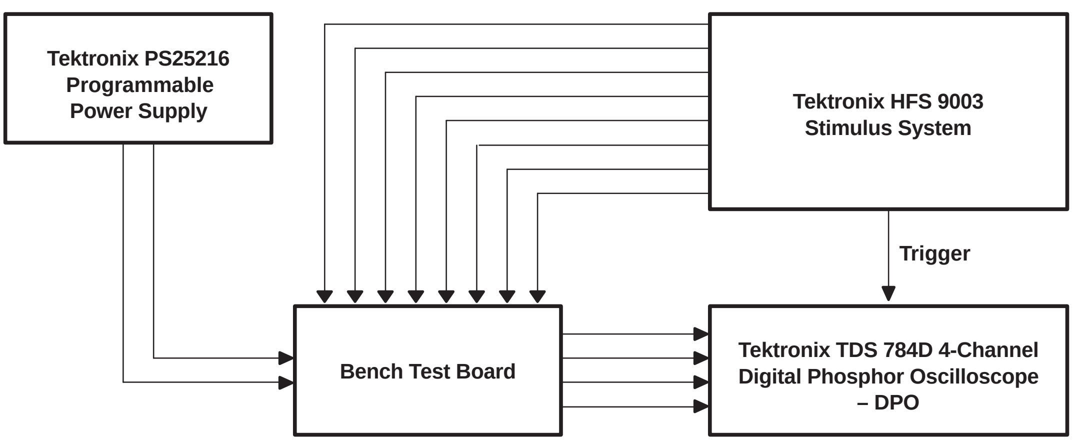


Figure 16. Equipment Setup

APPLICATION INFORMATION (continued)

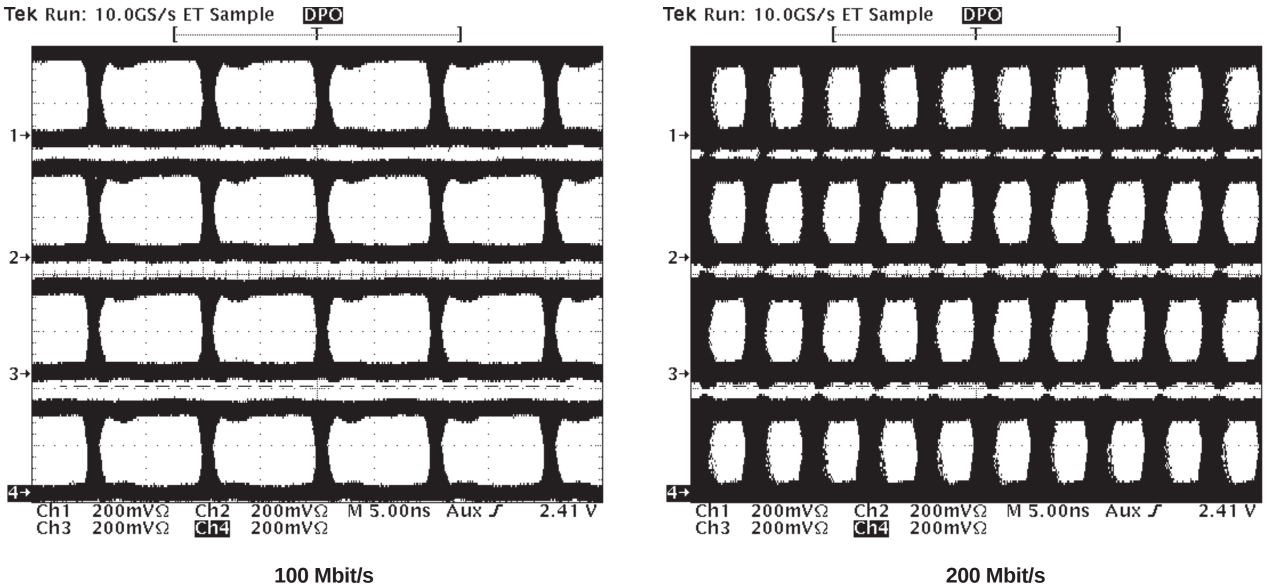


Figure 17. Typical Eye Pattern SN65LVDS32B

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN65LVDS32BD	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS32B	Samples
SN65LVDS32BDG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS32B	Samples
SN65LVDS32BDR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS32B	Samples
SN65LVDS3486BD	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS3486B	Samples
SN65LVDS3486BDR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS3486B	Samples
SN65LVDS9637BD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	DK637B	Samples
SN65LVDS9637BDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	DK637B	Samples
SN65LVDT32BD	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDT32B	Samples
SN65LVDT32BDG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDT32B	Samples
SN65LVDT32BDR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDT32B	Samples
SN65LVDT3486BD	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDT3486B	Samples
SN65LVDT3486BDR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDT3486B	Samples
SN65LVDT9637BD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	DR637B	Samples
SN65LVDT9637BDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	DR637B	Samples
SN65LVDT9637BDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	DR637B	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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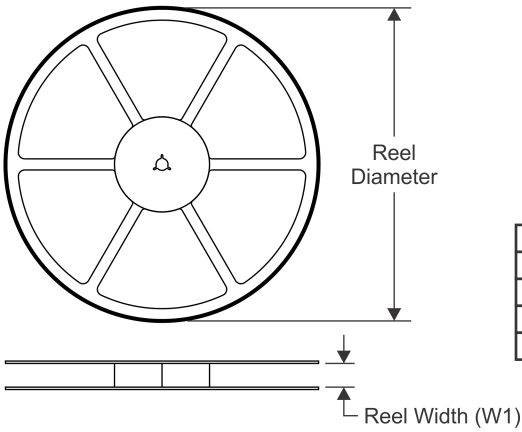
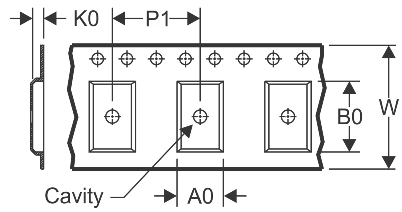
TAPE AND REEL INFORMATION

REEL DIMENSIONS

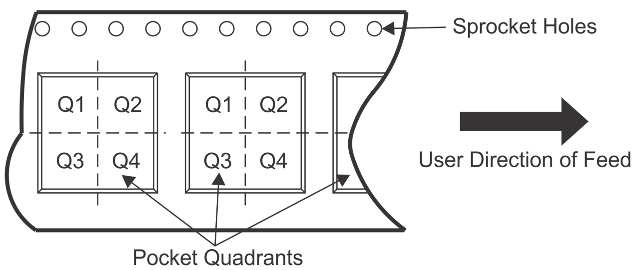


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

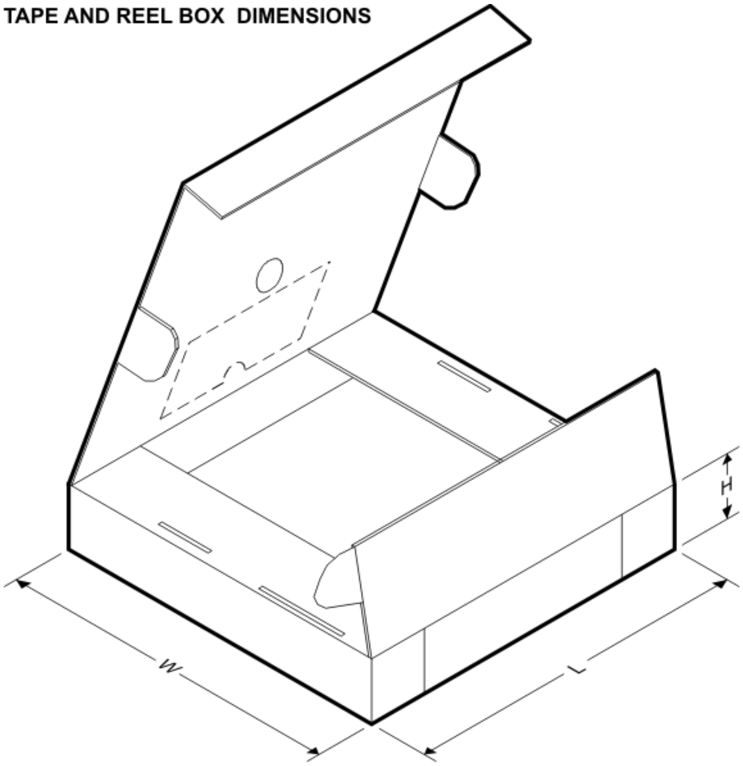
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65LVDS32BDR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN65LVDS3486BDR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN65LVDS9637BDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN65LVDT32BDR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN65LVDT3486BDR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN65LVDT9637BDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65LVDS32BDR	SOIC	D	16	2500	333.2	345.9	28.6
SN65LVDS3486BDR	SOIC	D	16	2500	350.0	350.0	43.0
SN65LVDS9637BDR	SOIC	D	8	2500	340.5	338.1	20.6
SN65LVDT32BDR	SOIC	D	16	2500	350.0	350.0	43.0
SN65LVDT3486BDR	SOIC	D	16	2500	350.0	350.0	43.0
SN65LVDT9637BDR	SOIC	D	8	2500	340.5	338.1	20.6

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