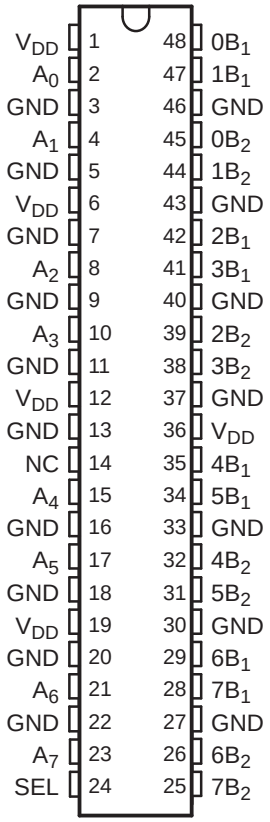
TS3DV416
4-CHANNEL DIFFERENTIAL 8:16 MULTIPLEXER SWITCH FOR DVI/HDMI APPLICATIONS

SCDS198C – OCTOBER 2005 – REVISED MAY 2006

FEATURES

- **Compatible With HDMI v1.2a (Type A) DVI 1.0 High-Speed Digital Interface**
  - **Wide Bandwidth of Over 1.65 Gbps (Bandwidth 1.8 Gbps Typ)**
  - **165-MHz Speed Operation**
  - **Serial Data Stream at 10× Pixel Clock Rate**
  - **Supports All Video Formats up to 1080p and SXGA (1280 × 1024 at 75 Hz)**
  - **Total Raw Capacity 4.95 Gbps (Single Link)**
  - **HDCP Compatible**
- **Low Crosstalk (X_{TALK} = –41 dB Typ)**
- **Low Bit-to-Bit Skew ($t_{sk(o)}$ = 0.2 ns Max)**
- **Low and Flat ON-State Resistance (r_{on} = 4 Ω Typ, $r_{on(flat)}$ = 0.7 Ω Typ)**
- **Low Input/Output Capacitance (C_{ON} = 10 pF Typ)**
- **Rail-to-Rail Switching on Data I/O Ports (0 to 5 V)**
- **V_{DD} Operating Range From 3 V to 3.6 V**
- **I_{off} Supports Partial-Power-Down Mode Operation**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Performance Tested Per JESD 22**
  - **2000-V Human-Body Model (A114-B, Class II)**
  - **1000-V Charged-Device Model (C101)**

DGG OR DGV PACKAGE
(TOP VIEW)



NC − No internal connection

APPLICATIONS

- **Digital Video Signal Switching**
- **Differential DVI, HDMI Signal Multiplexing for Audio/Video Receivers and High-Definition Television (HDTV)**

DESCRIPTION/ORDERING INFORMATION

The TS3DV416 is a 16-bit to 8-bit multiplexer/demultiplexer digital video switch with a single select (SEL) input. SEL controls the data path of the multiplexer/demultiplexer.

The device provides a low and flat ON-state resistance (r_{on}) and an excellent ON-state resistance match. Low input/output capacitance, high bandwidth, low skew, and low crosstalk among channels make this device suitable for various digital video applications, such as DVI and HDMI.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

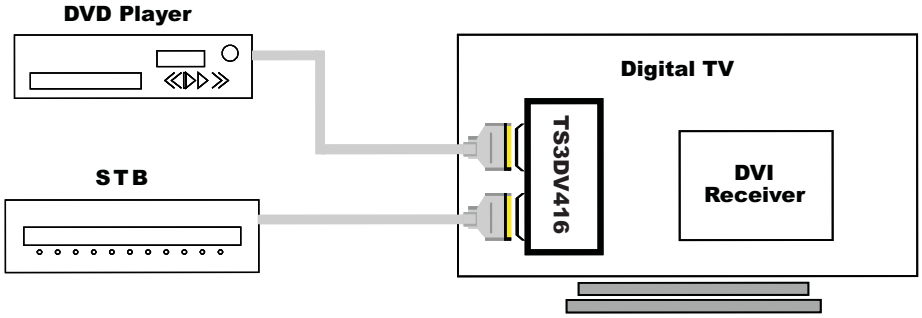
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ORDERING INFORMATION

T_A	PACKAGE(1)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	TSSOP – DGG	Tape and reel	TS3DV416DGGR	TS3DV416
	TVSOP – DGV	Tape and reel	TS3DV416DGVR	SD416

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

TYPICAL APPLICATION



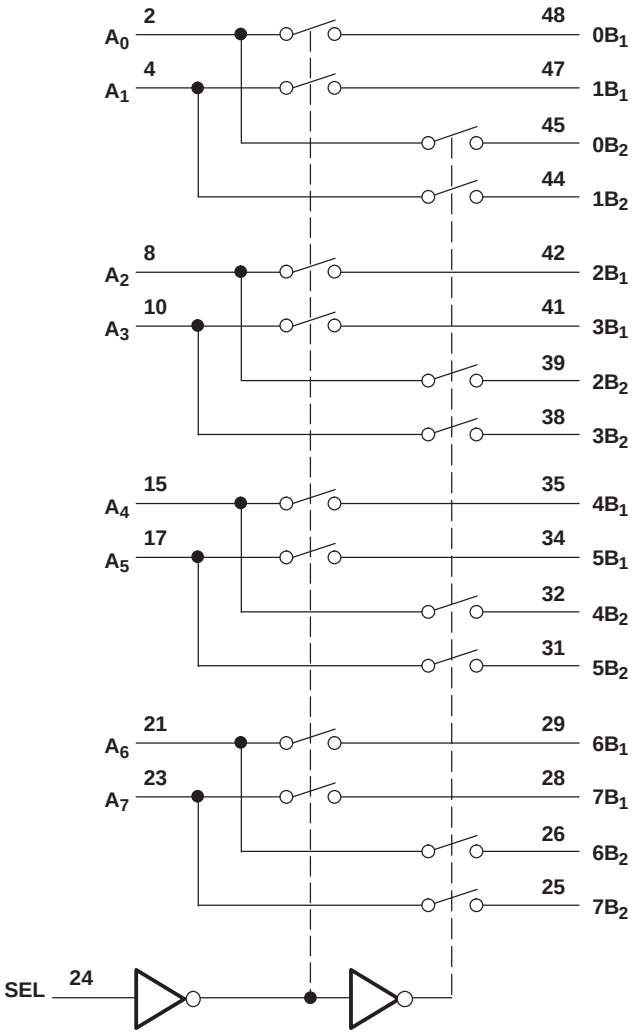
FUNCTION TABLE

INPUT SEL	INPUT/ OUTPUT A_n	FUNCTION	
L	nB_1	$A_n = nB_1$	nB_2 high-impedance mode
H	nB_2	$A_n = nB_2$	nB_1 high-impedance mode

PIN DESCRIPTION

NAME	DESCRIPTION
A_n	Data I/O
nB_m	Data I/O
SEL	Select input

LOGIC DIAGRAM (POSITIVE LOGIC)



Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{DD}	Supply voltage range		–0.5	4.6	V
V_{IN}	Control input voltage range(2)(3)		–0.5	7	V
$V_{I/O}$	Switch I/O voltage range(2)(3)(4)		–0.5	7	V
I_{IK}	Control input clamp current	$V_{IN} < 0$		–50	mA
$I_{I/OK}$	I/O port clamp current	$V_{I/O} < 0$		–50	mA
$I_{I/O}$	ON-state switch current(5)			±128	mA
	Continuous current through V_{DD} or GND			±100	mA
θ_{JA}	Package thermal impedance(6)	DGG package		70	°C/W
		DGV package		58	
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to ground, unless otherwise specified.
(3) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(4) V_I and V_O are used to denote specific conditions for $V_{I/O}$.
(5) I_I and I_O are used to denote specific conditions for $I_{I/O}$.
(6) The package thermal impedance is calculated in accordance with JESD 51-7.

Recommended Operating Conditions(1)

		MIN	MAX	UNIT
V_{DD}	Supply voltage	3	3.6	V
V_{IH}	High-level control input voltage (SEL)	2	5.5	V
V_{IL}	Low-level control input voltage (SEL)	0	0.8	V
$V_{I/o}$	Input/output voltage	0	5.5	V
T_A	Operating free-air temperature	–40	85	°C

(1) All unused inputs of the device must be held at V_{DD} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

Electrical Characteristics(1)

for high-frequency switching over recommended operating free-air temperature range, V_{DD} = 3.3 V ± 0.3 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS				MIN	TYP(2)	MAX	UNIT
V_{IK}	SEL	V_{DD} = 3.6 V,	I_{IN} = –18 mA				–0.7	–1.2	V
I_{IH}	SEL	V_{DD} = 3.6 V,	V_{IN} = V_{DD}					±1	µA
I_{IL}	SEL	V_{DD} = 3.6 V,	V_{IN} = GND					±1	µA
I_{off}		V_{DD} = 0,	V_O = 0 to 3.6 V,	V_I = 0				1	µA
I_{DD}		V_{DD} = 3.6 V,	$I_{I/O}$ = 0,	Switch ON or OFF			250	600	µA
C_{IN}	SEL	f = 1 MHz,	V_{IN} = 0				2.5	3	pF
C_{OFF}	B port	V_I = 0,	f = 1 MHz,	Outputs open,	Switch OFF		3.5	4	pF
C_{ON}		V_I = 0,	f = 1 MHz,	Outputs open,	Switch ON		10	10.9	pF
r_{on}		V_{DD} = 3 V,	1.5 V ≤ V_I ≤ V_{DD},	I_O = –40 mA			4	8	Ω
$r_{on(flat)}$(3)		V_{DD} = 3 V,	V_I = 1.5 V and V_{DD},	I_O = –40 mA			0.7		Ω
Δr_{on}(4)		V_{DD} = 3 V,	1.5 V ≤ V_I ≤ V_{DD},	I_O = –40 mA			0.2	1.2	Ω

(1) V_I, V_O, I_I, and I_O refer to I/O pins. V_{IN} refers to the control inputs.
(2) All typical values are at V_{DD} = 3.3 V (unless otherwise noted), T_A = 25°C.
(3) $r_{on(flat)}$ is the difference of r_{on} in a given channel at specified voltages.
(4) Δr_{on} is the difference of r_{on} from center (A_4, A_5) ports to any other port.

Switching Characteristics

over recommended operating free-air temperature range, V_{DD} = 3.3 V ± 0.3 V, R_L = 200 Ω, C_L = 10 pF (unless otherwise noted) (see Figure 4 and Figure 5)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP(1)	MAX	UNIT
t_{pd}(2)	A or B	B or A		0.04		ns
t_{PZH}, t_{PZL}	SEL	A or B	1.5		11.5	ns
t_{PHZ}, t_{PLZ}	SEL	A or B	1		8.5	ns
$t_{sk(o)}$(3)	A or B	B or A		0.1	0.2	ns
$t_{sk(p)}$(4)				0.1	0.2	ns

(1) All typical values are at V_{DD} = 3.3 V (unless otherwise noted), T_A = 25°C.
(2) The propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance when driven by an ideal voltage source (zero output impedance).
(3) Output skew between center port (A_4 to A_5) to any other port
(4) Skew between opposite transitions of the same output in a given device $|t_{PHL} - t_{PLH}|$

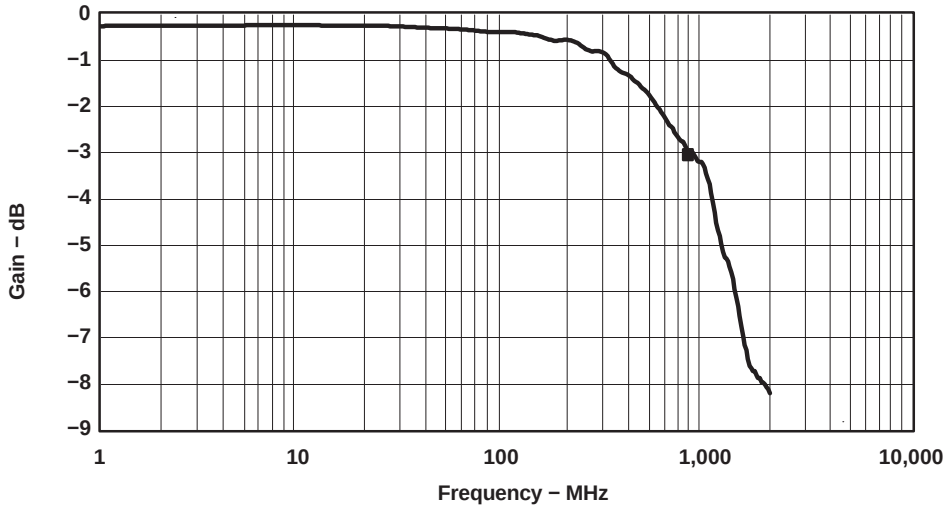
Dynamic Characteristics

over recommended operating free-air temperature range, V_{DD} = 3.3 V ± 0.3 V (unless otherwise noted)

PARAMETER	TEST CONDITIONS			TYP(1)	UNIT
X_{TALK}	R_L = 100 Ω,	f = 250 MHz,	See Figure 7	–41	dB
O_{IRR}	R_L = 100 Ω,	f = 250 MHz,	See Figure 8	–39	dB
BW	See Figure 6			900	MHz

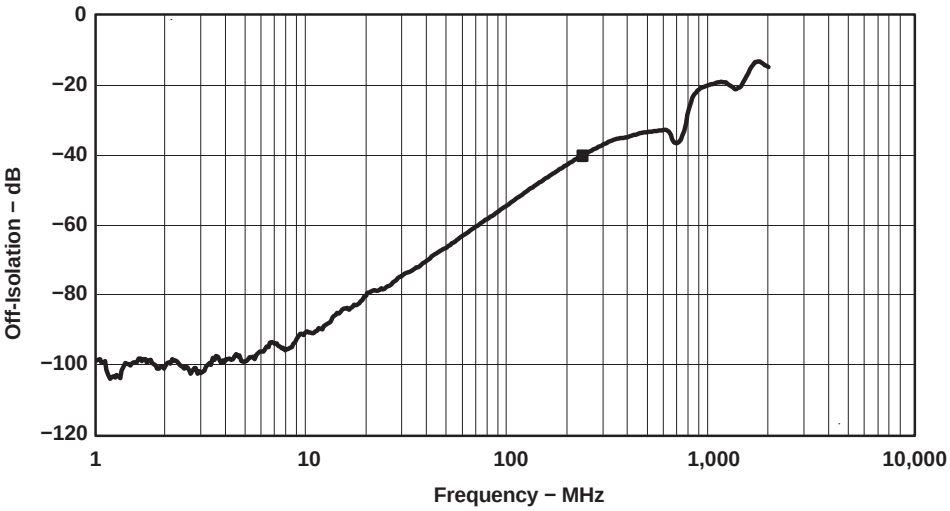
(1) All typical values are at V_{DD} = 3.3 V (unless otherwise noted), T_A = 25°C.

OPERATING CHARACTERISTICS



■ Gain at 900 MHz, −3 dB

Figure 1. Gain vs Frequency



■ OFF Isolation at 250 MHz, −39 dB

Figure 2. OFF Isolation vs Frequency

OPERATING CHARACTERISTICS (continued)

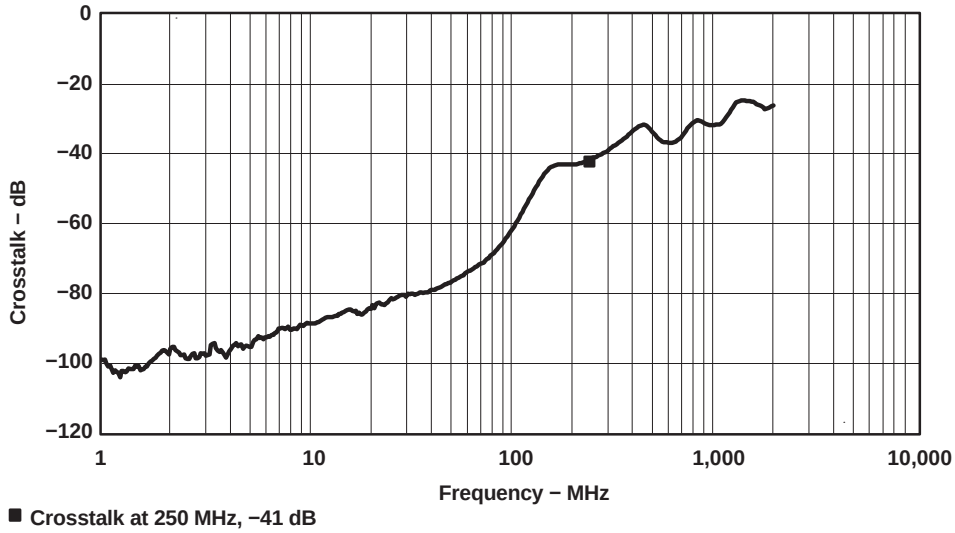
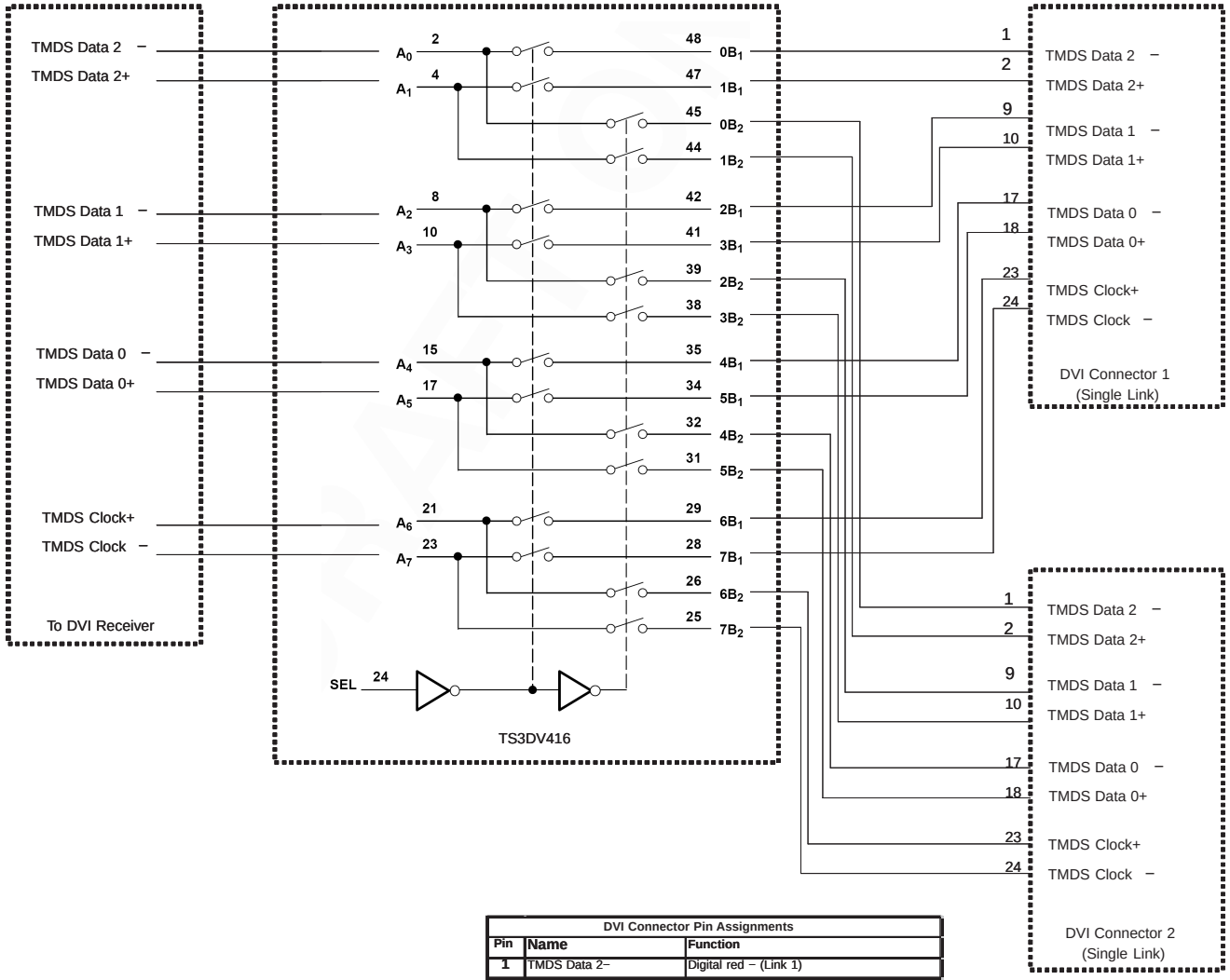
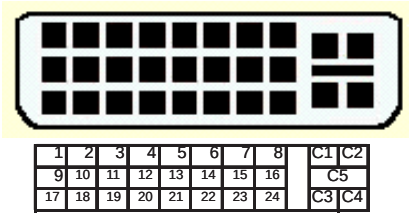


Figure 3. Crosstalk vs Frequency

APPLICATION INFORMATION



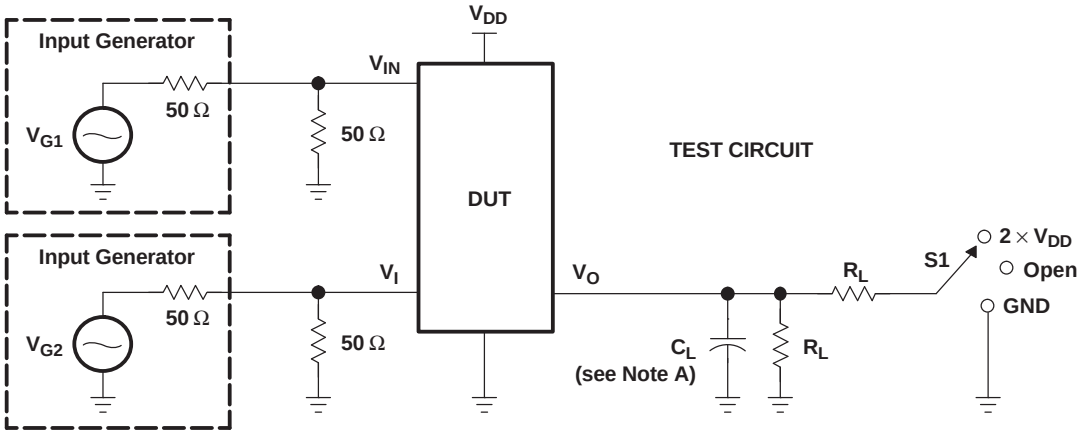
Typical DVI Connector



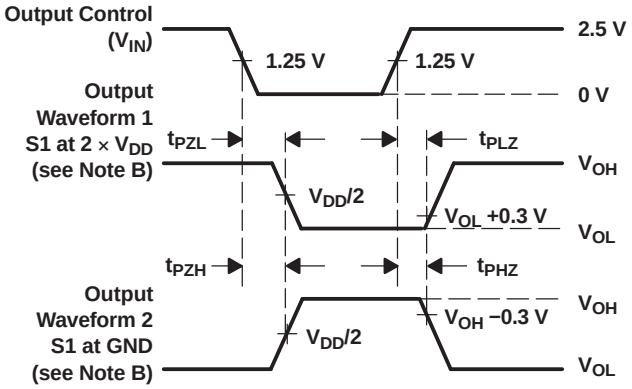
The TS3DV416 can be used to switch between two digital video ports.

DVI Connector Pin Assignments		
Pin	**Name**	**Function**
1	TMDS Data 2–	Digital red – (Link 1)
2	TMDS Data 2+	Digital red + (Link 1)
3	TMDS Data 2/4 shield	
4	TMDS Data 4–	Digital green – (Link 2)
5	TMDS Data 4+	Digital green + (Link 2)
6	DDC clock	
7	DDC data	
8	Analog Vertical Sync	
9	TMDS Data 1–	Digital green – (Link 1)
10	TMDS Data 1+	Digital green + (Link 1)
11	TMDS Data 1/3 shield	
12	TMDS Data 3–	Digital blue – (Link 2)
13	TMDS Data 3+	Digital blue + (Link 2)
14	+5V	Power for monitor when in standby
15	Ground	Return for pin 14 and analog sync
16	Hot Plug Detect	
17	TMDS data 0–	Digital blue – (Link 1) and digital sync
18	TMDS data 0+	Digital blue + (Link 1) and digital sync
19	TMDS data 0/5 shield	
20	TMDS data 5–	Digital red – (Link 2)
21	TMDS data 5+	Digital red + (Link 2)
22	TMDS clock shield	
23	TMDS clock+	Digital clock + (Links 1 and 2)
24	TMDS clock–	Digital clock – (Links 1 and 2)
C1	Analog Red	
C2	Analog Green	
C3	Analog Blue	
C4	Analog Horizontal Sync	
C5	Analog Ground	Return for R, G and B signals

PARAMETER MEASUREMENT INFORMATION
(Enable and Disable Times)



TEST	V_{DD}	S1	R_L	V_I	C_L	V_Δ
t_{PLZ}/t_{PZL}	3.3 V ± 0.3 V	2 × V_{DD}	200 Ω	GND	10 pF	0.3 V
t_{PHZ}/t_{PZH}	3.3 V ± 0.3 V	GND	200 Ω	V_{DD}	10 pF	0.3 V

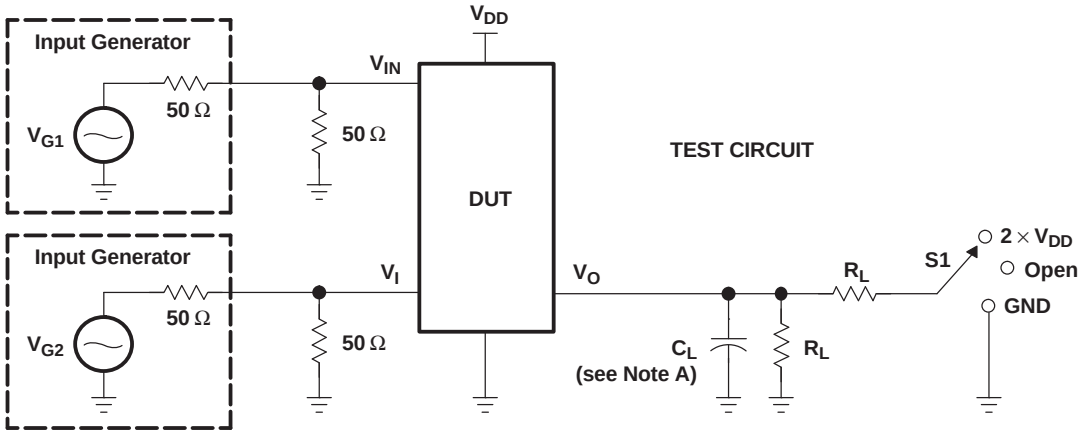


VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

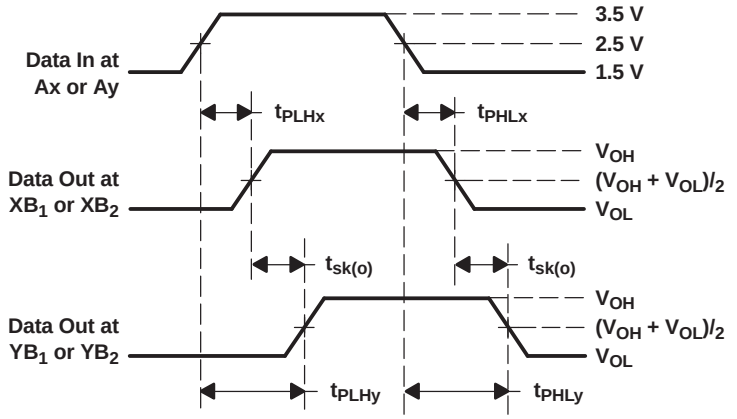
NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.

Figure 4. Test Circuit and Voltage Waveforms

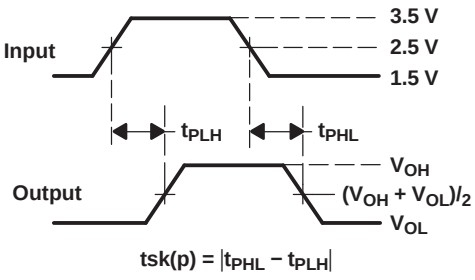
PARAMETER MEASUREMENT INFORMATION
(Skew)



TEST	V_{DD}	S1	R_L	V_I	C_L	V_Δ
$t_{sk(o)}$	3.3 V ± 0.3 V	Open	200 Ω	V_{DD} or GND	10 pF	
$t_{sk(p)}$	3.3 V ± 0.3 V	Open	200 Ω	V_{DD} or GND	10 pF	



VOLTAGE WAVEFORMS
OUTPUT SKEW ($t_{sk(o)}$)

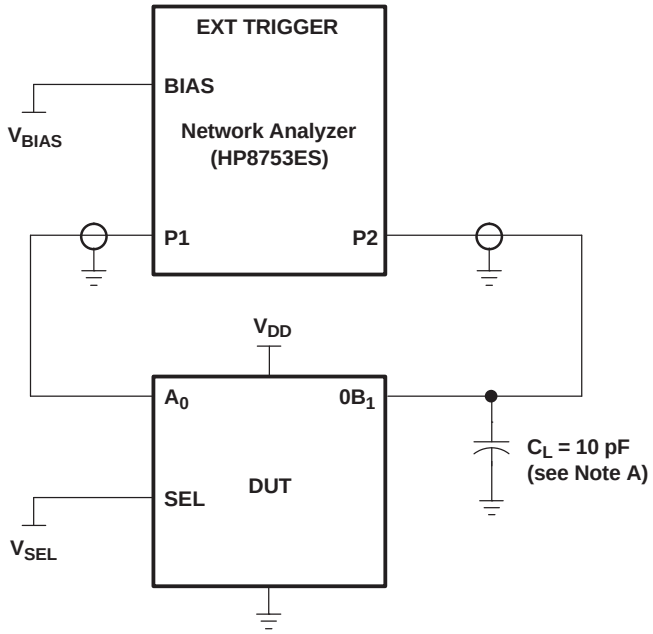


VOLTAGE WAVEFORMS
PULSE SKEW ($t_{sk(p)}$)

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time, with one transition per measurement.

Figure 5. Test Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION



NOTE A: C_L includes probe and jig capacitance.

Figure 6. Test Circuit for Frequency Response (BW)

Frequency response is measured at the output of the ON channel. For example, when V_{SEL} = 0 and A_0 is the input, the output is measured at $0B_1$. All unused analog I/O ports are left open.

HP8753ES Setup

Average = 4

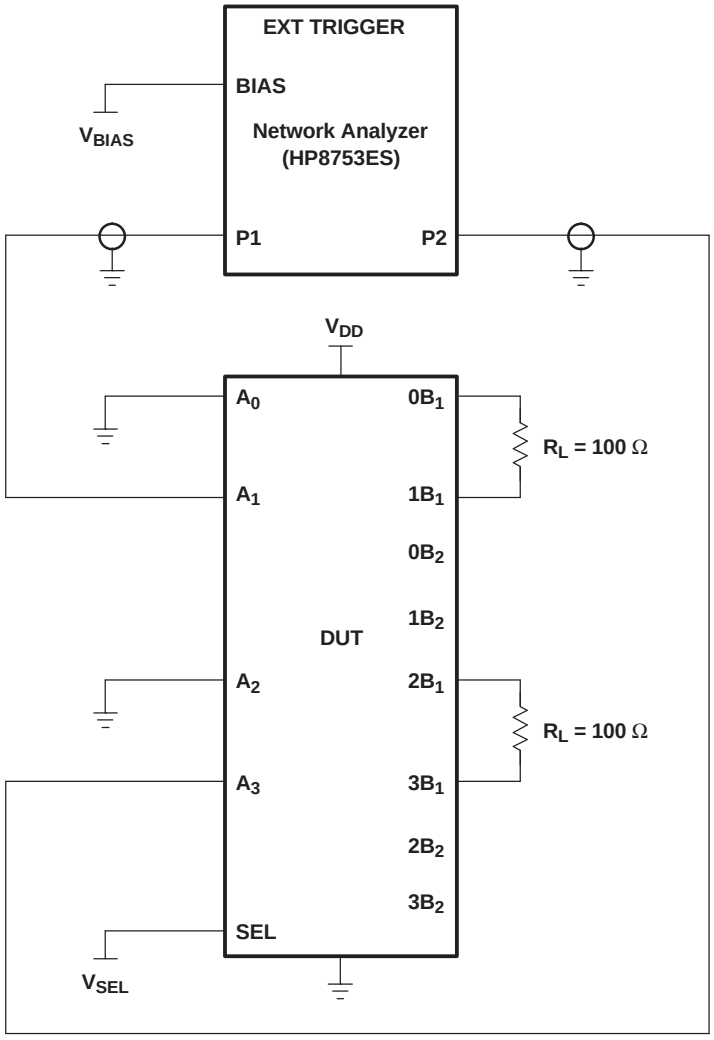
RBW = 3 kHz

V_{BIAS} = 0.35 V

ST = 2 s

P1 = 0 dBM

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.
B. A 50-Ω termination resistor is needed to match the loading of the network analyzer.

Figure 7. Test Circuit for Crosstalk (X_{TALK})

Crosstalk is measured at the output of the nonadjacent ON channel. For example, when V_{SEL} = 0 and A_1 is the input, the output is measured at A_3. All unused analog input (A) ports are connected to GND, and output (B) ports are left open.

HP8753ES Setup

Average = 4

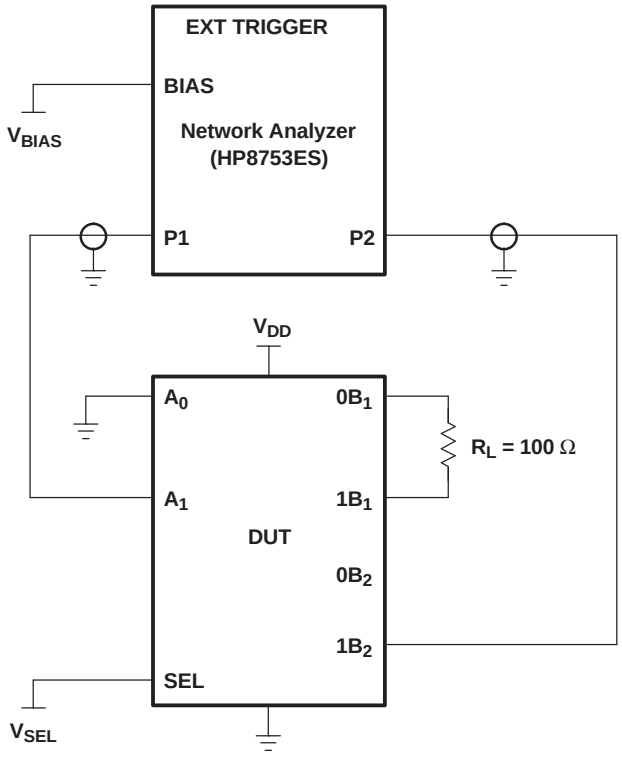
RBW = 3 kHz

V_{BIAS} = 0.35 V

ST = 2 s

P1 = 0 dBM

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.
B. A 50-Ω termination resistor is needed to match the loading of the network analyzer.

Figure 8. Test Circuit for OFF Isolation (O_{IRR})

OFF isolation is measured at the output of the OFF channel. For example, when V_{SEL} = GND and A_1 is the input, the output is measured at $1B_2$. All unused analog input (A) ports are connected to ground, and output (B) ports are left open.

HP8753ES Setup

Average = 4

RBW = 3 kHz

V_{BIAS} = 0.35 V

ST = 2 s

P1 = 0 dBM

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TS3DV416DGGR	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TS3DV416	Samples
TS3DV416DGVR	ACTIVE	TVSOP	DGV	48	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	SD416	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

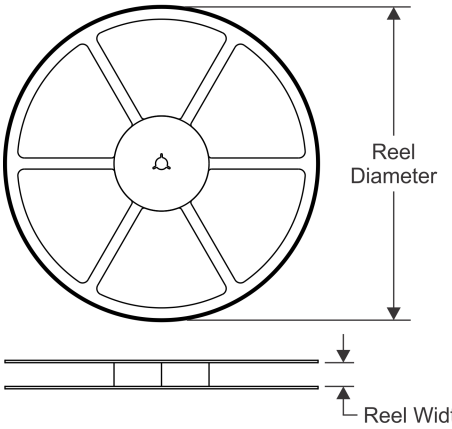
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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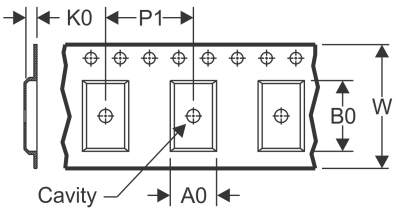
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

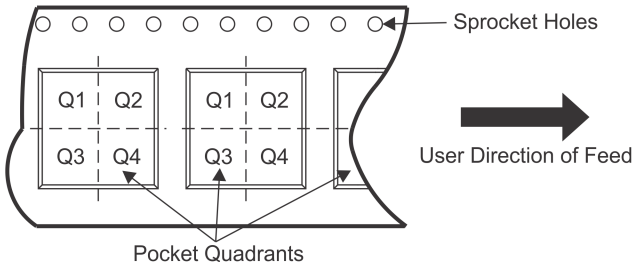


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

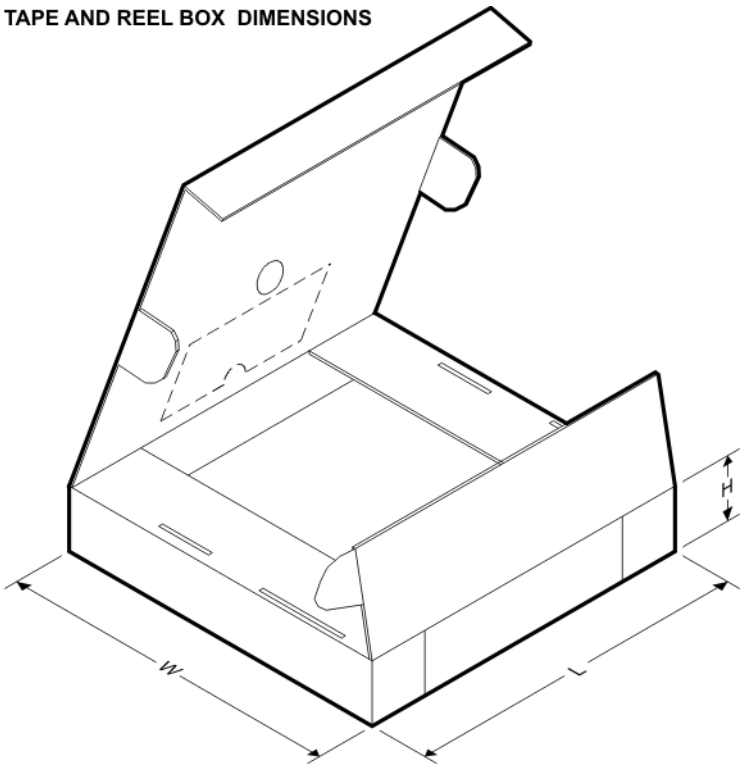
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TS3DV416DGGR	TSSOP	DGG	48	2000	330.0	24.4	8.6	13.0	1.8	12.0	24.0	Q1
TS3DV416DGVR	TVSOP	DGV	48	2000	330.0	16.4	7.1	10.2	1.6	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS

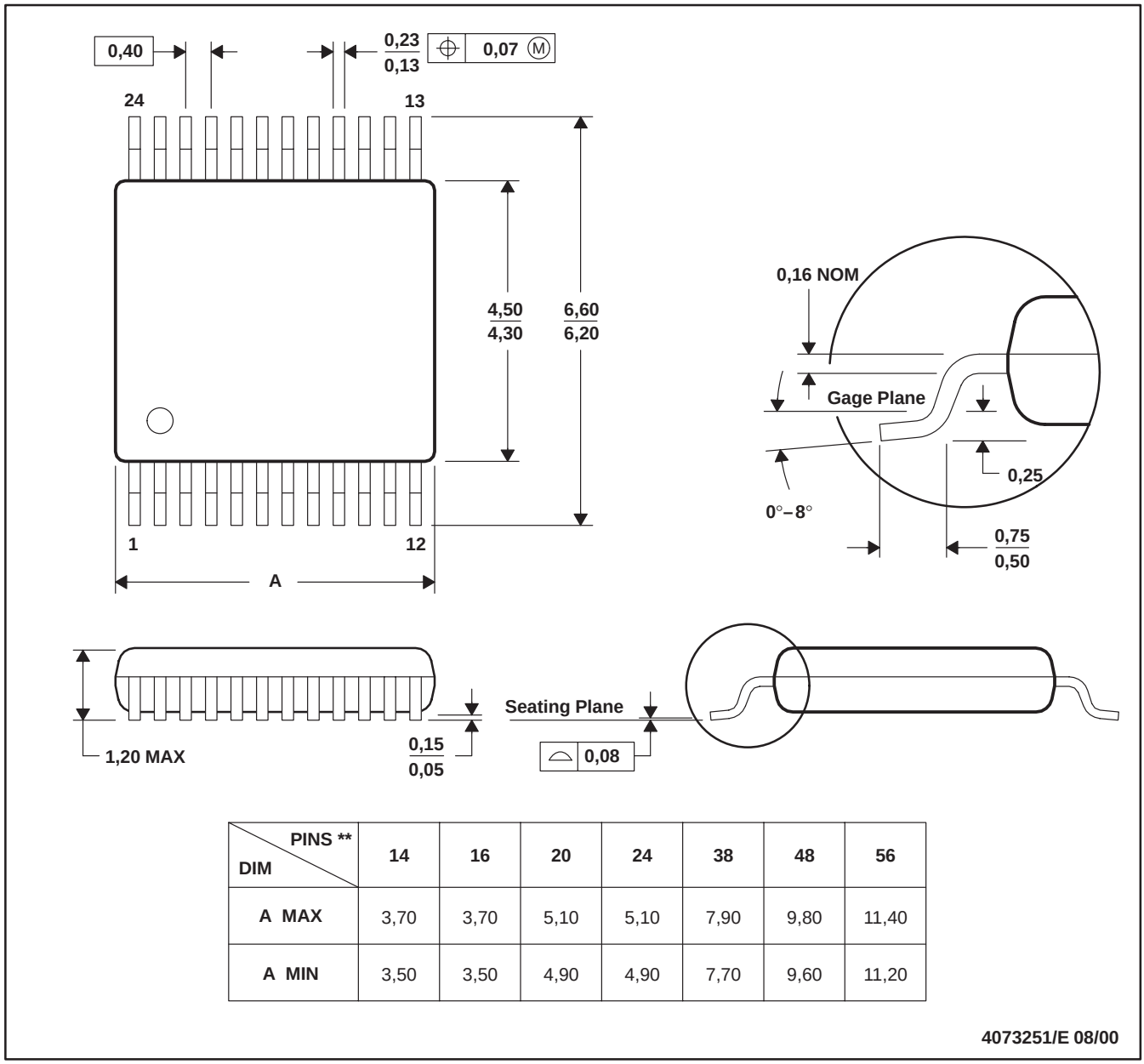


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TS3DV416DGGR	TSSOP	DGG	48	2000	367.0	367.0	45.0
TS3DV416DGVR	TVSOP	DGV	48	2000	367.0	367.0	38.0

DGV (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

24 PINS SHOWN



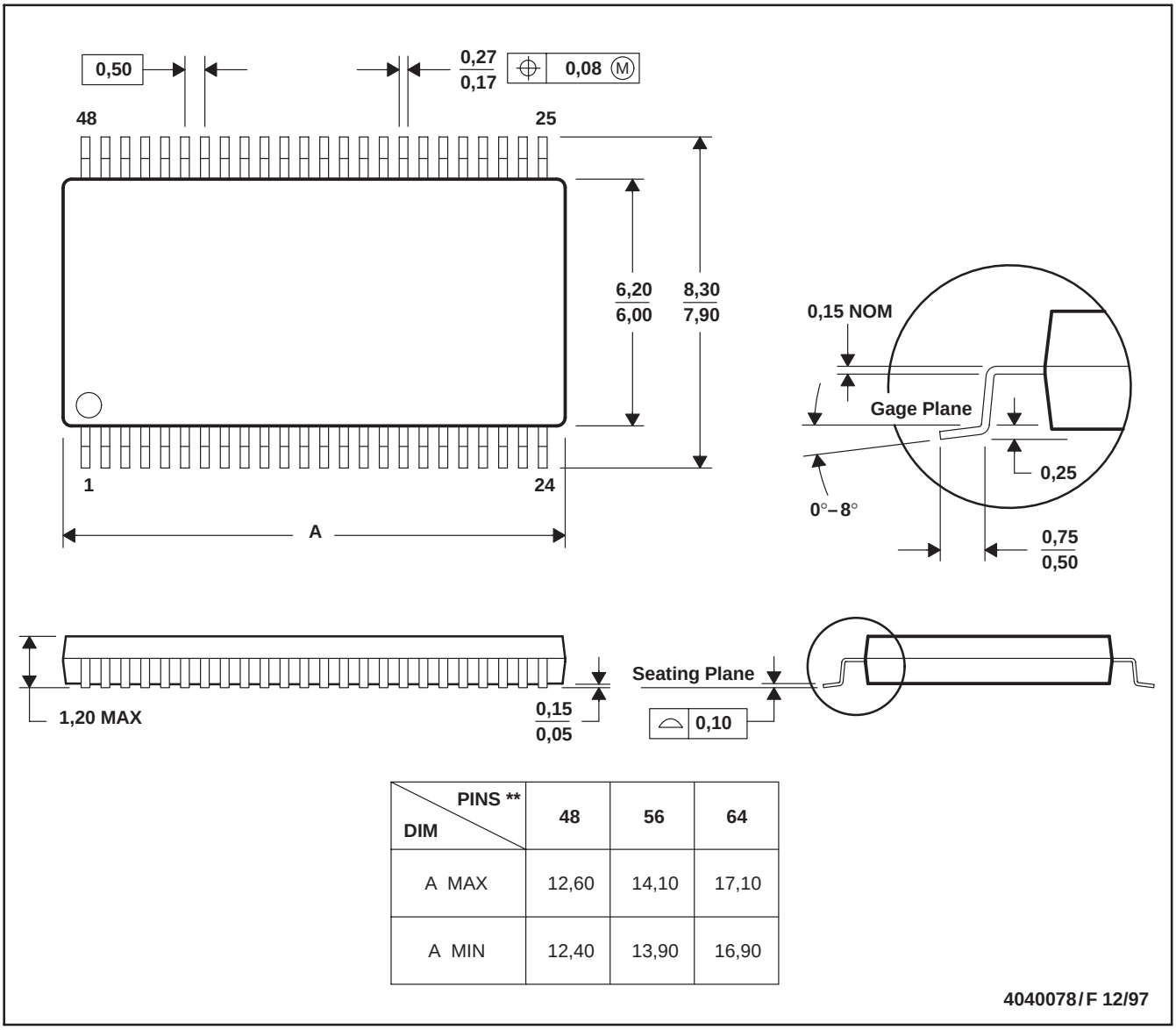
DIM \ PINS **	14	16	20	24	38	48	56
A MAX	3,70	3,70	5,10	5,10	7,90	9,80	11,40
A MIN	3,50	3,50	4,90	4,90	7,70	9,60	11,20

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NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
D. Falls within JEDEC: 24/48 Pins – MO-153
14/16/20/56 Pins – MO-194

DGG (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

48 PINS SHOWN



DIM \ PINS **	48	56	64
A MAX	12,60	14,10	17,10
A MIN	12,40	13,90	16,90

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

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