MICRF500

700MHz to 1.1GHz RadioWire™ RF Transceiver

Final

General Description

The MICRF500 is a single chip UHF transceiver designed for spread spectrum communication (FHSS) intended for ISM (Industrial, Scientific and Medical) and SRD (Short Range Device) frequency bands from 700MHz to 1100MHz with FSK data rates up to 128k baud.

The transmitter consists of a PLL frequency synthesizer and a power amplifier. The frequency synthesizer consists of a voltage-controlled oscillator (VCO), a crystal oscillator, dual-modulus prescaler, programmable frequency dividers and a phase-detector. The loop filter is external for flexibility and can be a simple passive circuit. The VCO is a Colpitts oscillator which requires an external resonator and varactor. FSK modulation can be applied externally to the VCO. The synthesizer has two different N, M and A frequency dividers. FSK modulation can also be implemented by switching between these dividers (max. 2400bps). The lengths of the N and M and A registers are 12, 10 and 6 bits respectively. For all types of FSK modulation, data is entered at the DATAIXO pin (see application circuit). The output power of the power amplifier can be programmed to eight levels. A lock detect circuit detects when the PLL is in lock.

In receive mode the PLL synthesizer generates the local oscillator (LO) signal. The N, M and A values that give the LO frequency are stored in the N0, M0 and A0 registers. The receiver is a zero intermediate frequency (IF) type in order to make channel filtering possible with low-power integrated low-pass filters. The receiver consists of a low-noise amplifier (LNA) that drives a quadrature mixer pair. The mixer outputs feed two identical signal channels in phase quadrature. Each channel includes a preamplifier, a third order Sallen-Key RC low pass filter that protects the following gyrator filter from strong adjacent channel signals and finally, a limiter. The main channel filter is a gyrator capacitor implementation of a seven-pole elliptic low pass filter. The elliptic filter minimizes the total capacitance required for a given selectivity and dynamic range. The cut-off frequency of the Sallen-Key RC filter can be programmed to four different frequencies: 10kHz, 30kHz, 60kHz and 200kHz. An external resistor adjusts the cut-off frequency of the gyrator filter. The demodulator demodulates the I and Q channel outputs and produces a digital data output. It detects the relative phase of the I and the Q channel signal. If the I channel signal lags the Q channel, the FSK tone frequency lies above the LO frequency (data '1'). If the I channel leads the Q channel, the FSK tone lies below the LO frequency (data '0'). The output of the receiver is available on the DATAIXO pin. A RSSI (Receive Signal Strength Indicator) circuit indicates the received signal level.



RadioWire™

A two pin serial interface is used to program the circuit.

External components are necessary for RF input and output impedance matching and decoupling of power. Other external components are the VCO resonator circuit with varactor, crystal, feedback capacitors and components for FSK modulation with the VCO, loop filter, bias resistors for the power amplifier and gyrator filters. A T/R switch can be implemented with 2-pin diodes. This gives maximum input sensitivity and transmit output power.

Features

- Frequency range: 700MHz to 1100MHz
- Modulation: FSK
- RF output power: 10dBm
- Sensitivity (19.2k bauds, BER=10^{-3}): –104dBm
- Maximum data rate: 128k bauds

Applications

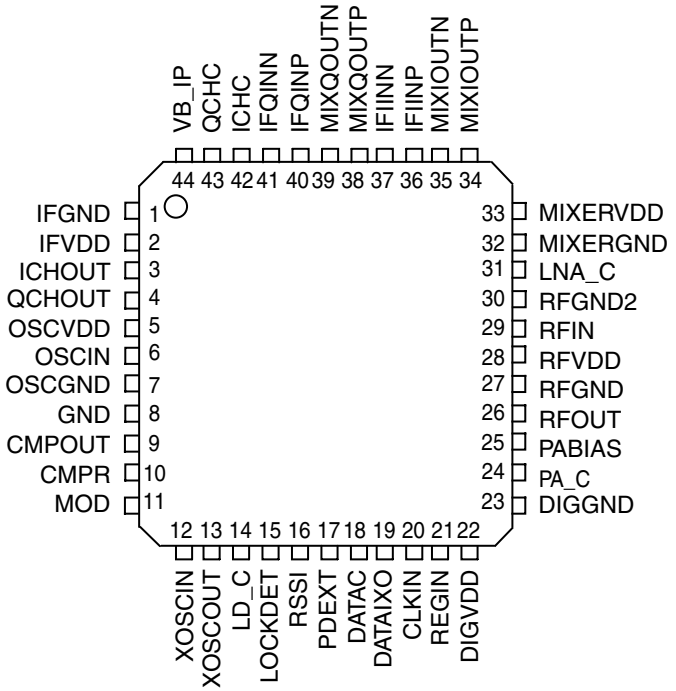
- Telemetry
- Remote metering
- Wireless controller
- Wireless data repeaters
- Remote control systems
- Wireless modem
- Wireless security system

Ordering Information

Part Number	Ambient Temp. Range	Package
MICRF500BLQ	–40°C to +85°C	44-Lead LQFP

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Pin Configuration



44-Pin LQFP (BLQ)

Pin Description

Pin Number	Pin Name	Pin Function
1	IFGND	IF Ground
2	IFVDD	IF Power
3	ICHOUT	I-Channel Output
4	QCHOUT	Q-Channel Output
5	OSCVDD	Colpitts Oscillator Power
6	OSCIN	Colpitts Oscillator Input
7	OSCGND	Colpitts Oscillator and Substrate Ground
8	GND	Substrate Ground
9	CMPOUT	Charge Pump Output
10	CMPR	Charge Pump Resistor Input
11	MOD	Output for VCO Modulation
12	XOSCIN	Crystal Oscillator Input
13	XOSCOUT	Crystal Oscillator Output
14	LD_C	External Capacitor for Lock Detector
15	LOCKDET	Lock Detector Output
16	RSSI	Received Signal Strength Indicator Output
17	PDEXT	Power Down Input (0=Power Down)
18	DATAC	Data Filter Capacitor
19	DATAIXO	Data Input/Output
20	CLKIN	Clock Input for Programming
21	REGIN	Data Input for Programming
22	DIGVDD	Digital Circuitry Power
23	DIGGND	Digital Circuitry Ground

Pin Description, cont't

Pin Number	Pin Name	Pin Function
24	PA_C	Capacitor for Slow Ramp Up/Down of PA
25	PABIAS	External Bias Resistor for Power Amplifier
26	RFOUT	Power Amplifier Output
27	RFGND	LNA, PA and Substrate Ground
28	RFVDD	LNA and PA Power
29	RFIN	Low Noise RF Amplifier (LNA) Input
30	RFGND2	LNA First Stage Ground
31	LNA_C	External LNA Stabilizing Capacitor
32	MIXERGND	Mixer Ground
33	MIXERVDD	Mixer Power
34	MIXIOUTP	I-Channel Mixer Positive Output
35	MIXIOUTN	I-Channel Mixer Negative Output
36	IFIINP	I-Channel IF Amplifier Positive Input
37	IFIINN	I-Channel IF Amplifier Negative Input
38	MIXQOUTP	Q-Channel Mixer Positive Output
39	MIXQOUTN	Q-Channel Mixer Negative Output
40	IFQINP	Q-Channel IF Amplifier Positive Input
41	IFQINN	Q-Channel IF Amplifier Negative Input
42	ICHC	I-Channel Amplifier Capacitor
43	QCHC	Q-Channel Amplifier Capacitor
44	VB_IP	Gyrator Filter Resistor

Absolute Maximum Ratings (Note 1)

Maximum Supply Voltage (V_{DD}) ..... +7V
Maximum NPN Reverse Base-Emitter Voltage ..... +2.5V
Storage Temperature Range (T_S) ..... –55°C to +150°C
ESD Rating, **Note 3** 500V

Operating Ratings (Note 2)

Supply Voltage (V_{IN}) ..... +2.5V to +3.4V
Ambient Temperature (T_A) ..... –40°C to +85°C
Package Thermal Resistance
TQFP(θ_{JA})-Multilayer board ..... 46.3°C/W

Electrical Characteristics

F_{REF} = 850MHz, V_{DD} = 2.5 to 3.4V, T_A = 25°C, unless otherwise specified.

Parameter	Condition	Min	Typ	Max	Units
Overall					
Operating Frequency		700	850	1100	MHz
Power Down Current			< 1	2	µA
Logic High Input, V_{IH}		70%			V_{DD}
Logic Low Input, V_{IL}				30%	V_{DD}
DATAIXO, Logic High Output (V_{OH})	I_{OH} = –500µA	V_{DD}-0.3			V
DATAIXO, Logic Low Output (V_{OL})	I_{OL} = 500µA			0.3	V
LockDet, Logic High Output (V_{OH})	I_{OH} = –100µA	V_{DD}-0.25			V
LockDet, Logic Low Output (V_{OL})	I_{OL} = 100µA			0.25	V
Clock/Data Frequency				10	MHz
Clock/Data Duty-Cycle		25		75	%
Data Setup to Clock (rising edge)		25			ns
VCO and PLL Section					
Prescaler Divide Ratio			64/65		
Reference Frequency				40	MHz
PLL Lock Time (int. modulation)	4kHz loop filter bandwidth		1		ms
PLL Lock Time (ext. modulation)	1kHz loop filter bandwidth		4		ms
Rx – (Tx with PA on) Switch Time	1kHz loop filter bandwidth		2.5		ms
Charge Pump Current		±95/±380	±125/±500	±155/±620	µA
Transmit Section	f_{OUT} = 850MHz				
Output Power	R_{LOAD} = 50Ω, V_{DD} = 3.0V		10		dBm
Transmit Data Rate (ext. modulation) **Note 4**			19.2	128	kbauds
Transmit Data Rate (int. modulation) **Note 5**				2.4	kbauds
Frequency Deviation to Modulation Rate Ratio	unfiltered FSK	1.0	1.5		
Current Consumption Transmit Mode	10 dBm, R_{LOAD} = 50Ω		50		mA

Parameter	Condition	Min	Typ	Max	Units
Receive Section	f_{IN} = 850MHz				
Receiver Sensitivity **(Note 6)**	BER=10^{-3}		–104[6]		dBm
Input 1dB Compression Level			–34		dBm
Input IP3			–24		dBm
Input Impedance			22.5-j28.5		W
RSSI Dynamic Range			60		dB
RSSI Output Voltage	P_{IN} = –100dBm P_{IN} = –30dBm		0.7 2.1		V V
Adjacent Channel Rejection: f_C = 10kHz f_C = 30kHz f_C = 60kHz f_C = 200kHz	 25kHz channel spacing 100kHz channel spacing 200kHz channel spacing 700kHz channel spacing		 26 37 45 48		 dB dB dB dB
Blocking Immunity (1MHz)	RC filter: f_C = 10kHz RC filter: f_C = 30kHz RC filter: f_C = 60kHz RC filter: f_C = 200kHz		66 61 59 53		dB dB dB
Maximum Receiver Bandwidth				175	kHz
Receiver Settling Time			1		ms
Current Consumption Receive Mode	gyrator filter f_C = 60kHz		12		mA
Current Consumption XCO			300		µA

Note 1. Exceeding the absolute maximum rating may damage the device.

Note 2. The device is not guaranteed to function outside its operating rating.

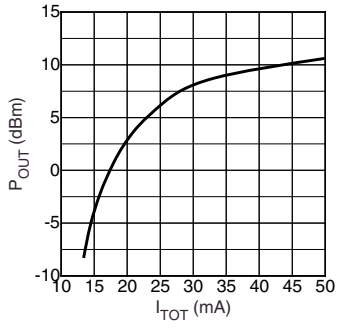
Note 3. Devices are ESD sensitive. Handling precautions recommended. Human body model, 1.5k in series with 100pF.

Note 4. Modulation is applied to the VCO and therefore the modulation cannot have any DC component. Some kind of coding is needed to ensure that the modulation is DC free, e.g., Manchester code or block code. With Manchester code the bitrate is half the baudrate, but with 3B4B block code the bitrate is $^3/_4$ of the baudrate.

Note 5: Bitrate is the same as the baudrate.

Note 6: Measured at 19.2k bauds and frequency deviation ±25kHz (external modulation), jitter of received data: < 45%.

Output Power vs. Current @ 25°C



Functional Diagram

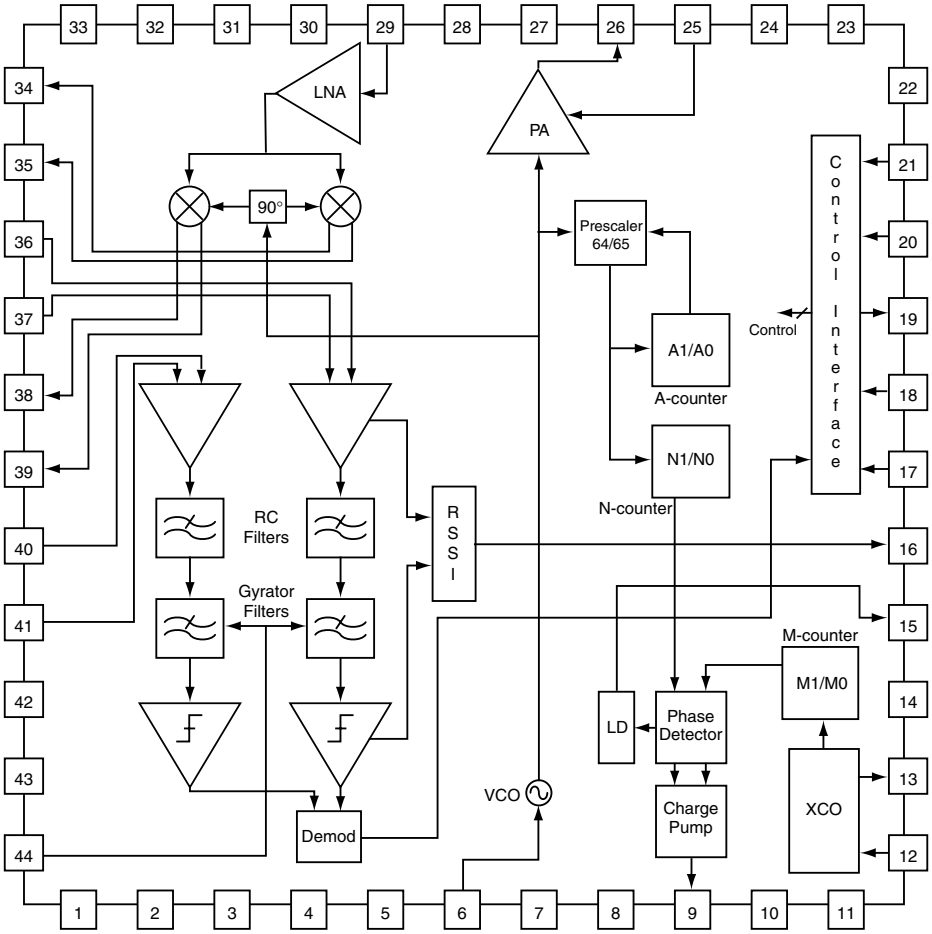


Figure 1. Transceiver Internal Blocks

Typical Application

Figure 2 shows an example of a transceiver with modulation applied to the VCO. The VCO and matching components are optimized for 915MHz, 120kbps data rate. The inductors and trimming capacitors must have a good high frequency performance.

The varactor SMV1215-011 is a single variable capacitance diode manufactured by Skyworks Solutions (formerly Alpha Industries). The pin diode SMP1320 is also manufactured by Skyworks Solutions.

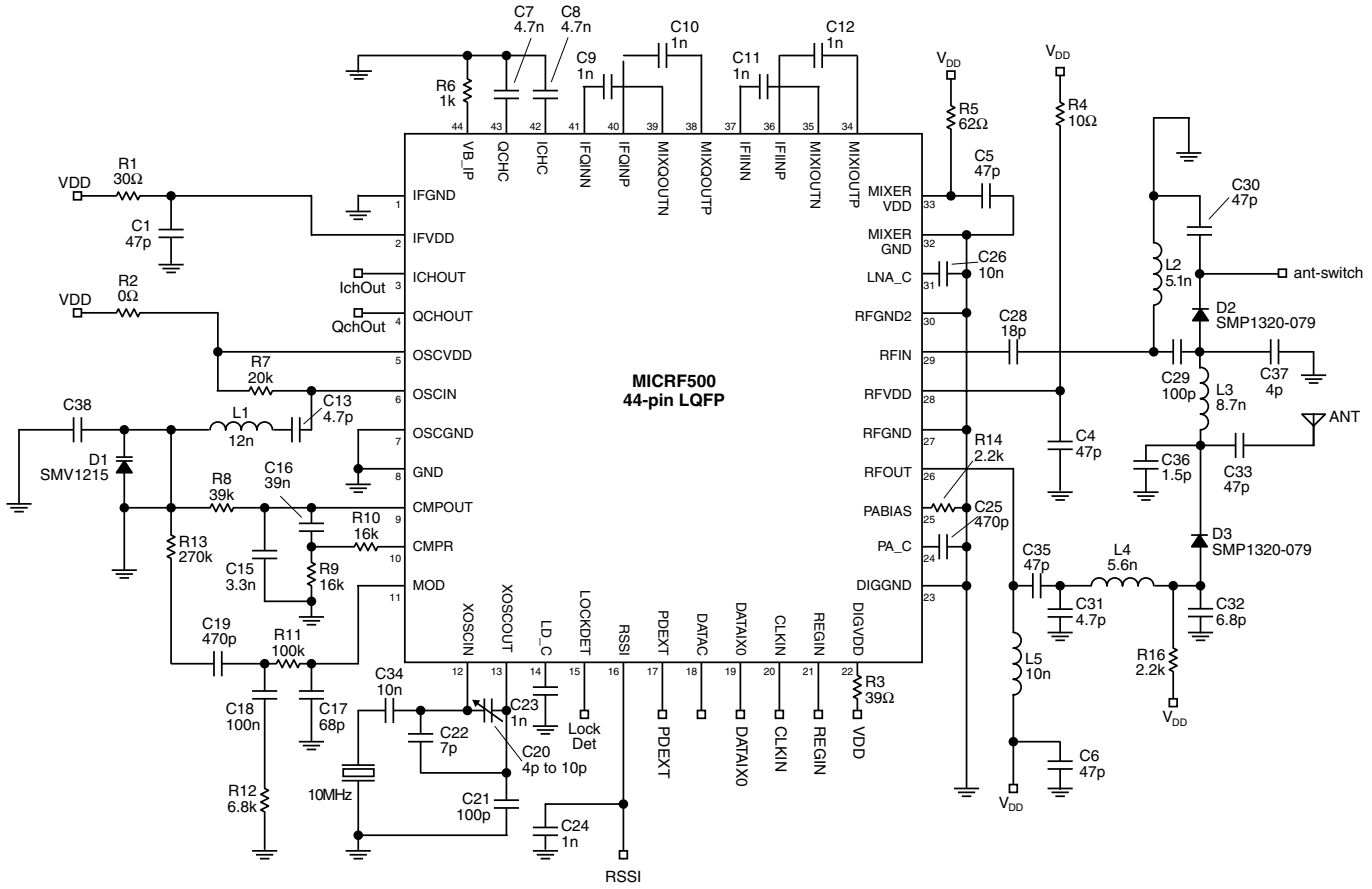


Figure 2. Application Circuit - Optimized for 915MHz. 120kbps

List of components

Component	Values	Component	Values	Component	Values
R1	30Ω	C8	4.7nF	C30	47pF
R2	0Ω	C9	1nF	C31	5.6pF
R3	39Ω	C10	1nF	C32	6.8pF
R4	10Ω	C11	1nF	C33	47pF
R5	62Ω	C12	1nF	C34	10µF
R6	1kΩ	C13	4.7pF	C35	47pF
R7	20kΩ	C15	3.3nF	C36	1.5pF
R8	39kΩ	C16	39nF	C37	4pF
R9	16kΩ	C17	68pF	C38	(np)
R10	16kΩ	C18	100nF	L1	12nH
R11	100kΩ	C19	470pF	L2	5.1nH
R12	6.8kΩ	C20	4pF-100pF	L3	8.7nH
R13	270kΩ	C21	100pF	L4	5.6nH
R14	2.2kΩ	C22	7pF	L5	10nH
R16	2.2kΩ	C23	1nF	D1	SMV1215-011
C1	47pF	C24	1nF	D2	SMP1320-079
C4	47pF	C25	470pF	D3	SMP1320-079
C5	47pF	C26	10nF	crystal	10MHz
C6	47pF	C28	18pF		
C7	4.7nF	C29	100pF		

Applications Information

VCO and PLL Section

The frequency synthesizer consists of a VCO, crystal oscillator, dual-modulus prescaler, programmable frequency dividers, phase-detector, charge pump, lock detector and an external loop filter. The dual-modulus prescaler divides the VCO-frequency by 64/65. This mode is controlled by the A-divider. There are two sets of M, N and A-frequency dividers. Using both sets in transmit mode, FSK can be implemented by switching between those two sets. The phase-detector is a frequency/phase detector with back slash pulses to minimize phase noise. The VCO, crystal oscillator, charge pump, lock detector and the loop filter will be described in detail below.

Voltage Controlled Oscillator (VCO)

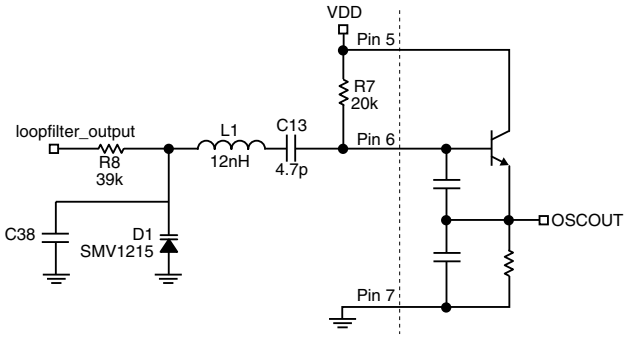


Figure 3. VCO

The circuit schematic of the VCO with external components is shown in Figure 3. The VCO is basically a Colpitts oscillator. The oscillator has an external resonator and varactor.

The resonator consists of inductor L1 and the series connection of capacitor C13, the internal capacitance and the capacitance of the varactor. The capacitance of the varactor (D1) decreases as the input voltage increases. The VCO frequency will therefore increase as the input voltage increases. The VCO has a positive gain (MHz/Volt). If necessary a parallel capacitor can be added next to D1 to bring the VCO tuning voltage to its middle range or VDD/2, which is measured at Pin 9 - CMPOUT.

If the value of capacitor C13 becomes too small the amplitude of the VCO signal decreases, which leads to lower output power.

The layout of the VCO is very critical. The external components should be placed as close to the input pin (Pin 6) as possible. The anode of D1 must be placed next to Pins 7 and 8 in the PCB layout. Ground vias should be next to component pads.

Crystal Oscillator

The crystal oscillator is the reference for the RF output frequency as well as for the LO frequency in the receiver. The crystal oscillator is a very critical block since very good phase and frequency stability is required. The schematic of the crystal oscillator with external components for 10MHz is shown in Figure 4. These components are optimized for a crystal with 15pF load capacitance.

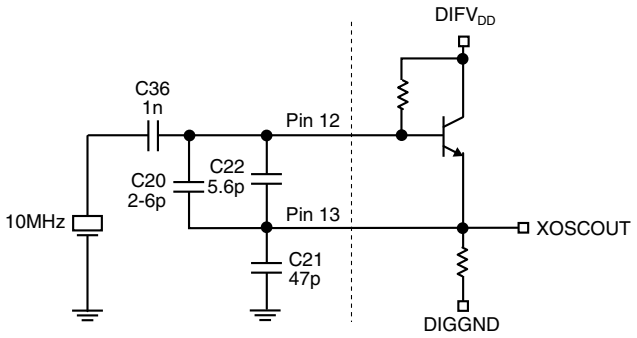


Figure 4. Crystal Oscillator

The crystal oscillator is tuned by varying the trimming capacitor C20. The drift of the RF frequency is the same as the drift of crystal frequency when measured in ppm. The total difference in ppm, $\Delta f(ppm)$, between the tuned RF frequency and the drifted frequency is given by:

$$\Delta f(ppm) = S_T \times \Delta T + n \times \Delta t$$

where:

- S_T is the total temperature coefficient of the oscillator frequency (due to crystal and components) in ppm°C.
- ΔT is the change in temperature from room temperature, at which the crystal was tuned.
- n is the ageing in ppm/year.
- Δt is the time (in years) elapsed since the transceiver was last tuned.

The demodulator will not be able to decode data when $\Delta f(Hz) = \Delta f(ppm) \times f_{RF}$ is larger than the FSK frequency deviation. For small frequency deviations, the crystal should be pre-aged, and should have a small temperature coefficient. The circuit has been tested with a 10MHz crystal, but other crystal frequencies can be used as well.

Prestart of XCO

The start-up time of a crystal oscillator is typically some milliseconds. Therefore, to save current consumption, the MICRF500 circuit has been designed so that the XCO is turned on before any other circuit block. During start-up the XCO amplitude will eventually reach a sufficient level to trigger the M-counter. After counting two M-counter output pulses the rest of the circuit will be turned on. The current consumption during the prestart period is approximately 300µA.

Lock Detector

The MICRF500 circuit has a lock detector feature that indicates whether the PLL is in lock or not. A logic high on Pin 15 (LOCKDET) means that the PLL is in lock.

The phase detector output is converted into a voltage that is filtered by the external capacitor C23, connected to Pin 14, LDC. The resulting DC voltage is compared to a reference window set by bits Ref0 – Ref5. The reference window can be stepped up/down linearly between 0V, Ref0 – Ref5 = 1, and Ref0 – Ref5 = 0, which gives the highest value (DC voltage) of the reference window. The size of the window can either be equal to two (Ref6 = 1) reference steps or four reference steps (Ref6 = 0).

The bit setting that corresponds to lock can vary, depending on temperature, loop filter and type of varactor. Therefore, the lock detect circuit needs to be calibrated regularly by a software routine that finds the correct bit setting, by running through all combinations of bits Ref0 – Ref5. Depending on the size of the reference window, there will be several bit combinations that show lock. For instance, with a large reference window, as much as five bit combinations can make the lock detector show lock. To have the maximum robustness to noise, the third of the bit settings should be chosen.

Charge Pump

The charge pump can be programmed to four different modes with two currents, ±125µA and ±500µA. Bit 70 and 71 in the control word (cpmp1 and cpmp0) controls the operation. The four modes are:

1. cpmp1 = 0, cpmp0 = 0: Current is constant ±125µA. Used in applications where short PLL lock time is not important.
2. cpmp1 = 0, cpmp0 = 1: Current is constant ±500µA. Used in applications where a short PLL lock time is important, e.g., internal modulation. See *"Modulation Inside PLL"* section.
3. cpmp1 = 1, cpmp0 = 0: Current is ±500µA when PLL is out of lock and ±125µA when it is in lock. Controlled by LOCKDET (Pin 15). Lock time is halved. See *"Modulation Outside PLL"* section.
4. cpmp1 = 1, cpmp0 = 1: Same as above in Tx. In Rx the current is ±500µA. Used when using dual-loop filters. See *"Modulation Outside PLL Dual-Loop Filters"* section.

Tuning of VCO and XCO

There are two circuit blocks that may need tuning, the VCO and the crystal oscillator.

VCO Tuning

When the VCO voltage is not at its mid-point, a capacitor may be added in parallel with D1or by small increments changes in the L1 or C13 values.

This is particularly important when using VCO modulation. The gain curve of the VCO (MHz/Volt) is not linear and the gain will therefore vary with loop voltage. This means that the FSK frequency deviation also varies with loop voltage.

When using internal modulation, tuning the VCO can be omitted as long as the VCO gain is large enough to allow the PLL to handle variations in process parameters and temperature without going out of lock.

XCO Tuning

Tune the trimming capacitor in the crystal oscillator to the precise desired transmit frequency. It is not possible to tune the crystal oscillator over a large frequency range. N, M and A values must therefore be chosen to give a RF frequency very close to the desired frequency. Because of the small tuning range the VCO will not go out of lock when tuning the crystal oscillator.

FSK Modulation

The circuit has two sets of frequency dividers A0, N0, M0 and A1, N1, M1. The frequency dividers are programmed via the control word. A0, N0, M0 are to be programmed with the receive frequency and are used in receive mode. There are three ways of implementing FSK:

- FSK modulation can be applied to the VCO. This way of implementing FSK modulation is explained more in detail in the next section. The values corresponding to the transmit frequency should be programmed in dividers A1, N1 and M1. Pin DATAIXO **must** be kept in tri-state from the time Tx-mode is entered until one starts sending data.
- FSK modulation by switching between the two sets of A, N and M dividers. A, N and M values corresponding to the receive frequency and both transmit frequencies have to be found. In transmit the values corresponding to data '0' should be programmed in dividers A0, N0 and M0, and the values corresponding to data '1' should be programmed in dividers A1, N1 and M1.
- FSK modulation by adding/subtracting 1 to divider A1. The frequency deviation will be equal to the comparison frequency. The values corresponding to the transmit frequency should be programmed in dividers A1, N1 and M1.

For all types of FSK modulation, data is entered at the DATAIXO pin.

Loop Filter

The design of the loop filter is of great importance for optimizing parameters like modulation rate, PLL lock time, bandwidth and phase noise. Low bitrates will allow modulation inside the PLL, which means the loop will lock on different frequency for 1s and 0s. This can be implemented by switching the internal dividers (M, N and A).

Higher modulation rates (above 2400bps) imply implementation of modulation outside the PLL. This can be implemented by applying the modulation directly to the VCO.

Loop filter values can be found using an appropriate software program.

Modulation Inside PLL

A fast PLL requires a loop filter with relatively high bandwidth. If a second order loop filter is chosen, it may not give adequate attenuation of the comparison frequency. Therefore in the following example a third order loop filter is chosen.

Example 1:

Radio frequency	f_{RF}	868MHz
Comparison frequency	f_C	100kHz
Loop bandwidth	BW	3.8kHz
VCO gain	K_o	30MHz/V
Phase comparator gain	K_d	500µA/rad
Phase margin	j	62°
Breakthrough suppression	A	20dB

The component values will be:

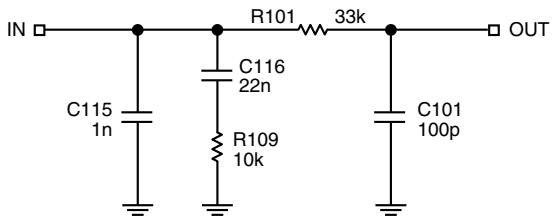


Figure 5. Third Order Loop Filter

With this loop filter, internal modulation up to 2400bps is possible. The PLL lock time from power-down to Rx will be approximately 1ms.

Modulation Outside PLL (Closed Loop)

When modulation is applied outside the PLL, it means that the PLL should not track the changes in the loop due to the modulation signal. A loop filter with relatively low bandwidth is therefore necessary. The exact bandwidth will depend on the actual modulation rate. Because the loop bandwidth will be significantly lower than the comparison frequency, a second order loop filter will normally give adequate attenuation of the comparison frequency. If not, a third order loop filter may give the extra attenuation needed.

Example 2:

Radio frequency	f_{RF}	868MHz
Comparison frequency	f_C	140kHz
Loop bandwidth	BW	900Hz
VCO gain	K_o	30MHz/V
Phase comparator gain	K_d	125µA/rad
Phase margin	j	61°

The component values will be:

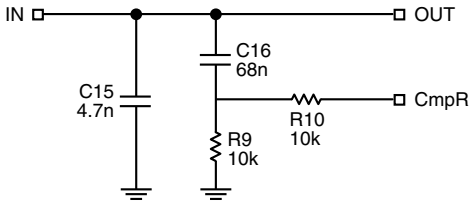


Figure 6. Second Order Loop Filter

Data rates above approximately 19200baud (including Manchester coding) can be used with this loop filter without significant tracking of the modulating signal. PLL lock time will be approximately 4ms.

If a faster PLL lock time is wanted, the charge pump can be made to deliver a current of 500µA per unit phase error, while an open drain NMOS on chip (Pin 10, CmpR) switches in a second damping resistor (R10) to ground as shown in Figure 6. Once locked on the correct frequency, the PLL automatically returns to standard low noise operation (charge pump current: 125µA/rad). If correct settings have been made in the control word (cpmp1 = 1, cpmp0 = 0), the fast locking feature is activated and will reduce PLL lock time by a factor of two without affecting the phase margin in the loop.

Components C17, C18 C19, R11, R12 and R13 (see application circuit) are necessary if FSK modulation is applied to the VCO. Data entered at the DATAIXO pin will then be fed through the Mod pin (Pin 11) which is a current output. The pin sources a current of 50µA when Logic 1 is entered at the DATAIXO and drains the current for Logic 0. The capacitance of C17 will set the order of filtering of the baseband signal. A large capacitance will give a slow ramp-up and therefore a high order of filtering of the baseband signal, while a small capacitance gives a fast ramp-up, which in turn also gives a broader frequency spectrum. Resistors R11 and R12 set the frequency deviation. If C18 is large compared to C17, the frequency deviation will be large. R13 should be large to avoid influencing the loop filter. Pin DATAIXO **must** be kept in tri-state from the time Tx-mode is entered until one starts sending data.

Modulation Outside PLL, Dual-Loop Filters

Modulation outside the PLL requires a loop filter with a relatively low bandwidth compared to the modulation rate. This results in a relatively long loop lock time. In applications where modulation is applied to the VCO, but at the same time a short start-up time from power down to receive mode is needed, dual-loop filters can be implemented. Figure 7 shows how to implement dual-loop filters.

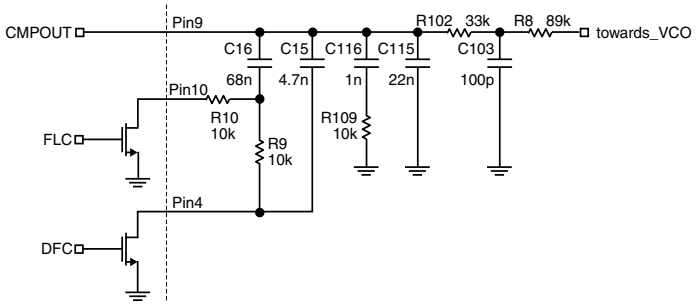


Figure 7. Dual-Loop Filters

The loop filter used in transmit mode is made up of C15, C16, R9 and R10. The fast lock feature is also included (internal NMOS controlled by FLC, Fast Lock Control). This filter is automatically switched in/out by an internal NMOS at Pin 4, QchOut, which is controlled by DFC (Dual Filter Control). Bits OutS2, OutS1, OutS0 must be set to 110. When QchOut is used to switch the Tx loop filter to ground, neither QchOut nor IchOut can be used as test pins to look at the different receiver signals. The receive mode loop filter comprises C115, C116, R109, R101 and C101.

Modulation Outside PLL (Open Loop)

In this mode the charge pump output is tri-stated. The loop is open and will therefore not track the modulation. This means that the loop filter can have a relatively high bandwidth, which give short switching times. However, the loop voltage will decrease with time due to current leakage. The transmit time will therefore be limited and is dependent on the bandwidth of the loop filter. High bandwidth gives low capacitor values and the loop voltage will decrease faster, which gives a shorter transmit time.

The loop is closed until the PLL is locked on the desired frequency and the power amplifier is turned on. The loop immediately opens when the modulation starts. The loop will not track the modulation, but the modulation still needs to be DC free due to the AC coupling in the modulation network.

Transmit

Power Amplifier (PA)

The power amplifier is biased in class AB. The last stage has an open collector, and an external load inductor (L2) is therefore necessary. The DC current in the amplifier is adjusted with an external bias resistor (R14). A good starting point when designing the PA is a 1.5kΩ bias resistor which gives a bias current of approximately 50µA. This will give a bias current in the last stage of about 15mA.

The impedance matching circuit will depend on the type of antenna used, but should be designed for maximum output power. For maximum output power the load seen by the PA must be resistive and should be about 100Ω. The output power is programmable in eight steps, with approximately 3dB between each step. This is controlled by bits Pa2 - Pa0.

To prevent spurious components from being transmitted the PA should be switched on/off slowly, by allowing the bias current to ramp up/down at a rate determined by the external capacitor C25 connected to Pin 24. The ramp up/down current is typically 1.1µA, which makes the on/off rate for a 3.0V power supply 2.6µs/pF. Turning the PA on/off affects the PLL. Therefore the on/off rate must be adjusted to the PLL bandwidth.

PA Buffer

A buffer amplifier is connected between the VCO and the PA to ensure that the input signal of the PA has sufficient amplitude to achieve the desired output power. This buffer can be bypassed by setting the bit Gc to 0.

Receive

Front End (LNA and Mixers)

A low noise amplifier in RF receivers is used to boost the incoming signal prior to the frequency conversion process. This is important in order to prevent mixer noise from dominating the overall front end noise performance. The LNA is a two-stage amplifier and has a nominal gain of 23dB at 900MHz. The LNA has a dc feedback loop, which provides bias for the LNA. The external capacitor C26 decouples and stabilizes the overall dc feedback loop, which has a large low frequency loop gain. Figure 8 shows the input impedance of the LNA. Input matching is very important to get high receive sensitivity.

The LNA can be bypassed by setting bit ByLNA to '1'. This is useful for very strong signal levels.

The RSSI signal can be used to drive a microcontroller in a way when a strong RF income signal is present the LNA can be bypassed. This will increase the dynamic range by approximately 25dB.

The mixers have a gain of about 12dB at 900MHz. The differential outputs of the mixers are available at Pins 34, 35 and at Pins 38, 39. The output impedance of each mixer is about 15kΩ.

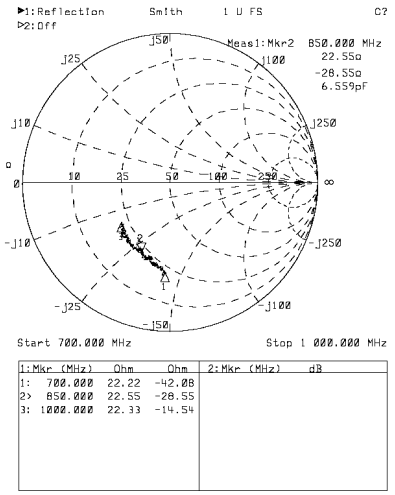


Figure 8. Input Impedance

Sallen-Key Filter and Preamplifier

Each channel includes a preamplifier and a prefilter, which is a three-pole elliptic Sallen-Key low pass filter with 20dB stopband attenuation. It protects the following gyrator filter from strong adjacent channel signals. The preamplifier has a gain of 20dB when bit Gc = 0 and 30dB when bit Gc = 1. The output voltage swing is about $200mV_{PP}$ for the 30dB gain setting and $1V_{PP}$ for the 20dB gain setting.

The third order Sallen-Key low pass filter is programmable to four different cut-off frequencies according to the table below:

Fc1	Fc0	Cut-Off Frequency (kHz)	Recommended Channel Spacing
0	0	10 ±2.5	25kHz
0	1	30 ±7.5	100kHz
1	0	60 ±15	200kHz
1	1	200 ±50	700kHz

For the 10kHz cut-off frequency the first pole must be generated externally by connecting a 820pF capacitor between the outputs of each mixer. For the 30kHz cut-off frequency a 68pF capacitor is needed between the outputs.

As the cut-off frequency of the gyrator filter can be set by varying an external resistor, the optimum channel spacing will depend on the cut-off frequencies of the Sallen-Key filter. The table above shows the recommended channel spacing depending on the different bit settings.

Gyrator Filter

The main channel filter is a gyrator capacitor implementation of a seven-pole elliptic low pass filter. The elliptic filter minimizes the total capacitance required for a given selectivity and dynamic range. An external resistor can adjust the cut-off frequency of the gyrator filter. The following table shows how the cut-off frequency varies with bias resistor:

Bias Resistor (kΩ)	Cut-Off Frequency (kHz)
2.2	175
6.8	70
8.2	55
15	30
30	14
47	8

The gyrator filter cut-off frequency should be chosen to be approximately the same as the cut-off frequency of the Sallen-Key filter. The maximum cut-off frequency of the gyrator filter is 175kHz.

Cut-Off Frequency Setting

The cut-off frequency must be high enough to pass the received signal (frequency deviation + modulation). The minimum cut-off frequency is given by:

$$f_{C(min)} = f_{DEV} + Baudrate/2$$

For a frequency deviation of f_{DEV} = 30kHz and a baudrate of 20k baud, the minimum cut-off frequency is 40kHz. Bit setting Fc1 = 1 and Fc0 = 0, which gives a cut-off of (60 ±15) kHz, would be the best choice. The gyrator filter bias resistor should therefore be 7.5kΩ or 8.2 kΩ, to set the gyrator filter cut-off frequency to approximately 60kHz.

The crystal tolerance must also be taken into account when selecting the receiver bandwidth. If the crystal has a temperature tolerance of say ±10ppm over the total temperature range, the incoming RF signal and the LO signal can theoretically be 20ppm away from each other.

The frequency deviation must always be larger than the maximum frequency drift for the demodulator to be able to demodulate the signal. The minimum frequency deviation (f_{DEVmin}) is equal to the baudrate, according to the specification on page 2. **This means that the frequency deviation has to be at least equal to the baudrate plus the maximum frequency drift.**

The frequency deviation may therefore vary from the minimum frequency deviation to the minimum frequency deviation plus two times the maximum frequency drift. The minimum cut-off frequency when crystal tolerances are considered is therefore given by:

$$f_{Cmin} = \Delta f \times 2\, f_{DEVmin} + Baudrate/2$$

where Δf is the maximum frequency drift between the LO signal and the incoming RF signal due to crystal tolerances.

A frequency drift of 20ppm is 8680Hz at 434MHz. The frequency deviation must be higher than 28.68kHz for a baudrate of 20k baud. The frequency deviation may then vary from 20kHz, when the RF signal is 20ppm lower than the LO signal; to 37.36kHz when the RF signal is 20ppm higher than the LO signal. The minimum cut-off frequency is tûeref•re 47.36kHz.

Limiter

The limiter serves as a zero crossing detector, thus removing amplitude variations in the IF signal, while retaining only the phase variations. The limiter outputs are ideally suited to measure the I-Q phase difference, since its outputs are square waves with sharp edges.

Demodulator

The demodulator demodulates the I and Q channel outputs and produces a digital data output. It detects the relative phase difference between the I and the Q channel signals. For every edge (positive and negative) of the I channel limiter output, the amplitude of the Q channel limiter output is sampled, and vice versa. The output of the demodulator is available on the DATAIXO pin. The data output is therefore updated 4 times per cycle of the IF signal. This also means that the maximum jitter of the data output is 1/(4×Δf) (valid only for zero frequency offsets). If the I channel signal lags the Q channel, the FSK tone frequency lies above the LO frequency (data '1'). If the I channel leads the Q channel, the FSK tone lies below the LO frequency (data '0').

The inputs and the output of the demodulator are filtered by first order RC low pass filters and then amplified by Schmitt triggers to produce clean square waves.

It is recommended for low bitrates (<10kbps) that an additional capacitor is connected to Pin 18 (DataC) to decrease the bandwidth of the Rx data signal filter. The bandwidth of the filter must be adjusted for the bitrate. This functionality is controlled by bit RxFilt.

Received Signal Strength Indicator (RSSI)

The RSSI provides a DC output voltage proportional to the strength of the RF input signal. A graph of a typical RSSI response is shown in Figure 9 (f_{DEV} = 30kHz, Gc=1).

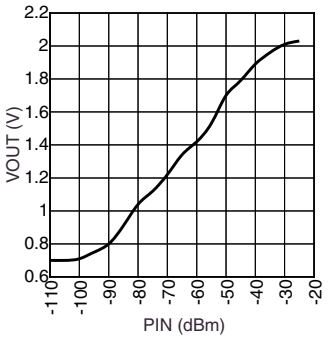


Figure 9. Typical RSSI Characteristics

This graph shows a range of 0.7V to 2.05V over a RF input range of 70dB.

The RSSI can be used as a signal presence indicator. When a RF signal is received, the RSSI output increases. This could be used to wake up circuitry that is normally in a sleep mode configuration to conserve battery life.

Another application for which the RSSI could be used is to determine if transmit power can be reduced in a system. If the RSSI detects a strong signal, it could tell the transmitter to reduce the transmit power to reduce current consumption.

Programming

A two-line bus is used to program the circuit; the two lines being CLKIN and REGIN. The 2-line serial bus interface allows control over the frequency dividers and the selective powering up of Tx, Rx and Synthesizer circuit blocks. The interface consists of an 80-bit programming register. Data is entered on the REGIN line with the most significant bit first. The first bit entered is called p1, the last one p80. The bits in the programming register are arranged as shown in Table 1.

p1 – p6	p7 - p12	p13 – p24	p25 – p36	p37 – p46	p47 – p56	p57	p58
A1	A0	N1	N0	M1	M0	RxFilt	Pa2
p59	p60	p61	p62	p63	p64	p65	p66
Pa1	Pa0	Gc	ByLNA	Ref6	Ref5	Ref4	Ref3
p67	p68	p69	p70	p71	p72	p73	p74
Ref2	Ref1	Ref0	Cpmp1	Cpmp0	Fc1	Fc0	OutS2
p75	p76	p77	p78	p79	p80	—	—
OutS1	OutS0	Mod1	Mod0	RT	Pu	—	—

Table 1. Bit Allocation

Name	Description
A1	frequency divider A1, 6 bits
A0	frequency divider A0, 6 bits
N1	frequency divider N1, 12 bits
N0	frequency divider N0, 12 bits
M1	frequency divider M1, 10 bits
M0	frequency divider M0, 10 bits
RxFilt	1=external capacitor for filtering of Rx data signal
Pa2	gain setting in power amplifier
Pa1	pa2, pa1, pa0 = 0 : lowest output power
Pa0	pa2, pa1, pa0 = 1 : highest output power
Gc	gain control in power amplifier buffer: 1=high gain gain control in preamplifier in receiver: 1=high gain
ByLNA	1 = the LNA is bypassed
Ref6	reference settings in lock detector all 0's: highest reference all 1's: lowest reference
Ref5	
Ref4	
Ref3	
Ref2	
Ref1	
Ref0	
Cpmp1	charge pump setting: Cpmp1=0, Cpmp0=0 : ±125µA Cpmp1=0, Cpmp0=1 : ±500µA Cpmp1=1, Cpmp0=0 : controlled by LockDet (LD) LD=0: ±500µA, LD=1: ±125µA Cpmp1=1, Cpmp0=1 : same as previous in Tx. In Rx the current is ±500µA.
Cpmp0	
Fc1	Active RC-filter settings Fc1=0, Fc0=0 : 10kHz Fc1=1, Fc0=0 : 60kHz Fc1=0, Fc0=1 : 30kHz Fc1=1, Fc0=1 : 200kHz
Fc0	
OutS2	I- and Q-channel output select sk:_*:Sallen-Key filter output, gm_*:gyrator filter output, lim_*:limiter output, *_div:frequency divider output (for testing). 110 is for dual-loop filter applications, see "Modulation Outside PLL, Dual-Loop Filters."
OutS1	
OutS0	
Mod1	Mod1 = 0, Mod0 = 0: FSK modulation can be applied to the VCO
Mod0	Mod1 = 0, Mod0 = 1: FSK modulation can be applied to the VCO: open loop modulation Mod1 = 1, Mod0 = 0: FSK modulation by switching between the two sets of dividers Mod1 = 1, Mod0 = 1: FSK modulation by adding/subtracting 1 to divider A1: $f_{deviation} = f_{comparison}$
RT	0 = receive mode 1 = transmit mode
Pu	1 = power up, 0 = power down (When Pu=1, power down is controlled by PuExt)

OutS2	OutS1	OutS0	IchOut	QchOut	OutS2	OutS1	OutS0	IchOut	QchOut
0	0	0	high Z	high Z	1	0	0	lim_qch	gm_qch
0	0	1	sk_ich	sk_qch	1	0	1	gm_ich	lim_ich
0	1	0	gm_ich	gm_qch	1	1	0	high Z	Dual LF
0	1	1	lim_ich	lim_qch	1	1	1	N_div	M_div

Table 2. Bit Description

When FSK modulation is applied to the VCO the PLL is using the dividers A1, N1 and M1. When Mod1 = 1 and Mod0 = 0 it is possible to switch between the different dividers in the PLL. DATAIXO controls the switching. When DATAIXO = 0 the PLL uses dividers A0, N0 and M0. When DATAIXO = 1 the PLL uses dividers A1, N1 and M1. Switching between the different dividers can be used to implement FSK modulation.

The N, M and A values can be calculated from the formula:

$$f_C = \frac{f_{XCO}}{M} = \frac{f_{RF}}{64 \times N + A}$$

where f_C is the comparison frequency.

The 80bit control word is first read into a shift-register, and is then loaded into a parallel register by a transition of the REGIN signal (positive or negative) when the CLKIN signal is high. The circuit then goes directly into the specified mode (receive, transmit, etc.).

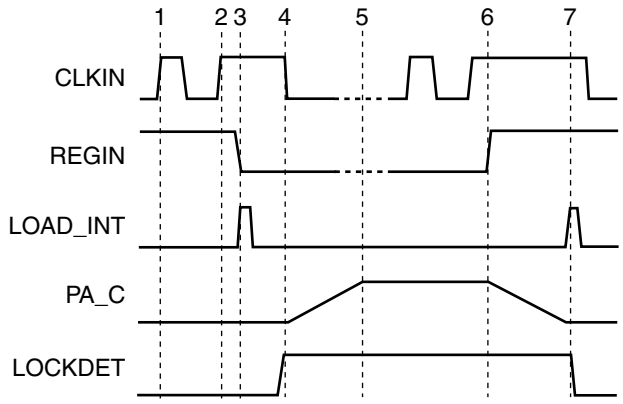


Figure 10. Timing of CLKIN, REGIN and the Internal LOAD_INT and PA_C Signals

1. The second last bit is clocked into the first shift register ('1').
2. The last bit is clocked into the first shift register ('1').
3. A transition on the REGIN signal generates an internal load pulse that loads the control word into the parallel register. The circuit enters the new mode (in this case Tx-mode). The circuit stabilizes in the new mode.
4. When the clock signal goes low, the power amplifier (PA) is turned on slowly in order to minimize spurious components on the RF output signal. To be sure the PLL is in lock before the PA is turned on, the PA should be turned on after LOCKDET has been set.
   The negative transition on the clock signal should come a minimum time of one period of the comparison frequency after the internal load pulse is generated.
5. The power amplifier is fully turned on.
6. A new control word is entered into the first register. A transition on the REGIN signal when CLKIN is high will now turn the power amplifier off.
7. When the power amplifier is turned off an internal load pulse is generated. The new control word is loaded into the parallel register and the circuit enters a new mode (in this case power down mode). CLKIN must go low after the internal load pulse is generated.

As long as transitions on REGIN are avoided when CLKIN is high, a new control word can be clocked into the first register any time without affecting the operation of the transceiver.

Example 1. f_{RF} = 869.0MHz, frequency deviation: ≈ ±10kHz, f_{XCO} = 10.00MHz. FSK modulation is implemented by switching between dividers.

	A1	A0	N1	N0	M1	M0
Tx	9	27	137	134	101	99
Rx	50	50	135	135	100	100
	RxFilt	Pa2	Pa1	Pa0	Gc	ByLNA
Tx	0	1	1	1	1	0
Rx	0	1	1	1	1	0
	Ref6	Ref5	Ref4	Ref3	Ref2	Ref1
Tx	0	0	0	0	0	0
Rx	0	0	0	0	0	0
	Ref0	Cpmp1	Cpmp0	Fc1	Fc0	OutS2
Tx	0	1	0	0	1	0
Rx	0	1	0	0	1	0
	OutS1	OutS0	Mod1	Mod0	RT	Pu
Tx	0	0	1	0	1	1
Rx	0	0	1	0	0	1

Binary form: (MSB to the left):

Tx: 001001 011011 000010001001
000010000110 0001100101 0001100011
011110000000001010001011

Rx: 110010 110010 000010000111
000010000111 0001100100 0001100100
010111100000000001010001001

When FSK modulation is implemented by switching between the different dividers A, N and M values corresponding to the receive frequency and both transmit frequencies have to be found.

Example 2. f_{RF} = 869.0MHz, f_{RF} = 10.00MHz. FSK modulation is applied to the VCO.

	A1	A0	N1	N0	M1	M0
Tx	50	50	135	135	100	100
Rx	50	50	135	135	100	100
	RxFilt	Pa2	Pa1	Pa0	Gc	ByLNA
Tx	0	1	1	1	1	0
Rx	0	1	1	1	1	0
	Ref6	Ref5	Ref4	Ref3	Ref2	Ref1
Tx	0	0	0	0	0	0
Rx	0	0	0	0	0	0
	Ref0	Cpmp1	Cpmp0	Fc1	Fc0	OutS2
Tx	0	0	1	1	0	0
Rx	0	0	1	1	0	0
	OutS1	OutS0	Mod1	Mod0	RT	Pu
Tx	0	0	0	0	1	1
Rx	0	0	0	0	0	1

Binary form: (MSB to the left):

Tx: 110010 110010 000010000111
000010000111 0001100100 0001100100
010111100000000010100000011

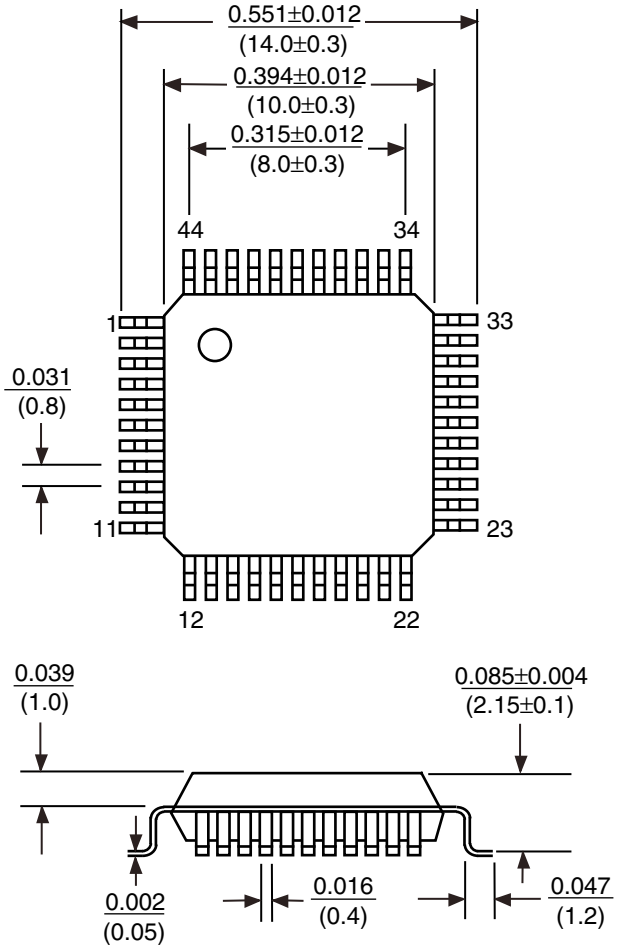
Rx: 111011 111011 000010001110
000010001110 0001101010 0001101010
010111100000000010100000001

With modulation applied to the VCO, A, N and M values corresponding to the receive frequency have to be found. The same set of A, N and M values are used in all modes.

Programming After Battery Reset

In order to ensure a successful programming after V_{DD} has been zero volts, the P_{DEXT} needs to be kept low during the first programming sequence. This can be done by a separate 110-line from a microcontroller, or a RC circuit on the P_{DEXT} pin to V_{DD} (A capcitor between P_{DEXT} and V_{DD}). Using the latter method, R and C values need to be chosen so that the voltage on the P_{DEXT} pin is lower than $V_{DD}/2$ when the controller word is loaded into the parallel register (see Figure 10).

Package Information



44-Pin LQFP (BLQ)

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