



ON Semiconductor®

FDMA3027PZ

Dual P-Channel PowerTrench® MOSFET

-30 V, -3.3 A, 87 mΩ

Features

- Max $r_{DS(on)}$ = 87 mΩ at $V_{GS} = -10$ V, $I_D = -3.3$ A
- Max $r_{DS(on)}$ = 152 mΩ at $V_{GS} = -4.5$ V, $I_D = -2.3$ A
- HBM ESD protection level > 2 KV typical (Note 3)
- Low profile - 0.8 mm maximum - in the new package MicroFET 2x2 mm
- RoHS Compliant

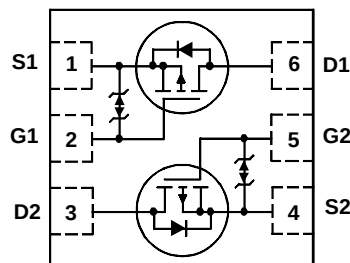
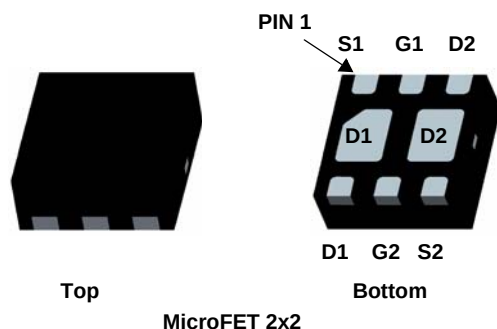


General Description

This device is designed specifically as a single package solution for dual switching requirements such as gate driver for larger Mosfets. It features two independent P-Channel MOSFETs with low on-state resistance for minimum conduction losses. The MicroFET 2x2 package offers exceptional thermal performance for its physical size and is well suited to linear mode applications. G-S zener has been added to enhance ESD voltage level.

Applications

- Load Switch
- Discrete Gate Driver



MOSFET Maximum Ratings $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Ratings	Units
V_{DS}	Drain to Source Voltage	-30	V
V_{GS}	Gate to Source Voltage	± 25	V
I_D	Drain Current -Continuous (Note 1a)	-3.3	A
	-Pulsed	-15	
P_D	Power Dissipation (Note 1a)	1.4	W
	Power Dissipation (Note 1b)	0.7	
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to +150	$^\circ\text{C}$

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance for Single Operation, Junction to Ambient (Note 1a)	86	$^\circ\text{C/W}$
	Thermal Resistance for Single Operation, Junction to Ambient (Note 1b)	173	
	Thermal Resistance for Dual Operation, Junction to Ambient (Note 1c)	69	
	Thermal Resistance for Dual Operation, Junction to Ambient (Note 1d)	151	
	Thermal Resistance for Single Operation, Junction to Ambient (Note 1e)	160	
	Thermal Resistance for Dual Operation, Junction to Ambient (Note 1f)	133	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
327	FDMA3027PZ	MicroFET 2X2	7 "	8 mm	3000 units

Electrical Characteristics $T_J = 25\text{ }^{\circ}\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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Off Characteristics

BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = -250\text{ }\mu\text{A}$, $V_{GS} = 0\text{ V}$	-30			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = -250\text{ }\mu\text{A}$, referenced to $25\text{ }^{\circ}\text{C}$		-22		mV/ $^{\circ}\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = -24\text{ V}$, $V_{GS} = 0\text{ V}$			-1	μA
I_{GSS}	Gate to Source Leakage Current	$V_{GS} = \pm 25\text{ V}$, $V_{DS} = 0\text{ V}$			± 10	μA

On Characteristics

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$, $I_D = -250\text{ }\mu\text{A}$	-1	-1.9	-3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = -250\text{ }\mu\text{A}$, referenced to $25\text{ }^{\circ}\text{C}$		5		mV/ $^{\circ}\text{C}$
$r_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = -10\text{ V}$, $I_D = -3.3\text{ A}$		69	87	m Ω
		$V_{GS} = -4.5\text{ V}$, $I_D = -2.3\text{ A}$		108	152	
		$V_{GS} = -10\text{ V}$, $I_D = -3.3\text{ A}$, $T_J = 125\text{ }^{\circ}\text{C}$		97	122	
g_{FS}	Forward Transconductance	$V_{DS} = -5\text{ V}$, $I_D = -3.3\text{ A}$		6		S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = -15\text{ V}$, $V_{GS} = 0\text{ V}$, $f = 1\text{ MHz}$		324	435	pF
C_{oss}	Output Capacitance			59	80	pF
C_{rss}	Reverse Transfer Capacitance			53	80	pF
R_g	Gate Resistance			12		Ω

Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = -15\text{ V}$, $I_D = -3.3\text{ A}$, $V_{GS} = -10\text{ V}$, $R_{GEN} = 6\text{ }\Omega$		5.2	11	ns
t_r	Rise Time			3	10	ns
$t_{d(off)}$	Turn-Off Delay Time			17	31	ns
t_f	Fall Time			11	25	ns
$Q_{g(TOT)}$	Total Gate Charge	$V_{GS} = 0\text{ V to } -10\text{ V}$	$V_{DD} = -15\text{ V}$, $I_D = -3.3\text{ A}$	7.2	10	nC
	Total Gate Charge	$V_{GS} = 0\text{ V to } -5\text{ V}$		4.1	6	nC
Q_{gs}	Gate to Source Charge			1.0		nC
Q_{gd}	Gate to Drain "Miller" Charge			1.9		nC

Drain-Source Diode Characteristics

V_{SD}	Source to Drain Diode Forward Voltage	$V_{GS} = 0\text{ V}$, $I_S = -3.3\text{ A}$ (Note 2)		-0.94	-1.3	V
t_{rr}	Reverse Recovery Time	$I_F = -3.3\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$		20	32	ns
Q_{rr}	Reverse Recovery Charge			10	18	nC

Electrical Characteristics $T_J = 25\text{ }^{\circ}\text{C}$ unless otherwise noted

Notes:

1. $R_{\theta JA}$ is determined with the device mounted on a 1 in² oz. copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta JA}$ is determined by the user's board design.

- (a) $R_{\theta JA} = 86\text{ }^{\circ}\text{C/W}$ when mounted on a 1 in² pad of 2 oz copper, 1.5 " x 1.5 " x 0.062 " thick PCB. For single operation.
- (b) $R_{\theta JA} = 173\text{ }^{\circ}\text{C/W}$ when mounted on a minimum pad of 2 oz copper. For single operation.
- (c) $R_{\theta JA} = 69\text{ }^{\circ}\text{C/W}$ when mounted on a 1 in² pad of 2 oz copper, 1.5 " x 1.5 " x 0.062 " thick PCB. For dual operation.
- (d) $R_{\theta JA} = 151\text{ }^{\circ}\text{C/W}$ when mounted on a minimum pad of 2 oz copper. For dual operation.
- (e) $R_{\theta JA} = 160\text{ }^{\circ}\text{C/W}$ when mounted on a 30 mm² pad of 2 oz copper. For single operation.
- (f) $R_{\theta JA} = 133\text{ }^{\circ}\text{C/W}$ when mounted on a 30 mm² pad of 2 oz copper. For dual operation.



a. 86 $^{\circ}\text{C/W}$ when mounted on a 1 in² pad of 2 oz copper



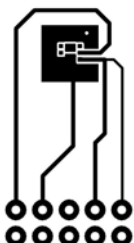
b. 173 $^{\circ}\text{C/W}$ when mounted on a minimum pad of 2 oz copper



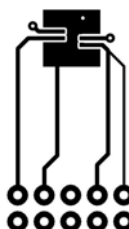
c. 69 $^{\circ}\text{C/W}$ when mounted on a 1 in² pad of 2 oz copper



d. 151 $^{\circ}\text{C/W}$ when mounted on a minimum pad of 2 oz copper



e. 160 $^{\circ}\text{C/W}$ when mounted on 30 mm² pad of 2 oz copper



f. 133 $^{\circ}\text{C/W}$ when mounted on 30 mm² pad of 2 oz copper

2. Pulse Test : Pulse Width < 300 us, Duty Cycle < 2.0%

3. The diode connected between gate and source serves only as protection against ESD. No gate overvoltage rating is implied.

Typical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

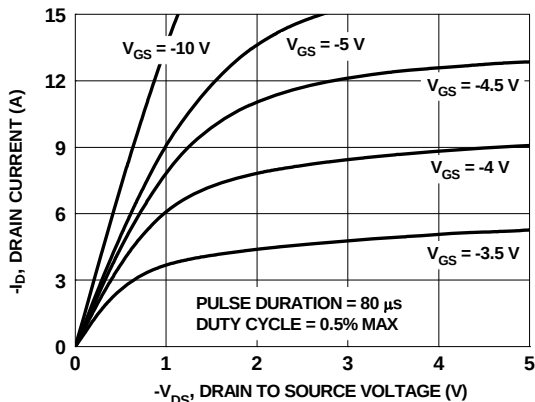


Figure 1. On-Region Characteristics

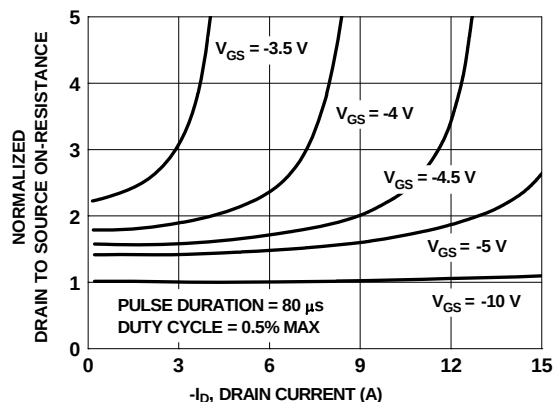


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

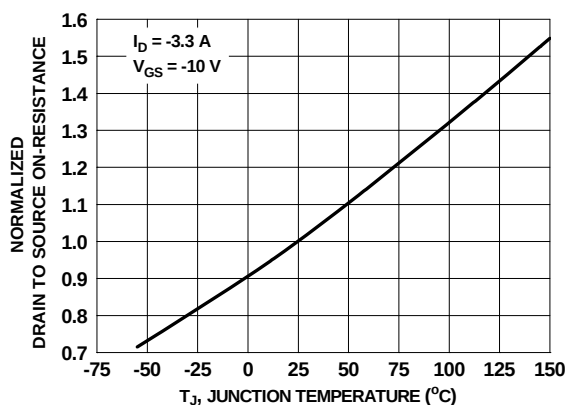


Figure 3. Normalized On-Resistance vs Junction Temperature

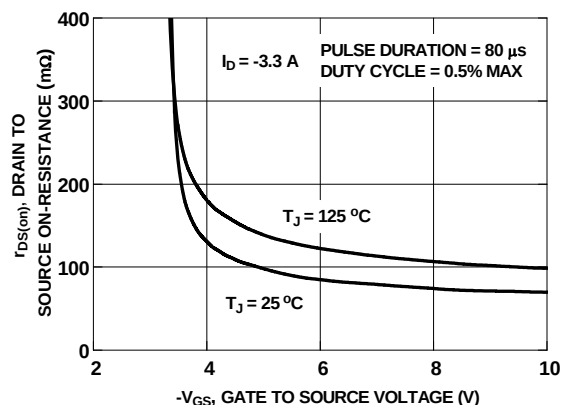


Figure 4. On-Resistance vs Gate to Source Voltage

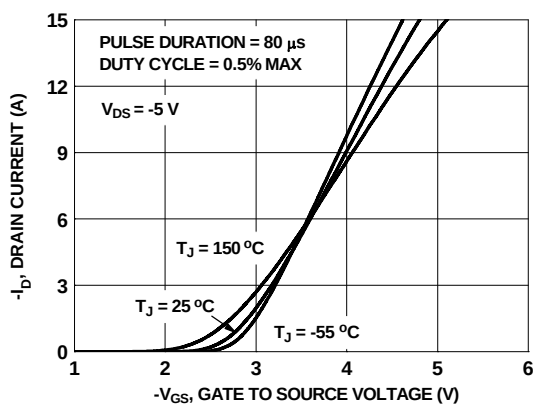


Figure 5. Transfer Characteristics

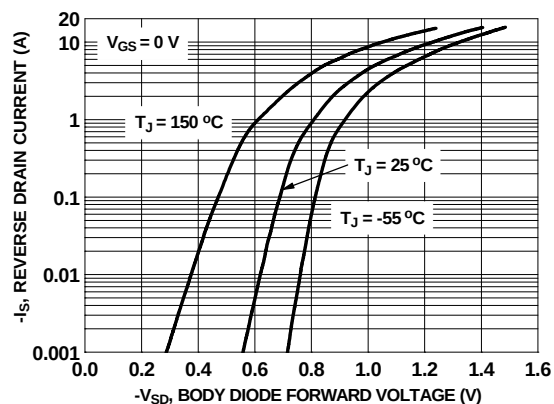


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

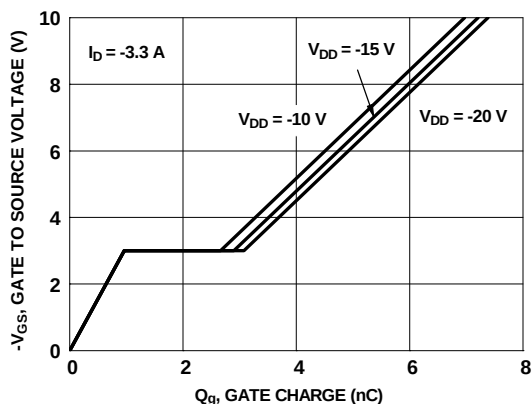


Figure 7. Gate Charge Characteristics

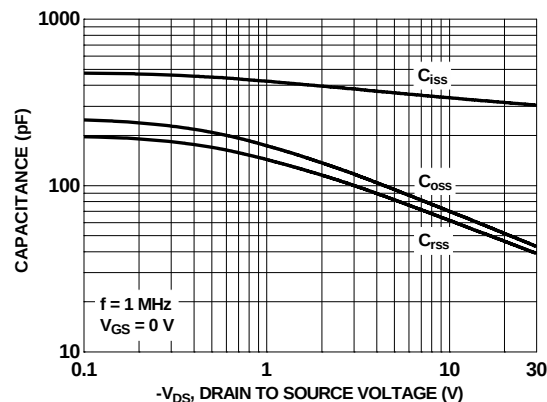


Figure 8. Capacitance vs Drain to Source Voltage

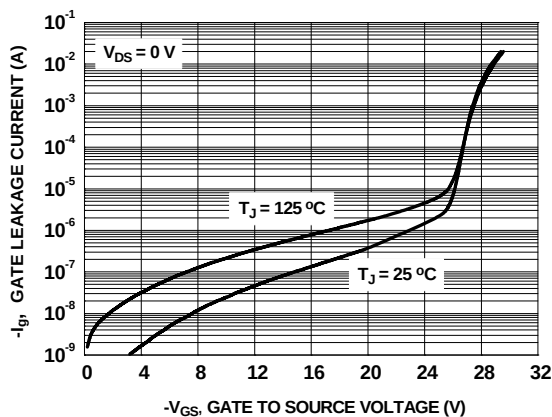


Figure 9. Gate Leakage Current vs Gate to Source Voltage

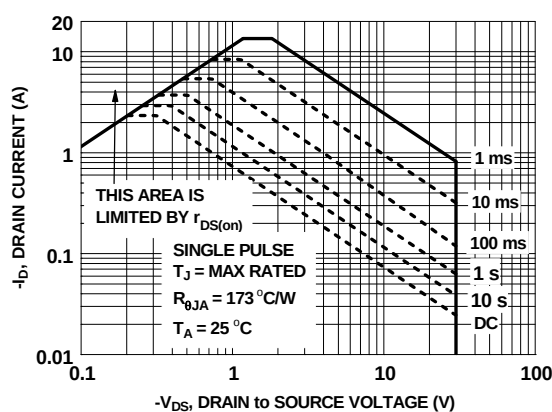


Figure 10. Forward Bias Safe Operating Area

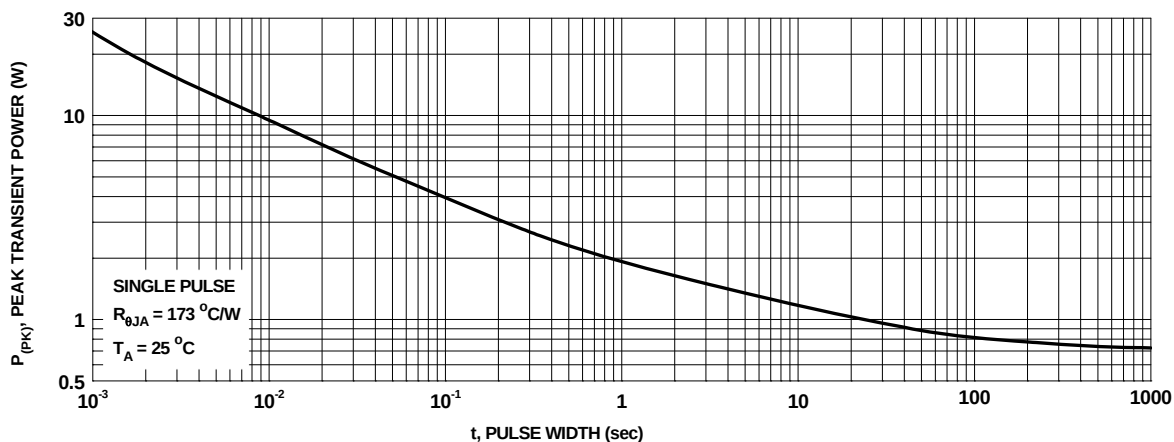
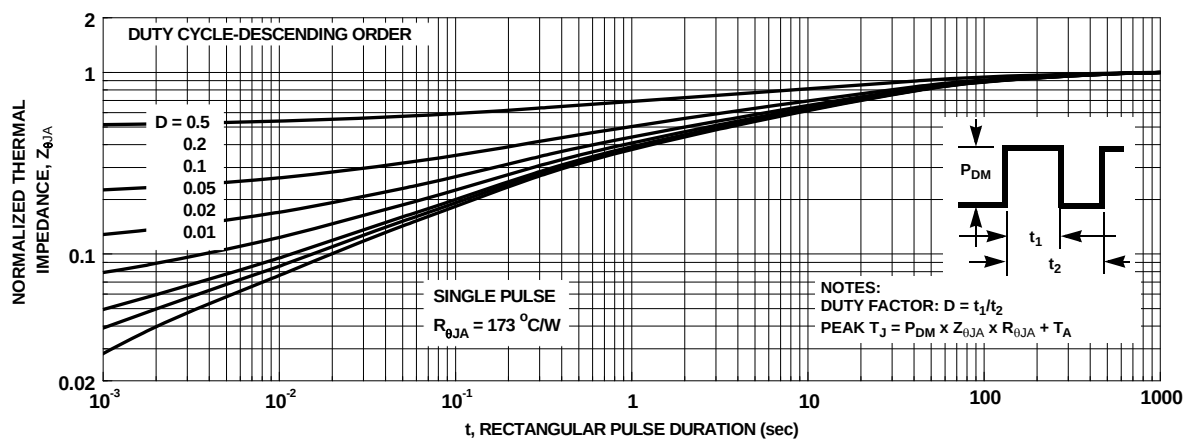
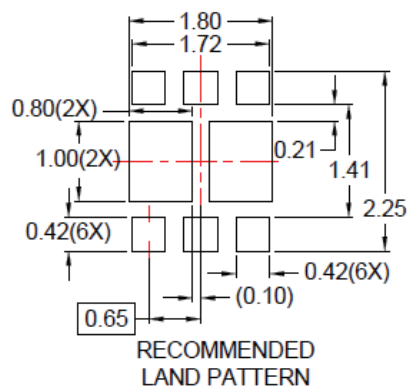
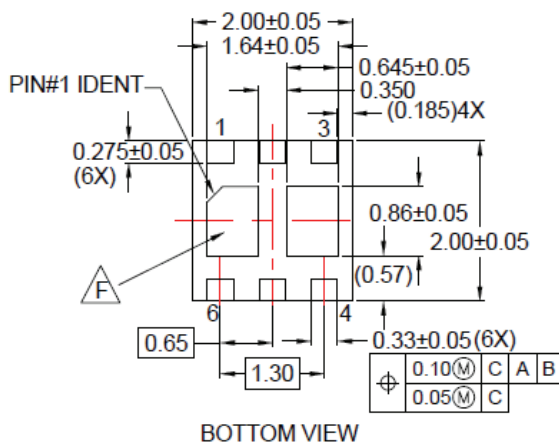
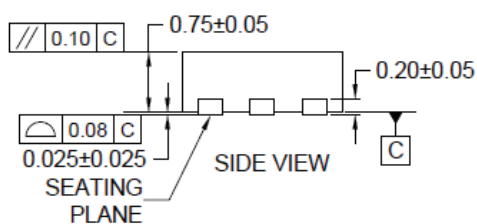
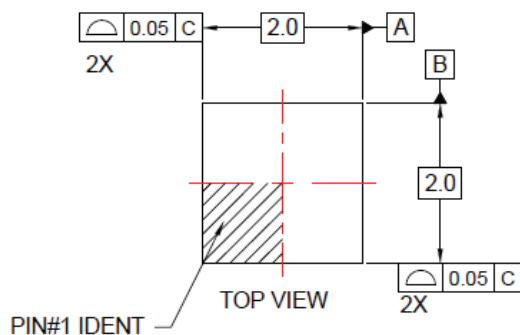


Figure 11. Single Pulse Maximum Power Dissipation

Typical Characteristics $T_J = 25\text{ }^{\circ}\text{C}$ unless otherwise noted



Dimensional Outline and Pad Layout



NOTES:

- CONFORM TO JEDEC REGISTRATIONS MO-229, VARIATION VCCC, EXCEPT WHERE NOTED.
- DIMENSIONS ARE IN MILLIMETERS.
- DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.
- LAND PATTERN RECOMMENDATION IS EXISTING INDUSTRY LAND PATTERN.
- DRAWING FILENAME: MKT-UMLP16Erev4
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