

## FEATURES

- Member of the Texas Instruments Widebus™ Family
- Operates From 1.65 to 3.6 V
- Max  $t_{pd}$  of 4.2 ns at 3.3 V
- $\pm 24$ -mA Output Drive at 3.3 V
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)

## DESCRIPTION/ORDERING INFORMATION

This 16-bit edge-triggered D-type flip-flop is designed for 1.65-V to 3.6-V  $V_{CC}$  operation.

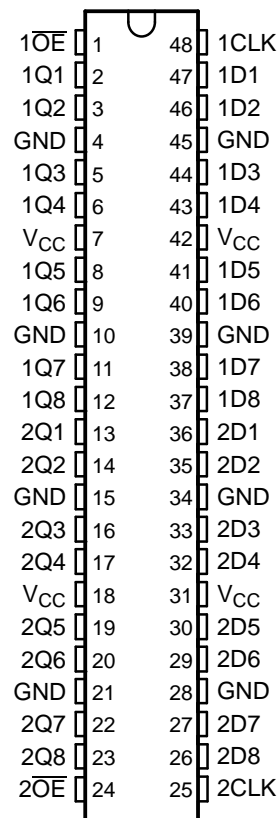
The SN74ALVCH16374 is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers. It can be used as two 8-bit flip-flops or one 16-bit flip-flop. On the positive transition of the clock (CLK) input, the Q outputs of the flip-flop take on the logic levels at the data (D) inputs.  $\overline{OE}$  can be used to place the eight outputs in either a normal logic state (high or low logic levels) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without need for interface or pullup components.

$\overline{OE}$  does not affect internal operations of the flip-flop. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry holds unused or undriven inputs at a valid logic state. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

DGG, DGV, OR DL PACKAGE  
(TOP VIEW)



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

Widebus is a trademark of Texas Instruments.

# SN74ALVCH16374

## 16-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOP WITH 3-STATE OUTPUTS

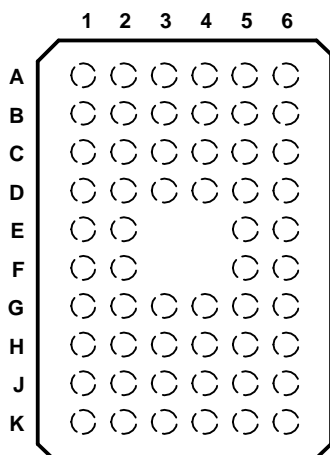
SCES021L—JULY 1995—REVISED SEPTEMBER 2004

### ORDERING INFORMATION

T <sub>A</sub>	PACKAGE <sup>(1)</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	SSOP - DL	Tube	SN74ALVCH16374DL	ALVCH16374
		Tape and reel	SN74ALVCH16374DLR	
	TSSOP - DGG	Tape and reel	SN74ALVCH16374DGGR	ALVCH16374
	TVSOP - DGV	Tape and reel	SN74ALVCH16374DGVR	VH374
	VFBGA - GQL	Tape and reel	SN74ALVCH16374KR	VH374
	VFBGA - ZQL (Pb-free)		74ALVCH16374ZQLR	

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guideline are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).

GQL OR ZQL PACKAGE  
(TOP VIEW)



TERMINAL ASSIGNMENTS<sup>(1)</sup>

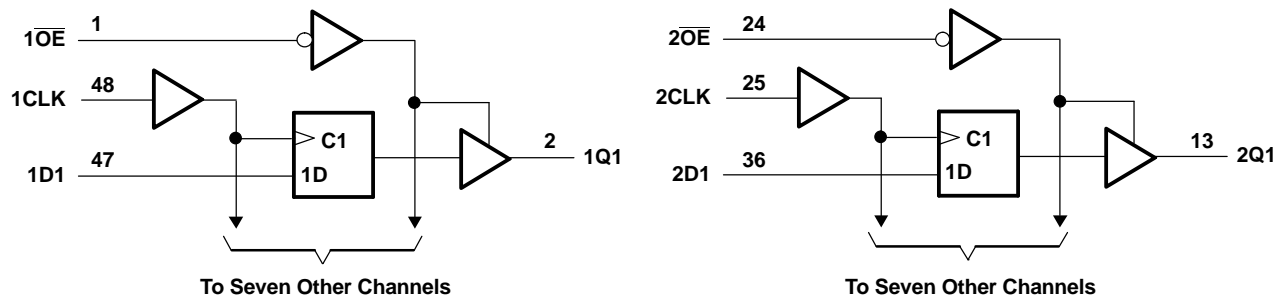
	1	2	3	4	5	6
A	1OE	NC	NC	NC	NC	1CLK
B	1Q2	1Q1	GND	GND	1D1	1D2
C	1Q4	1Q3	V <sub>CC</sub>	V <sub>CC</sub>	1D3	1D4
D	1Q6	1Q5	GND	GND	1D5	1D6
E	1Q8	1Q7			1D7	1D8
F	2Q1	2Q2			2D2	2D1
G	2Q3	2Q4	GND	GND	2D4	2D3
H	2Q5	2Q6	V <sub>CC</sub>	V <sub>CC</sub>	2D6	2D5
J	2Q7	2Q8	GND	GND	2D8	2D7
K	2OE	NC	NC	NC	NC	2CLK

(1) NC - No internal connection

FUNCTION TABLE  
(each flip-flop)

INPUTS			OUTPUT Q
OE	CLK	D	
L	↑	H	H
L	↑	L	L
L	H or L	X	Q <sub>0</sub>
H	X	X	Z

LOGIC DIAGRAM (POSITIVE LOGIC)



Pin numbers shown are for the DGG, DGV, and DL packages.

**ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>**

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage range	-0.5	4.6	V
V <sub>I</sub>	Input voltage range <sup>(2)</sup>	-0.5	4.6	V
V <sub>O</sub>	Output voltage range <sup>(2)(3)</sup>	-0.5	V <sub>CC</sub> + 0.5	V
I <sub>IK</sub>	Input clamp current	V <sub>I</sub> < 0		-50 mA
I <sub>OK</sub>	Output clamp current	V <sub>O</sub> < 0		-50 mA
I <sub>O</sub>	Continuous output current		±50	mA
	Continuous current through each V <sub>CC</sub> or GND		±100	mA
θ <sub>JA</sub>	Package thermal impedance <sup>(4)</sup>	DGG package		70
		DGV package		58
		DL package		63
		GQL/ZQL package		42
T <sub>stg</sub>	Storage temperature range	-65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) This value is limited to 4.6 V, maximum.
- (4) The package thermal impedance is calculated in accordance with JESD 51-7.

**RECOMMENDED OPERATING CONDITIONS<sup>(1)</sup>**

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage	1.65	3.6	V
V <sub>IH</sub>	High-level input voltage	V <sub>CC</sub> = 1.65 V to 1.95 V	0.65 × V <sub>CC</sub>	V
		V <sub>CC</sub> = 2.3 V to 2.7 V	1.7	
		V <sub>CC</sub> = 2.7 V to 3.6 V	2	
V <sub>IL</sub>	Low-level input voltage	V <sub>CC</sub> = 1.65 V to 1.95 V	0.35 × V <sub>CC</sub>	V
		V <sub>CC</sub> = 2.3 V to 2.7 V	0.7	
		V <sub>CC</sub> = 2.7 V to 3.6 V	0.8	
V <sub>I</sub>	Input voltage	0	V <sub>CC</sub>	V
V <sub>O</sub>	Output voltage	0	V <sub>CC</sub>	V
I <sub>OH</sub>	High-level output current	V <sub>CC</sub> = 1.65 V	-4	mA
		V <sub>CC</sub> = 2.3 V	-12	
		V <sub>CC</sub> = 2.7 V	-12	
		V <sub>CC</sub> = 3 V	-24	
I <sub>OL</sub>	Low-level output current	V <sub>CC</sub> = 1.65 V	4	mA
		V <sub>CC</sub> = 2.3 V	12	
		V <sub>CC</sub> = 2.7 V	12	
		V <sub>CC</sub> = 3 V	24	
Δt/Δv	Input transition rise or fall rate		10	ns/V
T <sub>A</sub>	Operating free-air temperature	-40	85	°C

- (1) All unused control inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

# SN74ALVCH16374

## 16-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOP WITH 3-STATE OUTPUTS

SCES021L–JULY 1995–REVISED SEPTEMBER 2004

### ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	$V_{CC}$	MIN	TYP <sup>(1)</sup>	MAX	UNIT
$V_{OH}$		$I_{OH} = -100 \mu A$	1.65 V to 3.6 V	$V_{CC} - 0.2$			V
		$I_{OH} = -4 \text{ mA}$	1.65 V	1.2			
		$I_{OH} = -6 \text{ mA}$	2.3 V	2			
	$I_{OH} = -12 \text{ mA}$		2.3 V	1.7			
			2.7 V	2.2			
			3 V	2.4			
	$I_{OH} = -24 \text{ mA}$	3 V	2				
$V_{OL}$		$I_{OL} = 100 \mu A$	1.65 V to 3.6 V			0.2	V
		$I_{OL} = 4 \text{ mA}$	1.65 V			0.45	
		$I_{OL} = 6 \text{ mA}$	2.3 V			0.4	
	$I_{OL} = 12 \text{ mA}$		2.3 V			0.7	
			2.7 V			0.4	
		$I_{OL} = 24 \text{ mA}$	3 V			0.55	
$I_I$		$V_I = V_{CC}$ or GND	3.6 V			$\pm 5$	$\mu A$
$I_{I(\text{hold})}$		$V_I = 0.58 \text{ V}$	1.65 V	25			$\mu A$
		$V_I = 1.07 \text{ V}$	1.65 V	-25			
		$V_I = 0.7 \text{ V}$	2.3 V	45			
		$V_I = 1.7 \text{ V}$	2.3 V	-45			
		$V_I = 0.8 \text{ V}$	3 V	75			
		$V_I = 2 \text{ V}$	3 V	-75			
		$V_I = 0$ to $3.6 \text{ V}^{(2)}$	3.6 V			$\pm 500$	
$I_{OZ}$		$V_O = V_{CC}$ or GND	3.6 V			$\pm 10$	$\mu A$
$I_{CC}$		$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V			40	$\mu A$
$\Delta I_{CC}$		One input at $V_{CC} - 0.6 \text{ V}$ , Other inputs at $V_{CC}$ or GND	3 V to 3.6 V			750	$\mu A$
$C_i$	Control inputs	$V_I = V_{CC}$ or GND	3.3 V	3			pF
	Data inputs			6			
$C_o$	Outputs	$V_O = V_{CC}$ or GND	3.3 V	7			pF

(1) All typical values are at  $V_{CC} = 3.3 \text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

(2) This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

### TIMING REQUIREMENTS

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

		$V_{CC} = 1.8 \text{ V}$		$V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$		$V_{CC} = 2.7 \text{ V}$		$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$		UNIT
		MIN	TYP	MIN	MAX	MIN	MAX	MIN	MAX	
$f_{\text{clock}}$	Clock frequency	(1)		150		150		150		MHz
$t_w$	Pulse duration, CLK high or low	(1)		3.3		3.3		3.3		ns
$t_{su}$	Setup time, data before CLK $\uparrow$	(1)		2.1		2.2		1.9		ns
$t_h$	Hold time, data after CLK $\uparrow$	(1)		0.6		0.5		0.5		ns

(1) This information was not available at the time of publication.

## SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 1.8\text{ V}$		$V_{CC} = 2.5\text{ V}$ $\pm 0.2\text{ V}$		$V_{CC} = 2.7\text{ V}$		$V_{CC} = 3.3\text{ V}$ $\pm 0.3\text{ V}$		UNIT
			MIN	TYP	MIN	MAX	MIN	MAX	MIN	MAX	
$f_{\max}$			(1)		150		150		150		MHz
$t_{pd}$	CLK	Q		(1)	1	5.3	4.9		1	4.2	ns
$t_{en}$	$\overline{OE}$	Q		(1)	1	6.2	5.9		1	4.8	ns
$t_{dis}$	$\overline{OE}$	Q		(1)	1	5.3	4.7		1.2	4.3	ns

(1) This information was not available at the time of publication.

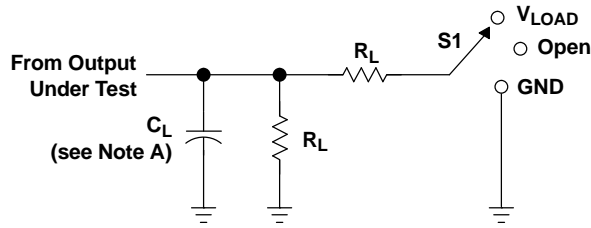
## OPERATING CHARACTERISTICS

$T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	$V_{CC} = 1.8\text{ V}$	$V_{CC} = 2.5\text{ V}$	$V_{CC} = 3.3\text{ V}$	UNIT
			TYP	TYP	TYP	
$C_{pd}$ Power dissipation capacitance	Outputs enabled	$C_L = 50\text{ pF}, f = 10\text{ MHz}$	(1)	31	30	pF
	Outputs disabled		(1)	16	18	

(1) This information was not available at the time of publication.

**PARAMETER MEASUREMENT INFORMATION**



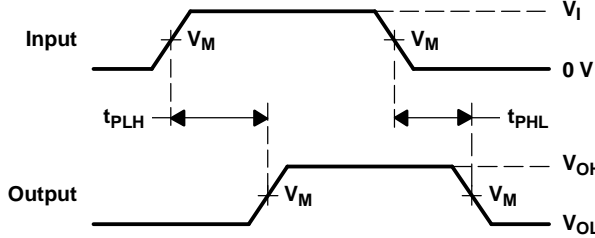
**LOAD CIRCUIT**

TEST	S1
$t_{pd}$ $t_{PLZ}/t_{PZL}$ $t_{PHZ}/t_{PZH}$	Open $V_{LOAD}$ GND

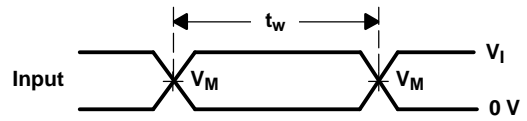
$V_{CC}$	INPUT		$V_M$	$V_{LOAD}$	$C_L$	$R_L$	$V_{\Delta}$
	$V_I$	$t_r/t_f$					
1.8 V	$V_{CC}$	$\leq 2$ ns	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	1 k $\Omega$	0.15 V
$2.5 V \pm 0.2 V$	$V_{CC}$	$\leq 2$ ns	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	500 $\Omega$	0.15 V
2.7 V	2.7 V	$\leq 2.5$ ns	1.5 V	6 V	50 pF	500 $\Omega$	0.3 V
$3 V \pm 0.3 V$	2.7 V	$\leq 2.5$ ns	1.5 V	6 V	50 pF	500 $\Omega$	0.3 V



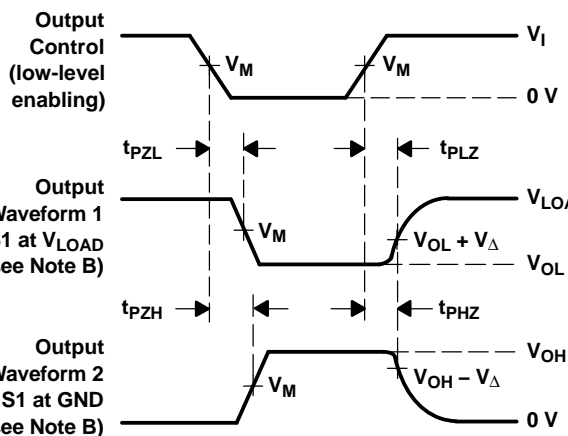
**VOLTAGE WAVEFORMS**  
**SETUP AND HOLD TIMES**



**VOLTAGE WAVEFORMS**  
**PROPAGATION DELAY TIMES**



**VOLTAGE WAVEFORMS**  
**PULSE DURATION**



**VOLTAGE WAVEFORMS**  
**ENABLE AND DISABLE TIMES**

- NOTES: A.  $C_L$  includes probe and jig capacitance.  
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.  
C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10$  MHz,  $Z_O = 50 \Omega$ .  
D. The outputs are measured one at a time, with one transition per measurement.  
E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .  
F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .  
G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .  
H. All parameters and waveforms are not applicable to all devices.

**Figure 1. Load Circuit and Voltage Waveforms**

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
74ALVCH16374DGGRE4	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ALVCH16374	<a href="#">Samples</a>
74ALVCH16374ZQLR	LIFEBUY	BGA MICROSTAR JUNIOR	ZQL	56	1000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	VH374	
SN74ALVCH16374DGGR	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ALVCH16374	<a href="#">Samples</a>
SN74ALVCH16374DGVR	ACTIVE	TVSOP	DGV	48	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	VH374	<a href="#">Samples</a>
SN74ALVCH16374DL	ACTIVE	SSOP	DL	48	25	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ALVCH16374	<a href="#">Samples</a>
SN74ALVCH16374DLR	ACTIVE	SSOP	DL	48	1000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ALVCH16374	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

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## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
74ALVCH16374ZQLR	BGA MICROSTAR JUNIOR	ZQL	56	1000	330.0	16.4	4.8	7.3	1.5	8.0	16.0	Q1
SN74ALVCH16374DGGR	TSSOP	DGG	48	2000	330.0	24.4	8.6	13.0	1.8	12.0	24.0	Q1
SN74ALVCH16374DGVR	TVSOP	DGV	48	2000	330.0	16.4	7.1	10.2	1.6	12.0	16.0	Q1
SN74ALVCH16374DLR	SSOP	DL	48	1000	330.0	32.4	11.35	16.2	3.1	16.0	32.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
74ALVCH16374ZQLR	BGA MICROSTAR JUNIOR	ZQL	56	1000	350.0	350.0	43.0
SN74ALVCH16374DGGR	TSSOP	DGG	48	2000	367.0	367.0	45.0
SN74ALVCH16374DGVR	TVSOP	DGV	48	2000	367.0	367.0	38.0
SN74ALVCH16374DLR	SSOP	DL	48	1000	367.0	367.0	55.0

# MECHANICAL DATA

DL (R-PDSO-G48)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - Falls within JEDEC MO-118

PowerPAD is a trademark of Texas Instruments.

DGV (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE

24 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.  
 D. Falls within JEDEC: 24/48 Pins – MO-153  
 14/16/20/56 Pins – MO-194

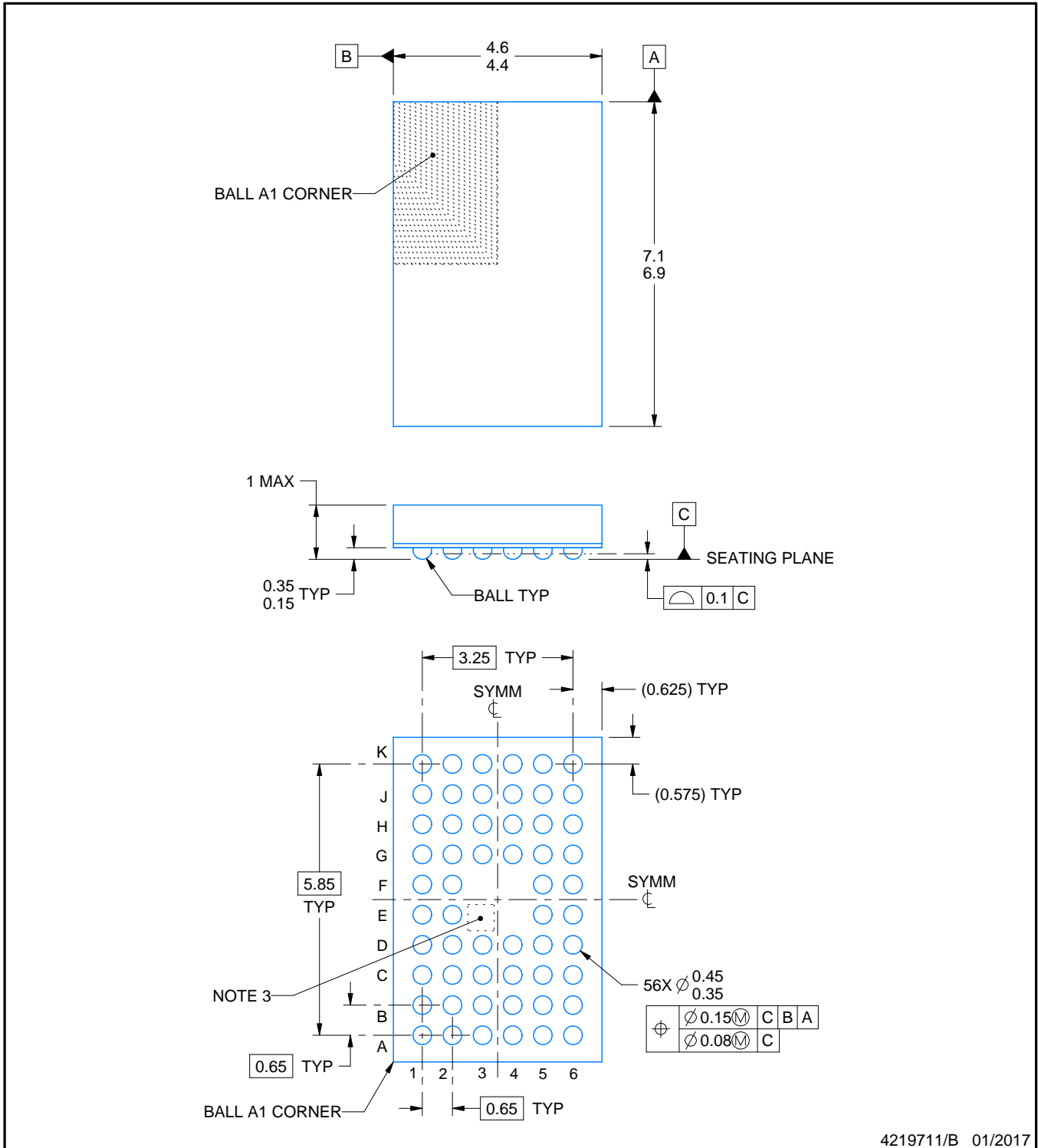
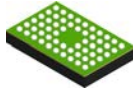
DGG (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-153



4219711/B 01/2017

NOTES:

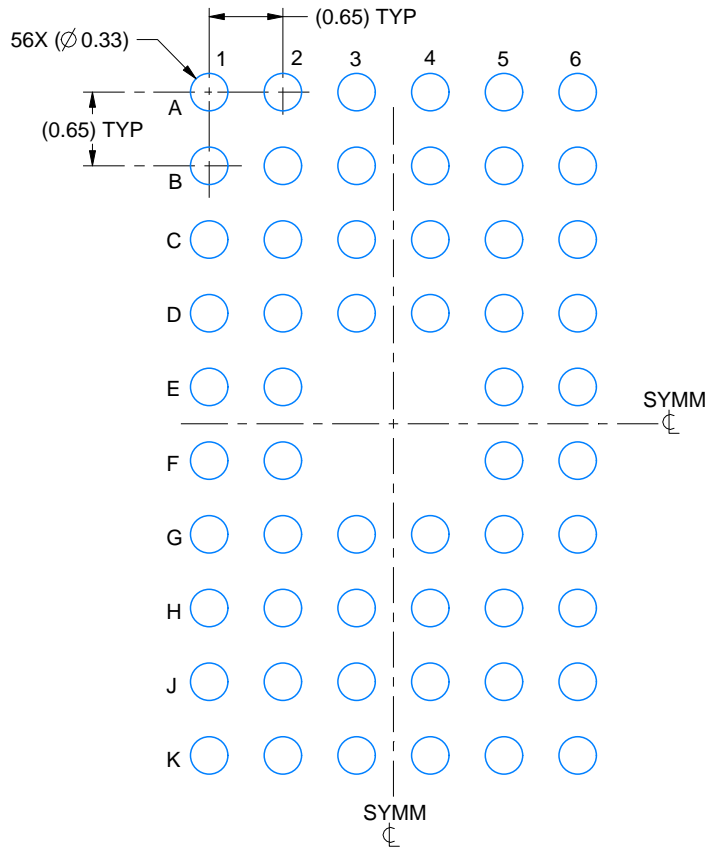
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. No metal in this area, indicates orientation.

# EXAMPLE BOARD LAYOUT

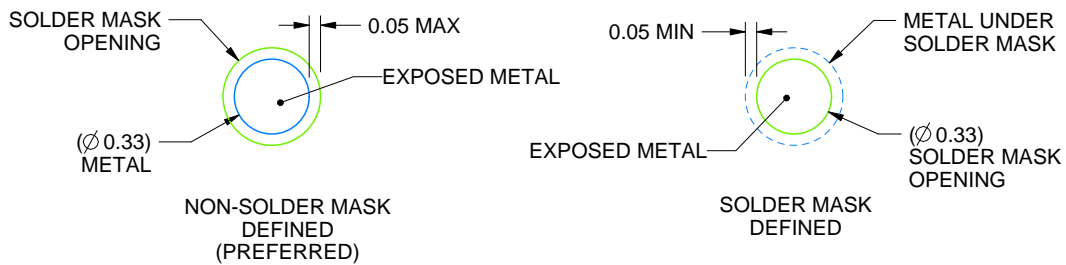
ZQL0056A

JRBGA - 1 mm max height

PLASTIC BALL GRID ARRAY



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:15X



SOLDER MASK DETAILS  
NOT TO SCALE

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NOTES: (continued)

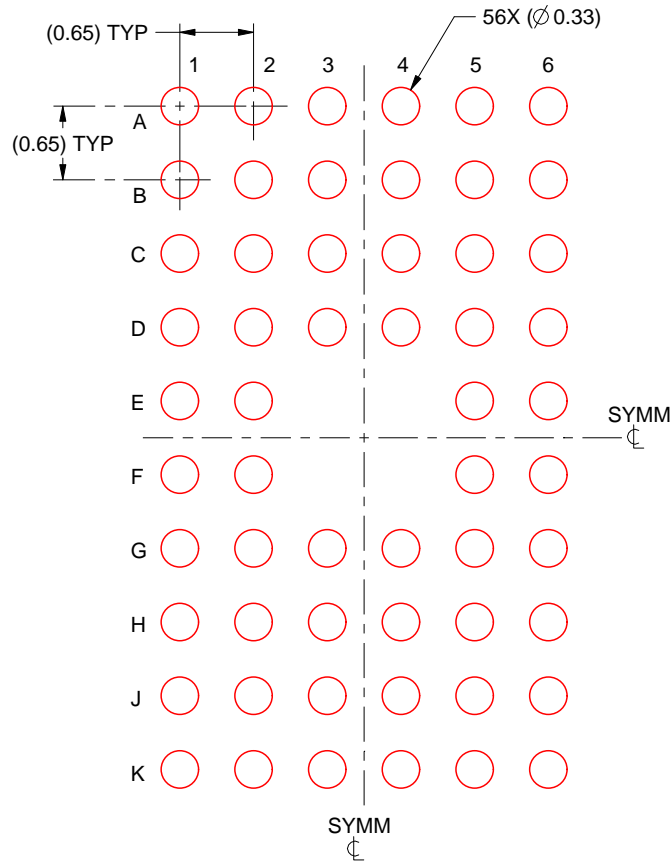
- Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For information, see Texas Instruments literature number SPRAA99 ([www.ti.com/lit/spraa99](http://www.ti.com/lit/spraa99)).

# EXAMPLE STENCIL DESIGN

ZQL0056A

JRBGA - 1 mm max height

PLASTIC BALL GRID ARRAY



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:15X

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NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.



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