LM10507 Triple Buck + LDO Power Management Unit

1 Features

- Three Highly Efficient Programmable Buck Regulators
  - Integrated FETs with Low R_{DS-ON}
  - Bucks Operate with their Phases Shifted to Reduce the Input Current Ripple and Capacitor Size
  - Programmable Output Voltage via the SPI Interface
  - Over and Under-Voltage-Lockout
  - Automatic Internal Soft Start with Power-On Reset
  - Current Overload and Thermal Shutdown Protection
  - PFM Mode for High Efficiency at Light Load Conditions
- Low-Dropout Regulator 2.5 V, 250mA
- Hardware ENABLE and PWR_OK Terminal
- Fast Start-up for All Voltage Rails in about 3.5ms to PWR_OK
- Fast Turn-off / Active Discharge on Regulator Outputs
- Programmable Buck Regulators:
  - Buck 1: 0.9 - 3.4 V; 1.6A
  - Buck 2: 0.9 - 3.4 V; 1A
  - Buck 3: 0.865 - 1.5 V; 1A
  - ±3% Feedback Voltage Accuracy
  - Up to 95% efficient Buck Regulators
  - 2MHz Switching Frequency for Smaller Inductor Size
  - 2.8 x 2.8 mm, 0.4 mm pitch, 34-bump µSMD Package

2 Applications

Solid-State Drives

3 Description

The LM10507 is an advanced PMU containing three configurable, high-efficiency buck regulators for supplying variable voltages. The device is ideal for supporting ASIC and SOC designs for Solid-State and Flash drives.

LM10507 operates cooperatively with ASIC to optimize the supply voltage for low power conditions and power saving modes via SPI interface. It also supports a 2.5 V 250 mA LDO.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LM10507	DSBGA (34)	2.82 mm x 2.82 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

4 Simplified Schematic

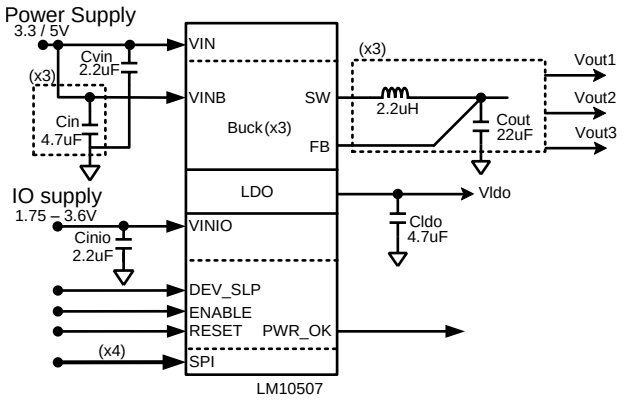


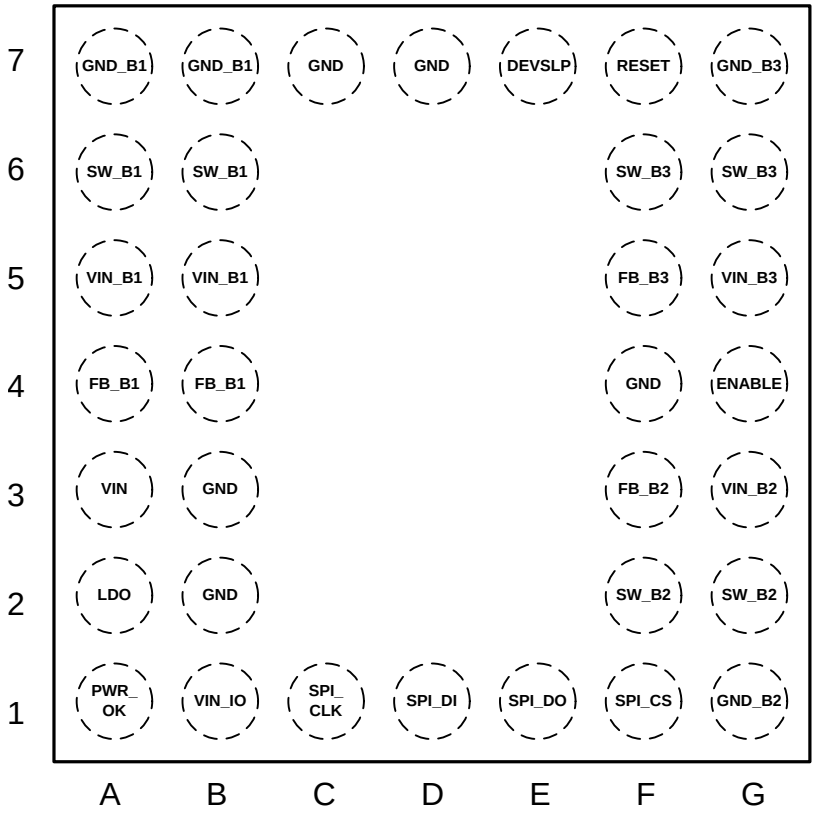
Table of Contents

5 Revision History

DATE	REVISION	NOTES
May 2014	*	Initial release.

6 Pin Configuration and Functions

34 bump DSBGA with 0.4mm pitch
TOP VIEW



Pin Functions

Pin		I/O	Description
Name	No.		
VIN_B1	A/B5	I	Buck Switcher Regulator 1 - Power supply voltage input for power stage PFET, if buck 1 is not used, tie to ground to reduce leakage.
SW_B1	A/B6	O	Buck Switcher Regulator 1 - Power Switching node, connect to inductor
FB_B1	A/B4	I	Buck Switcher Regulator 1 - Voltage output feedback for Buck Regulator 1
GND_B1	A/B7	G	Buck Switcher Regulator 1 - Power ground for Buck Regulator
VIN_B2	G3	I	Buck Switcher Regulator 2 - Power supply voltage input for power stage PFET, if buck 2 is not used, tie to ground to reduce leakage.
SW_B2	F/G2	O	Buck Switcher Regulator 2 - Power Switching node, connect to inductor
FB_B2	F3	I	Buck Switcher Regulator 2 - Voltage output feedback for Buck Regulator 2
GND_B2	G1	G	Buck Switcher Regulator 2 - Power ground for Buck Regulator
VIN_B3	G5	I	Buck Switcher Regulator 3 - Power supply voltage input for power stage PFET
SW_B3	F/G6	O	Buck Switcher Regulator 3 - Power Switching node, connect to inductor
FB_B3	F5	I	Buck Switcher Regulator 3 - Voltage output feedback for Buck Regulator 3
GND_B3	G7	G	Buck Switcher Regulator 3 - Power ground for Buck Regulator
VIN	A3	I	Power supply Input Voltage, must be present for device to work
LDO	A2	O	LDO Regulator - LDO regulator output voltage
SPI_CS	F1	I	SPI Interface – chip select
SPI_DI	D1	I	SPI Interface – serial data input
SPI_DO	E1	O	SPI Interface – serial data output

Pin Functions (continued)

Pin		I/O	Description
Name	No.		
SPI_CLK	C1	I	SPI Interface – serial clock input
ENABLE	G4	I	Digital Input Control Signal to Enable/Disable PMIC. Signal Level is related to VIN_IO. This is an active High pin with an internal pull-down resistor.
GND	F4	I	Digital Input Control Signal – Not Used – Connect to GND.
DEVSLP	E7	I	Digital Input Control Signal for entering Device Sleep Mode – see table 1. This is an active High pin with an internal pull-down resistor.
RESET	F7	I	Digital Input Control Signal to abort SPI transactions and resets the PMIC to default Voltages. This is an active Low pin with an internal pull-up resistor.
GND	C7	I	Not Used – Connect to GND.
PWR_OK	A1	O	Digital Output of Power Good signal – all output rails are started.
VIN_IO	B1	P	Supply Voltage for Digital Interface Signals to ASIC like SPI, RESET, DEVSLP, ENABLE, PWR_OK.
GND	B2	G	Ground. Connect to system Ground.
GND	B3	G	Ground. Connect to system Ground.
GND	D7	G	Ground. Connect to system Ground.
A: Analog Pin D : Digital Pin G: Ground Pin P: Power Pin I: Input Pin O: Output Pin			

7 Specifications

7.1 Absolute Maximum Ratings(1)(2)(3)

	MIN	MAX	UNIT
VIN,	-0.3	6.0	V
VIN_IO, VIN_B1, VIN_B2, VIN_B3, SPI_CS, SPI_DI, SPI_CLK, SPI_DO, ENABLE, RESET, PWR_OK, DEVSLP	-0.3	VIN	V
Junction Temperature ($T_{J\text{-}MAX}$)		150	°C

(1) Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions under which operation of the device is ensured. Operating Ratings do not imply ensured performance limits. For ensured performance limits and associated test conditions, see the Electrical Characteristics tables.
(2) Internal thermal shutdown protects device from permanent damage. Thermal shutdown engages at T_J = +140°C and disengages at T_J = +120°C (typ.). Thermal shutdown is ensured by design.
(3) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.

7.2 Handling Ratings

			MIN	MAX	UNIT
T_{stg}	Storage temperature range		-65	150	°C
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)		1.0	kV

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions(1)(2)

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
VIN_B1, VIN_B2_VIN_B3, VIN	3.0	5.5	V
VIN_IO	1.75	3.63, but less than VIN	V
Junction Temperature (T_J)	-30	125	°C
Ambient Temperature (T_A)	-30	85	°C
Maximum Continuous Power Dissipation ($P_{D\text{-}MAX}$) (1)		0.9	W

(1) In applications where high power dissipation and/or poor thermal resistance is present the maximum ambient temperature may have to be derated. Maximum ambient temperature ($T_{A\text{-}MAX}$) is dependent on the maximum operating junction temperature ($T_{J\text{-}MAX\text{-}OP}$ = +125°C), the maximum power dissipation of the device in the application ($P_{D\text{-}MAX}$), and the junction-to-ambient thermal resistance of the part/package in the application (θ_{JA}), as given by the following equation: $T_{A\text{-}MAX} = T_{J\text{-}MAX\text{-}OP} – (\theta_{JA} \times P_{D\text{-}MAX})$.
(2) The amount of Absolute Maximum power dissipation allowed for the device depends on the ambient temperature and can be calculated using the formula: $P = (T_J – T_A)/\theta_{JA}$, where T_J is the junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance. θ_{JA} is highly application and board-layout dependent. Internal thermal shutdown circuitry protects the device from permanent damage (see General Electrical Characteristics)

7.4 Thermal Information

	THERMAL METRIC	TYP	UNIT
$R_{\theta JA}$	Junction-to-Ambient Thermal Resistance(1)	44.5	°C/W

(1) In applications where high power dissipation and/or poor thermal resistance is present the maximum ambient temperature may have to be derated. Maximum ambient temperature ($T_{A\text{-}MAX}$) is dependent on the maximum operating junction temperature ($T_{J\text{-}MAX\text{-}OP}$ = +125°C), the maximum power dissipation of the device in the application ($P_{D\text{-}MAX}$), and the junction-to-ambient thermal resistance of the part/package in the application (θ_{JA}), as given by the following equation: $T_{A\text{-}MAX} = T_{J\text{-}MAX\text{-}OP} – (\theta_{JA} \times P_{D\text{-}MAX})$.

7.5 General Electrical Characteristics(1)(2)(3)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{Q(STANDBY)}$	Quiescent Supply Current	DEVSLP=High Only Buck3 is ON ,PFM mode, no load. (4)		50	150	µA
UNDER/OVERVOLTAGE LOCK OUT						
V_{UVLO_RISING}		LM10507-A(4)	2.5	2.8	2.95	V
$V_{UVLO\_FALLING}$		(4)	2.35	2.5	2.65	
V_{OVLO_RISING}		LM10507-A(4)	5.7	5.9		
$V_{OVLO\_FALLING}$		LM10507-A(4)	5.6	5.8		
DIGITAL INTERFACE						
V_{IL}	Logic input low	SPI_CS, SPI_DI, SPI_CLK, ENABLE, RESET, DEVSLP(5)(4)			$0.3*V_{VIN\_IO}$	V
V_{IH}	Logic input high		$0.7*V_{VIN\_I0}$			
V_{OL}	Logic output low	PWR_OK (at 2mA load), SPI_DO(4)			$0.2*V_{VIN\_IO}$	
V_{OH}	Logic output high		$0.8*V_{VIN\_IO}$			
I_{IL}	Input current, pindriven low	SPI_CS, SPI_DI, SPI_CLK, ENABLE, DEVSLP	−2			µA
		RESET	−5			
I_{IH}	Input current, pindriven high	SPI_CS, SPI_DI, SPI_CLK, RESET			2	µA
		ENABLE, DEVSLP			5	
f_{SPI_MAX}	SPI max frequency	(4)			10	MHz
t_{DEVSLP}	Minimum pulse width (5)			2		µs
t_{RESET}	Minimum pulse width (5)			2		µs
t_{ENABLE}	Minimum pulse width (5)			5		
t_{COMP}	Transition time of PWR_OK output (5)			0	1	

(1) All limits are ensured by design, test and/or statistical analysis. All electrical characteristics having room-temperature limits are tested during production with T_J = 25°C. All hot and cold limits are ensured by correlating the electrical characteristics to process and temperature variations and applying statistical process control.
(2) Capacitors: Low-ESR Surface-Mount Ceramic Capacitors (MLCCs) are used in setting electrical characteristics.
(3) Unless otherwise noted, V_{IN} = 5.0V where: $V_{IN} = V_{VIN\_B1} = V_{VIN\_B2} = V_{VIN\_B3}$. Limits apply for T_J = 25°C unless otherwise noted.
(4) Limits apply over the entire operating junction temperature range of −30°C ≤TA = TJ ≤ +85°C.
(5) Specification ensured by design. Not tested during production.

7.6 Buck 1 Electrical Characteristics(1)(2)(3)(4)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_Q	DC Bias Current in V_{IN}	No Load, PFM Mode(5)		15	50	µA
$I_{OUT-MAX}$	Continuous maximum load current (6)(7)(8)	Buck 1 enabled, switching in PWM (5)	1.6			A
I_{PEAK}	Peak switching current limit	Buck 1 enabled, switching in PWM(5)	1.9	2.2	2.8	A
η	Efficiency peak, Buck 1	I_{OUT} = 0.3A, V_{VIN} = 5.0 V		90%		
F_{SW}	Switching Frequency(6)	(5)	1.75	2	2.3	MHz
C_{IN}	Input Capacitor (6)	0mA ≤ I_{OUT} ≤ $I_{OUT-MAX}$		4.7		µF
C_{OUT}	Output Filter Capacitor (6)		10	10	100	µF
	Output Capacitor ESR (6)				20	mΩ
L	Output Filter Inductance (6)			2.2		µH
ΔVOUT	DC Line regulation (6)	3.3V ≤ V_{IN} ≤ 5.0V, I_{OUT} = $I_{OUT-MAX}$		0.5		%/V
	DC Load regulation, PWM (6)	V_{VIN}=5 V, 0.1 *$I_{OUT-MAX}$≤ I_{OUT} ≤ $I_{OUT-MAX}$		0.3		%/A
I_{FB}	Feedback pininput bias current	V_{FB} = 1 V(5)		1.2	5	µA
V_{FB}	Feedback accuracy	V_{FB} =1 V(5)	-3%		3%	
$R_{DS-ON-HS}$	High Side Switch On Resistance	V_{IN} =5.0 V		135		mΩ
		V_{IN} = 2.6 V		215		mΩ
$R_{DS-ON-LS}$	Low Side Switch On Resistance	V_{VIN}=5.0 V(5)		85	190	mΩ
STARTUP						
T_{START_NoLoad}	Internal soft-start (turn on time) (6)	Startup from shutdown, V_{OUT} = 0V, no load, LC = recommended circuit, using software enable, to V_{OUT} = 95% of final value		0.1		ms
$T_{START\_FullLoad}$	Internal soft-start (turn on time) (6)	Startup from shutdown, V_{OUT} = 0V, Maximum Load, LC = recommended circuit, using software enable, to V_{OUT} = 95% of final value		0.5		ms

(1) All limits are ensured by design, test and/or statistical analysis. All electrical characteristics having room-temperature limits are tested during production with T_J = 25°C. All hot and cold limits are ensured by correlating the electrical characteristics to process and temperature variations and applying statistical process control.
(2) Capacitors: Low-ESR Surface-Mount Ceramic Capacitors (MLCCs) are used in setting electrical characteristics.
(3) BUCK normal operation is ensured if V_{IN} ≥ V_{OUT}+1.0V.
(4) Unless otherwise noted, V_{IN} = 5.0V where: V_{IN} = V_{VIN_B1} = V_{VIN_B2} = V_{VIN_B3}. Limits apply for T_J = 25°C unless otherwise noted.
(5) Limits apply over the entire operating junction temperature range of −30°C ≤TA = TJ ≤ +85°C.
(6) Specification ensured by design. Not tested during production.
(7) In applications where high power dissipation and/or poor thermal resistance is present the maximum ambient temperature may have to be derated. Maximum ambient temperature (T_{A-MAX}) is dependent on the maximum operating junction temperature ($T_{J-MAX-OP}$ = +125°C), the maximum power dissipation of the device in the application (P_{D-MAX}), and the junction-to-ambient thermal resistance of the part/package in the application (θ_{JA}), as given by the following equation: $T_{A-MAX} = T_{J-MAX-OP} – (\theta_{JA} \times P_{D-MAX})$.
(8) The amount of Absolute Maximum power dissipation allowed for the device depends on the ambient temperature and can be calculated using the formula: $P = (T_J – T_A)/\theta_{JA}$, where T_J is the junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance. θ_{JA} is highly application and board-layout dependent. Internal thermal shutdown circuitry protects the device from permanent damage (see General Electrical Characteristics)

7.7 Buck 2 Electrical Characteristics(1)(2)(3)(4)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_Q	DC Bias Current in V_{IN}	No Load, PFM Mode(5)		15	50	µA
$I_{OUT\ -MAX}$	Continuous maximum load current (6)(7)(8)	Buck 1 enabled, switching in PWM(5)	1			A
I_{PEAK}	Peak switching current limit	Buck 1 enabled, switching in PWM(5)	1.35	1.6	1.85	A
η	Efficiency peak, Buck 2	I_{OUT} = 0.3A, V_{VIN} = 5.0 V		90%		
F_{SW}	Switching Frequency(6)	(5)	1.75	2	2.3	MHz
C_{IN}	Input Capacitor (6)	0mA ≤ I_{OUT} ≤$I_{OUT-MAX}$		4.7		µF
C_{OUT}	Output Filter Capacitor (6)		10	10	100	µF
	Output Capacitor ESR (6)				20	mΩ
L	Output Filter Inductance (6)			2.2		µH
ΔV_{OUT}	DC Line regulation (6)	3.3 V ≤ V_{IN} ≤ 5.0 V, I_{OUT} = $I_{OUT-MAX}$		0.5		%/V
	DC Load regulation (6), PWM	VIN = 5 V, 0.1*$I_{OUT-MAX}$≤ I_{OUT} ≤ I_{OUTMAX}		0.3		%/A
I_{FB}	Feedback pininput bias current	V_{FB} = 1.8 V(5)		2.2	5	µA
V_{FB}	Feedback accuracy	V_{FB} = 2 V(5)	-3%		-3%	
$R_{DS-ON-HS}$	High Side Switch On Resistance	V_{VIN} = 5.0 V		135		mΩ
		V_{IN} = 2.6 V		215		
$R_{DS-ON-LS}$	Low Side Switch On Resistance	V_{VIN} = 5.0 V(5)		85	190	
STARTUP						
T_{START_NoLoad}	Internal soft-start (turn on time) (6)	Startup from shutdown, V_{OUT} = 0V, no load, LC = recommended circuit, using software enable, to V_{OUT} = 95% of final value		0.1		ms
$T_{START\_FullLoad}$	Internal soft-start (turn on time) (6)	Start up from shutdown, V_{OUT} =0V, Maximum Load, LC = recommended circuit, using software enable, to V_{OUT} = 95% of final value		0.5		ms

(1) All limits are ensured by design, test and/or statistical analysis. All electrical characteristics having room-temperature limits are tested during production with T_J = 25°C. All hot and cold limits are ensured by correlating the electrical characteristics to process and temperature variations and applying statistical process control.
(2) Capacitors: Low-ESR Surface-Mount Ceramic Capacitors (MLCCs) are used in setting electrical characteristics.
(3) BUCK normal operation is ensured if V_{IN} ≥ V_{OUT}+1.0V.
(4) Unless otherwise noted, V_{IN} = 5.0V where: V_{IN} = V_{VIN_B1} = V_{VIN_B2} = V_{VIN_B3}. Limits apply for T_J = 25°C unless otherwise noted.
(5) Limits apply over the entire operating junction temperature range of −30°C ≤TA = TJ ≤ +85°C.
(6) Specification ensured by design. Not tested during production.
(7) In applications where high power dissipation and/or poor thermal resistance is present the maximum ambient temperature may have to be derated. Maximum ambient temperature (T_{A-MAX}) is dependent on the maximum operating junction temperature ($T_{J-MAX-OP}$ = +125°C), the maximum power dissipation of the device in the application (P_{D-MAX}), and the junction-to-ambient thermal resistance of the part/package in the application (θ_{JA}), as given by the following equation: $T_{A-MAX} = T_{J-MAX-OP} – (\theta_{JA} \times P_{D-MAX})$.
(8) The amount of Absolute Maximum power dissipation allowed for the device depends on the ambient temperature and can be calculated using the formula: $P = (T_J–T_A)/\theta_{JA}$, where T_J is the junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance. θ_{JA} is highly application and board-layout dependent. Internal thermal shutdown circuitry protects the device from permanent damage (see General Electrical Characteristics)

7.8 Buck 3 Electrical Characteristics[1][2][3][4]

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_Q	DC Bias Current in V_{IN}	No Load, PFM Mode[5]		15	50	µA
$I_{OUT-MAX}$	Continuous maximum load current[6][7][8]	Buck 1 enabled, switching in PWM [5]	1			A
I_{PEAK}	Peak switching current limit	Buck 1 enabled, switching in PWM[5]	1.35	1.6	1.85	A
η	Efficiency peak, Buck 3 [6]	I_{OUT} = 0.3A, V_{VIN}=5.0 V		90%		
F_{SW}	Switching Frequency[6]	[5]	1.75	2	2.3	MHz
C_{IN}	Input Capacitor [6]	0mA ≤ I_{OUT} ≤ $I_{OUT-MAX}$		4.7		µF
C_{OUT}	Output Filter Capacitor [6]		10	10	100	µF
	Output Capacitor ESR [6]				20	mΩ
L	Output Filter Inductance [6]			2.2		µH
ΔVOUT	DC Line regulation [6]	3.3 V ≤ V_{IN} ≤ 5.0 V, I_{OUT} = $I_{OUT-MAX}$		0.5		%/V
	DC Load regulation, PWM [6]	VIN=5 V, 0.1* $I_{OUT-MAX}$ ≤ I_{OUT}≥$I_{OUT-MAX}$		0.3		%/A
I_{FB}	Feedback pininput bias current	V_{FB} = 1.5 V[5]		1.0	5	µA
V_{FB}	Feedback accuracy	V_{FB} = 3 V [5]	-3%		-3%	
$R_{DS-ON-HS}$	High Side Switch On Resistance	V_{VIN}=5.0 V		135		mΩ
		V_{IN} = 2.6 V		215		
$R_{DS-ON-LS}$	Low Side Switch On Resistance	V_{VIN}=5.0 V[5]		85	190	
STARTUP						
T_{START_NoLoad}	Internal soft-start (turn on time) [6]	Startup from shutdown, V_{OUT} = 0 V, no load, LC = recommended circuit, using software enable, to V_{OUT} = 95% of final value		0.1		ms
$T_{START\_FullLoad}$	Internal soft-start (turn on time) [6]	Start up from shutdown, V_{OUT}=0 V, Maximum Load, LC = recommended circuit, using software enable, to V_{OUT} = 95% of final value		0.5		ms

(1) All limits are ensured by design, test and/or statistical analysis. All electrical characteristics having room-temperature limits are tested during production with T_J = 25°C. All hot and cold limits are ensured by correlating the electrical characteristics to process and temperature variations and applying statistical process control.
(2) Capacitors: Low-ESR Surface-Mount Ceramic Capacitors (MLCCs) are used in setting electrical characteristics.
(3) BUCK normal operation is ensured if V_{IN} ≥ V_{OUT}+1.0 V.
(4) Unless otherwise noted, V_{IN} = 5.0V where: V_{IN} = V_{VIN_B1} = V_{VIN_B2} = $V_{VIN\_B3.}$ Limits apply for T_J = 25°C unless otherwise noted.
(5) Limits apply over the entire operating junction temperature range of −30°C ≤TA = TJ ≤ +85°C.
(6) Specification ensured by design. Not tested during production.
(7) In applications where high power dissipation and/or poor thermal resistance is present the maximum ambient temperature may have to be derated. Maximum ambient temperature (T_{A-MAX}) is dependent on the maximum operating junction temperature ($T_{J-MAX-OP}$ = +125°C), the maximum power dissipation of the device in the application (P_{D-MAX}), and the junction-to-ambient thermal resistance of the part/package in the application (θ_{JA}), as given by the following equation: $T_{A-MAX} = T_{J-MAX-OP} – (\theta_{JA} \times P_{D-MAX})$.
(8) The amount of Absolute Maximum power dissipation allowed for the device depends on the ambient temperature and can be calculated using the formula: $P = (T_J – T_A)/\theta_{JA}$, where T_J is the junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance. θ_{JA} is highly application and board-layout dependent. Internal thermal shutdown circuitry protects the device from permanent damage (see General Electrical Characteristics)

7.9 LDO Electrical Characteristics(1)(2)(3)

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OUT}	Output Voltage Accuracy	I_{OUT} = 1mA, V_{OUT}= 2.5 V(4)		−3%		+3%	
I_{OUT}	Maximum Output Current	(4)		250			mA
I_{SC}	Short-Circuit Current Limit				0.5		A
V_{DO}	Dropout Voltage(5)	I_{OUT} = 250 mA(4)			200	260	mV
ΔV_{OUT}	Line Regulation	3.3 V ≤ V_{IN} ≤ 5.5 V, I_{OUT} = 1mA			5		mV
	Load Regulation	1mA ≤ I_{OUT} ≤ 250 mA, V_{IN} = 3.3 V, 5.0 V			5		mV
e_N	Output Noise Voltage (6)	10 Hz ≤ f ≤ 100 kHz	V_{IN} = 5.0 V		10		μV_{RMS}
			V_{IN} = 3.3 V		35		μV_{RMS}
PSRR	Power Supply Rejection Ratio (6)	F = 10 kHz, C_{OUT} = 4.7 µF, I_{OUT} = 20 mA	V_{IN} = 5.0 V		65		dB
			V_{IN} = 3.3 V		40		dB
$t_{STARTUP}$	Startup Time from Shutdown (6)	C_{OUT} = 4.7 µF I_{OUT} = 250mA	V_{IN} = 5.0 V		45		µs
			V_{IN} = 3.3 V		60		µs
$T_{TRANSIENT}$	Startup Transient Overshoot (6)	C_{OUT} = 4.7 µF I_{OUT} = 250mA(4)				30	mV

(1) All limits are ensured by design, test and/or statistical analysis. All electrical characteristics having room-temperature limits are tested during production with T_J = 25°C. All hot and cold limits are ensured by correlating the electrical characteristics to process and temperature variations and applying statistical process control.
(2) Capacitors: Low-ESR Surface-Mount Ceramic Capacitors (MLCCs) are used in setting electrical characteristics.
(3) Unless otherwise noted, V_{IN} = 5.0V where: V_{IN} = V_{VIN_B1} = V_{VIN_B2} = V_{VIN_B3}. Limits apply for T_J = 25°C unless otherwise noted.
(4) Limits apply over the entire operating junction temperature range of −30°C ≤TA = TJ ≤ +85°C.
(5) Dropout voltage is the voltage difference between the input and the output at which the output voltage drops to 100 mV below its nominal value.
(6) Specification ensured by design. Not tested during production.

7.10 Typical Characteristics

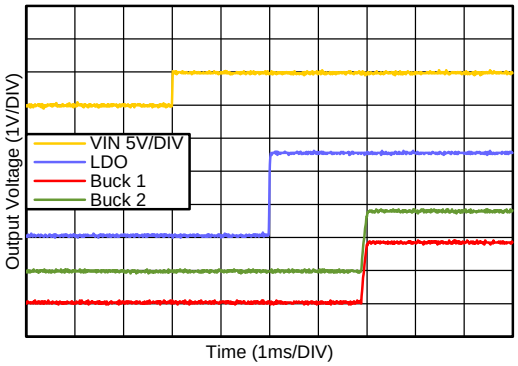


Figure 1. Start-up from VIN Enable

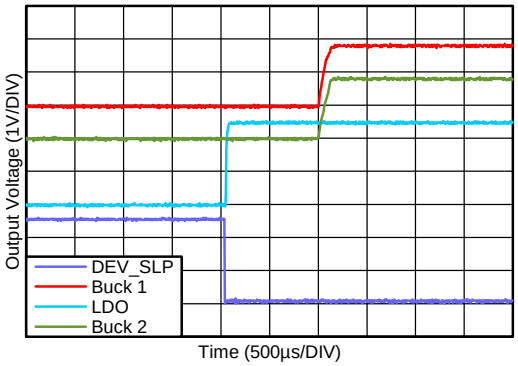


Figure 2. Power-up Out of DEVSLP

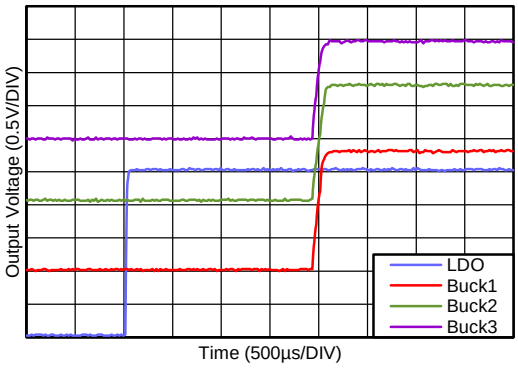


Figure 3. Start-up Plot

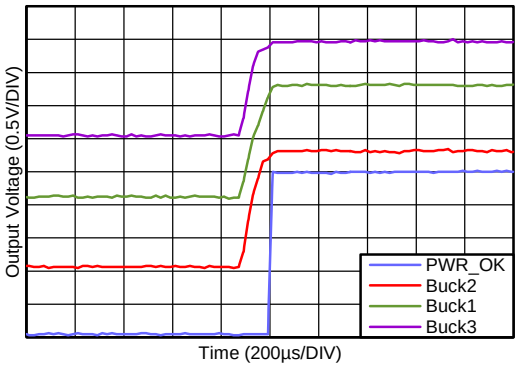


Figure 4. POK Plot

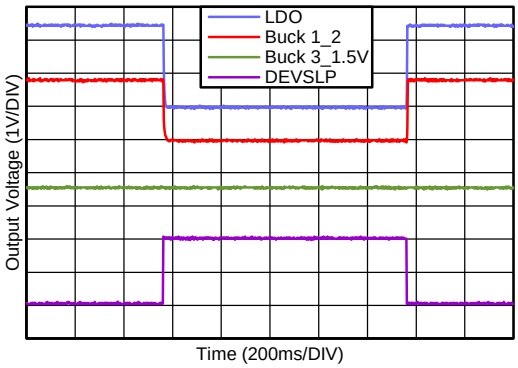


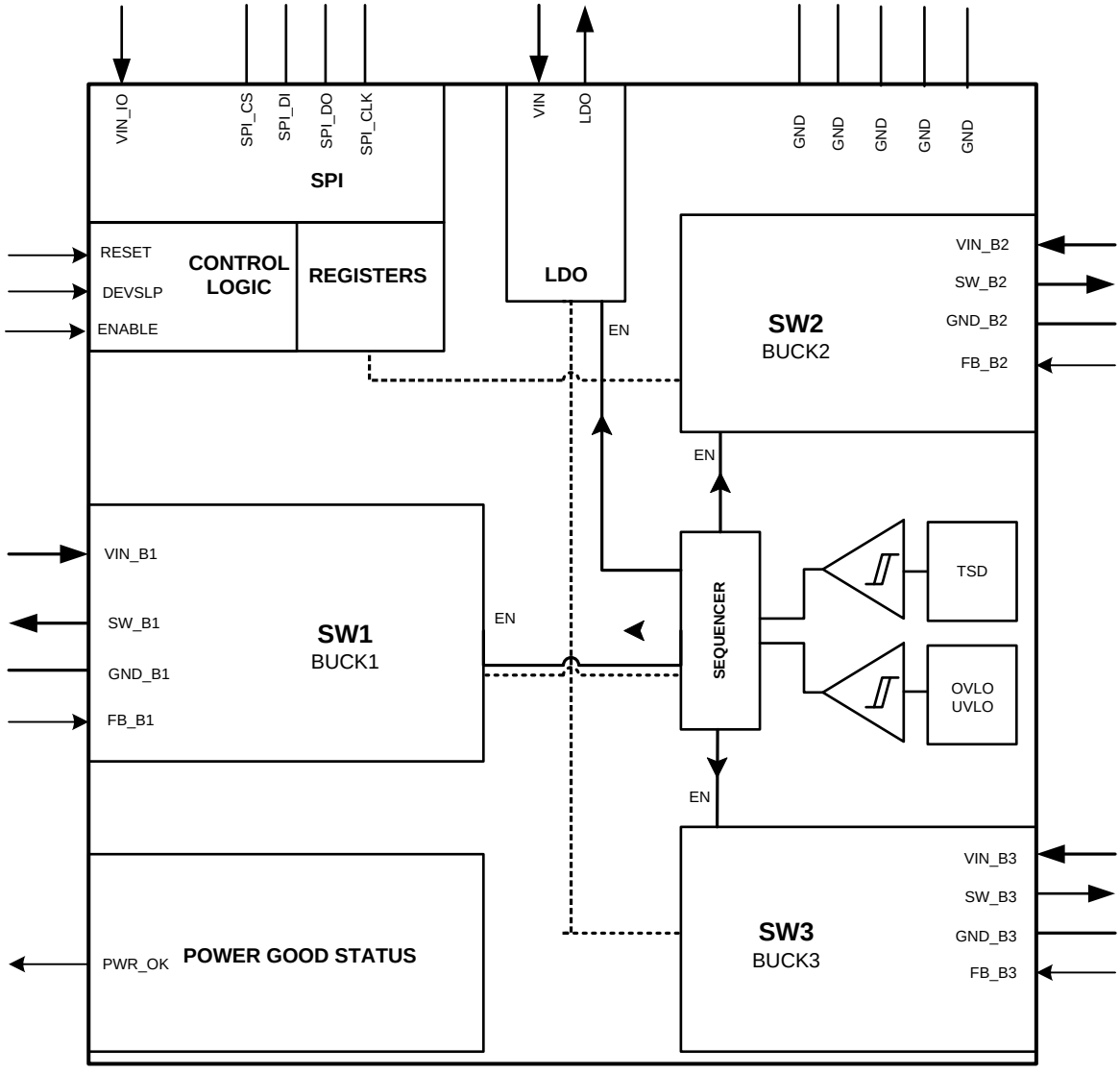
Figure 5. DEVSLP Plot

8 Detailed Description

8.1 Overview

LM10507 is a highly efficient and integrated Power Management Unit for Systems-on-a-Chip (SoCs), ASICs, and processors. It operates cooperatively and communicates with processors over an SPI interface with output Voltage programmability and Standby Mode. The device incorporates three high-efficiency synchronous buck regulators and one LDO that deliver four output voltages from a single power source. The device also includes a SPI-programmable Comparator Block that provides an interrupt output signal

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Buck Regulators Operation

A buck converter contains a control block, a switching PFET connected between input and output, a synchronous rectifying NFET connected between the output and ground and a feedback path. The following figure shows the block diagram of each of the three buck regulators integrated in the device.

Feature Description (continued)

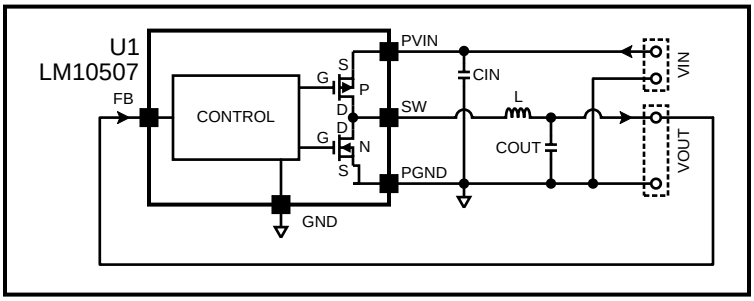


Figure 6. Buck Functional Diagram

During the first portion of each switching cycle, the control block turns on the internal PFET switch. This allows current to flow from the input through the inductor to the output filter capacitor and load. The inductor limits the current to a ramp with a slope of $(V_{IN} – V_{OUT})/L$ by storing energy in a magnetic field. During the second portion of each cycle, the control block turns the PFET switch off, blocking current flow from the input, and then turns the NFET synchronous rectifier on. The inductor draws current from ground through the NFET to the output filter capacitor and load, which ramps the inductor current down with a slope of $(–V_{OUT})/L$.

The output filter stores charge when the inductor current is high, and releases it when low, smoothing the voltage across the load. The output voltage is regulated by modulating the PFET switch on time to control the average current sent to the load. The effect is identical to sending a duty-cycle modulated rectangular wave formed by the switch and synchronous rectifier at the SW pinto a low-pass filter formed by the inductor and output filter capacitor. The output voltage is equal to the average voltage at the SW terminal.

8.3.2 Buck Regulators Description

The LM10507 incorporates three high-efficiency synchronous switching buck regulators that deliver various voltages from a single DC input voltage. They include many advanced features to achieve excellent voltage regulation, high efficiency and fast transient response time. The bucks feature voltage mode architecture with synchronous rectification.

Each of the switching regulators is specially designed for high-efficiency operation throughout the load range. With a 2MHz typical switching frequency, the external L- C filter can be small and still provide very low output voltage ripple. The bucks are internally compensated to be stable with the recommended external inductors and capacitors as detailed in the application diagram. Synchronous rectification yields high efficiency for low voltage and high output currents.

All bucks can operate up to a 100% duty cycle allowing for the lowest possible input voltage that still maintains the regulation of the output. The lowest input to output dropout voltage is achieved by keeping the PMOS switch on.

Additional features include soft-start, undervoltage lockout, bypass, and current and thermal overload protection. To reduce the input current ripple, the device employs a control circuit that operates the 3 bucks at 120° phase. These bucks are nearly identical in performance and mode of operation. They can operate in FPWM (forced PWM) or automatic mode (PWM/PFM).

8.4 Device Functional Modes

8.4.1 PWM Operation

During PWM operation the converter operates as a voltage-mode controller with input voltage feed forward. This allows the converter to achieve excellent load and line regulation. The DC gain of the power stage is proportional to the input voltage. To eliminate this dependence, a feed forward voltage inversely proportional to the input voltage is introduced.

In **Forced PWM Mode** the bucks always operate in PWM mode regardless of the output current.

Device Functional Modes (continued)

In **Automatic Mode**, if the output current is less than 70 mA (typ.), the bucks automatically transition into PFM (Pulse Frequency Modulation) operation to reduce the current consumption. At higher than 70 mA (typ.) they operate in PWM mode. This increases the efficiency at lower output currents.

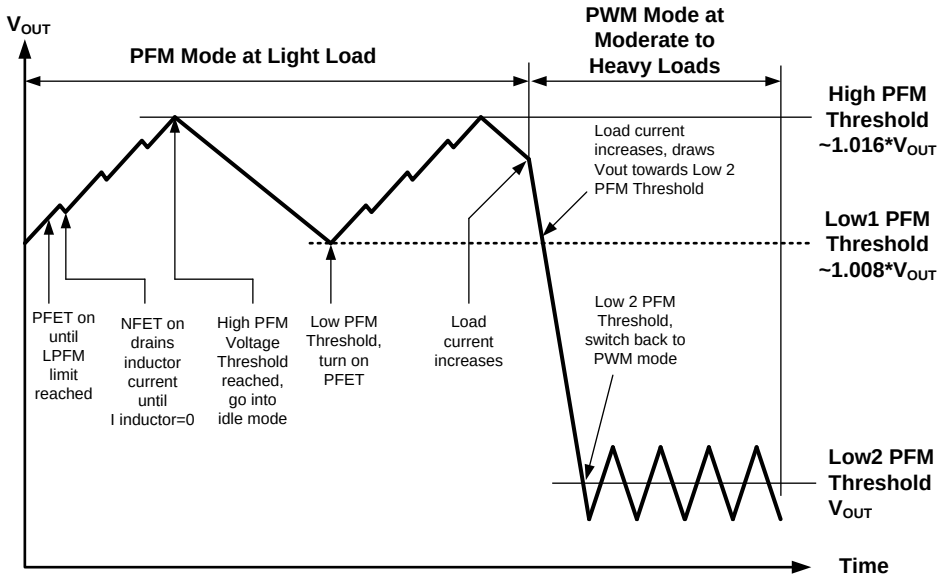


Figure 7. PFM vs PWM Operation

8.4.2 PFM Operation (Bucks 1, 2 & 3)

At very light loads, Bucks 1, 2, and Buck 3 enter PFM mode and operate with reduced switching frequency and supply current to maintain high efficiency.

Bucks 1, 2 and 3 will automatically transition into PFM mode when either of two conditions occurs for a duration of 32 or more clock cycles:

1. The inductor current becomes discontinuous, or
2. The peak PMOS switch current drops below the I_{MODE} level.

During PFM operation, the converter positions the output voltage slightly higher than the nominal output voltage during PWM operation, allowing additional headroom for voltage drop during a load transient from light to heavy load. The PFM comparators sense the output voltage via the feedback pinand control the switching of the output FETs such that the output voltage ramps between 0.8% and 1.6% (typical) above the nominal PWM output voltage. If the output voltage is below the ‘high’ PFM comparator threshold, the PMOS power switch is turned on. It remains on until the output voltage exceeds the ‘high’ PFM threshold or the peak current exceeds the I_{PFM} level set for PFM mode.

Once the PMOS power switch is turned off, the NMOS power switch is turned on until the inductor current ramps to zero. When the NMOS zero-current condition is detected, the NMOS power switch is turned off. If the output voltage is below the ‘high’ PFM comparator threshold (see Figure 7), the PMOS switch is again turned on and the cycle is repeated until the output reaches the desired level. Once the output reaches the ‘high’ PFM threshold, the NMOS switch is turned on briefly to ramp the inductor current to zero and then both output switches are turned off and the part enters an extremely low power mode. Quiescent supply current during this ‘idle’ mode is less than 100 µA, which allows the part to achieve high efficiencies under extremely light load conditions. When the output drops below the ‘low’ PFM threshold, the cycle repeats to restore the output voltage to ~1.6% above the nominal PWM output voltage.

If the load current should increase during PFM mode causing the output voltage to fall below the ‘low2’ PFM threshold, the part will automatically transition into fixed-frequency PWM mode.

Device Functional Modes (continued)

8.4.3 Soft Start

Each of the buck converters has an internal soft-start circuit that limits the in-rush current during startup. This allows the converters to gradually reach the steady-state operating point, thus reducing startup stresses and surges. During startup, the switch current limit is increased in steps.

For **Bucks 1, 2 and 3** the soft start is implemented by increasing the switch current limit in steps that are gradually set higher. The startup time depends on the output capacitor size, load current and output voltage. Typical startup time with the recommended output capacitor of 10 µF is 0.1-0.5ms. It is expected that in the final application the load current condition will be more likely in the lower load current range during the startup.

8.4.4 Current Limiting

A current limit feature protects the device and any external components during overload conditions. In PWM mode the current limiting is implemented by using an internal comparator that trips at current levels according to the buck capability. If the output is shorted to ground the device enters a timed current limit mode where the NFET is turned on for a longer duration until the inductor current falls below a low threshold, ensuring inductor current has more time to decay, thereby preventing runaway.

8.4.5 Internal Synchronous Rectification

While in PWM mode, the bucks use an internal NFET as a synchronous rectifier to reduce the rectifier forward voltage drop and the associated power loss. Synchronous rectification provides a significant improvement in efficiency whenever the output voltage is relatively low compared to the voltage drop across an ordinary rectifier diode.

8.4.6 Low Dropout Operation

The device can operate at 100% duty cycle (no switching; PMOS switch completely on) for low dropout support. In this way the output voltage will be controlled down to the lowest possible input voltage. When the device operates near 100% duty cycle, output voltage ripple is approximately 25 mV.

The minimum input voltage needed to support the output voltage:

$$V_{IN\_MIN}=V_{OUT}+I_{LOAD}*(R_{DSON\_PFET}+R_{IND}) \quad (1)$$

where

- I_{LOAD} : Load Current
- R_{DSON_PFET} : Drain to source resistance of PFET (high side)
- R_{IND} : Inductor resistance

8.4.7 Device Operating Modes

8.4.7.1 Startup Sequence

Once VVIN reaches the UVLO threshold and the ENABLE pin= High the LM10507 will start up. There is a fixed delay of approx. 1 ms before the LDO starts up, followed by Buck1 at 1ms. After a delay of 1msec from Buck1, Buck2 and Buck3 regulators start together. There is a maximum of 500us soft-start with full load for the Bucks

The Startup Sequence will be:

1. 2.5ms delay after ENABLE.
2. LDO -> 2.5 V,
3. 2ms delay.
4. Buck1 -> 1.8 V, Buck2 -> 1.8 V, Buck3 -> 1.5 V
5. PWR_OK goes high

Device Functional Modes (continued)

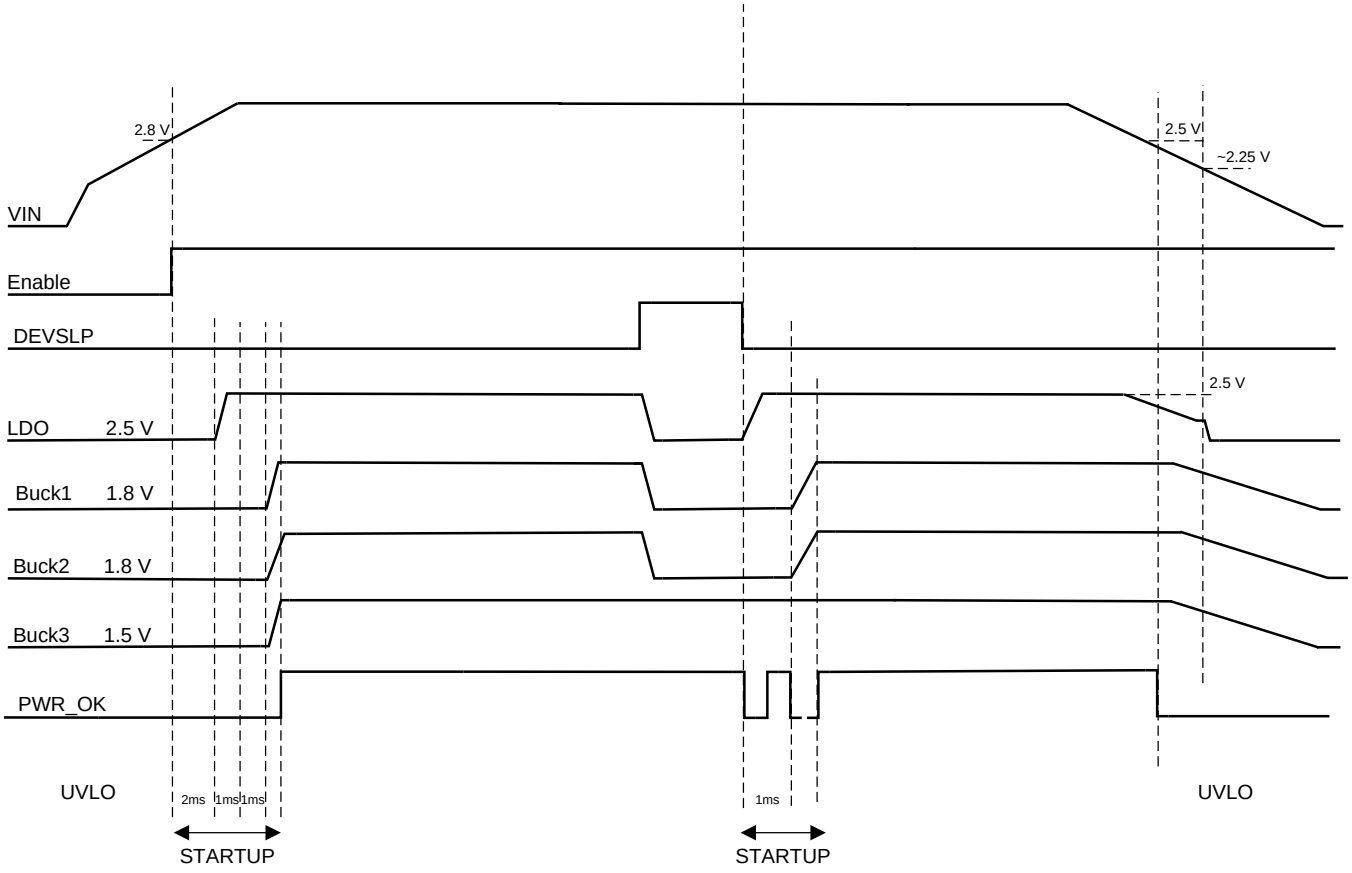


Figure 8. Normal Operating Mode

8.4.7.2 Power-On Default and Device Enable

The device will be enabled over the ENABLE terminal, unless outside of operating voltage range. Once V_{VIN} reaches a minimum required input Voltage and ENABLE=High the power-up sequence will be started. Once the device is started, the output voltage of the Bucks can be individually disabled by accessing their corresponding BK1EN, BK2EN register bits (BUCK CONTROL).

8.4.7.3 RESET: Pin Function

The RESET pinis internally pulled up. If the RESET pinis set low, the device will perform a complete reset of all the registers to their default states. This means that all of the voltage settings on the regulators will go back to their default state and all Regulators will be turned ON. All Registers will be set back to default instantaneously but no Start-Up Sequence initiated like it would be with ENABLE terminal.

8.4.7.4 DEVSLP (Device Sleep) Function

The Device can be programmed into Standby mode. There are 2 ways for doing that:

1. DEVSLP terminal
2. Programming via SPI

Device Functional Modes (continued)

8.4.7.5 DEVSLP Terminal

When the DEVSLP pinis asserted high, the LM10507 will enter Device Sleep Mode. While in Device Sleep Mode, all Regulator outputs are turned OFF except Buck3. Note: Bucks1,2 and LDO will turn off when the DEVSLP signal is given. All disabled output Rails will turn off immediately and at the same time (no sequencing). An internal 22 kΩ (typ.) pull down resistor is attached to the FB pinof Buck 1 and Buck2. Buck 1 and 2 outputs are pulled to ground level when they are disabled to discharge any residual charge present in the output circuitry. When Device Sleep transitions to a low, Buck 1, Buck2 and LDO are enabled. Buck 3 will go back to its previous state

8.4.7.6 Device Sleep (DEVSLP) Programming via SPI

There is no bit which has the same function as DEVSLP terminal. Disabling or programming the Bucks to new level is the user's decision based on power consumption and other requirements

The following section describes how to program the chip into Device Sleep Mode corresponding to DEVSLP pinfunction: Buck 3 must be PFM. To program the LM10507 to Device Sleep Mode via SPI, Buck 1 and Buck2 must be disabled by host device (Register 0x0A bit 0). The LDO must be disabled (Register 0x0B bit 1 and 0). Then stop the oscillator (Register 0x0E bit 1) To wake LM10507 from Device Sleep Mode, reverse this sequence.

8.4.7.7 ENABLE, Function

The ENABLE pinis a digital function to control the Start-Up of PMIC. ENABLE has an internal pull-down and is active High. A pull-down resistor is connected to GND. Transitions of the ENABLE pinto Low during device operation will disable all regulators and actively force down all the output voltages. Register defaults are restored while ENABLE is low.

8.4.7.8 Under Voltage Lock Out (UVLO)

The VIN voltage is monitored for a supply under voltage condition, for which the operation of the device cannot be guaranteed. The part will automatically disable PMIC. To prevent unstable operation, the UVLO has a hysteresis window of about 300mV. An under voltage lockout (UVLO) will disable all buck outputs, all internal registers are reset. Once the supply voltage is above the UVLO hysteresis, the device will initiate a power-up sequence and then enter the active state.

The LDO will remain functional past the UVLO threshold until V_{VIN} reaches approximately 2.25V.

8.4.7.9 Over Voltage Lock Out (OVLO)

The VIN voltage is monitored for a supply over voltage condition, for which the operation of the device cannot be guaranteed. The purpose of OVLO is to protect the part and all other components connected to the PMU outputs from any damage and malfunction. Once V_{VIN} rises over about 5.8V all the Bucks and LDO will be disabled automatically. To prevent unstable operation, the OVLO has a hysteresis window of about 100mV. An over voltage lockout (OVLO) will force the device into the reset state, all internal registers are reset. Once the supply voltage goes below the OVLO lower threshold, the device will initiate a power-up sequence and then enter the active state. Operating maximum input voltage at which parameters are guaranteed is 5.5 V. Absolute maximum of the device is 6.0 V.

8.4.7.10 PWR_OK – Pin Function

The LM10507 has PWR_OK pinto signal that all output rails are valid. PWR_OK is Low if Buck3 is disabled in register0x0A. If PWR_OK condition is detected, then the Hardware PWR_OK pinwill be set immediately. There are four PWR_OK generating conditions, all must be fulfilled :

- Buck 3 output is over flag level (90% when rising,85% when falling).
- Buck 2 output is over flag level (90% when rising,85% when falling) , but not applicable if disabled in register 0x0A.
- Buck 1 output is over flag level (90% when rising,85% when falling) , but not applicable if disabled in register 0x0A
- LDO output is over flag level (90% when rising,85% when falling) , but not applicable if disabled in register 0x0B.

Device Functional Modes (continued)

NOTE

SPI commanded Disable of any output, followed by a subsequent SPI commanded ENABLE will cause a temporary logic LOW of the PWR_OK pinuntil that Buck output voltage has risen back to the 90% flag level.

8.4.7.11 Thermal Shutdown (TSD)

The temperature of the silicon die is monitored for an over-temperature condition, for which the operation of the device cannot be guaranteed. The part will automatically be disabled if the temperature is too high. The thermal shutdown (TSD) will force the device into the reset state. In reset, all circuitry is disabled. To prevent unstable operation, the TSD has a hysteresis window of about 20°C. Once the temperature has decreased below the TSD hysteresis, the device will initiate a power-up sequence and then enter the active state. In the active state, the part will start up as if for the first time, all registers will be in their default state.

8.5 Programming

8.5.1 SPI Data Interface

The device is programmable via 4-wire SPI Interface. The signals associated with this interface are CS, DI, DO and CLK. Through this interface, the user can enable/disable the device, program the output voltages of the individual bucks and of course read the status of Flag registers.

By accessing the registers in the device through this interface, the user can get access and control the operation of the buck controllers and program the reference voltage of the comparator in the device.

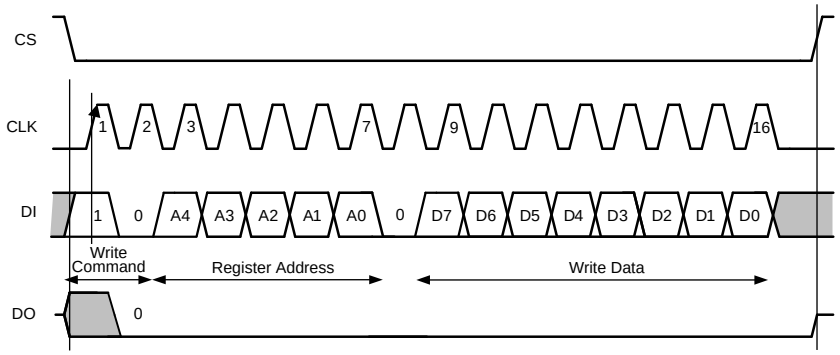


Figure 9. SPI Interface Write

- Data In (DI)
  - 1 to 0 Write Command
  - $A_4$to A_0 Register address to be written
  - D_7 to D_0 Data to be written
- Data Out (DO)
  - All Os

Programming (continued)

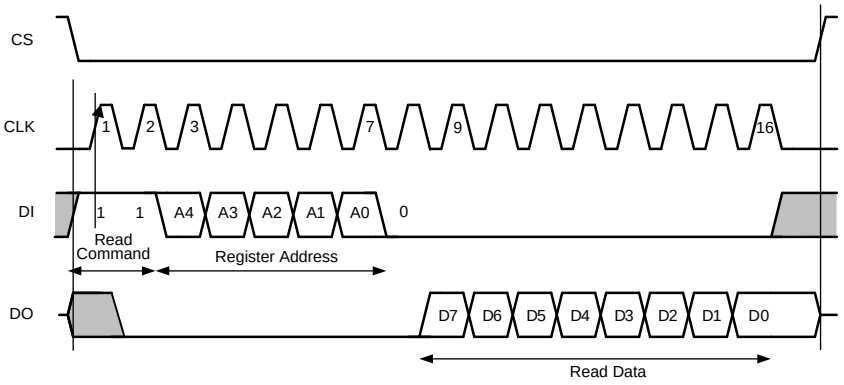


Figure 10. SPI Interface Read

- Data In (DI)
  - 1 to 1 Read Command
  - $A_4$to A_0 Register address to be read
- Data Out (DO)
  - D_7 to D_0 Data Read

8.6 Register Maps

8.6.1 Registers Configurable Via The SPI Interface

Addr	Reg Name	Bit	R/W	Default	Description	Notes
0x00	Buck 3 Voltage	7	—	—		Reset default: 0x7F (1.5 V) Range: 0.865-1.5 V
		6	R/W	1	Buck 3 Voltage Code[6]	
		5	R/W	1	Buck 3 Voltage Code[5]	
		4	R/W	1	Buck 3 Voltage Code[4]	
		3	R/W	1	Buck 3 Voltage Code[3]	
		2	R/W	1	Buck 3 Voltage Code[2]	
		1	R/W	1	Buck 3 Voltage Code[1]	
		0	R/W	1	Buck 3 Voltage Code[0]	
0x07	Buck 1 Voltage	7	—	—	—	Reset default: 0x12 (1.8 V) Range: 0.9-3.4
		6	—	—		
		5	R/W	0	Buck 1 Voltage Code[5]	
		4	R/W	1	Buck 1 Voltage Code[4]	
		3	R/W	0	Buck 1 Voltage Code[3]	
		2	R/W	0	Buck 1 Voltage Code[2]	
		1	R/W	1	Buck 1 Voltage Code[1]	
		0	R/W	0	Buck 1 Voltage Code[0]	
0x08	Buck 2 Voltage	7	—	—	—	Reset default: 0x12 (1.8 V) Range: 0.9-3.4
		6	—	—	—	
		5	R/W	0	Buck 2 Voltage Code[5]	
		4	R/W	1	Buck 2 Voltage Code[4]	
		3	R/W	0	Buck 2 Voltage Code[3]	
		2	R/W	0	Buck 2 Voltage Code[2]	
		1	R/W	1	Buck 2 Voltage Code[1]	
		0	R/W	0	Buck 2 Voltage Code[0]	

Register Maps (continued)

Addr	Reg Name	Bit	R/W	Default	Description	Notes
0x09	DevSLP Mode Voltage for Buck 3	7	R/W	—	—	Reset default:
		6	R/W	1	Buck 3 Voltage Code[6]	0x7F (1.5 V)
		5	R/W	1	Buck 3 Voltage Code[5]	
		4	R/W	1	Buck 3 Voltage Code[4]	
		3	R/W	1	Buck 3 Voltage Code[3]	
		2	R/W	1	Buck 3 Voltage Code[2]	
		1	R/W	1	Buck 3 Voltage Code[1]	
		0	R/W	1	Buck 3 Voltage Code[0]	
0x0A	Buck Control	7	R/W	1	BK3EN	Enable/Disable Buck 3
		6	—	—	—	
		5	—	—	—	
		4	R/W	—	BK1FPWM	Buck 1 forced PWM mode when high
		3	R/W	0	BK2FPWM	Buck 2 forced PWM mode when high
		2	R/W	0	BK3FPWM	Buck 3 forced PWM mode when high
		1	R/W	1	BK1EN	Enables Buck 1 0-disabled, 1-enabled
		0	R/W	1	BK2EN	Enables Buck 2 0-disabled, 1-enabled
0x0B	LDO Control	7	—	—	—	
		6	—	—	—	
		5	—	—	—	
		4	—	—	—	
		3	—	—	—	
		2	—	—	—	
		1	—	—	—	
		0	R/W	1	LDO Enable	
0x0D	Status	7	—			
		6	—			
		5	—			
		4	R		LDO OK	LDO is greater than 90% of target
		3	R		Buck 3 OK	Buck 3 is greater than 90% of target
		2	R		Buck 2 OK	Buck 2 is greater than 90% of target
		1	R		Buck 1 OK	Buck 1 is greater than 90% of target
		0	R		PWR_OK	PWR_OK output is high
0x0E	MISC Control	7	—			
		6	—			
		5	—			
		4	—			
		3	—			
		2	—			
		1	R/W	0	Oscillator Disable	OSC ENABLE/DISABLE
		0				

8.6.1.1 ADDR 0x07 & 0x08: Buck 1 and Buck 2 Voltage Code and V_{OUT} Level Mapping

Voltage Code	Voltage	Voltage Code	Voltage
0x00	0.9	0x20	2.5
0x01	0.95	0x21	2.55
0x02	1	0x22	2.6
0x03	1.05	0x23	2.65
0x04	1.1	0x24	2.7
0x05	1.15	0x25	2.75
0x06	1.2	0x26	2.8
0x07	1.25	0x27	2.85
0x08	1.3	0x28	2.9
0x09	1.35	0x29	2.95
0x0A	1.4	0x2A	3
0x0B	1.45	0x2B	3.05
0x0C	1.5	0x2C	3.1
0x0D	1.55	0x2D	3.15
0x0E	1.6	0x2E	3.2
0x0F	1.65	0x2F	3.25
0x10	1.7	0x30	3.3
0x11	1.75	0x31	3.35
0x12	1.8	0x32	3.4
0x13	1.85	0x33	3.4
0x14	1.9	0x34	3.4
0x15	1.95	0x35	3.4
0x16	2	0x36	3.4
0x17	2.05	0x37	3.4
0x18	2.1	0x38	3.4
0x19	2.15	0x39	3.4
0x1A	2.2	0x3A	3.4
0x1B	2.25	0x3B	3.4
0x1C	2.3	0x3C	3.4
0x1D	2.35	0x3D	3.4
0x1E	2.4	0x3E	3.4
0x1F	2.45	0x3F	3.4

8.6.1.2 ADDR 0x00 Buck 3 Voltage Code and V_{OUT} Level Mapping

Voltage Code	Voltage	Voltage Code	Voltage	Voltage Code	Voltage	Voltage Code	Voltage
0x00	0.865	0x20	1.025	0x40	1.185	0x60	1.345
0x01	0.87	0x21	1.03	0x41	1.19	0x61	1.35
0x02	0.875	0x22	1.035	0x42	1.195	0x62	1.355
0x03	0.88	0x23	1.04	0x43	1.2	0x63	1.36
0x04	0.885	0x24	1.045	0x44	1.205	0x64	1.365
0x05	0.89	0x25	1.05	0x45	1.21	0x65	1.37
0x06	0.895	0x26	1.055	0x46	1.215	0x66	1.375
0x07	0.9	0x27	1.06	0x47	1.22	0x67	1.38
0x08	0.905	0x28	1.065	0x48	1.225	0x68	1.385
0x09	0.91	0x29	1.07	0x49	1.23	0x69	1.39
0x0A	0.915	0x2A	1.075	0x4A	1.235	0x6A	1.395
0x0B	0.92	0x2B	1.08	0x4B	1.24	0x6B	1.4
0x0C	0.925	0x2C	1.085	0x4C	1.245	0x6C	1.405
0x0D	0.93	0x2D	1.09	0x4D	1.25	0x6D	1.41
0x0E	0.935	0x2E	1.095	0x4E	1.255	0x6E	1.415
0x0F	0.94	0x2F	1.1	0x4F	1.26	0x6F	1.42
0x10	0.945	0x30	1.105	0x50	1.265	0x70	1.425
0x11	0.95	0x31	1.11	0x51	1.27	0x71	1.43
0x12	0.955	0x32	1.115	0x52	1.275	0x72	1.435
0x13	0.96	0x33	1.12	0x53	1.28	0x73	1.44
0x14	0.965	0x34	1.125	0x54	1.285	0x74	1.445
0x15	0.97	0x35	1.13	0x55	1.29	0x75	1.45
0x16	0.975	0x36	1.135	0x56	1.295	0x76	1.455
0x17	0.98	0x37	1.14	0x57	1.3	0x77	1.46
0x18	0.985	0x38	1.145	0x58	1.305	0x78	1.465
0x19	0.99	0x39	1.15	0x59	1.31	0x79	1.47
0x1A	0.995	0x3A	1.155	0x5A	1.315	0x7A	1.475
0x1B	1	0x3B	1.16	0x5B	1.32	0x7B	1.48
0x1C	1.005	0x3C	1.165	0x5C	1.325	0x7C	1.485
0x1D	1.01	0x3D	1.17	0x5D	1.33	0x7D	1.49
0x1E	1.015	0x3E	1.175	0x5E	1.335	0x7E	1.495
0x1F	1.02	0x3F	1.18	0x5F	1.34	0x7F	1.5

9 Applications and Implementation

9.1 Application Information

The LM10507 device provides 4 regulated outputs from 3 step-down switching regulators and one linear regulator. The regulated outputs are achieved using a minimum of external components. The device outputs are controlled via an ENABLE input with control for a sleep mode via a further input, DEV_SLP.

A 4-wire SPI interface may be used to reconfigure the device outputs and return an indication of output status. A separate device output also provides a digital indication of output status. All programmed settings may be returned to default state via a RESET input.

9.2 Typical Application

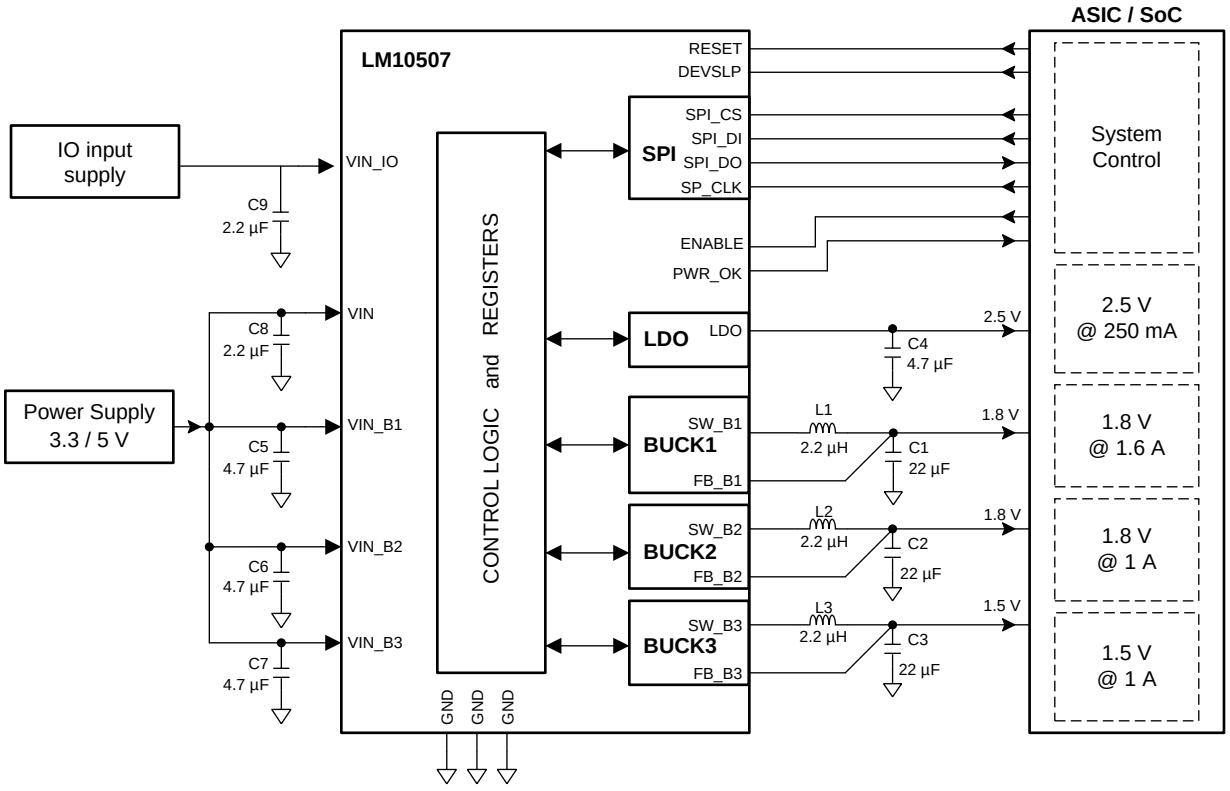


Figure 11. Typical Application Diagram

9.2.1 Design Requirements

Regulator	Default V_{OUT} DEVSLP=Low	Default V_{OUT} DEVSLP=High	V_{OUT} Range	Maximum Output Current
BUCK 1	1 V	OFF	0.9 – 3.4 V; 50mV steps	1.6 A
BUCK 2	1.8 V	OFF	0.9 – 3.4 V; 50mV steps	1 A
BUCK 3	1.5 V	1.5 V	0.865-1.5 V; 5mV steps	1 A
LDO	2.5 V	OFF	2.5 V	250 mA

Default voltage values are determined when working in PWM mode. Voltage may be 0.8-1.6% higher when in PFM mode.

9.2.2 Detailed Design Procedure

9.2.2.1 Input Voltage

VIN, VIN_B1, VIN_B2 and VIN_B3 must all be connected to the same power source.

9.2.2.2 Output Enable

For normal operation it is recommended that the ENABLE input is controlled via an independent voltage applied to the input.

To enable the device outputs at device power up the ENABLE input may be connected to the supply voltage either directly or via a divider to the input supply to ensure correct voltage within the specified range. In this case start up timing may vary from the specified values depending on the supply start up slew rate.

9.2.2.3 Recommendations for Unused Functions and Pins

If any function is not used in the end application then the following recommendations for tying-off the associated pins on the circuit boards should be used.

FUNCTION	PIN	IF UNUSED
BUCK1	VIN_B1	Connect to VIN
	SW_B1	Connect to VIN
	FB_B1	Connect to GND
BUCK2	VIN_B2	Connect to VIN
	SW_B2	Connect to VIN
	FB_B2	Connect to GND
BUCK3	VIN_B3	Connect to VIN
	SW_B3	Connect to VIN
	FB_B3	Connect to GND
SPI	SPI_CS	Connect to VIN_IO
	SPI_DI	Connect to GND
	SPI_DO	Connect to GND
	SPI_CK	Connect to GND
CONTROL and MONITOR	DEVSLP	Connect to GND
	RESET	Connect to VIN_IO
	PWR_OK	Leave open

9.2.2.4 External Components Selection

All three switchers require an input capacitor, and an output inductor-capacitor filter. These components are critical to the performance of the device. All three switchers are internally compensated and do not require external components to achieve stable operation. The output voltage of the Bucks can be programmed through the SPI terminals.

9.2.2.5 Output Inductors and Capacitors Selection

There are several design considerations related to the selection of output inductors and capacitors:

- Load transient response
- Stability
- Efficiency
- Output ripple voltage
- Over current ruggedness

The device has been optimized for use with nominal LC values as shown in the Application Diagram.

9.2.2.6 Inductor Selection

The recommended inductor values are shown in the Application Diagram. It is important to guarantee the inductor core does not saturate during any foreseeable operational situation. The inductor should be rated to handle the peak load current plus the ripple current: Care should be taken when reviewing the different saturation current ratings that are specified by different manufacturers. Saturation current ratings are typically specified at 25C, so ratings at maximum ambient temperature of the application should be requested from the manufacturer.

$$I_{L(MAX)} = I_{LOAD(MAX)} + \Delta I_{RIPPLE}$$

$$= I_{LOAD(MAX)} + \frac{D \times (V_{IN} - V_{OUT})}{2 \times L \times F_S}$$

$$\simeq I_{LOAD(MAX)} + \frac{D \times (V_{IN} - V_{OUT})}{2 \times 2.2 \times 2.0} \text{ (A typ.),}$$

$$D = \frac{V_{OUT}}{V_{IN}}, F_S = 2 \text{ MHz}, L = 2.2 \mu H$$

where

- $I_{L(MAX)}$: Max inductor Current
- $I_{LOAD(MAX)}$: Max load current
- I_{RIPPLE} : Peak-to-Peak inductor current
- D : Estimated duty factor
- V_{IN} : Input voltage
- V_{OUT} : Output voltage
- F_S : Switching frequency, Hertz

(2)

There are two methods to choose the inductor saturation current rating:

9.2.2.7 Recommended Method for Inductor Selection

The best way to guarantee the inductor does not saturate is to choose an inductor that has saturation current rating greater than the maximum device current limit, as specified in the Electrical Characteristics. In this case the device will prevent inductor saturation by going into current limit before the saturation level is reached.

9.2.2.8 Alternate Method for Inductor Selection

If the recommended approach cannot be used care must be taken to guarantee that the saturation current is greater than the peak inductor current:

$$I_{SAT} > IL_{PEAK}$$

$$IL_{PEAK} = I_{OUTMAX} + \frac{I_{RIPPLE}}{2}$$

$$I_{RIPPLE} = \frac{D \times (V_{IN} - V_{OUT})}{L \times F_S}$$

$$D = \frac{V_{OUT}}{V_{IN} \times EFF}$$

where

- I_{SAT} : Inductor saturation current at operating temperature
- I_{LPEAK} : Peak inductor current during worst case conditions
- I_{OUTMAX} : Maximum average inductor current
- I_{RIPPLE} : Peak-to-Peak inductor current
- V_{OUT} : Output voltage
- V_{IN} : Input voltage (V_{VIN_B1}, V_{VIN_B2}, V_{VIN_B3})
- L : Inductor value in Henries at I_{OUTMAX}
- F_S : Switching frequency, Hertz
- D : Estimated duty factor
- EFF : Estimated power supply efficiency (3)

I_{SAT} may not be exceeded during any operation, including transients, startup, high temperature, worst case conditions, etc.

9.2.2.9 Suggested Inductors and Their Suppliers

The designer should choose the inductors that best match the system requirements. A very wide range of inductors are available as regarding physical size, height, maximum current (thermally limited, and inductance loss limited), series resistance, maximum operating frequency, losses, etc. In general, smaller physical size inductors will have higher series resistance (DCR) and implicitly lower overall efficiency is achieved. Very low profile inductors may have even higher series resistance. The designer should try to find the best compromise between system performance and cost.

Table 1. Typical Recommended Inductors

Value	Mfr	Part Number	DCR	Current	Package
2.2µH	Murata	LQH55PN2R2NR0L	31mOhms	2.5A	2220
2.2µH	TDK	NLC565050T-2R2K-PF	60mOhms	1.3A	2220
2.2µH	Murata	LQM2MPN2R2NG0	110mOhms	1.2A	806
2.2uH	Vishay Dale	IFSC1008ABER2R2M01	80mOhms	1.85A	2.5 x 2.0
2.2uH	Taiyo Yuden	MAMK2520T2R2M	117mOhm	1.9A	2.5 x 2.0

9.2.2.10 Output and Input Capacitors Characteristics

Special attention should be paid when selecting these components. As shown in the following figure, the DC bias of these capacitors can result in a capacitance value that falls below the minimum value given in the recommended capacitor specifications table. Note that the graph shows the capacitance out of spec for the 0402 case size capacitor at higher bias voltages. It is therefore recommended that the capacitor manufacturers' specifications for the nominal value capacitor are consulted for all conditions, as some capacitor sizes (e.g. 0402) may not be suitable in the actual application.

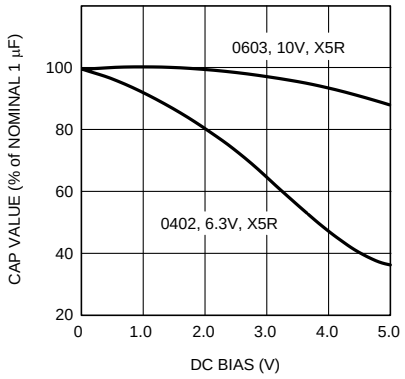


Figure 12. Typical Variation in Capacitance vs. DC Bias

The ceramic capacitor's actual capacitance can vary with temperature. The capacitor type X7R, which operates over a temperature range of −55°C to +125°C, will only vary the capacitance to within ±15%. The capacitor type X5R has a similar tolerance over a reduced temperature range of −55°C to +85°C. Many large value ceramic capacitors, larger than 1 µF are manufactured with Z5U or Y5V temperature characteristics. Their capacitance can drop by more than 50% as the temperature varies from 25°C to 85°C. Therefore X5R or X7R is recommended over Z5U and Y5V in applications where the ambient temperature will change significantly above or below 25°C.

Tantalum capacitors are less desirable than ceramic for use as output capacitors because they are more expensive when comparing equivalent capacitance and voltage ratings in the 0.47 µF to 44 µF range. Another important consideration is that tantalum capacitors have higher ESR values than equivalent size ceramics. This means that while it may be possible to find a tantalum capacitor with an ESR value within the stable range, it would have to be larger in capacitance (which means bigger and more costly) than a ceramic capacitor with the same ESR value. It should also be noted that the ESR of a typical tantalum will increase about 2:1 as the temperature goes from 25°C down to −40°C, so some guard band must be allowed.

9.2.2.11 Output Capacitor Selection

The output capacitor of a switching converter absorbs the AC ripple current from the inductor and provides the initial response to a load transient. The ripple voltage at the output of the converter is the product of the ripple current flowing through the output capacitor and the impedance of the capacitor. The impedance of the capacitor can be dominated by capacitive, resistive, or inductive elements within the capacitor, depending on the frequency of the ripple current. Ceramic capacitors have very low ESR and remain capacitive up to high frequencies. Their inductive component can be usually neglected at the frequency ranges the switcher operates.

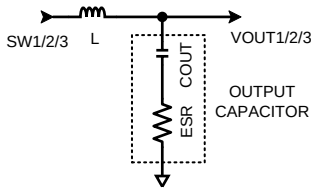


Figure 13. Output Filter

The output-filter capacitor smoothes out the current flow from the inductor to the load and helps maintain a steady output voltage during transient load changes. It also reduces output voltage ripple. These capacitors must be selected with sufficient capacitance and low enough ESR to perform these functions.

Note that the output voltage ripple increases with the inductor current ripple and the Equivalent Series Resistance of the output capacitor (ESR_{COUT}). Also note that the actual value of the capacitor's ESR_{COUT} is frequency and temperature dependent, as specified by its manufacturer. The ESR should be calculated at the applicable switching frequency and ambient temperature.

$$V_{OUT\text{-}RIPPLE\text{-}PP} = \frac{\Delta I_{RIPPLE}}{8 \times F_S \times C_{OUT}} \text{ where } \Delta I_{RIPPLE} = \frac{D \times (V_{IN} - V_{OUT})}{2 \times L \times F_S} \text{ and } D = \frac{V_{OUT}}{V_{IN}}$$

where

- $V_{OUT\text{-}RIPPLE\text{-}PP}$: estimated output voltage ripple
- I_{RIPPLE} : estimated current ripple
- D : Estimated duty factor (4)

Output ripple can be estimated from the vector sum of the reactive (capacitance) voltage component and the real (ESR) voltage component of the output capacitor:

$$V_{OUT\text{-}RIPPLE\text{-}PP} = \sqrt{V^2_{ROUT} + V^2_{COUT}} \quad (5)$$

$$V_{ROUT} = I_{RIPPLE} \times ESR_{COUT} \text{ and } V_{COUT} = \frac{I_{RIPPLE}}{8 \times F_S \times C_{OUT}}$$

where

- $V_{OUT\text{-}RIPPLE\text{-}PP}$: estimated output ripple,
- V_{ROUT} : estimated real output ripple,
- V_{COUT} : estimated reactive output ripple. (6)

The device is designed to be used with ceramic capacitors on the outputs of the buck regulators. The recommended dielectric type of these capacitors is X5R, X7R, or of comparable material to maintain proper tolerances over voltage and temperature. The recommended value for the output capacitors is 22 µF, 6.3V with an ESR of 2mΩ or less. The output capacitors need to be mounted as close as possible to the output/ground terminals of the device.

Table 2. Typical Recommended Output Capacitors

Model	Vendor Type	Vendor	Voltage Rating	Inch (mm) Case Size
08056D226MAT2A	Ceramic, X5R	AVX Corporation	6.3 V	0805, (2012)
C0805L226M9PACTU	Ceramic, X5R	Kemet	6.3 V	0805, (2012)
ECJ-2FB0J226M	Ceramic, X5R	Panasonic – ECG	6.3 V	0805, (2012)
JMK212BJ226MG-T	Ceramic, X5R	Taiyo Yuden	6.3 V	0805, (2012)
C2012X5R0J226M	Ceramic, X5R	TDK Corporation	6.3 V	0805, (2012)
GRM188R60G226MEA0L	Ceramic, X5R	Murata	4.0 V	0603

9.2.2.12 Input Capacitor Selection

There are 3 buck regulators in the LM10507 device. Each of these buck regulators has its own input capacitor which should be located as close as possible to their corresponding VIN_Bx and GND_Bx terminals, where x designates the buck 1,2 or 3. The 3 buck regulators operate at 120o out of phase, which means that is they switch on at equally spaced intervals, in order to reduce the input power rail ripple. It is recommended to connect all the supply/ground terminals of the buck regulators, VIN_Bx to two solid internal planes located under the device. In this way, the 3 input capacitors work together and further reduce the input current ripple. A larger tantalum capacitor can also be located in the proximity of the device.

The input capacitor supplies the AC switching current drawn from the switching action of the internal power FETs. The input current of a buck converter is discontinuous, so the ripple current supplied by the input capacitor is large. The input capacitor must be rated to handle both the RMS current and the dissipated power.

The input capacitor must be rated to handle this current:

$$I_{RMS\_CIN} = I_{OUT} \frac{\sqrt{V_{OUT}(V_{IN} - V_{OUT})}}{V_{IN}} \quad (7)$$

The power dissipated in the input capacitor is given by:

$$P_{D\_CIN} = I^2_{RMS\_CIN} \times R_{ESR\_CIN} \quad (8)$$

The device is designed to be used with ceramic capacitors on the inputs of the buck regulators. The recommended dielectric type of these capacitors is X5R, X7R, or of comparable material to maintain proper tolerances over voltage and temperature.

The minimum recommended value for the input capacitor is 10 µF with an ESR of 10 mΩ or less. The input capacitors need to be mounted as close as possible to the power/ground input terminals of the device.

The input power source supplies the average current continuously. During the PFET switch on-time, however, the demanded di/dt is higher than can be typically supplied by the input power source. This delta is supplied by the input capacitor.

A simplified “worst case” assumption is that all of the PFET current is supplied by the input capacitor. This will result in conservative estimates of input ripple voltage and capacitor RMS current.

Input ripple voltage is estimated as follows:

$$V_{PPIN} = \frac{I_{OUT} \times D}{C_{IN} \times F_S} + I_{OUT} \times ESR_{CIN}$$

where

- V_{PPIN} : Estimated peak-to-peak input ripple voltage
- I_{OUT} : Output current
- C_{IN} : Input capacitor value
- ESR_{IN} Input capacitor ESR (9)

This capacitor is exposed to significant RMS current, so it is important to select a capacitor with an adequate RMS current rating. Capacitor RMS current estimated as follows:

$$I_{RMSCIN} = \sqrt{D \times \left(I^2_{OUT} + \frac{I^2_{RIPPLE}}{12} \right)}$$

where

- I_{RMSCIN} Estimated input capacitor RMS current (10)

9.2.3 Application Performance Plots

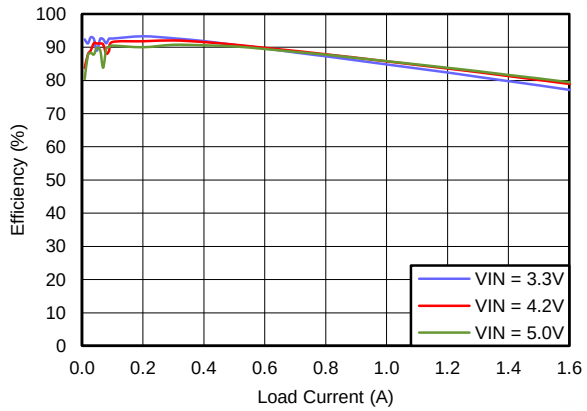


Figure 14. Efficiency Buck 1

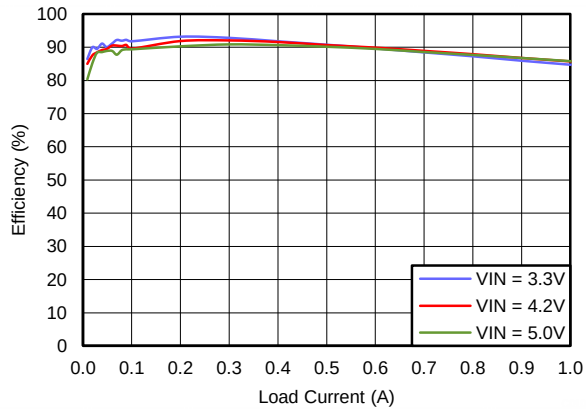


Figure 15. Efficiency Buck 2

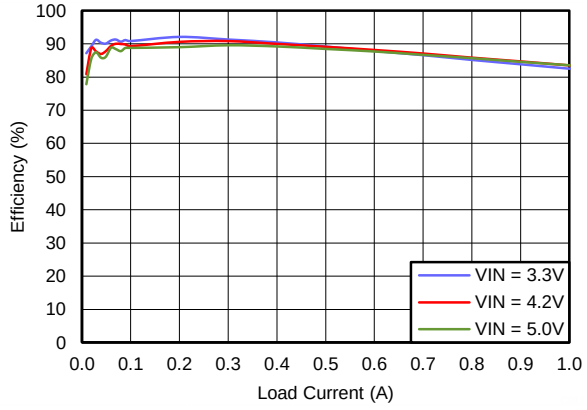


Figure 16. Efficiency Buck 3

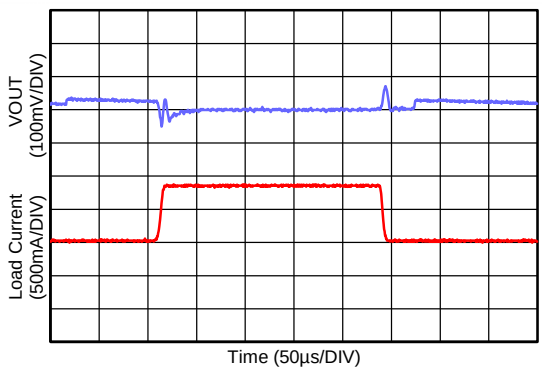


Figure 17. Buck 1 Load Transient (0 to 800mA)

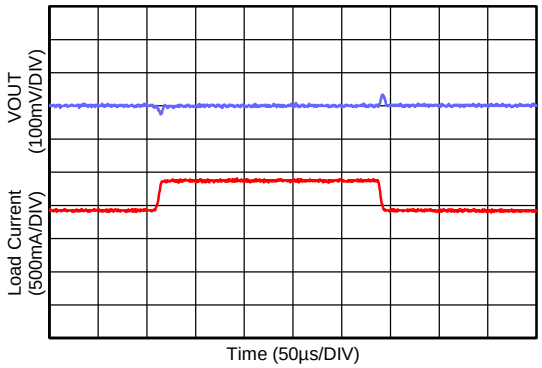


Figure 18. Buck 1 Load Transient (800mA to 1.6A)

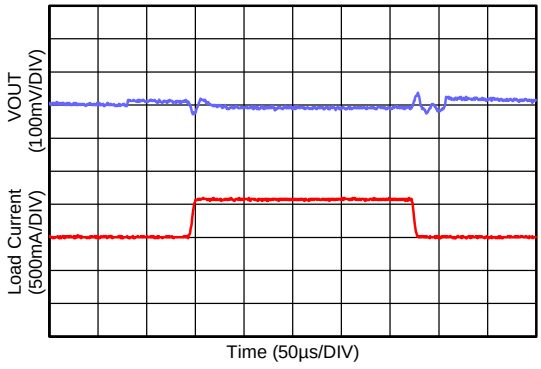


Figure 19. Buck 2 Load Transient (0 to 500mA)

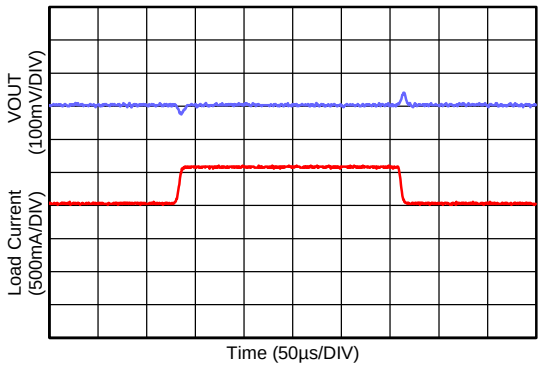


Figure 20. Buck 2 Load Transient (500mA to 1A)

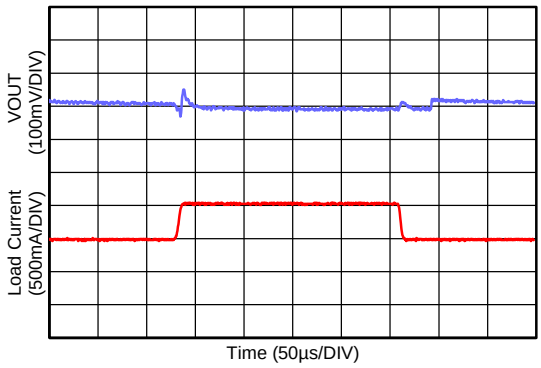


Figure 21. Buck 3 Load Transient (0 to 500mA)

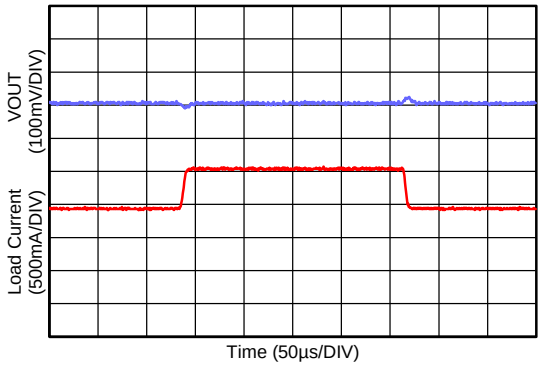


Figure 22. Buck 3 Load Transient (500mA to 1A)

10 Power Supply Recommendations

The devices are designed to operate from an input voltage supply range between 4.5 V and 28 V. This input supply must be well regulated. If the input supply is located more than a few inches from the GDS9999 device or GDS9991 converter, additional bulk capacitance may be required in addition to the ceramic bypass capacitors. An electrolytic capacitor with a value of 47 µF is a typical choice.

11 Layout

11.1 Layout Guidelines

PC board layout is an important part of DC-DC converter design. Poor board layout can disrupt the performance of a DC-DC converter and surrounding circuitry by contributing to EMI, ground bounce, and resistive voltage loss in the traces. These can send erroneous signals to the DC-DC converter resulting in poor regulation or instability. Good layout can be implemented by following a few simple design rules.

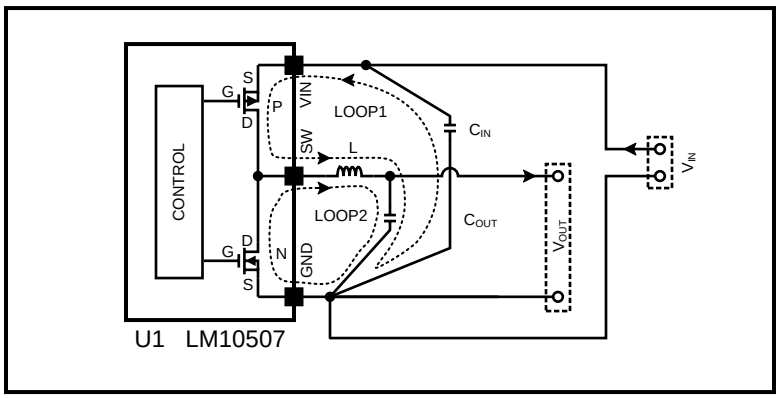


Figure 23. Schematic of LM10507 Highlighting Layout Sensitive Nodes

1. Minimize area of switched current loops. In a buck regulator there are two loops where currents are switched rapidly. The first loop starts from the CIN input capacitor, to the regulator VIN terminal, to the regulator SW terminal, to the inductor then out to the output capacitor COUT and load. The second loop starts from the output capacitor ground, to the regulator GND terminals, to the inductor and then out to COUT and the load (see Figure 23). To minimize both loop areas the input capacitor should be placed as close as possible to the VIN terminal. Grounding for both the input and output capacitors should consist of a small localized top side plane that connects to GND. The inductor should be placed as close as possible to the SW pin and output capacitor.
2. Minimize the copper area of the switch node. The SW terminals should be directly connected with a trace that runs on top side directly to the inductor. To minimize IR losses this trace should be as short as possible and with a sufficient width. However, a trace that is wider than 100 mils will increase the copper area and cause too much capacitive loading on the SW terminal. The inductors should be placed as close as possible to the SW terminals to further minimize the copper area of the switch node.
3. Have a single point ground for all device analog grounds. The ground connections for the feedback components should be connected together then routed to the GND pin of the device. This prevents any switched or load currents from flowing in the analog ground plane. If not properly handled, poor grounding can result in degraded load regulation or erratic switching behavior.
4. Minimize trace length to the FB terminal. The feedback trace should be routed away from the SW pin and inductor to avoid contaminating the feedback signal with switch noise.
5. Make input and output bus connections as wide as possible. This reduces any voltage drops on the input or output of the converter and can improve efficiency. If voltage accuracy at the load is important make sure feedback voltage sense is made at the load. Doing so will correct for voltage drops at the load and provide the best output accuracy.

11.1.1 PCB Layout Thermal Dissipation for DSBGA Package

1. Position ground layer as close as possible to uSMD package. Second PCB layer is usually good option. LM10507 evaluation board is a good example.
2. Draw power traces as wide as possible. Bumps which pass through high currents should be connected to wide area this helps the silicon to cool down. Look at LM10507 evaluation board PCB layout for reference

Packaging Information

34 pin uSMD Package, 0.4mm pitch

The dimension for X1, X2 and X3 are as given:

Layout Guidelines (continued)

X1 = 2.815 mm + / - 0.030 mm
X2 = 2.815 mm + / - 0.030 mm
X3 = 0.600 mm + / - 0.075 mm

11.2 Layout Example

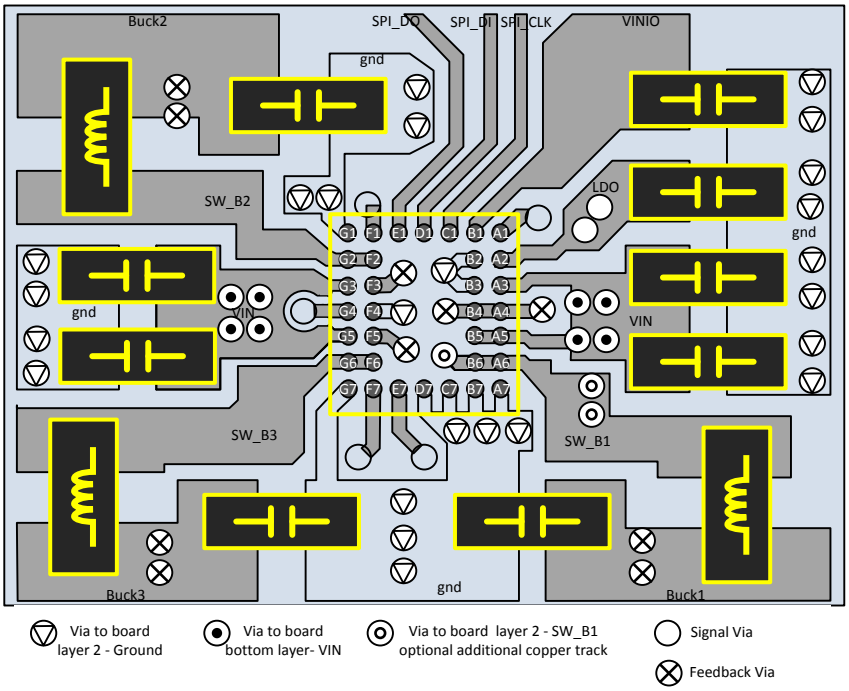


Figure 24. Example of PCB Layout Configuration

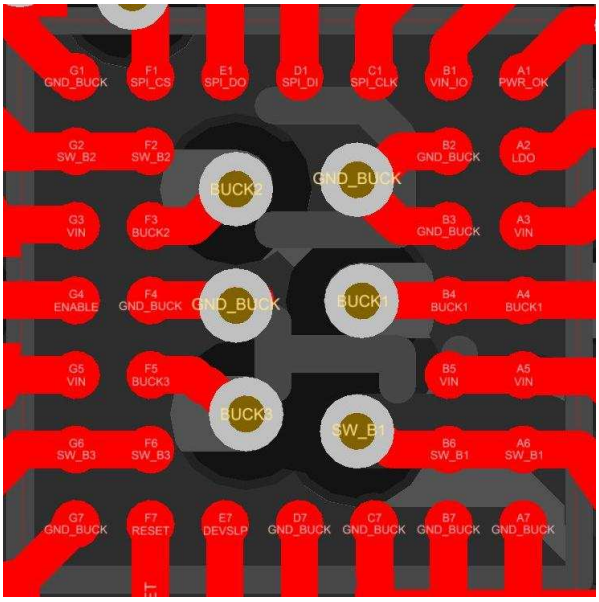


Figure 25. Detail of Device Pins and Centre Vias

12 Device and Documentation Support

12.1 Trademarks

All trademarks are the property of their respective owners.

12.2 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.3 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM10507TME-A/NOPB	NRND	DSBGA	YFR	34	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-30 to 125	V087	
LM10507TMX-A/NOPB	NRND	DSBGA	YFR	34	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-30 to 125	V087	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

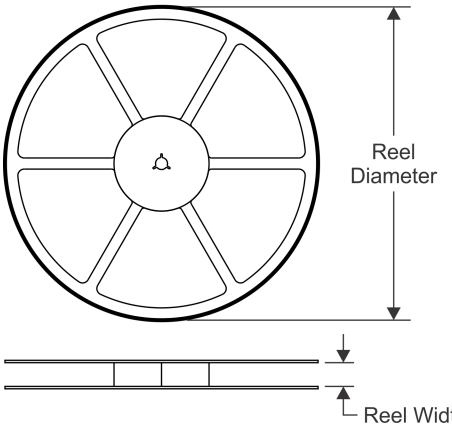
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

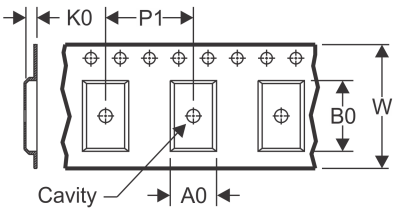
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

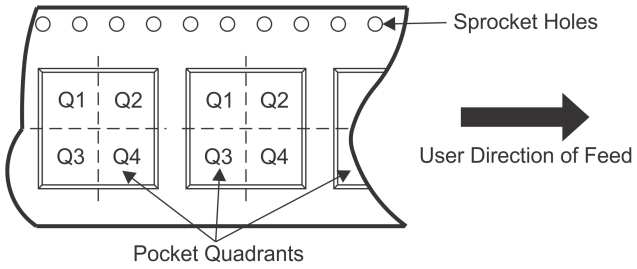


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

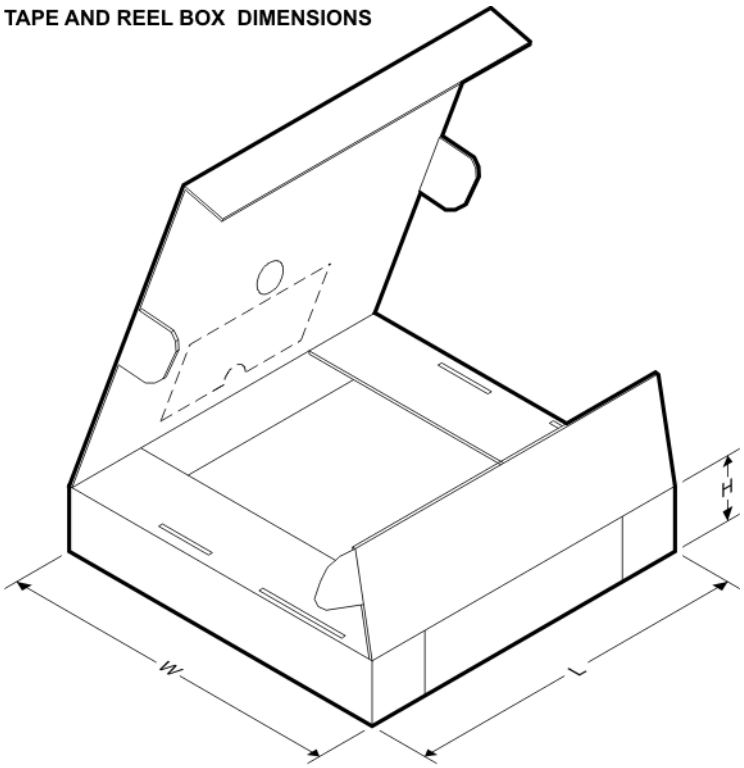
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM10507TME-A/NOPB	DSBGA	YFR	34	250	178.0	8.4	3.02	3.02	0.76	4.0	8.0	Q1
LM10507TMX-A/NOPB	DSBGA	YFR	34	3000	178.0	8.4	3.02	3.02	0.76	4.0	8.0	Q1

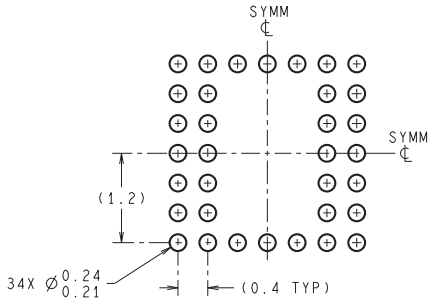
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

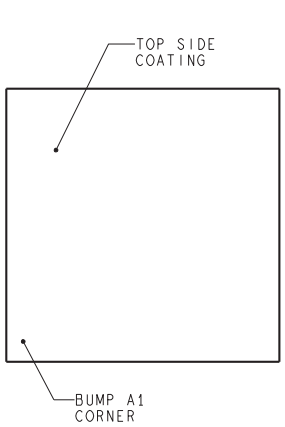
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM10507TME-A/NOPB	DSBGA	YFR	34	250	210.0	185.0	35.0
LM10507TMX-A/NOPB	DSBGA	YFR	34	3000	210.0	185.0	35.0

YFR0034

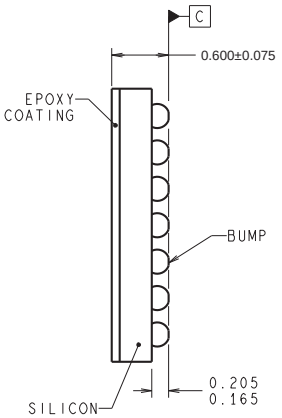


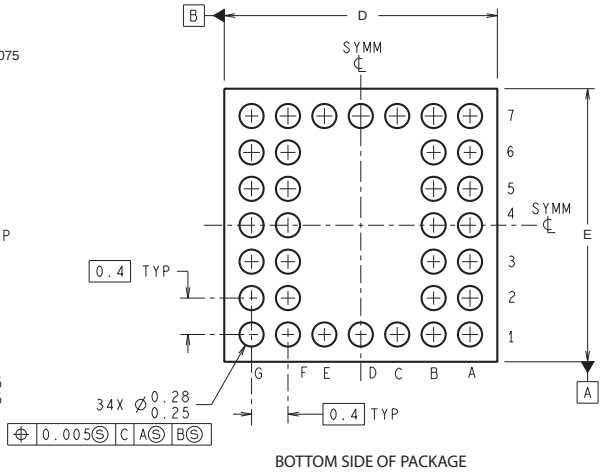
DIMENSIONS ARE IN MILLIMETERS
DIMENSIONS IN ( ) FOR REFERENCE ONLY

LAND PATTERN RECOMMENDATION



TOP SIDE OF PACKAGE





BOTTOM SIDE OF PACKAGE

TME34XXX (Rev B)

D: Max = 2.84 mm, Min = 2.78 mm

E: Max = 2.84 mm, Min = 2.78 mm

4215092/A 12/12

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale (www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265