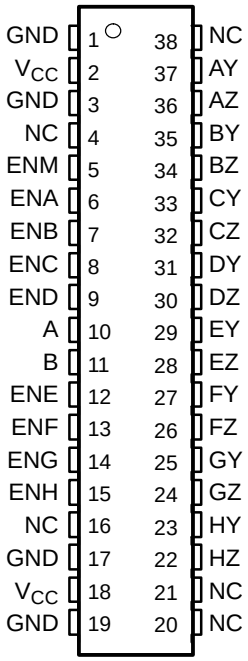
# 8-PORT LVDS REPEATER

## FEATURES

- **One Line Receiver and Eight Line Drivers Configured as an 8-Port LVDS Repeater**
- **Line Receiver and Line Drivers Meet or Exceed the Requirements of ANSI EIA/TIA-644 Standard**
- **Typical Data Signaling Rates to 400 Mbps or Clock Frequencies to 400 MHz**
- **Enabling Logic Allows Individual Control of Each Driver Output, Plus All Outputs**
- **Low-Voltage Differential Signaling With Typical Output Voltage of 350 mV and a 100-Ω Load**
- **Electrically Compatible With LVDS, PECL, LVPECL, LVTTL, LVCMOS, GTL, BTL, CTT, SSTL, or HSTL Outputs With External Termination Networks**
- **Propagation Delay Times < 4.7 ns**
- **Output Skew Less Than 300 ps and Part-to-Part Skew Less Than 1.5 ns**
- **Total Power Dissipation at 200 MHz Typically Less Than 330 mW With 8 Channels Enabled**
- **Driver Outputs or Receiver Input Equals High Impedance When Disabled or With $V_{CC}$ < 1.5 V**
- **Bus-Pin ESD Protection Exceeds 12 kV**
- **Packaged in Thin Shrink Small-Outline Package With 20-Mil Terminal Pitch**

**DBT PACKAGE**
**(TOP VIEW)**




NC – No internal connection

## DESCRIPTION

The SN65LVDS108 is configured as one differential line receiver connected to eight differential line drivers. Individual output enables are provided for each output and an additional enable is provided for all outputs.

The line receivers and line drivers implement the electrical characteristics of low-voltage differential signaling (LVDS). LVDS, as specified in EIA/TIA-644, is a data signaling technique that offers low power, low noise emission, high noise immunity, and high switching speeds. (Note: The ultimate rate and distance of data transfer is dependent upon the attenuation characteristics of the media, the noise coupling to the environment, and other system characteristics.)

The intended application of this device, and the LVDS signaling technique, is for point-to-point or point-to-multipoint (distributed simplex) baseband data transmission on controlled impedance media of approximately 100 Ω. The transmission media may be printed-circuit board traces, backplanes, or cables. The large number of drivers integrated into the same silicon substrate, along with the low pulse skew of balanced signaling, provides extremely precise timing alignment of the signals being repeated from the inputs. This is particularly advantageous for implementing system clock or data distribution trees.

The SN65LVDS108 is characterized for operation from –40°C to 85°C.

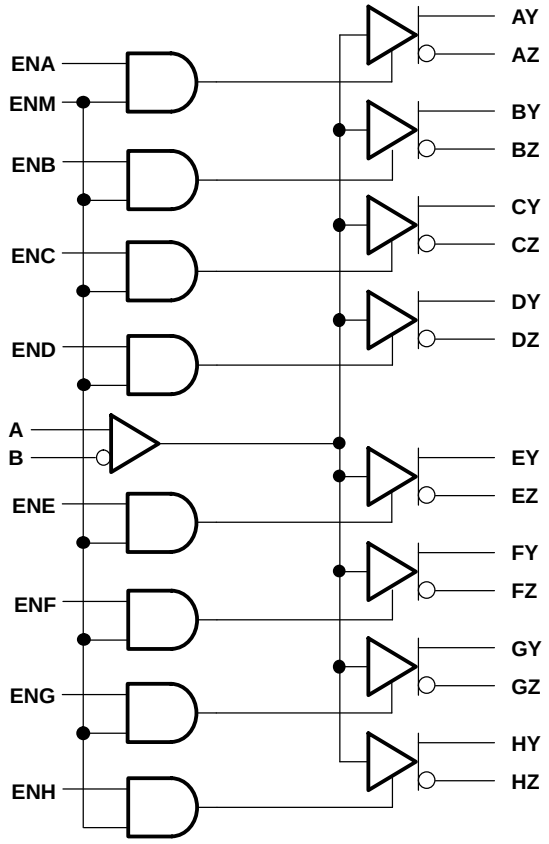
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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## LOGIC DIAGRAM (POSITIVE LOGIC)




## SELECTION GUIDE TO LVDS SPLITTER

The SN65LVDS108 is one member of a family of LVDS splitters and repeaters. A brief overview of the family is provided in the following table.

### LVDS SPLITTER AND REPEATER FAMILY

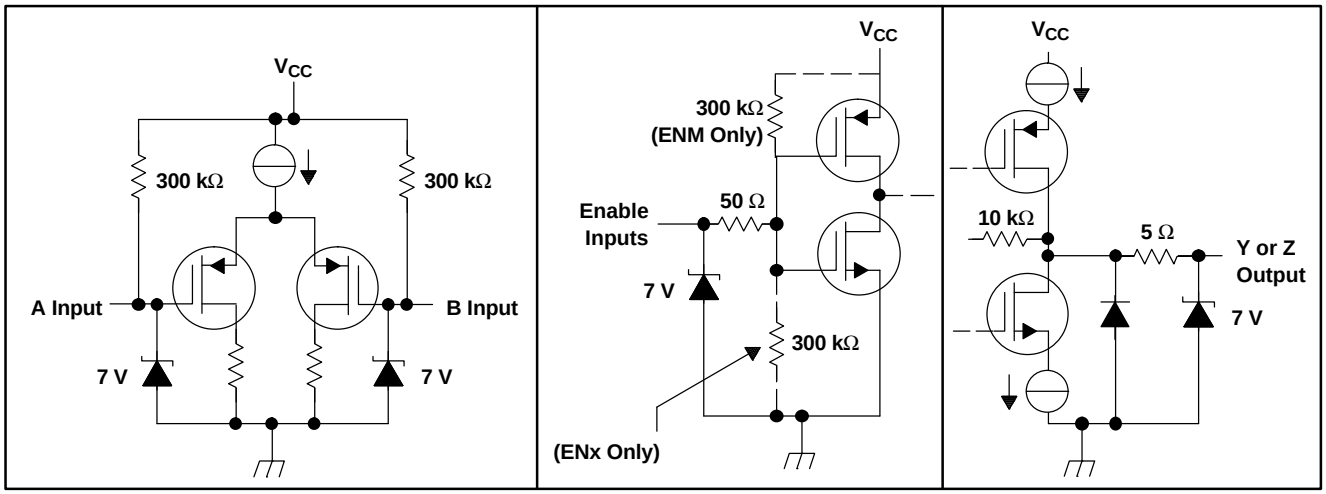
| DEVICE | NUMBER OF INPUTS | NUMBER OF OUTPUTS | PACKAGE | COMMENTS |
|---|---|---|---|---|
| SN65LVDS104 | 1 LVDS | 4 LVDS | 16-pin D | 4-Port LVDS repeater |
| SN65LVDS105 | 1 LVTTL | 4 LVDS | 16-pin D | 4-Port TTL-to-LVDS repeater |
| SN65LVDS108 | 1 LVDS | 8 LVDS | 38-pin DBT | 8-Port LVDS repeater |
| SN65LVDS109 | 2 LVDS | 8 LVDS | 38-pin DBT | Dual 4-port LVDS repeater |
| SN65LVDS116 | 1 LVDS | 16 LVDS | 64-pin DGG | 16-Port LVDS repeater |
| SN65LVDS117 | 2 LVDS | 16 LVDS | 64-pin DGG | Dual 8-port LVDS repeater |

## FUNCTION TABLE(1)

| INPUTS | | | OUTPUTS | |
|---|---|---|---|---|
| $V_{ID} = V_A - V_B$ | ENM | ENx | $\overline{xY}$ | $\overline{xZ}$ |
| X | L | X | Z | Z |
| X | X | L | Z | Z |
| $V_{ID} \geq 100$ mV | H | H | H | L |
| $-100$ mV $< V_{ID} < 100$ mV | H | H | ? | ? |
| $V_{ID} \leq -100$ mV | H | H | L | H |

(1) H = high level, L = low level, Z = high impedance, X = don't care, ? = indeterminate

## EQUIVALENT INPUT AND OUTPUT SCHEMATIC DIAGRAMS




## ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

| | | | UNIT |
|---|---|---|---|
| $V_{CC}$ | Supply voltage range(2) | | –0.5 V to 4 V |
| | Input voltage range | Enable inputs | –0.5 V to 6 V |
| | | A, B, Y or Z | –0.5 V to 4 V |
| | Electrostatic discharge, A, B, Y, Z, and GND(3) | | Class 3, A:12 kV, B: 500 V |
| | Continuous power dissipation | | See Dissipation Rating Table |
| | Storage temperature range | | –65°C to 150°C |
| | Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds | | 260°C |

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.
(3) Tested in accordance with MIL-STD-883C Method 3015.7.

## DISSIPATION RATING TABLE

| PACKAGE | $T_A \leq 25°C$ POWER RATING | DERATING FACTOR(1) ABOVE $T_A = 25°C$ | $T_A = 85°C$ POWER RATING |
|---|---|---|---|
| DBT | 1277 mW | 10.2 mW/°C | 644 mW |

(1) This is the inverse of the junction-to-ambient thermal resistance when board-mounted (low-k) with no air flow.

## RECOMMENDED OPERATING CONDITIONS

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | 3 | 3.3 | 3.6 | V |
| $V_{IH}$ | High-level input voltage | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | V |
| $V_I$ or $V_{IC}$ | Voltage at any bus terminal (separately or common-mode) | 0 | | $V_{CC}$– 0.8 | V |
| $T_A$ | Operating free-air temperature | 40 | | 85 | °C |

## ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP(1) | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{ITH+}$ | Positive-going differential input voltage threshold | See Figure 1 and Table 1 | | | 100 | mV |
| $V_{ITH-}$ | Negative-going differential input voltage threshold | | 100 | | | |
| $\|V_{OD}\|$ | Differential output voltage magnitude | $R_L$ = 100 Ω, $V_{ID}$ = ±100 mV, See Figure 1 and Figure 2 | 247 | 340 | 454 | mV |
| $\Delta\|V_{OD}\|$ | Change in differential output voltage magnitude between logic states | | 50 | | 50 | |
| $V_{OC(SS)}$ | Steady-state common-mode output voltage | See Figure 3 | 1.125 | | 1.375 | V |
| $\Delta V_{OC(SS)}$ | Change in steady-state common-mode output voltage between logic states | | 50 | | 50 | mV |
| $V_{OC(PP)}$ | Peak-to-peak common-mode output voltage | | | 50 | 150 | |
| $I_{CC}$ | Supply current | Enabled, $R_L$ = 100 Ω | | 62 | 85 | mA |
| | | Disabled | | 8 | 12 | |
| $I_I$ | Input current (A or B inputs) | $V_I$ = 0 V | 2 | | 20 | µA |
| | | $V_I$ = 2.4 V | 1.2 | | | |
| $I_{I(OFF)}$ | Power-off input current (A or B inputs) | $V_{CC}$ = 1.5 V, $V_I$ = 2.4 V | | | 20 | µA |
| $I_{IH}$ | High-level input current (enables) | $V_{IH}$ = 2 V | | | ±20 | µA |
| $I_{IL}$ | Low-level input current (enables) | $V_{IL}$ = 0.8 V | | | ±10 | µA |
| $I_{OS}$ | Short-circuit output current | $V_{OY}$ or $V_{OZ}$ = 0 V | | | ±24 | mA |
| | | $V_{OD}$ = 0 V | | | ±12 | |
| $I_{OZ}$ | High-impedance output current | $V_O$ = 0 V or $V_{CC}$ | | | ±1 | µA |
| $I_{O(OFF)}$ | Power-off output current | $V_{CC}$ = 1.5 V, $V_O$ = 3.6 V | | | ±1 | µA |
| $C_{IN}$ | Input capacitance (A or B inputs) | $V_I$ = 0.4 sin (4E6πt) + 0.5 V | | 5 | | pF |
| $C_O$ | Output capacitance (Y or Z outputs) | $V_I$ = 0.4 sin (4E6πt) + 0.5 V, Disabled | | 9.4 | | |

(1) All typical values are at 25°C and with a 3.3-V supply.

## SWITCHING CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP(1) | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{PLH}$ | Propagation delay time, low-to-high-level output | $R_L$ = 100 Ω, $C_L$ = 10 pF, See Figure 4 | 1.6 | 2.8 | 4.5 | ns |
| $t_{PHL}$ | Propagation delay time, high-to-low-level output | | 1.6 | 2.8 | 4.5 | |
| $t_r$ | Differential output signal rise time | | 0.3 | 0.8 | 1.2 | ns |
| $t_f$ | Differential output signal fall time | | 0.3 | 0.8 | 1.2 | |
| $t_{sk(p)}$ | Pulse skew ($\lvert t_{PHL} - t_{PLH} \rvert$)(2) | | | 150 | 500 | ps |
| $t_{sk(o)}$ | Output skew(3) | | | | 300 | |
| $t_{sk(pp)}$ | Part-to-part skew(4) | | | | 1.5 | ns |
| $t_{PZH}$ | Propagation delay time, high-impedance-to-high-level output | See Figure 5 | | 5.7 | 15 | ns |
| $t_{PZL}$ | Propagation delay time, high-impedance-to-low-level output | | | 7.7 | 15 | |
| $t_{PHZ}$ | Propagation delay time, high-level-to-high-impedance output | | | 3.2 | 15 | |
| $t_{PLZ}$ | Propagation delay time, low-level-to-high-impedance output | | | 3.2 | 15 | ns |

(1) All typical values are at 25°C and with a 3.3-V supply.
(2) $t_{sk(p)}$ is the magnitude of the time difference between the $t_{PLH}$ and $t_{PHL}$ of any output of a single device.
(3) $t_{sk(o)}$ is the magnitude of the time difference between the $t_{PLH}$ or $t_{PHL}$ measured at any two outputs.
(4) $t_{sk(pp)}$ is the magnitude of the time difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.

## PARAMETER MEASUREMENT INFORMATION

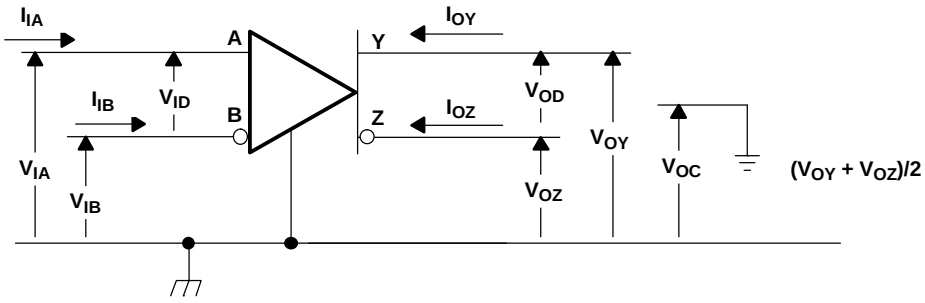



**Figure 1. Voltage and Current Definitions**

**Table 1. Receiver Minimum and Maximum Input Threshold Test Voltages**

| APPLIED VOLTAGES | | RESULTING DIFFERENTIAL INPUT VOLTAGE | RESULTING COMMON-MODE INPUT VOLTAGE |
|---|---|---|---|
| $V_{IA}$ | $V_{IB}$ | $V_{ID}$ | $V_{IC}$ |
| 1.25 V | 1.15 V | 100 mV | 1.2 V |
| 1.15 V | 1.25 V | –100 mV | 1.2 V |
| 2.4 V | 2.3 V | 100 mV | 2.35 V |
| 2.3 V | 2.4 V | –100 mV | 2.35 V |
| 0.1 V | 0 V | 100 mV | 0.05 V |
| 0 V | 0.1 V | –100 mV | 0.05 V |
| 1.5 V | 0.9 V | 600 mV | 1.2 V |
| 0.9 V | 1.5 V | –600 mV | 1.2 V |
| 2.4 V | 1.8 V | 600 mV | 2.1 V |
| 1.8 V | 2.4 V | –600 mV | 2.1 V |
| 0.6 V | 0 V | 600 mV | 0.3 V |
| 0 V | 0.6 V | –600 mV | 0.3 V |

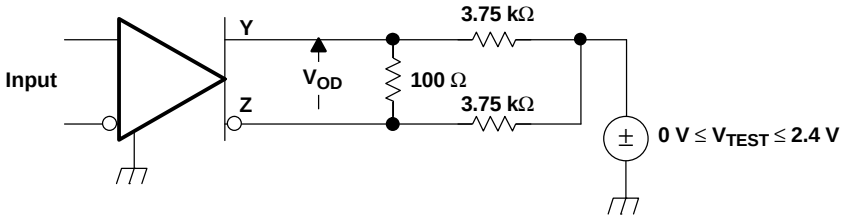
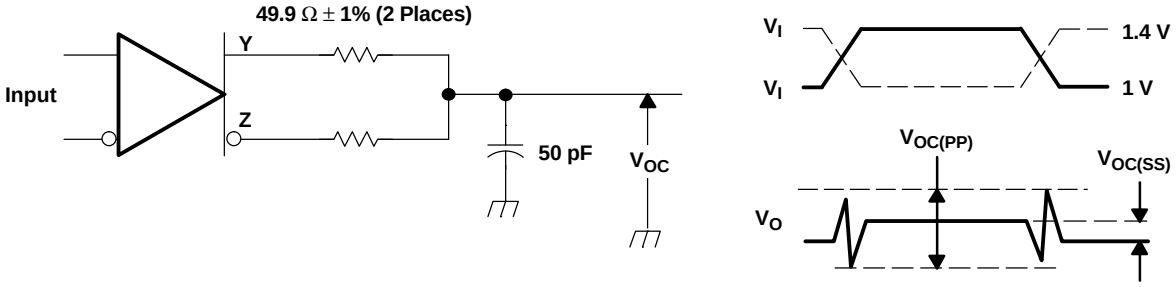
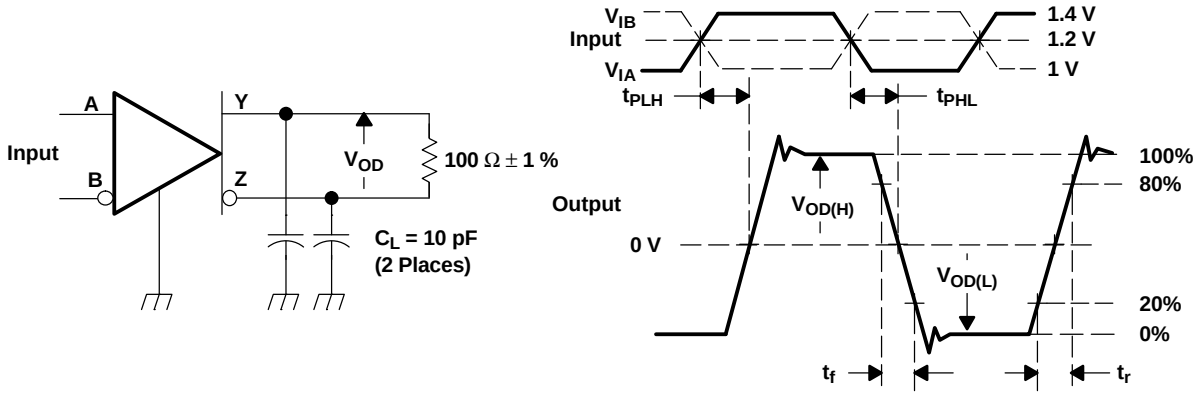



**Figure 2. $V_{OD}$ Test Circuit**



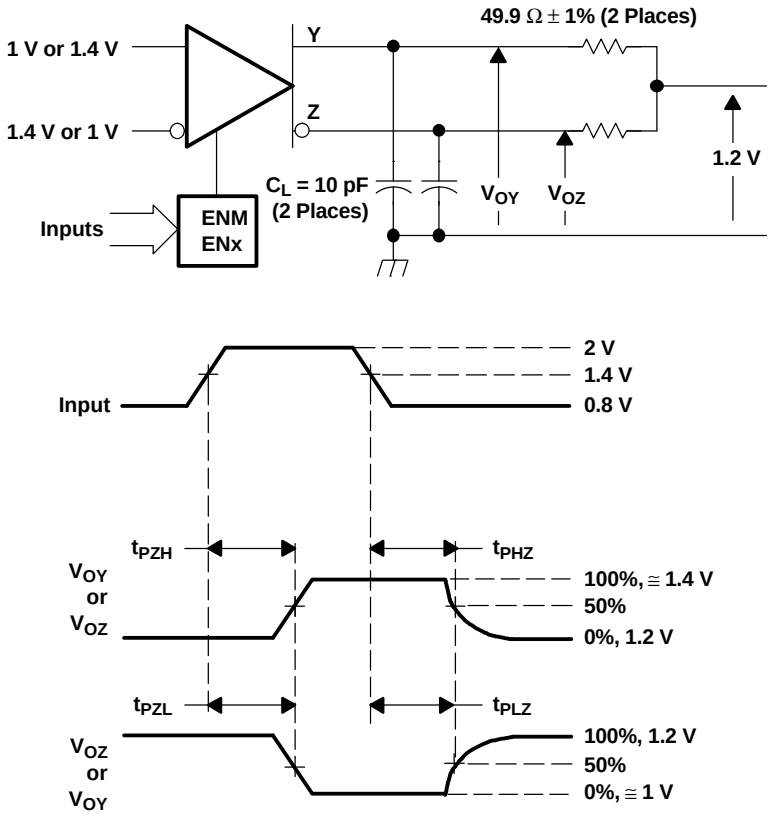

A. All input pulses are supplied by a generator having the following characteristics: $t_r$ or $t_f$ ≤ 1 ns, pulse repetition rate (PRR) = 0.5 Mpps, pulsewidth = 500 ±10 ns. $C_L$ includes instrumentation and fixture capacitance within 0,06 mm of the D.U.T. The measurement of $V_{OC(PP)}$ is made on test equipment with a –3 dB bandwidth of at least 300 MHz.

**Figure 3. Test Circuit and Definitions for the Driver Common-Mode Output Voltage**




A. All input pulses are supplied by a generator having the following characteristics: $t_r$ or $t_f$≤ 1 ns, pulse repetition rate (PRR) = 50 Mpps, pulsewidth = 10 ±0.2 ns . $C_L$ includes instrumentation and fixture capacitance within 0,06 mm of the D.U.T.

**Figure 4. Test Circuit, Timing, and Voltage Definitions for the Differential Output Signal**




A. All input pulses are supplied by a generator having the following characteristics: $t_r$ or $t_f \leq 1$ ns, pulse repetition rate (PRR) = 0.5 Mpps, pulsewidth = 500 ±10 ns . $C_L$ includes instrumentation and fixture capacitance within 0,06 mm of the D.U.T.

**Figure 5. Enable and Disable Time Circuit and Definitions**

## TYPICAL CHARACTERISTICS

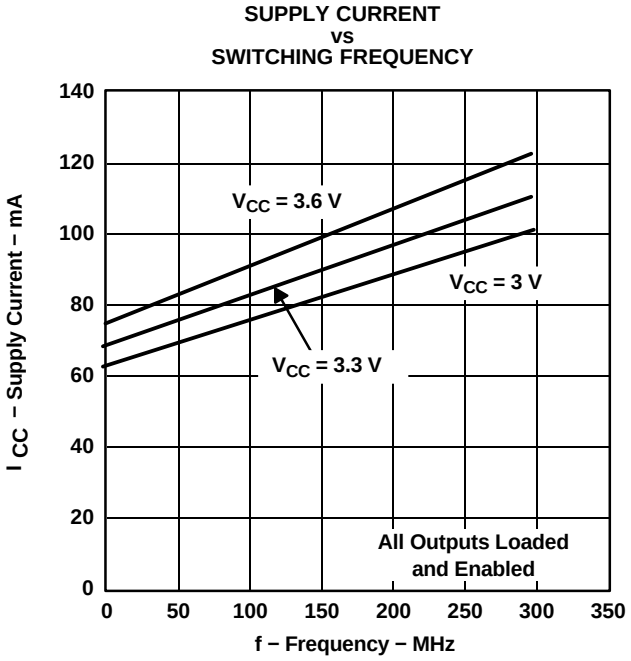



Figure 6.

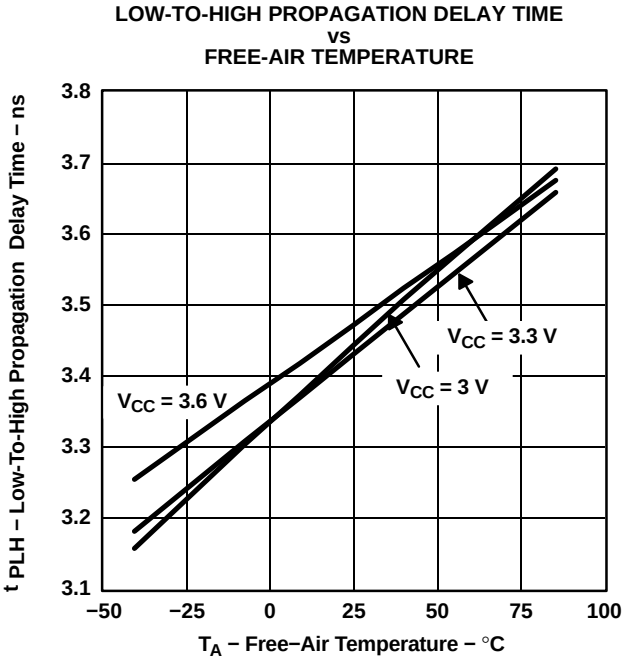



Figure 7.

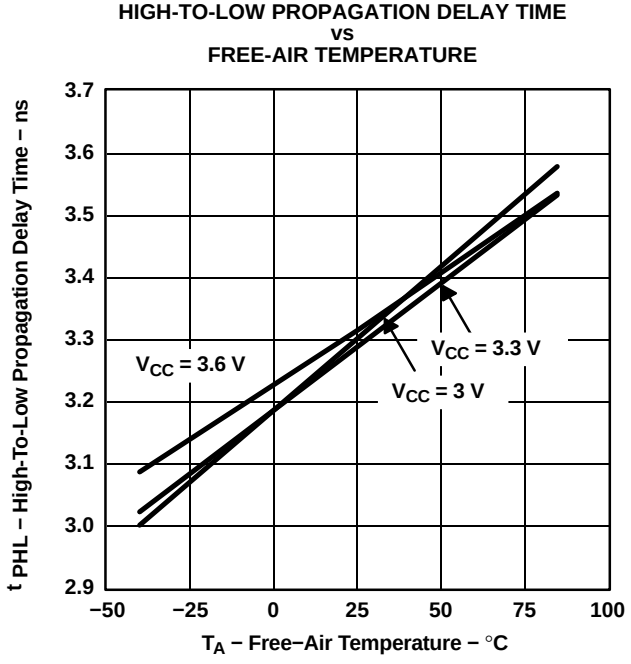



Figure 8.

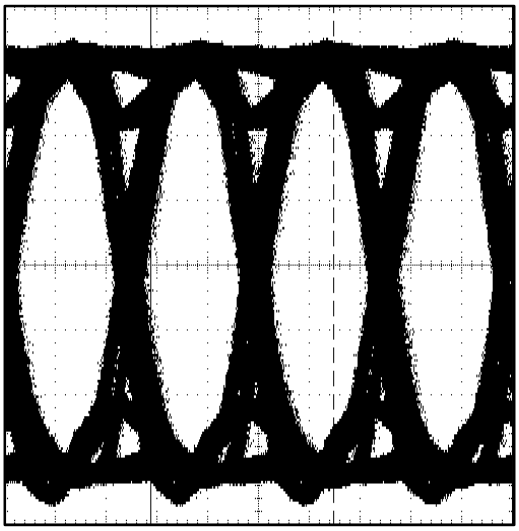
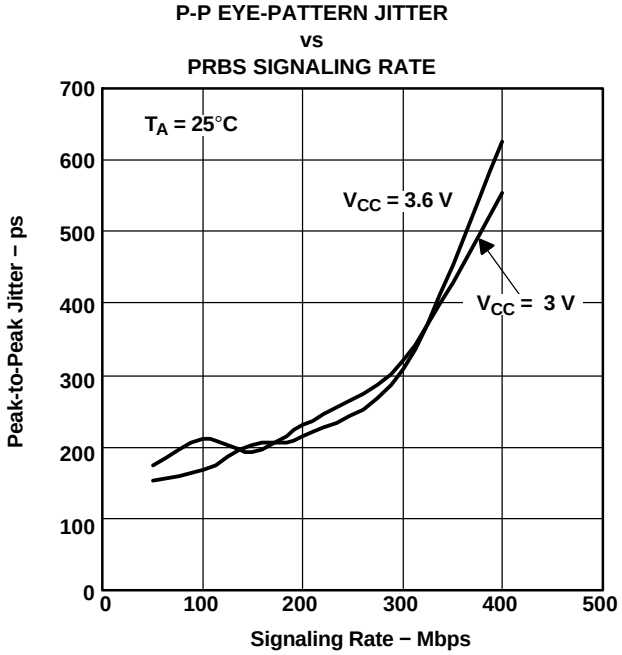


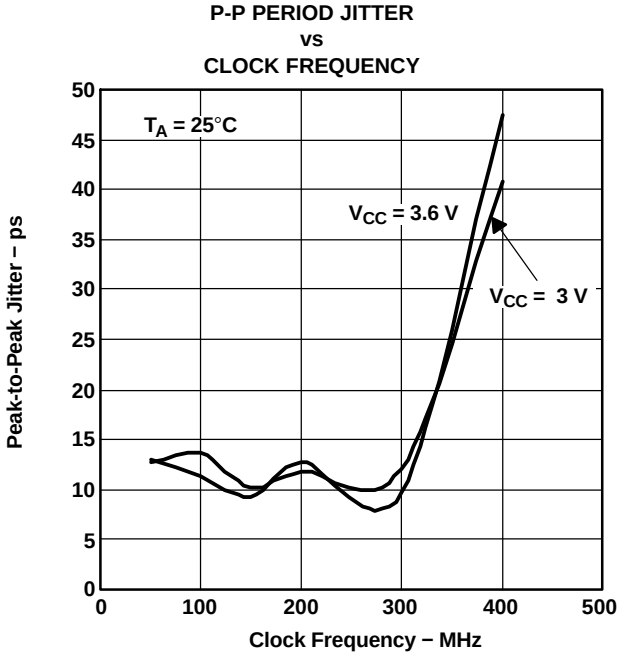
Figure 9. Typical Differential Eye Pattern at 400 Mbps

## TYPICAL CHARACTERISTICS (continued)




NOTES: Input: $2^{15}$ PRBS with peak-to-peak jitter < 100 ps at 100 Mbps, all outputs enabled and loaded with differential 100-Ω loads, worst-case output, supply decoupled with 0.1-µF and 0.001-µF ceramic 0603-style capacitors 1 cm from the device.

**Figure 10.**




NOTES: Input: 50% duty cycle square wave with period jitter < 9 ps at 100 MHz, all outputs enabled and loaded with differential 100-Ω loads,worst-case output, supply decoupled with 0.1-µF and 0.001- µF ceramic 0603-style capacitors 1 cm from the device.

**Figure 11.**

## APPLICATION INFORMATION

### FAIL SAFE

A common problem with differential signaling applications is how the system responds when no differential voltage is present on the signal pair. The LVDS receiver is like most differential line receivers, in that its output logic state can be indeterminate when the differential input voltage is between –100 mV and 100 mV and within its recommended input common-mode voltage range. Hovever, TI LVDS receivers handles the open-input circuit situation differently.

Open-circuit means that there is little or no input current to the receiver from the data line itself. This could be when the driver is in a high-impedance state or the cable is disconnected. When this occurs, the LVDS receiver pulls each line of the signal pair to near $V_{CC}$ through 300-kΩ resistors as shown in Figure 12. The fail-safe feature uses an AND gate with input voltage thresholds at about 2.3 V to detect this condition and force the output to a high-level regardless of the differential input voltage.

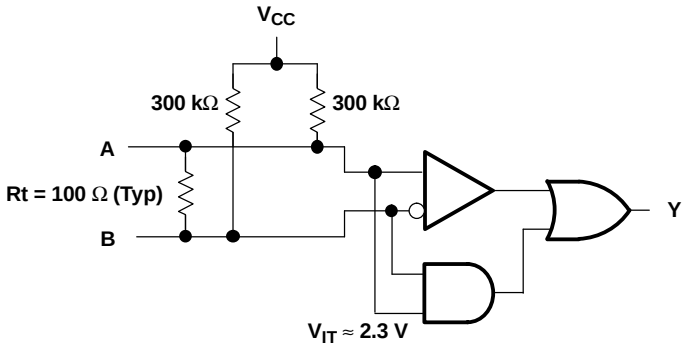



**Figure 12. Open-Circuit Fail Safe of the LVDS Receiver**

It is only under these conditions that the output of the receiver will be valid with less than a 100 mV differential input voltage magnitude. The presence of the termination resistor, Rt, does not affect the fail-safe function as long as it is connected as shown in Figure 12. Other termination circuits may allow a dc current to ground that could defeat the pullup currents from the receiver and the fail-safe feature.

### CLOCK DISTRIBUTION

The SN65LVDS108 device solves several problems common to the distribution of timing critical clock and data signals. These problems include:

- Excessive skew between the signal paths
- Noise pickup over long signaling paths
- High power consumption
- Control of which signal paths are enabled or disabled
- Elimination of radiation from unterminated lines

Buffering and splitting the signal on the same silicon die minimizes corruption of the timing relation between the copies of the signal. Buffering and splitting the signal in separate devices will introduce considerably higher levels of uncontrolled timing skew between the signals. Higher speed operation and more timing tolerance for other components of the system is enabled by the tighter system timing budgets provided by the single die implementations of the SN65LVDS108.

The use of LVDS signaling technology for both the inputs and the outputs provides superior common-mode and noise tolerance compared to single-ended I/O technologies. This is particularly important because the signals that are being distributed must be transmitted over longer distances, and at higher rates, than can be accommodated with single-ended I/Os. In addition, LVDS consumes considerably less power than other high-performance differential signaling schemes.

## APPLICATION INFORMATION (continued)

The enable inputs provided for each output may be used to turn on or off any of the paths. This function is required to prevent radiation of signals from the unterminated signal lines on open connectors when boards or devices are being swapped in the end equipment. The individual channel enables are also required if redundant paths are being utilized for reliability reasons.

The following diagram shows how an input signal is being identically repeated out two of the available outputs. A third output is shown in the disabled state.

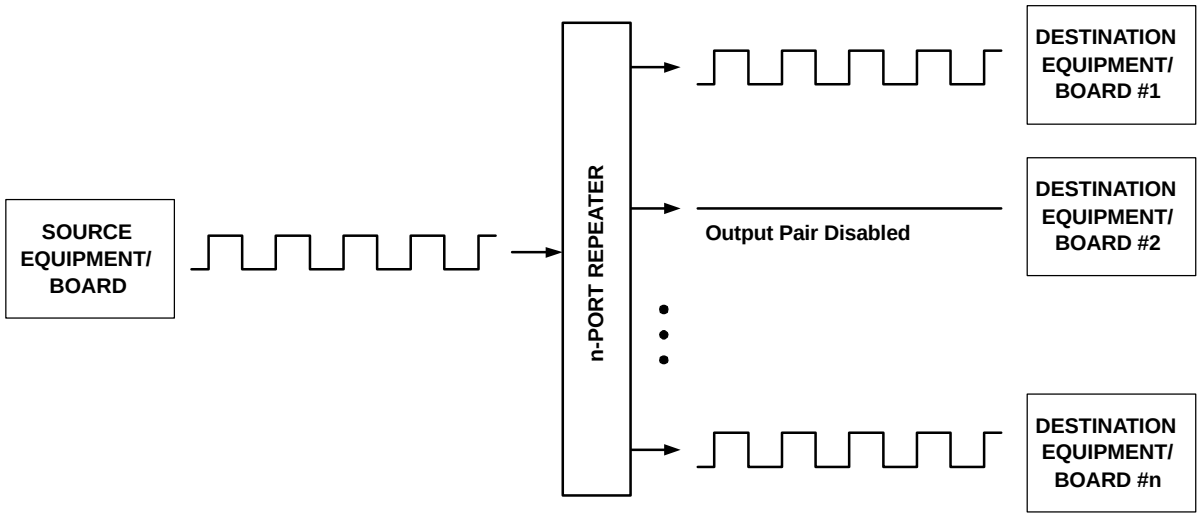



**Figure 13. LVDS Repeating Splitter Application Example Showing Individual Path Control**

## INPUT LEVEL TRANSLATION

An LVDS receiver can be used to receive various other types of logic signals. Figure 14 through Figure 22 show the termination circuits for SSTL, HSTL, CTT, GTL, BTL, LVPECL, PECL, CMOS, and TTL.

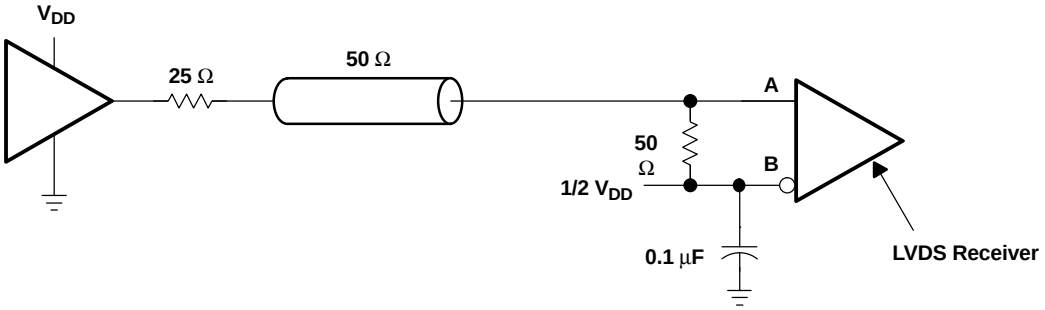



**Figure 14. Stub-Series Terminated (SSTL) or High-Speed Transceiver Logic (HSTL)**

## APPLICATION INFORMATION (continued)

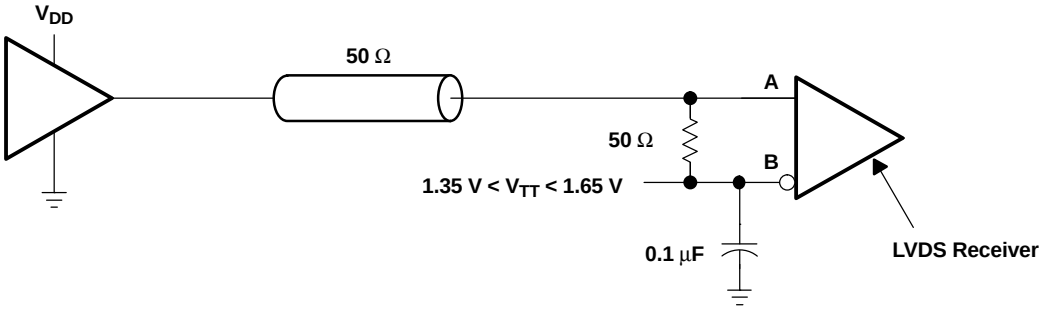



**Figure 15. Center-Tap Termination (CTT)**

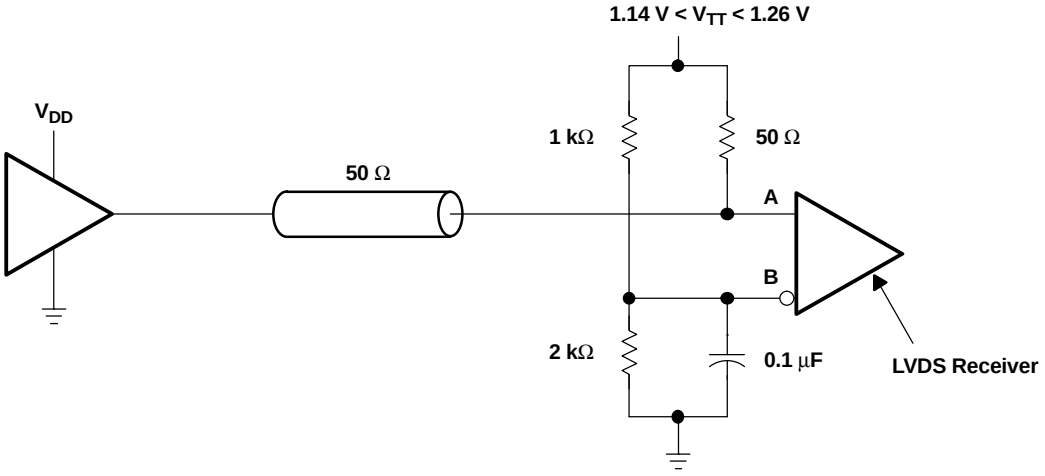



**Figure 16. Gunning Transceiver Logic (GTL)**

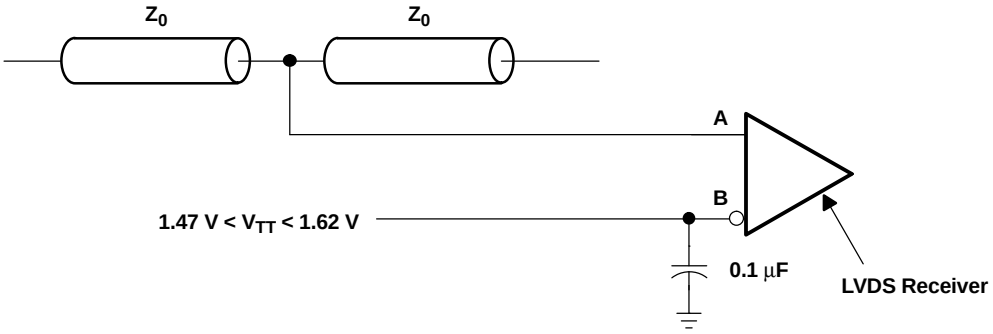



**Figure 17. Backplane Transceiver Logic (BTL)**

## APPLICATION INFORMATION (continued)

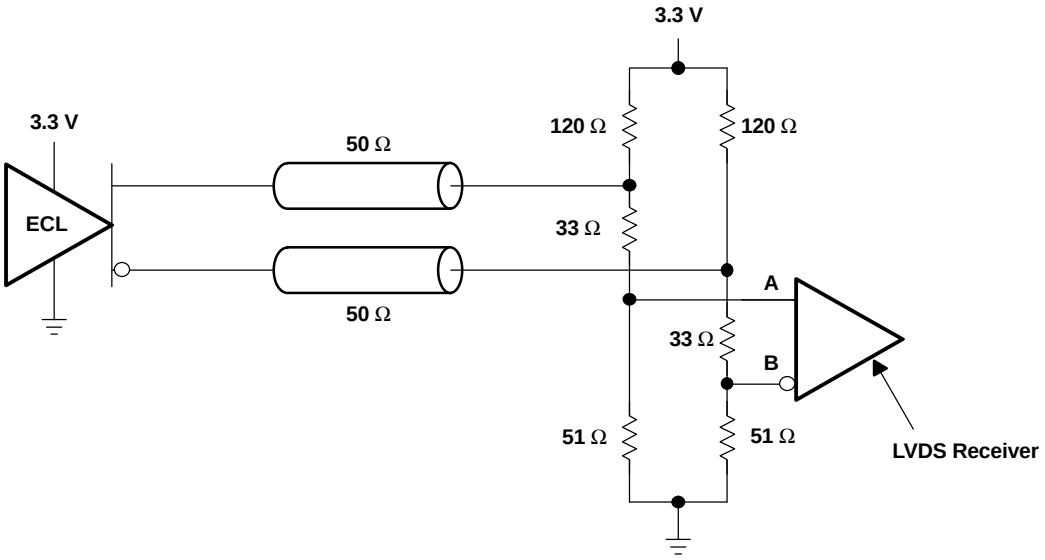



**Figure 18. Low-Voltage Positive Emitter-Coupled Logic (LVPECL)**

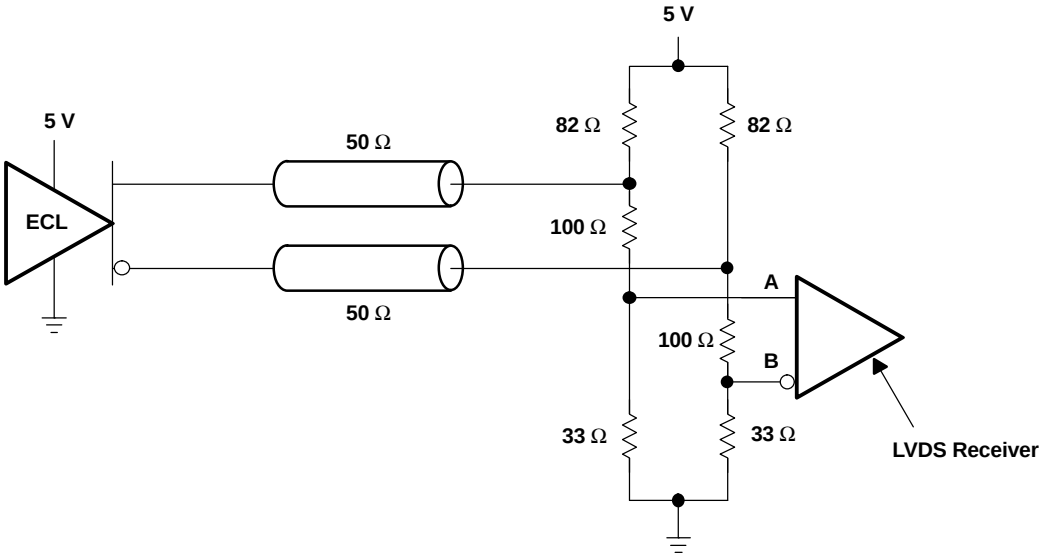



**Figure 19. Positive Emitter-Coupled Logic (PECL)**

## APPLICATION INFORMATION (continued)

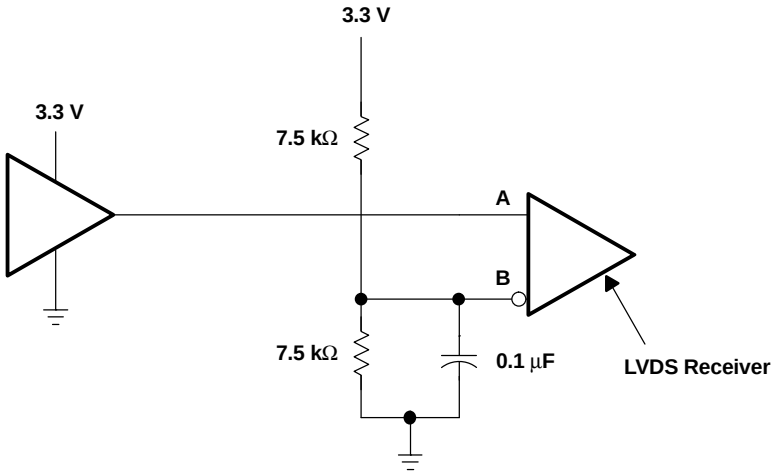



**Figure 20. 3.3-V CMOS**

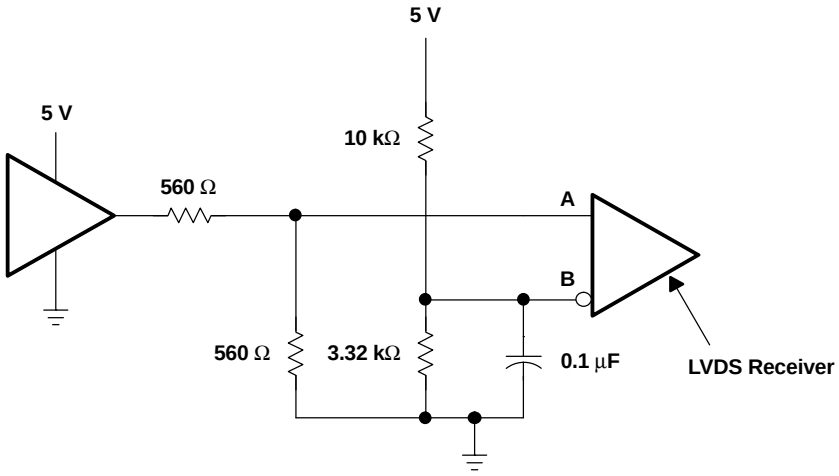



**Figure 21. 5-V CMOS**

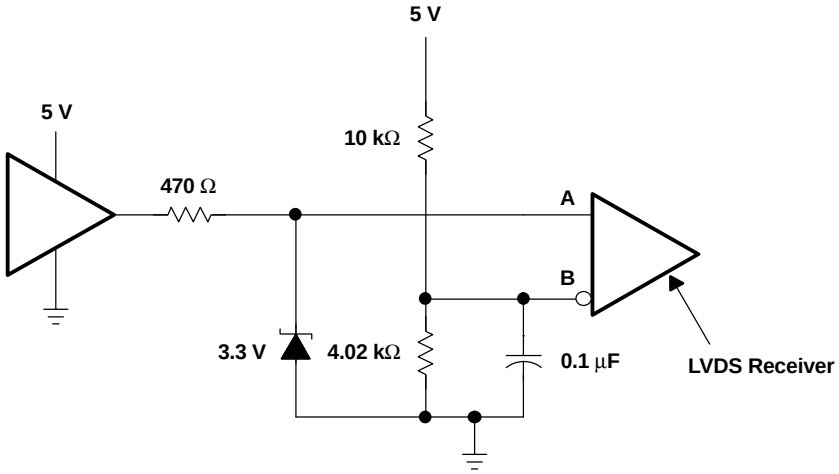



**Figure 22. TTL**

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| SN65LVDS108DBT | ACTIVE | TSSOP | DBT | 38 | 50 | Green (RoHS & no Sb/Br) | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | LVDS108 | Samples |
| SN65LVDS108DBTG4 | ACTIVE | TSSOP | DBT | 38 | 50 | Green (RoHS & no Sb/Br) | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | LVDS108 | Samples |
| SN65LVDS108DBTR | ACTIVE | TSSOP | DBT | 38 | 2000 | Green (RoHS & no Sb/Br) | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | LVDS108 | Samples |
| SN65LVDS108DBTRG4 | ACTIVE | TSSOP | DBT | 38 | 2000 | Green (RoHS & no Sb/Br) | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | LVDS108 | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

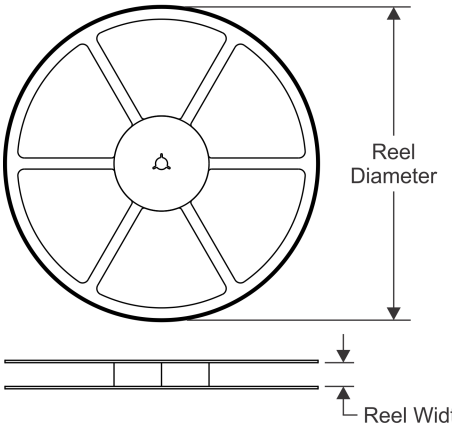
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TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

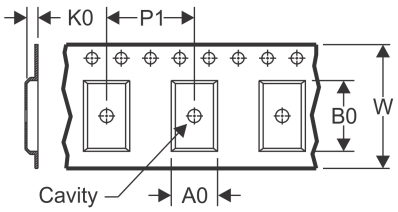
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## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

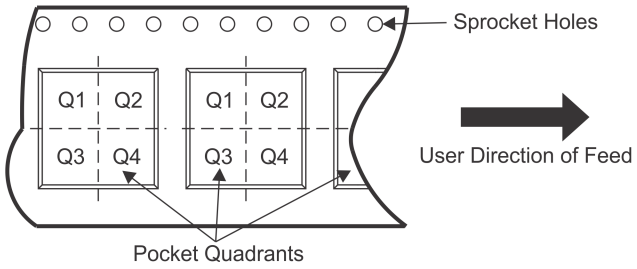



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

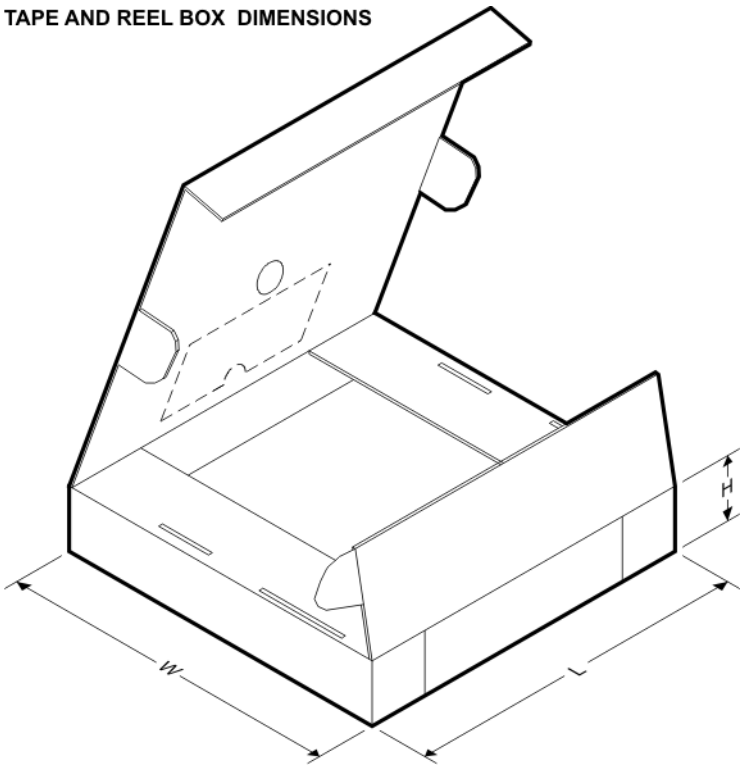
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SN65LVDS108DBTR | TSSOP | DBT | 38 | 2000 | 330.0 | 16.4 | 6.9 | 10.2 | 1.8 | 12.0 | 16.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

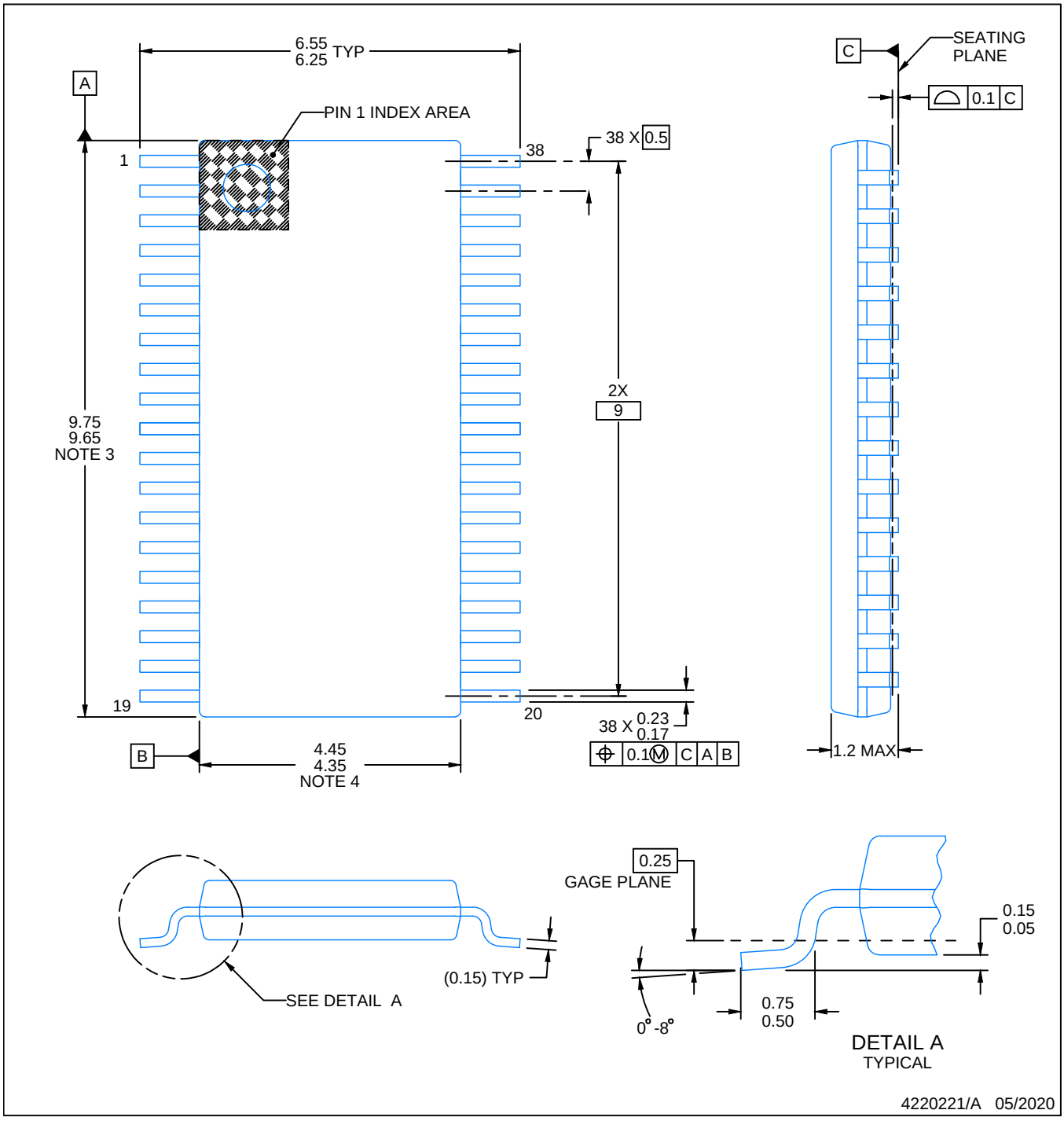
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| SN65LVDS108DBTR | TSSOP | DBT | 38 | 2000 | 350.0 | 350.0 | 43.0 |

# PACKAGE OUTLINE

## DBT0038A

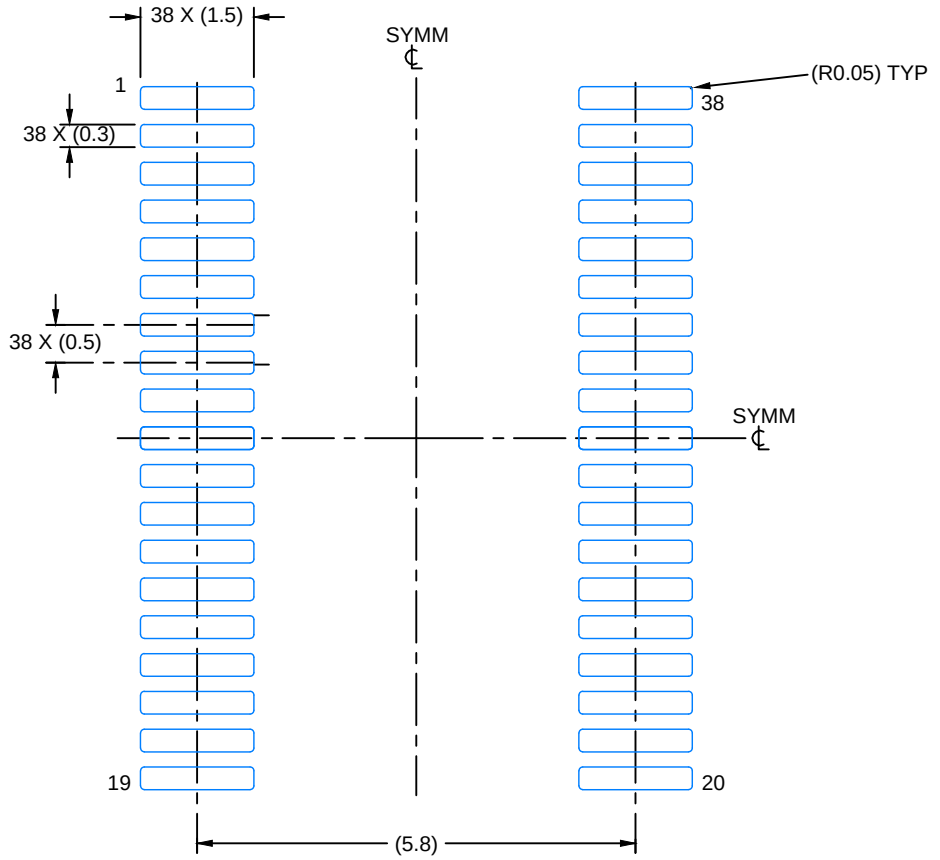
## TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

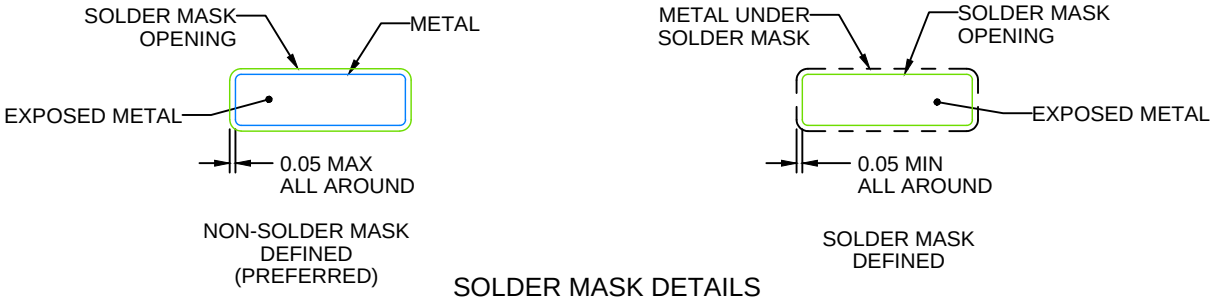



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

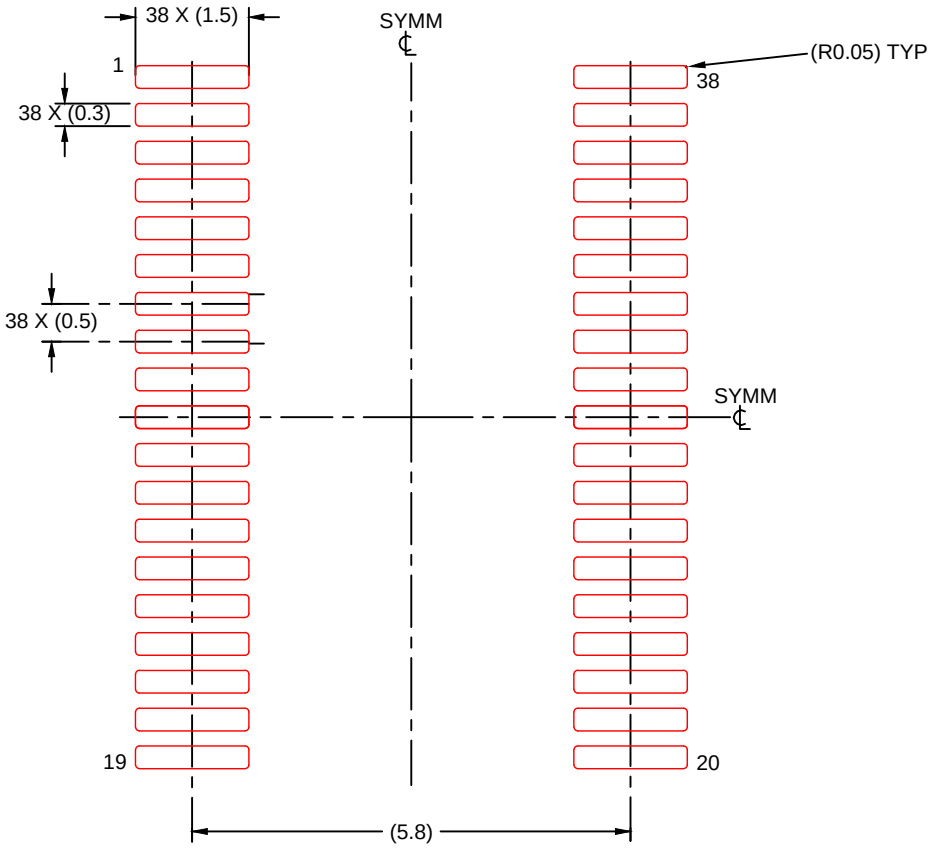



SOLDER MASK DETAILS

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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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