

Evaluating the **ADP5014** 4-Channel Power Management Unit

FEATURES

Full featured evaluation board for the **ADP5014**
Compact solution size
4-layer high glass transition temperature (T_g) PCB for superior thermal performance
Convenient connections through vertical printed circuit tail pin headers
Supply voltage
 2.75 V to 6.0 V for PVINx
Mode option to select manual or sequence enable
Mode option to select PSM or FPWM operation
Programmable switching frequency from 500 kHz to 2.5 MHz
Frequency synchronization input or output

DOCUMENT NEEDED

ADP5014 data sheet

EQUIPMENT NEEDED

DC power supply
 Voltmeter
 Ammeter
 Load resistors or electrical load
 Oscilloscope

GENERAL DESCRIPTION

This user guide describes the evaluation of the **ADP5014** and includes detailed schematics and printed circuit board (PCB) layouts.

The ADP5014-EVALZ evaluation board combines four high performance buck regulators in a 40-lead LFCSP package to meet the demanding performance and board space requirements.

Full details on the **ADP5014** regulator are provided in the **ADP5014** data sheet, available from Analog Devices, Inc. Consult the data sheet in conjunction with this user guide when working with this evaluation board.

ADP5014-EVALZ PHOTOGRAPH

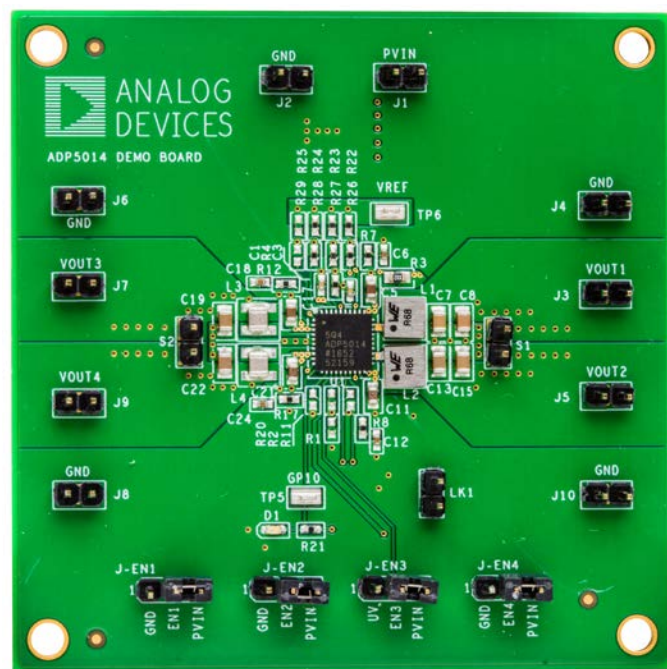


Figure 1.

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REVISION HISTORY

6/2017—Revision 0: Initial Version

USING THE EVALUATION BOARD

POWERING UP

The ADP5014-EVALZ evaluation board is supplied fully assembled and tested. Before applying power to the evaluation board, follow the procedures in this section.

Jumper J-EN1 (EN1/ENALL)

To enable Buck 1, short the middle pin of J-EN1 to PVIN. PVIN is the shared PVINx pin supply (see Figure 4).

To disable Buck 1, short the middle pin of J-EN1 to GND.

Jumper J-EN2 (EN2/DL12)

To enable Buck 2, short the middle pin of J-EN2 to PVIN.

To disable Buck 2, short the middle pin of J-EN2 to GND.

Jumper J-EN3 (EN3/UV)

To enable Buck 3, short the middle pin of J-EN3 to PVIN.

To disable Buck 3, short the middle pin of J-EN3 to EN3/UV.

Jumper J-EN4 (EN4/DL34)

To enable Buck 4, short the middle pin of J-EN4 to PVIN.

To disable Buck 4, short the middle pin of J-EN4 to GND.

Input Power Source

If the input dc power source includes a current meter, use that meter to monitor the input current. Connect the positive terminal of the power source to J1 (PVIN) of the evaluation board, and the negative terminal of the power source to J2 (GND) of the evaluation board.

If the dc power source does not include a current meter, connect a current meter in series with the input source voltage. Connect the positive lead (+) of the power source to the positive (+) ammeter terminal, the negative lead (–) of the power source to J2 (GND), and the negative lead (–) of the ammeter to J1 (PVIN).

Note that the power source trace must be short and thick enough to prevent a long trace voltage drop or a potential oscillation on the board supply, which may cause damage to the chip.

Output Load

Before connecting the load, ensure that all the regulators are turned off. Connect an electronic load or resistor for each regulator to set the load current.

Using Buck 1 as an example, connect the positive terminal of the load to J3 (VOUT1) of the evaluation board and connect the negative terminal of the load to J4 (GND).

Input and Output Voltmeter

Measure the input and output voltages using voltmeters. Ensure that the voltmeters are connected to the appropriate terminals of the evaluation board and not to the load or power source. If the voltmeters are not connected directly to the evaluation board, the measured voltages are incorrect due to the voltage drop across the leads and/or connections between the evaluation board, the power source, and/or the load.

To measure the input voltage, connect the input voltage measuring voltmeter positive (+) terminal to J1 (PVIN) and the input voltage measuring voltmeter negative (–) terminal to J2 (GND).

Likewise, to measure the output voltage of Buck 1, connect the output voltage measuring voltmeter positive (+) terminal to J3 (VOUT1), and connect the output voltage measuring voltmeter negative (–) terminal to J4 (GND).

The measurement method of the output voltage for the other regulators is the same as for Buck 1.

Quick Start

Ensure that the power source voltage for the buck regulators (PVIN) is 2.75 V to 6.0 V. Use the J-EN1, J-EN2, J-EN3, and J-EN4 jumpers to enable or disable the desired channel.

Figure 2 shows the ADP5014 evaluation board connection diagram. When the power source and load are connected to the evaluation board, the board can be powered for operation. If the load is not enabled, enable the load. Verify that the evaluation board is drawing the proper current and that the output voltage maintains voltage regulation.

After power-up, measure the following output voltages:

- $V_{OUT1} = 1.0$ V, supply up to a 4 A output load
- $V_{OUT2} = 1.5$ V, supply up to a 4 A output load
- $V_{OUT3} = 1.8$ V, supply up to a 2 A output load
- $V_{OUT4} = 3.3$ V, supply up to a 2 A output load

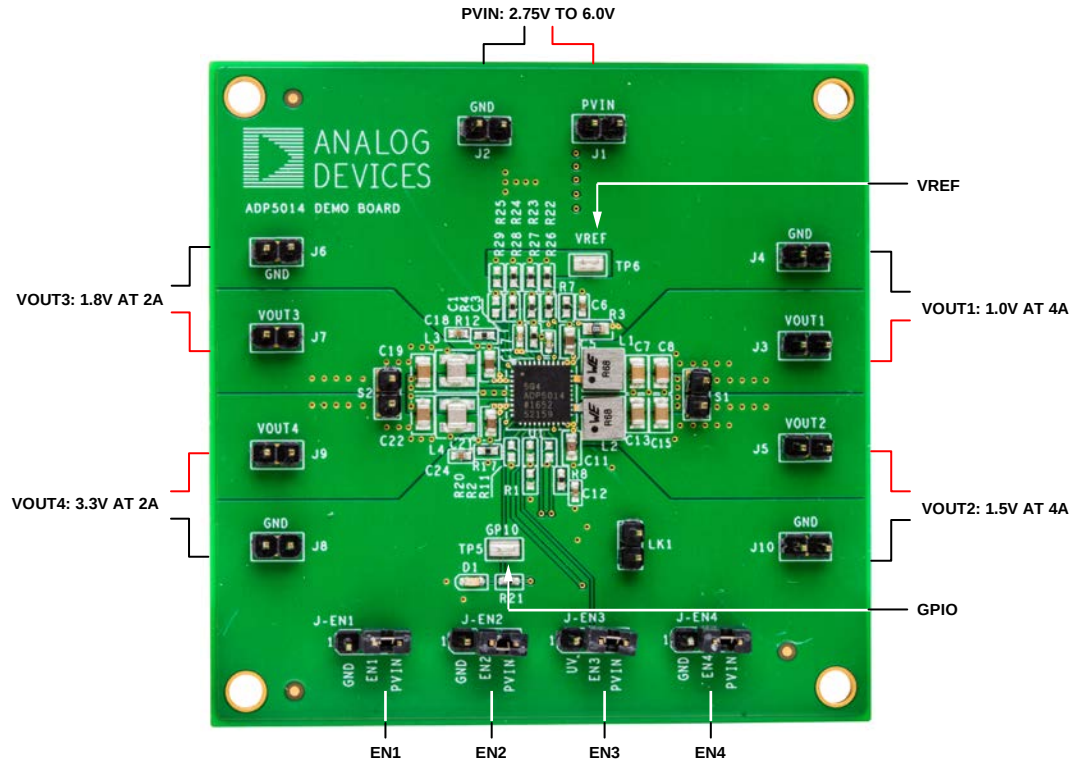


Figure 2. Evaluation Board Connection Diagram

MEASURING EVALUATION BOARD PERFORMANCE

Measuring the Switching Waveform

To observe the switching waveform with an oscilloscope, place the oscilloscope probe tip at the end of the inductor with the probe ground at GND. Set the scope to dc with the appropriate voltage and time divisions. The switching waveform limits alternate approximately between 0 V and the input voltage.

Measuring Load Regulation

Test the load regulation by observing the change in each output voltage when increasing each output load current. To minimize the voltage drop, use short, low resistance wires.

Measuring Line Regulation

Vary the input voltage and examine the change in each output voltage with the fixed output current.

Line Transient Response

Generate a step input voltage change and observe the behavior of each output voltage using an oscilloscope.

Load Transient Response

Generate a load current transient at each output and observe the output voltage response using an oscilloscope. Attach the current probe to the wire between the output and the load to capture the current transient waveform.

Measuring Efficiency

The efficiency, η , is measured by comparing the input power with the output power.

Measure the input and output voltages as close as possible to the input and output capacitors to reduce the effect of voltage drop.

To measure the efficiency of one specific regulator, enable only this regulator and disable the other regulators. The efficiency of the enabled regulator is as follows:

$$\eta_x = \frac{V_{OUTx} \times I_{OUTx}}{V_{IN} \times I_{IN}}$$

To measure the overall efficiency, enable all regulators. To calculate the overall efficiency, see Equation 1.

$$\eta = \frac{V_{OUT1} \times I_{OUT1} + V_{OUT2} \times I_{OUT2} + V_{OUT3} \times I_{OUT3} + V_{OUT4} \times I_{OUT4}}{V_{IN} \times I_{IN}} \quad (1)$$

Measuring Inductor Current

Measure the inductor current by removing one end of the inductor from its pad and connecting a current loop in series. A current probe can be connected onto this wire.

Measuring Output Voltage Ripple

To observe the output voltage ripple, place the oscilloscope probe across the output capacitor with the probe ground lead connected to the negative (–) capacitor terminal and the probe tip placed at the positive (+) capacitor terminal. Set the oscilloscope to ac, 10 mV/division, 2 μs/division time base, and 20 MHz bandwidth.

A standard oscilloscope probe has a long wire ground clip. For high frequency measurements, this ground clip picks up high frequency noise and injects it into the measured output ripple. Figure 3 shows an easy way to measure the output ripple properly. Remove the oscilloscope probe sheath and wrap an unshielded wire around the oscilloscope probe. By keeping the ground length of the oscilloscope probe as short as possible, the true ripple can be measured.

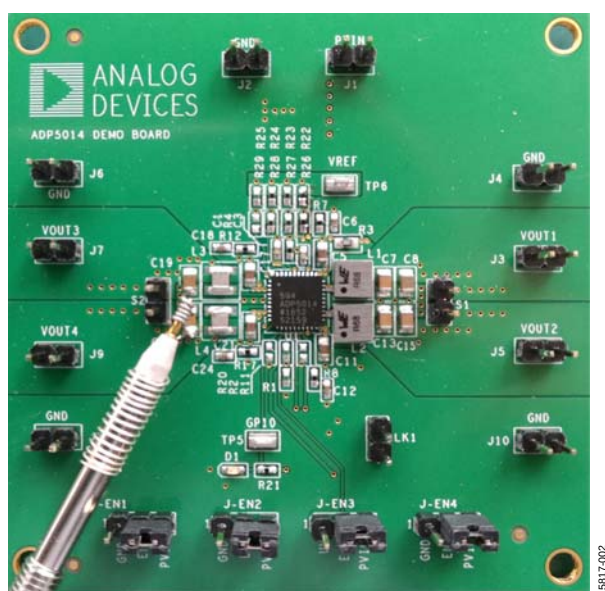


Figure 3. Measuring Output Voltage Ripple

MODIFYING THE BOARD

To modify the ADP5014 evaluation board configuration, unsolder, replace, or remove the appropriate passive components or jumpers on the board.

Changing the Output Voltages

The output voltage of the ADP5014-EVALZ evaluation board is externally set by a resistor divider from the VREF pin to the VSETx pin and a resistor divider from the output voltage to the FBx pin. To limit the degradation of the output voltage accuracy due to VSETx and FBx bias current, ensure that the bottom resistors in the dividers are not too large.

The ADP5014 provides adjustable output voltage settings. Use the resistor divider from the accurate internal VREF reference voltage (VREF pin) to set the desired output voltage, and directly tie the feedback pin (FBx) to the output when the desired output voltage setting is less than VREF voltage. If the desired output voltage exceeds the VREF voltage, use an external resistor divider from the output to the FBx pin to set the desired output voltage, tie VSETx to VREF directly, and use the VREF

reference as the error amplifier input (see the ADP5014 data sheet for details on output voltage programming).

The output voltage of Buck 1 of the ADP5014-EVALZ evaluation board is preset to 1 V. Change the output voltage by replacing the resistor divider composed of R22 and R26 when the desired output voltage setting is less than the VREF voltage. The equation for the output voltage setting is

$$V_{OUT} = V_{REF} \times (R26/(R22 + R26))$$

where:

V_{OUT} is the output voltage.

V_{REF} is the 2.0 V accurate low noise reference voltage.

If the desired output voltage exceeds the VREF voltage, replace the resistor divider composed of R5 and R6, and tie VSET1 to VREF directly. The equation for the output voltage setting is

$$V_{OUT} = V_{REF} \times (1 + (R6/R5))$$

where:

V_{OUT} is the output voltage.

V_{REF} is the 2.0 V accurate low noise reference voltage.

When the output voltage is changed, the values of the inductors, the output capacitors, and the compensation networks must be recalculated and changed for stable operation (see the ADP5014 data sheet for details on external component selection).

The method of changing the output voltage for the other regulators is the same as for Buck 1. Table 1 shows the external resistor dividers for each channel.

Table 1. External Resistor Dividers in Each Channel

Resistor Divider	Buck 1	Buck 2	Buck 3	Buck 4
VSETx Divider	R22, R26	R23, R27	R24, R28	R25, R29
FBx Divider	R5, R6	R9, R10	R13, R14	R18, R19

Changing the Switching Frequency

The switching frequency (f_{sw}) of the ADP5014-EVALZ evaluation board is preset to 1200 kHz. Change the switching frequency setpoint by replacing the R4 resistor with a different value, as shown in the following equation:

$$f_{sw} \text{ (kHz)} = 100,000/R4 \text{ (k}\Omega\text{)}$$

When the switching frequency is changed, the values of the inductors, the output capacitors, and the compensation networks must be recalculated and changed for stable operation (see the ADP5014 data sheet for details on external component selection).

Changing the Function Configurations (CFG1 and CFG2)

The ADP5014 includes the CFG1 and CFG2 pins to decode the function configurations for all channels. The CFG1 pin has eight logic statuses that is decoded by connecting one resistor to ground, whereas the CFG2 pin has 16 logic statuses decoded by connecting one resistor to ground. This decoder circuitry only works in the initiation stage of the ADP5014; therefore, the configurations cannot be changed during operation.

The CFG1 pin programs the load output capability and parallel operation for all channels. The value of R1 in the ADP5014-

EVALZ evaluation board is 0 Ω . To change the configuration, replace the R1 resistor at the CFG1 pin with a different value.

The CFG2 pin programs the operation mode (forced pulse-width modulation (FPWM) or pulse-width modulation/power savings mode (PWM/PSM)), the enable mode (manual mode or sequence mode), the delay timer ($\times 1$ or $\times 8$), GPIO functionalities (power-good, synchronization input, clock output, and undervoltage comparator output for all channels. The value of R2 on the ADP5014-EVALZ evaluation board is 0 Ω . To change the configuration, replace the R2 resistor at the CFG2 pin with a different value.

Changing the Delay Time in Sequence Enable Mode

In sequence mode, all channels in the ADP5014 turns on and off under the control of the internal sequencer, which is triggered by the EN1/ENALL pin, with the predefined delay timer set by the EN2/DL12 and EN4/DL34 pins.

EN2/DL12 configures the delay timer for Channel 1 and Channel 2 when R11 is connected to ground. Similarly, EN4/DL34 configures the delay timer for Channel 3 and Channel 4 when R20 is connected to ground. In parallel operation, the slave channel (Channel 2 or Channel 4) always follow up with the delay timer configuration of the master channel. The delay timer decoder circuitry only works in the initiation stage of the ADP5014; therefore, the delay timer cannot be changed during operation. Table 2 summarizes the resistors that can be replaced when changing the function configurations and delay time.

Table 2. Function Configurations and Delay Time Setting

Pin Name	Resistor	Comments
CFG1	R1	Load output capability and parallel operation settings.
CFG2	R2	Operation mode, enable mode, delay time, and GPIO functionality settings.
EN2/DL12	R11	Not connected in manual mode; delay time setting for Channel 1 and Channel 2 in sequence mode.
EN4/DL34	R20	Not connected in manual mode; delay time setting for Channel 3 and Channel 4 in sequence mode.

Configuring Channel 1/Channel 2 and Channel 3/Channel 4 as 2-Phase Parallel Outputs

Channel 1 and Channel 2 are programmed as individual outputs on the ADP5014-EVALZ evaluation board. Channel 3 and Channel 4 are configured as individual outputs as well.

To configure Channel 1 and Channel 2 as a combined 2-phase parallel output, the following steps are required:

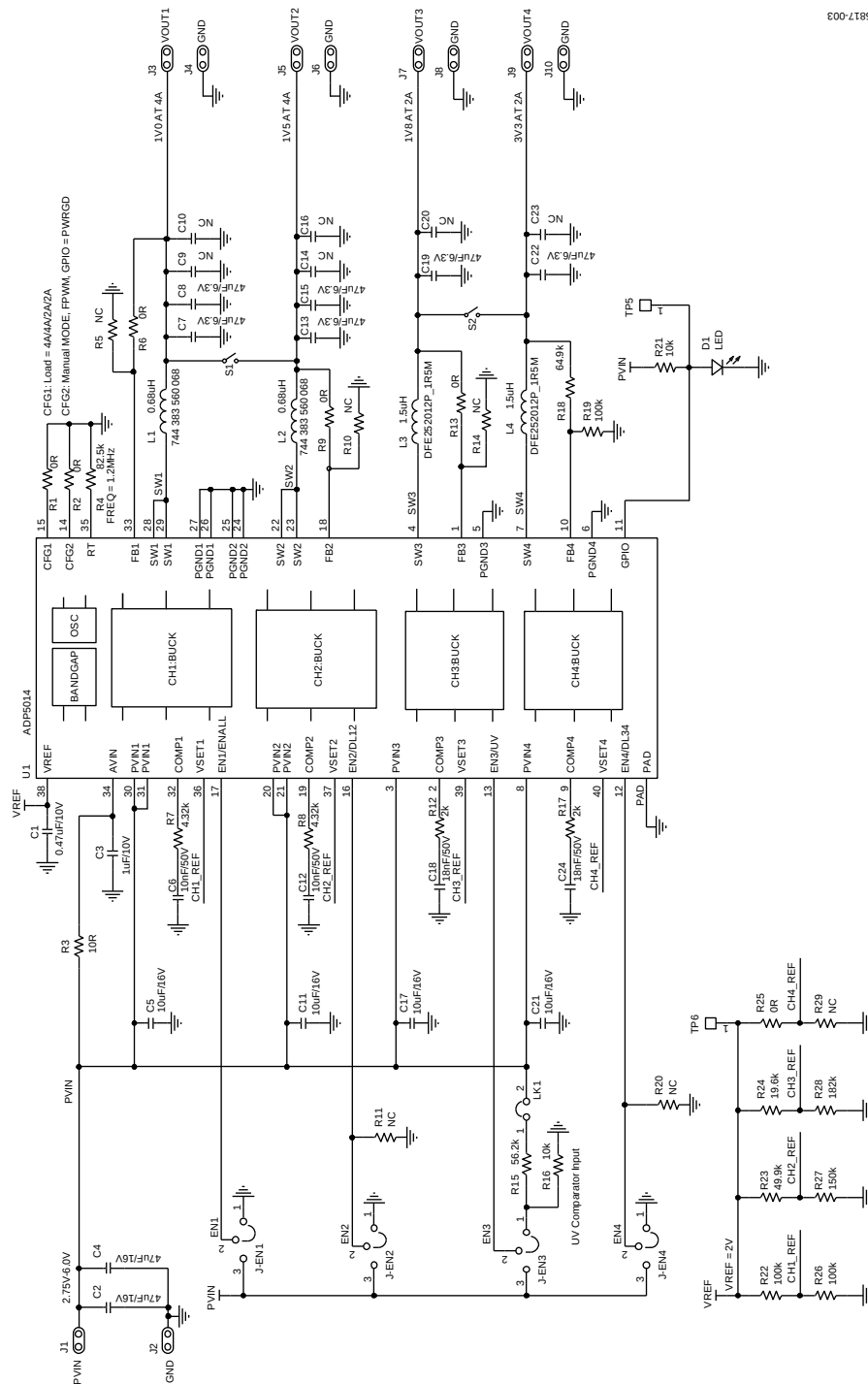
1. Short the S1 jumper.
2. Change R1 = 21.5 k Ω in the CFG1 pin setting.
3. Remove R8 and C12 from the COMP2 pin.
4. Remove R9, and replace R10 with 0 Ω on the FB2 pin.
5. Shunt the J-EN2 jumper to GND.
6. Use the VSET1 pin (R22 and R26) and the FB1 pin (R5 and R6) to set the output voltage.
7. Use the J-EN1 jumper (EN1/ENALL pin) to enable or disable Channel 1 and Channel 2.

To configure Channel 3 and Channel 4 as a combined 2-phase parallel output, the following steps are required:

1. Short the S2 jumper.
2. Change R1 = 26.1 k Ω in the CFG1 pin setting.
3. Remove R17 and C24 from the COMP4 pin.
4. Remove R18, and replace R19 with 0 Ω on the FB4 pin.
5. Shunt the J-EN4 jumper to GND.
6. Use the VSET3 pin (R24 and R28) and the FB3 pin (R13 and R14) to set the output voltage.
7. Use the J-EN3 jumper (EN3/UV pin) to enable or disable Channel 3 and Channel 4.

EVALUATION BOARD SCHEMATIC AND ARTWORK

SCHEMATIC



PCB LAYOUT

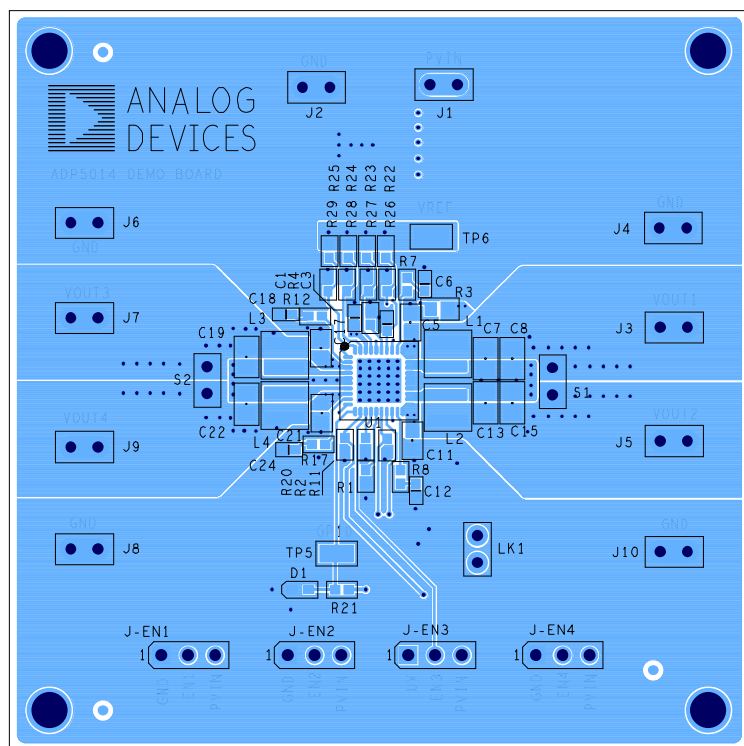


Figure 5. Layer 1, Top Side

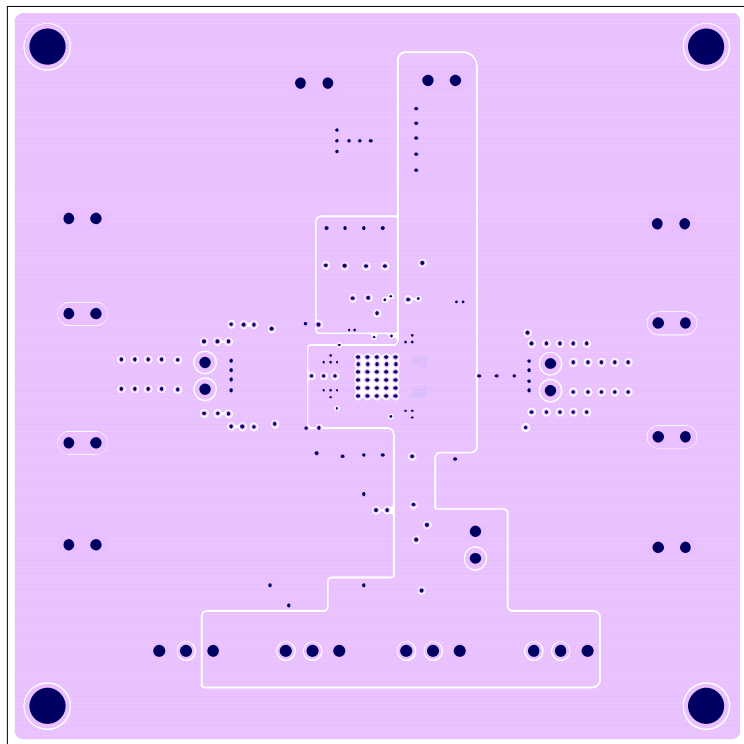


Figure 6. Layer 3, Power Plane



Figure 7. Layer 2, Ground Plane



Figure 8. Layer 4, Bottom Side

ORDERING INFORMATION

BILL OF MATERIALS

Table 3. Bill of Materials for the ADP5014-EVALZ

Qty	Reference Designator	Description	Part Number/Vendor
2	C1, C3	Capacitor, 0.47 μ F, 10 V, 0402	GRM155R61A474KE15D/Murata
2	C2, C4	Capacitor, 47 μ F, 16 V, 1210	GRM32ER61C476KE15L/Murata
4	C5, C11, C17, C21	Capacitor, 10 μ F, 16 V, 0603	GRM188R61C106MA73D/Murata
4	C6, C12, C18, C24	Capacitor, 10 nF, 50 V, 0402	GRM155R71H103KA/Murata
6	C7, C8, C13, C15, C19, C22	Capacitor, 47 μ F, 10 V, 0805	GRM21BR61A476ME15/Murata
6	C9, C10, C14, C16, C20, C23	Optional capacitor, 0805	Optional/Murata
1	D1	Red, diffused LED, 0603, SMD	SML-LX0603SRW-TR/Lumex Opto/Components
2	L1, L2 ¹	Chip inductor, 0.68 μ H, $I_{SAT} = 8.2$ A, DCR = 9 m Ω	744383560068/Wurth
2	L3, L4	Chip inductor, 1.5 μ H, $I_{SAT} = 3.5$ A, DCR = 60 m Ω	DFE252012P-1R5M=P2/Murata
6	R1, R2, R6, R9, R13, R25	Resistor, 0 Ω , 0402	CRCW04020000Z0ED/Vishay Dale
1	R3	Resistor, 10 Ω , 1%, 0603	CRCW060310R0FKEA/Vishay Dale
1	R4	Resistor, 82.5 k Ω , 1%, 0402	CRCW040282K5FKED/Vishay Dale
6	R5, R10, R11, R14, R20, R29	Optional resistor, 0402	Optional/Vishay Dale
2	R7, R8	Resistor, 4.32 k Ω , 1%, 0402	CRCW04024K32FKED/ Vishay Dale
2	R12, R17	Resistor, 2 k Ω , 1%, 0402	CRCW04022K00FKED/ Vishay Dale
1	R15	Resistor, 56.2 k Ω , 1%, 0402	CRCW040256K2FKED/ Vishay Dale
2	R16, R21	Resistor, 10 k Ω , 1%, 0402	CRCW040210K0FKED/ Vishay Dale
1	R18	Resistor, 64.9 k Ω , 1%, 0402	CRCW040264K9FKED/Vishay Dale
3	R19, R22, R26	Resistor, 100 k Ω , 1%, 0402	CRCW0402100KFKED/Vishay Dale
1	R23	Resistor, 49.9 k Ω , 1%, 0402	CRCW040249K9FKED/Vishay Dale
1	R24	Resistor, 19.6 k Ω , 1%, 0402	CRCW040219K6FKED/Vishay Dale
1	R27	Resistor, 150 k Ω , 1%, 0402	CRCW0402150KFKED/Vishay Dale
1	R28	Resistor, 182 k Ω , 1%, 0402	CRCW0402182KFKED/Vishay Dale
2	TP5, TP6	Test point, gold, 1206	HK-1-G/MAC8
1	U1	Power management unit with quad synchronous step-down regulators	ADP5014ACPZ-R7/Analog Devices
4	J-EN1, J-EN2, J-EN3, J-EN4	Jumper, 0.1-inch header, three-way, Single Inline Package 3 (SIP3)	M20-9990345/Harwin
13	J1, J2, J3, J4, J5, J6, J7, J8, J9, J10, S1, S2, LK1	Connector, 0.1-inch header, two-way, Single Inline Package 2 (SIP2)	M20-9990245/Harwin

¹ I_{SAT} is the saturation current of the inductor. DCR is the dc resistance of the inductor.

NOTES



ESD Caution

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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