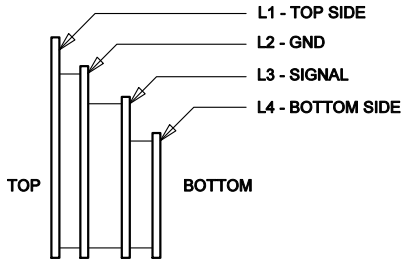
REVISION HISTORY				
ECO	REV	DESCRIPTION	APP. ENG.	DATE
–	2	PRODUCTION	YAN L.	9–11–14



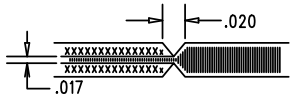
SIZE	QTY	SYM	PLATED	TOL
0.006	104	A	YES	+/–0.003
0.008	120	◇	YES	+/–0.003
0.02	8	C	YES	+/–0.003
0.035	6	⧖	YES	+/–0.003
0.036	22	D	YES	+/–0.003
0.055	10	B	YES	+/–0.003
0.07	2	+	NO	+/–0.003
0.095	12	□	YES	+/–0.003
0.187	4	×	NO	+/–0.005
0.215	4	⋈	YES	+/–0.005



LAYER CONSTRUCTION

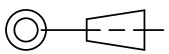
NOTES: UNLESS OTHERWISE SPECIFIED

1. FAB PER IPC–A–600.
2. MATERIAL: –LEAD FREE ASSEMBLY COMPLIANT, ISOLA FR–370HR OR EQUIVALENT.
   –FINISHED THICKNESS TO BE 0.062 +/– .005
   –TOTAL OF 4 LAYERS WITH 2 OZ. CU ON THE OUTER LAYERS AND 1 OZ. CU ON THE INNER LAYERS.
   –FLAMMABILITY RATING: 94 V–O MINIMUM.
3. SIZE: CUT TO DIMENSIONS AND TOLERANCES SHOWN. 0/0 ARE PRIMARY DATUMS.
4. DRILLING: –DRILL HOLES PER SCHEDULE. PLATE THROUGH HOLES WITH COPPER, 0.001 THICK MIN.
   –ALL HOLE SIZES ARE SPECIFIED AFTER PLATING.
   –HOLE LOCATION TOLERANCES ARE +/–0.003 IN RELATION TO CENTER
5. FINISH: –SMOBC USING LPI BOTH SIDES, COLOR GREEN.
   –GOLD IMMERSION BOTH SIDES.
   –FOR SILKSCREENS: USE WHITE NON–CONDUCTIVE INK.
6. DO NOT ALTER ARTWORK e.g. TO ADD LOGO OR DATE CODE. PAD SIZE CAN BE MODIFIED TO MEET END FINISH.
7. PCBS ARE TO BE RoHS COMPLIANT.
8. SCORING FOR PANELIZED PCB:



9. DESIGN HAS SOLDER MASK DEFINED PADS ON U1 WITH 0.029 PAD, 0.025 SOLDER MASK, AND 0.024 SOLDER PASTE. DO NOT CHANGE ANY SIZE ON THIS COMPONENT.

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES:
0.XX = ± 0.01
0.XXX = ± 0.005
INTERPRET DIM AND TOL PER ASME Y14.5M–1994
THIRD ANGLE PROJECTION



APPROVALS	
PCB DES.	LT
APP ENG.	YAN L.

SCALE = NONE

LINEAR TECHNOLOGY
1630 MCCARTHY BLVD
MILPITAS, CA 95035
PH: (408)432–1900
www.linear.com

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FOR CUSTOMER USE ONLY

TITLE: FABRICATION DRAWING

LOW VIN, 20A STEP–DOWN µMODULE REGULATOR

SIZE	IC NO.	REV
N/A	LTM4639EY DEMO CIRCUIT 2166A	2

FILENAME: DC2166A–2.PCB

SHT 1 OF 1