0 Hz/DC to 13 GHz, 2.5 kV HBM ESD, SP4T, MEMS Switch with Integrated Driver

Data Sheet **ADGM1004**

FEATURES

- Fully operational down to 0 Hz/dc
  - On resistance: 2.9 Ω (maximum)
  - Off leakage: 0.5 nA (maximum)
- −3 dB bandwidth
  - 10.8 GHz (typical) for RF1, RF4
  - 13 GHz (typical) for RF2, RF3
- RF performance characteristics
  - Insertion loss: 0.45 dB (typical) at 2.5 GHz
  - Isolation: 24 dB (typical) at 2.5 GHz
  - IP3: 67 dBm (typical)
  - RF input power: 32 dBm (maximum)
- Actuation lifetime: 1 billion cycles (minimum)
  - Hermetically sealed switch contacts
  - On switching time: 75 µs (maximum)
- ESD HBM rating
  - 5 kV for RF1 to RF4 and RFC pins
  - 2.5 kV for all other pins
- Integrated driver removes the need for an external driver
  - Supply voltage: 3.0 V to 3.6 V
  - CMOS/LVTTL compatible
  - Parallel and SPI Interface
  - Independently controllable switches
- Switch is in an open state with no power supply present
- Requirement to avoid floating nodes on all RFx pins (see the Floating Node section)
- 5 mm × 4 mm × 1.45 mm, 24-lead LFCSP
- Operating temperature range: 0°C to +85°C

APPLICATIONS

- Relay replacements
- Automatic test equipment (ATE): RF, digital, and mixed signals
- Load and probe boards: RF, digital, and mixed signals
- RF test instrumentation
- Reconfigurable filters and attenuators
- High performance RF switching

GENERAL DESCRIPTION

The ADGM1004 is a wideband, single-pole, four-throw (SP4T) switch fabricated using Analog Devices, Inc., microelectromechanical system (MEMS) switch technology. This technology enables a small form factor, wide RF bandwidth, highly linear, low insertion loss switch that is operational from 0 Hz/dc to 13 GHz, making it an ideal solution for a wide range of RF and precision equipment switching needs.

An integrated driver chip generates a high voltage to electrostatically actuate switch that can be controlled by a parallel interface and a serial peripheral interface (SPI). All four switches are independently controllable.

The device is packaged in a 24-lead, 5 mm × 4 mm × 1.45 mm, lead frame chip-scale package (LFCSP).

To ensure optimum operation of the ADGM1004, follow the Critical Operational Requirements section exactly.

The on resistance (R_{ON}) performance of the ADGM1004 is affected by part to part variation, channel to channel variation, cycle actuations, settling time post turn on, bias voltage, and temperature changes.

Note that throughout this data sheet, multifunction pins, such as IN1/SDI, are referred to either by the entire pin name or by a single function of the pin, for example, SDI, when only that function is relevant.

Rev. D

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700
Technical Support www.analog.com

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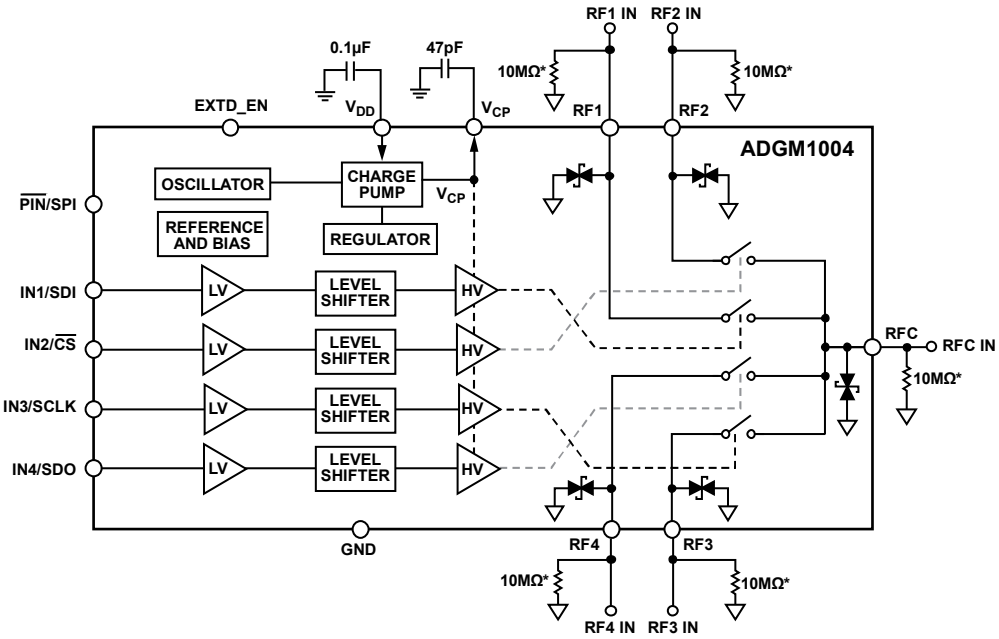
2/2017—Rev. 0 to Rev. A

1/2017—Revision 0: Initial Version

FUNCTIONAL BLOCK DIAGRAM



*10MΩ RESISTORS ARE REQUIRED TO AVOID ANY FLOATING NODES.
FOR MORE INFORMATION, REFER TO THE CRITICAL OPERATIONAL REQUIREMENTS SECTION

NOTES
1. LV = LOW VOLTAGE.
HV = HIGH VOLTAGE.

15173-001

Figure 1.

SPECIFICATIONS

Supply voltage (V_{DD}) = 3.0 V to 3.6 V, GND = 0 V, and all specifications at T_A = 25°C, unless otherwise noted. Typical specifications tested at T_A = 25°C with V_{DD} = 3.3 V.

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments[1]
ON-RESISTANCE PROPERTIES						See Figure 6 to Figure 13 for more details
Initial On-Resistance Properties						
On Resistance	R_{ON}			2.9	Ω	Drain source current (I_{DS}) = 50 mA, 0 V input bias, at 1 ms after first actuation, maximum specification from 0°C to 85°C
On-Resistance Match Between Channels	$\Delta R_{ON\ CH\_CH}$			1	Ω	Maximum value tested from 0°C to 85°C
On-Resistance Drift						
Over Time[2]	$\Delta R_{ON\ TIME}$			−0.25	Ω	R_{ON} changed from 1 ms to 100 ms after first actuation, maximum value tested from 0°C to 85°C
Over Actuations[3]	ΔR_{ON}		0.5		Ω	10^9 actuations, switch is actuated at 25°C and R_{ON} is measured at 25°C
				5	Ω	10^9 actuations, switch is actuated at 85°C and R_{ON} is measured at 25°C, 1 kHz actuating frequency, 220 mA load applied between toggles[4]
RELIABILITY PROPERTIES						
Continuously On Lifetime			7.2		Years	Median time before failure at 50°C[5], see Figure 60 for more details
Actuation Lifetime						
Cold Switched		10^9			Actuations	Load between toggling is 220 mA, tested at 85°C
Hot Switched						RF power = continuous wave (CW), terminated into 50 Ω, see Figure 14 for details
10 dBm			5.16×10^9		Actuations	50% of test population failure point (T50)
15 dBm			3.21×10^6		Actuations	50% of test population failure point (T50)
20 dBm			390×10^3		Actuations	50% of test population failure point (T50)
DYNAMIC CHARACTERISTICS						
Operating Frequency		0/dc		13	GHz	
−3 dB Bandwidth	BW					
RF1, RF4		9.5	10.8		GHz	RF1 to RFC and RF4 to RFC channels
RF2, RF3		11.5	13		GHz	RF2 to RFC and RF3 to RFC channels
Insertion Loss	IL		0.45	0.6	dB	At 2.5 GHz, RFC to RFx
			0.63	0.95	dB	At 6.0 GHz, RFC to RFx
Isolation						
RFx to RFC		22	24		dB	At 2.5 GHz, RFx to RFC (all channels off)
		16	19		dB	At 6.0 GHz, RFx to RFC (all channels off)
RF1 to RFC			27			At 6 GHz, RF2 to RFC is on, RF1 to RFC is off
RF2 to RFC			26			At 6 GHz, RF1 to RFC is on, RF2 to RFC is off
Crosstalk		27	30		dB	At 2.5 GHz, RFx to RFx
		22	24		dB	At 6.0 GHz, RFx to RFx
Return Loss	RL	14	17		dB	DC to 6.0 GHz
Third-Order Intermodulation Intercept	IP3		67		dBm	Input: 900 MHz and 901 MHz, input power = 27 dBm
Second-Order Intermodulation Intercept	IP2		95		dBm	Input: 900 MHz and 901 MHz, input power = 27 dBm
Second Harmonic Distortion	HD2		−90		dBc	Input: 5.4 MHz, input power = 0 dBm
			−74		dBc	Input: 150 MHz and 800 MHz, input power = 27 dBm

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments[1]
Third Harmonic Distortion	HD3		−80		dBc	Input: 150 MHz and 800 MHz, input power = 27 dBm
Total Harmonic Distortion plus Noise	THD + N		−102		dBc	Load resistance (R_L) = 300 Ω, f = 1 kHz, RFx = 2.5 V p-p
RF Input Power				32	dBm	Switch in the on state and terminated into 50 Ω, maximum specification tested at 25°C
DC Voltage Range		−6		+6	V	On switch dc voltage operation range, 0°C to 85°C
On Switching Time[6]	t_{ON}	0		75	µs	50% INx to 90% (0.05 dB of final IL value) RFx, 50 Ω termination, 0°C to 85°C
Off Switching Time[6]	t_{OFF}	0		75	µs	50% INx to 10% (0.05 dB of final IL value) RFx, 50 Ω termination, 0°C to 85°C
Actuation Frequency				5	kHz	All switches toggled simultaneously, 0°C to 85°C
Power-Up Time			0.75		ms	C_{CP} = 47 pF, 95% V_{DD} to 90% RFx, 0°C to 85°C
Video Feedthrough			16		mV peak	1 MΩ termination at RFx pin
Internal Oscillator Frequency		8	10	12	MHz	0°C to 85°C
Internal Oscillator Feedthrough[7]			−123		dBm	Spectrum analyzer resolution bandwidth (R_{BW}) = 200 Hz, one switch in on state, all other switches off with 50 Ω terminations[8]
			−146		dBm/Hz	
CAPACITANCE PROPERTIES						At 1 MHz, includes LFCSP package capacitance
On Switch Channel Capacitance	$C_{RF\ ON}$		3		pF	
Off Switch Channel Capacitance	$C_{RF\ OFF}$		1.5		pF	
LEAKAGE PROPERTIES						Maximum specification from 0°C to 85°C
On Leakage				5	nA	RFx (off channels) = −6 V, RFC to RFx (on channel) = −6 V
Off Leakage				0.5	nA	RFx = 6 V, RFC = −6 V
DIGITAL INPUTS						Minimum and maximum over 0°C to 85°C
Input High Voltage	V_{INH}	2			V	
Input Low Voltage	V_{INL}			0.8	V	
Input Current	I_{INL}, I_{INH}		0.025	1	µA	Input voltage (V_{IN}) = V_{INL} or V_{INH}
DIGITAL OUTPUTS						Minimum and maximum over 0°C to 85°C
Output Low Voltage	V_{OL}			0.4	V_{MAX}	Sink current (I_{SINK}) = 1 mA
Output High Voltage	V_{OH}	V_{DD} − 0.4			V_{MIN}	Source current (I_{SOURCE}) = 1 mA
POWER REQUIREMENTS						Minimum and maximum over 0°C to 85°C
Supply Voltage	V_{DD}	3.0		3.6	V	
Supply Current	I_{DD}			2.5	mA	Digital inputs = 0 V or V_{DD}, SDO is floating in SPI mode
Low Power Mode Current[9]	$I_{DD\ EXT\ VCP}$			50	µA	This value is I_{DD} in low power mode
External Drive Voltage[10]	VCP_{EXT}	79.2	80	80.8	V	
External Drive Current	$I_{CP\ EXT\ VCP}$			20	µA	

[1] RFx is RF1, RF2, RF3, and RF4. INx is IN1, IN2, IN3, and IN4.
[2] Maximum R_{ON} over time is R_{ON} (max) + $\Delta R_{ON\ TIME}$ (max) = 2.65 Ω.
[3] Maximum R_{ON} after 1 billion actuations is R_{ON} (max) + ΔR_{ON} (max) = 7.9 Ω.
[4] Actuating the switch at 85°C and measuring R_{ON} at 25°C is the most severe condition for ADGM1004 R_{ON} drift over actuations.
[5] Failure occurs when 50% of a sample lot fails. For more details, see the Cumulative On Switch Lifetime section.
[6] Switch is settled after 75 µs. Do not apply RF power between 0 µs and 75 µs.
[7] Disable the internal oscillator to eliminate feedthrough. When the internal oscillator and charge pump circuitry is disabled, the V_{CP} pin (Pin 24) must be driven with 80 V dc (VCP_{EXT}) from an external voltage supply required for MEMS switch actuation, as outlined in Table 3.
[8] The spectrum analyzer setup is as follows: R_{BW} = 200 Hz, video bandwidth (V_{BW}) = 2 Hz, span = 100 kHz, input attenuator = 0 dB, the detector type is peak, and the maximum hold is off. The fundamental feedthrough noise or harmonic (whichever is higher) is tested.
[9] For more details, see the Low Power Mode section.
[10] For more details, see the Internal Oscillator Feedthrough Mitigation section.

TIMING CHARACTERISTICS

V_{DD} = 3.0 V to 3.6 V, GND = 0 V, and all specifications T_{MIN} to T_{MAX} = 0°C to +85°C, unless otherwise noted.

Table 2.

Parameter	Description	Limit at T_{MIN}	Limit at T_{MAX}	Unit
t_1	SCLK period	100		ns
t_2	SCLK high pulse width	45		ns
t_3	SCLK low pulse width	45		ns
t_4	$\overline{CS}$ falling edge to SCLK active edge	25		ns
t_5	Data setup time	20		ns
t_6	Data hold time	20		ns
t_7	SCLK active edge to $\overline{CS}$ rising edge	25		ns
t_8	$\overline{CS}$ falling edge to SDO data available		20	ns
t_9[1]	SCLK falling edge to SDO data available		40	ns
t_{10}	$\overline{CS}$ rising edge to SDO returns to high impedance		25	ns
t_{11}	$\overline{CS}$ high time between SPI commands	100		ns
t_{12}	SCLK edge rejection to $\overline{CS}$ falling edge	25		ns
t_{13}	$\overline{CS}$ rising edge to SCLK edge rejection	25		ns

[1] Measured with a 20 pF load, t_9 determines the maximum SCLK frequency when the SDO pin is used.

Timing Diagrams

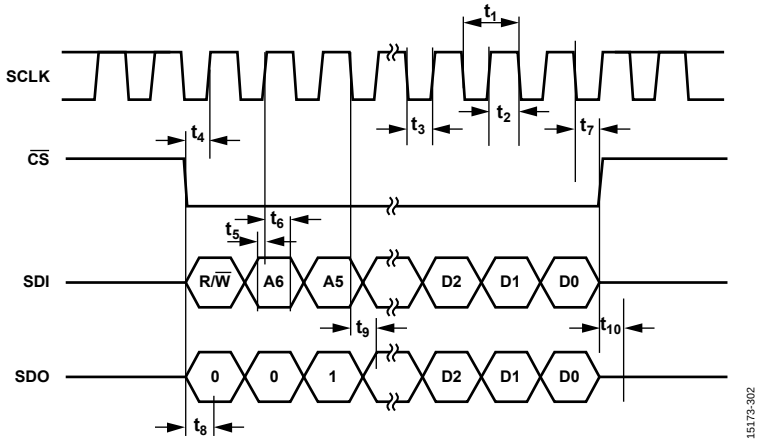


Figure 2. Addressable Mode Timing Diagram

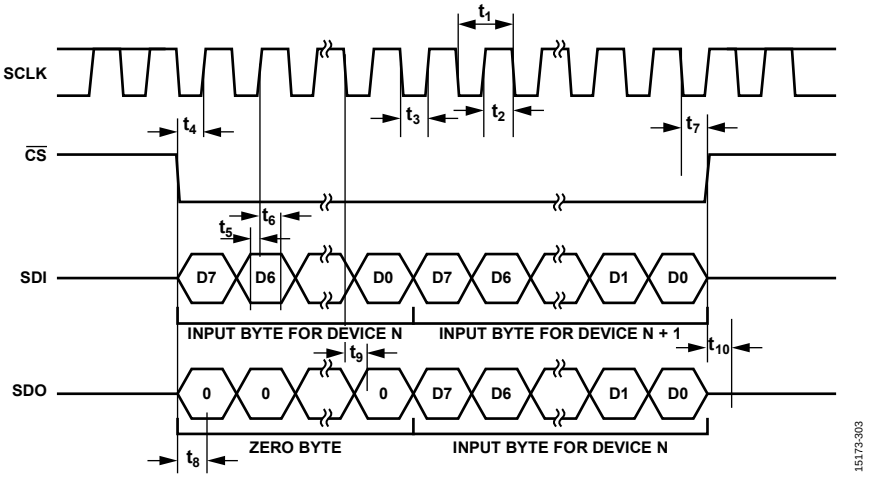


Figure 3. Daisy-Chain Timing Diagram

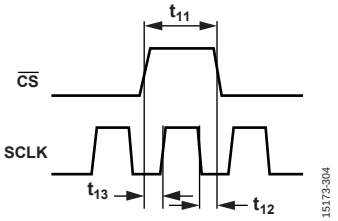


Figure 4. SCLK/$\overline{CS}$ Timing Relationship

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 3.

Parameter	Rating
V_{DD} to GND	−0.3 V to +6 V
Digital Inputs[1]	−0.3 V to V_{DD} + 0.3 V or +30 mA (whichever occurs first)
DC Voltage Rating[2]	±7 V
Standoff Voltage[3]	20 V
RFx to AGND	±10 V
RFC to AGND	±10 V
RFx to RFC	20 V
Current Rating[2]	250 mA
RF Power Rating[4]	33 dBm
Temperature	
Operating Range	0°C to +85°C
Storage Range	−65°C to +150°C
Reflow Soldering (Pb-Free)	
Peak	260 (+0/−5)°C
Time at Peak	10 sec to 30 sec
Electrostatic Discharge (ESD)	
Human Body Model (HBM)	
RF1 to RF4 and RFC	5 kV
All Other Pins	2.5 kV
Field Induced Charged Device Model[5]	
All Pins	1.25 kV
Group D	
Mechanical Shock (with 0.5 ms Pulse)[6]	1500 *g*
Vibration (Acceleration at 50 *g)*	20 Hz to 2000 Hz
Constant Acceleration	30,000 *g*

[1] Clamp overvoltages at INx by internal diodes. Limit the current to the maximum ratings given.
[2] This rating is with respect to the switch in the on position with no radio frequency signal applied.
[3] This rating is with respect to the switch in the off position.
[4] This rating is with respect to the switch in the on position and terminated into 50 Ω. The rating is 27 dBm when the switch is unterminated.
[5] A safe automated handling and assembly process is achieved at this rating level by implementing industry standard ESD controls.
[6] If the device is dropped during handling, do not use the device.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Only one absolute maximum rating can be applied at any one time.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JA} is the natural convection junction to ambient thermal resistance measured in a one cubic foot sealed enclosure. θ_{JC} is the junction to case thermal resistance.

Table 4. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
CP-24-4[1]	60	75	°C/W

[1] A simulated θ_{JA} number is evaluated using the maximum junction temperature in the package and the total power being dissipated in the package under operating conditions. For thermal performance calculation purposes at 25°C, a power dissipation of 113 mW per switch can be used. This value is calculated from a typical R_{ON} of 1.8 Ω and an absolute maximum current rating of 250 mA.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

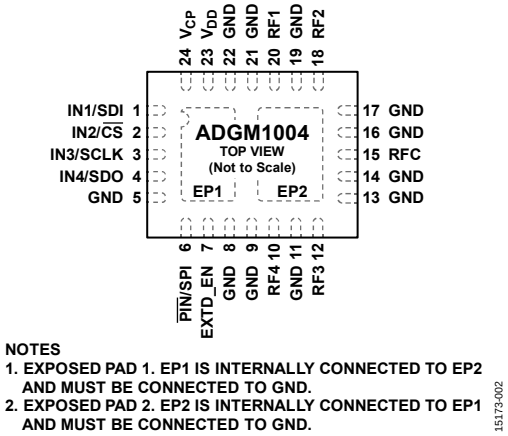


Figure 5. Pin Configuration

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	IN1/SDI	Parallel Logic Digital Control Input 1. The voltage applied to this pin controls the gate of the RF1 to RFC MEMS switch. In SPI mode, this pin is the serial data input pin. In parallel mode, if the IN1 pin is low, the RF1 to RFC switch is open (off). If the IN1 pin is high, the RF1 to RFC switch is closed (on). In SPI mode, this pin functions as the serial data input (SDI) pin.
2	IN2/$\overline{CS}$	Parallel Logic Digital Control Input 2. The voltage applied to this pin controls the gate of the RF2 to RFC MEMS switch. In parallel mode, if IN2 is low, the RF2 to RFC switch is open (off). If IN2 is high, the RF2 to RFC switch is closed (on). In SPI mode, this pin is the chip select ($\overline{CS}$) pin. $\overline{CS}$ is an active low signal that selects the slave device with which the master device intends to communicate. Typically, there is a dedicated $\overline{CS}$ signal between the master device and each slave device. The $\overline{CS}$ pin also functions to synchronize and frame the communications to and from the slave device.
3	IN3/SCLK	Parallel Logic Digital Control Input 3. The voltage applied to this pin controls the gate of the RF3 to RFC MEMS switch. In parallel mode, if IN3 is low, the RF3 to RFC switch is open (off). If IN3 is high, the RF3 to RFC switch is closed (on). In SPI mode, this pin functions as the serial clock (SCLK) pin that synchronizes the slave device(s) to the master device. Typically, the SCLK signal is shared for all slave devices on the serial bus. The SCLK signal is always driven by the master device.
4	IN4/SDO	Parallel Logic Digital Control Input 4. The voltage applied to this pin controls the gate of the RF4 to RFC MEMS switch. In parallel mode, if IN4 is low, the RF4 to RFC switch is open (off). If IN4 is high, the RF4 to RFC switch is closed (on). In SPI mode, this pin functions as the serial data output (SDO) pin. Typically, the SDO pin is shared for all slave devices on the serial bus. The SDO pin is driven by only one slave device at a time, otherwise it is high impedance. The SDO pin is always high impedance when the $\overline{CS}$ pin is deasserted high.
5, 8, 9, 11, 13, 14, 16, 17, 19, 21, 22	GND	Ground Connection.
6	$\overline{PIN}$/SPI	Parallel or Serial Logic Control Enable Pin. The SPI interface is enabled when this pin is high. When this pin is low the parallel digital interface is enabled.
7	EXTD_EN	External Voltage Drive Enable. In normal operation, set EXTD_EN low to enable the built in 10 MHz oscillator, which enables the internal driver IC voltage boost circuitry. Setting EXTD_EN high disables the internal 10 MHz oscillator and driver boost circuitry. With the oscillator disabled, the switch can still be controlled via the logic interface pins (IN1 to IN4) or via SPI interface, but the V_{CP} pin must be driven with 80 V dc from an external voltage supply. In this mode, the ADGM1004 only consumes 50 µA maximum supply current. Disabling the internal oscillator eliminates the associated 10 MHz noise feedthrough from the switch.
10	RF4	RF4 Port. This pin can be an input or an output. If unused, connect the pin to GND or terminate the pin with a 50 Ω resistor to GND.
12	RF3	RF3 Port. This pin can be an input or an output. If unused, connect the pin to GND or terminate the pin with a 50 Ω resistor to GND.
15	RFC	Common RF Port. This pin can be an input or an output.
18	RF2	RF2 Port. This pin can be an input or an output. If unused, connect the pin to GND or terminate the pin with a 50 Ω resistor to GND.
20	RF1	RF1 Port. This pin can be an input or an output. If unused, connect the pin to GND or terminate the pin with a 50 Ω resistor to GND.

Pin No.	Mnemonic	Description
23	V_{DD}	Positive Power Supply Input. The recommended decoupling capacitor to ground value is 0.1 µF. For the recommended input voltage for this chip, see the Specifications section.
24	V_{CP}	Charge Pump Capacitor Terminal. The recommended shunt capacitor to ground value is 47 pF (100 V rated). If the EXTD_EN pin is high, input an 80 V dc drive voltage into V_{CP} to drive the switches.
	EP1	Exposed Pad 1. EP1 is internally connected to EP2 and must be connected to GND.
	EP2	Exposed Pad 2. EP2 is internally connected to EP1 and must be connected to GND.

TYPICAL PERFORMANCE CHARACTERISTICS

In Figure 14, T50 refers to the number of cycles required for 50% of the population to fail.

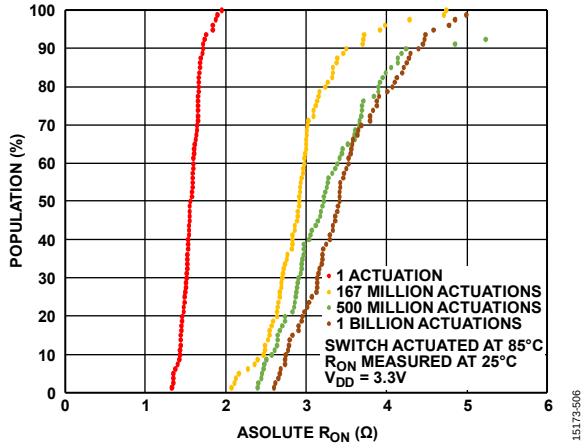


Figure 6. Population Percentage vs. Absolute R_{ON}, Switch Actuated at 85°C and R_{ON} measured at 25°C

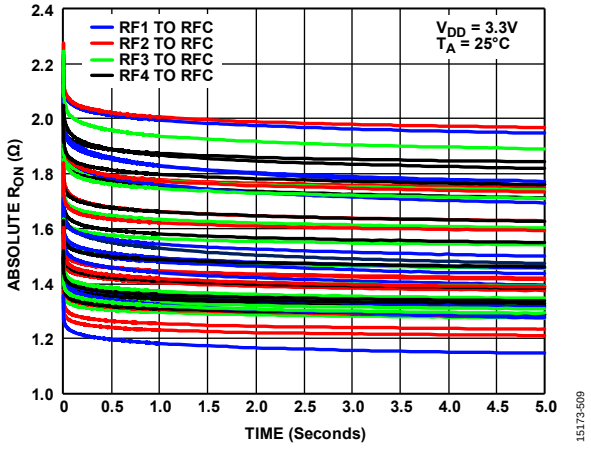


Figure 9. Absolute R_{ON} vs. Time (1 ms to 5 sec) on Linear Scale

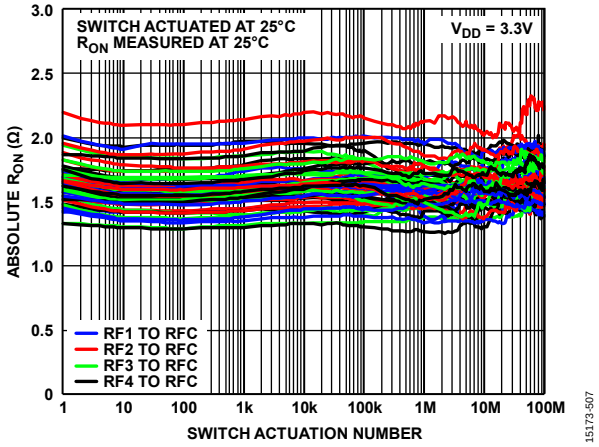


Figure 7. Absolute R_{ON} vs. Switch Actuation Number, Switch Actuated at 25°C and R_{ON} Measured at 25°C

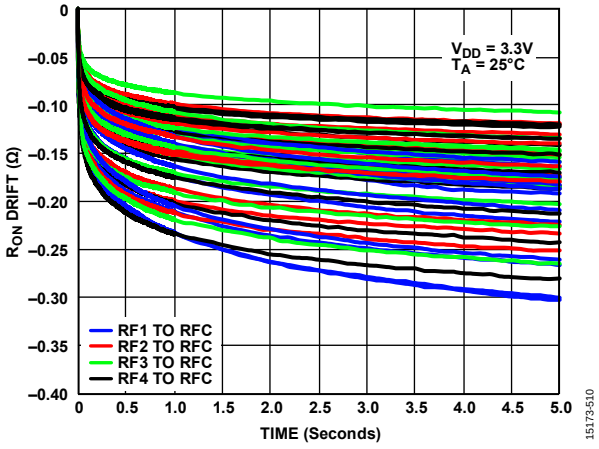


Figure 10. R_{ON} Drift vs. Time (1 ms to 5 sec) on Linear Scale, Normalized at Zero

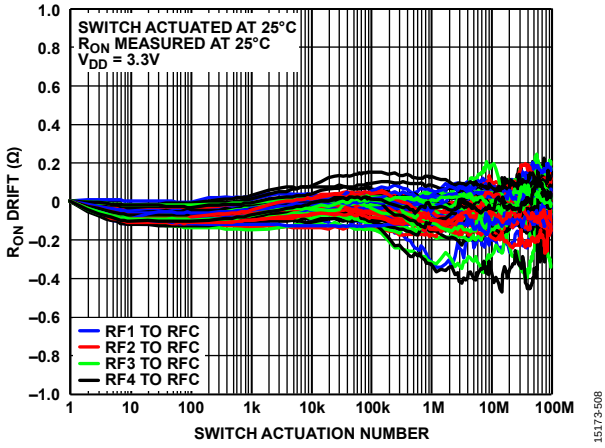


Figure 8. R_{ON} Drift vs. Switch Actuation Number, Normalized at Zero, Switch Actuated at 25°C and R_{ON} Measured at 25°C

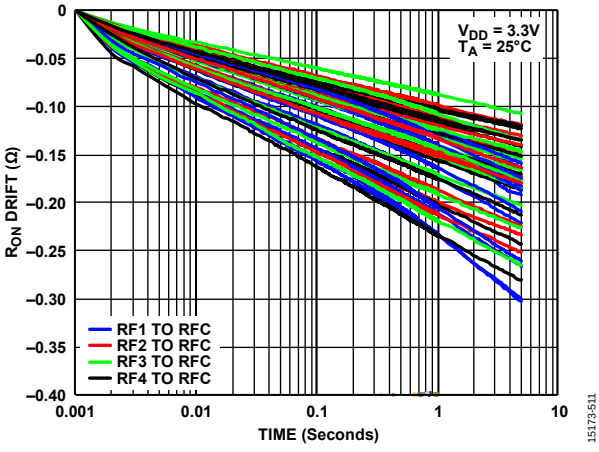


Figure 11. R_{ON} Drift vs. Time (1 ms to 5 sec) on Log Scale, Normalized at Zero

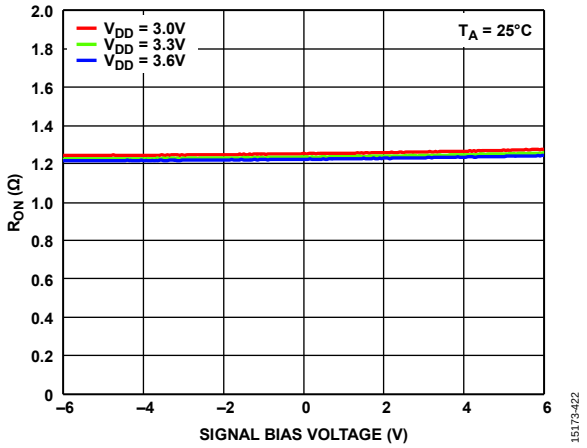


Figure 12. R_{ON} vs. Signal Bias Voltage over Supply Voltages (Measured 5 sec Post Switch Turn On Time, RF1 to RFC on)

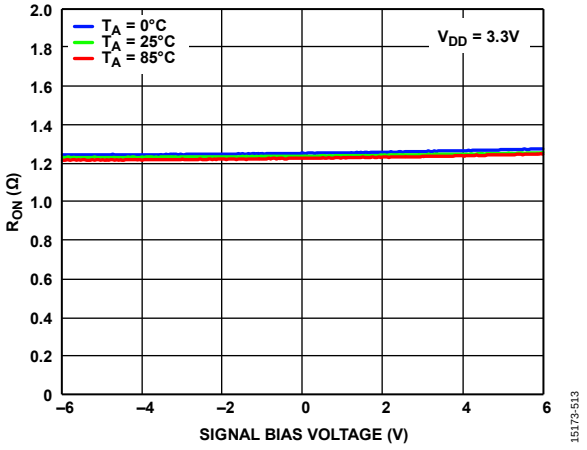


Figure 13. R_{ON} vs. Signal Bias Voltage over Temperature (Measured 5 sec Post Switch Turn On Time, RF1 to RFC on)

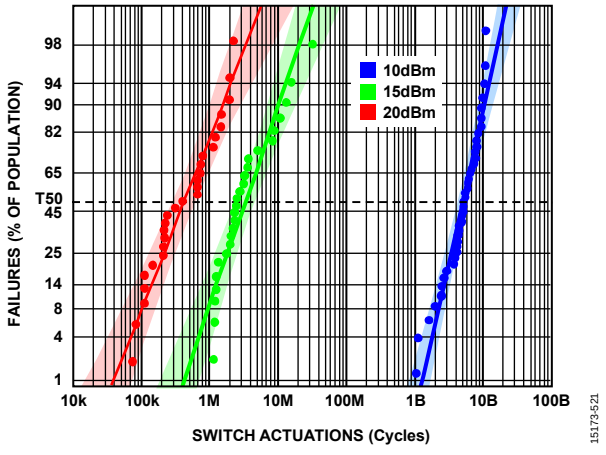


Figure 14. Hot Switching Probability Distribution on Log Normal with 95% Confidence Interval (CI) (RF Power = CW, Terminated into 50 Ω, T_A = 25°C, V_{DD} = 3.3 V)

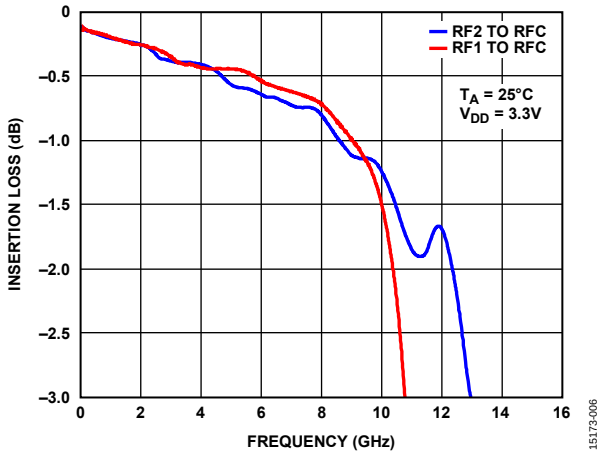


Figure 15. Insertion Loss vs. Frequency, Linear Scale (V_{DD} = 3.3 V)

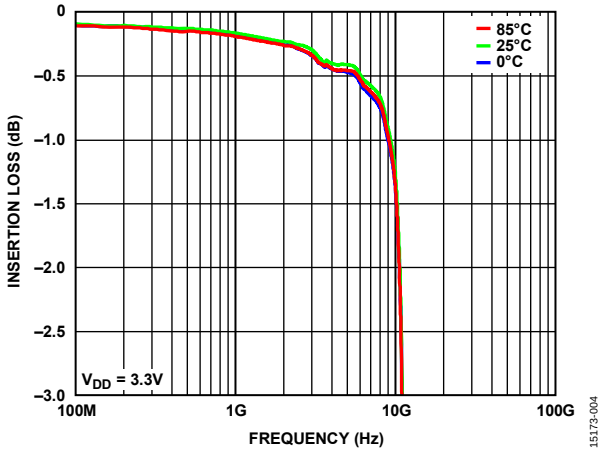


Figure 16. Insertion Loss vs. Frequency over Temperature (V_{DD} = 3.3 V, RF1 to RFC)

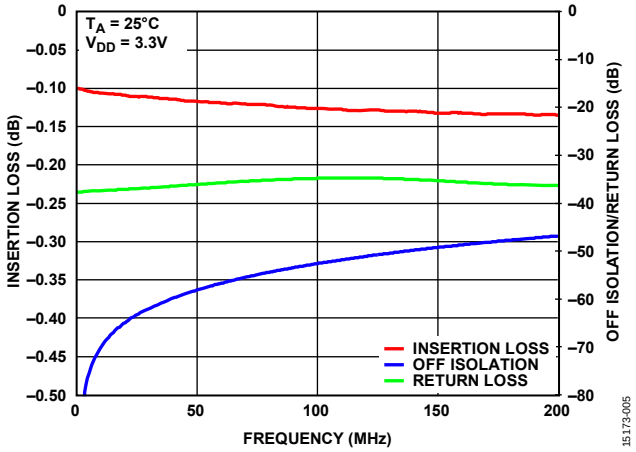


Figure 17. Insertion Loss and Off Isolation/Return Loss vs. Frequency (V_{DD} = 3.3 V, RF1 to RFC)

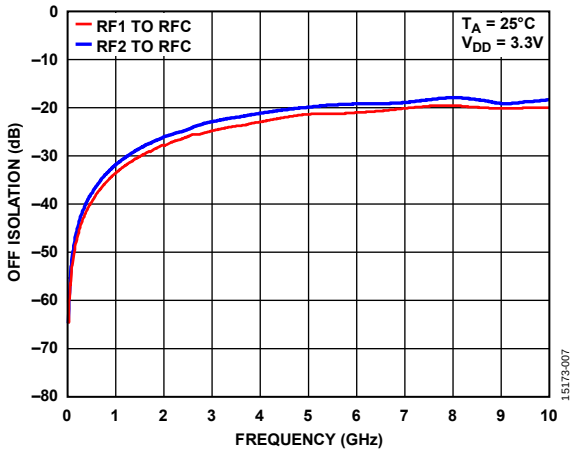


Figure 18. Off Isolation vs. Frequency, All Channels Off (V_{DD} = 3.3 V)

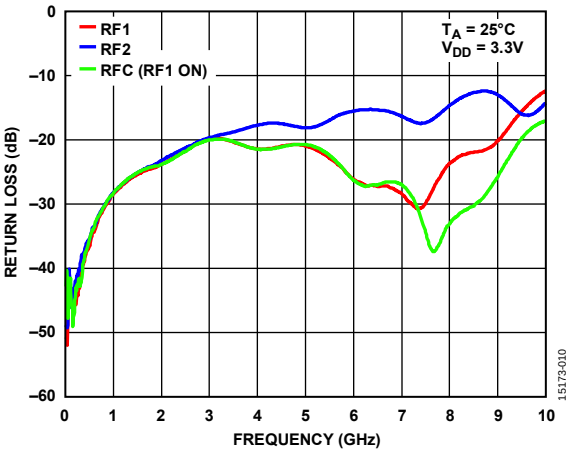


Figure 21. Return Loss vs. Frequency (V_{DD} = 3.3 V)

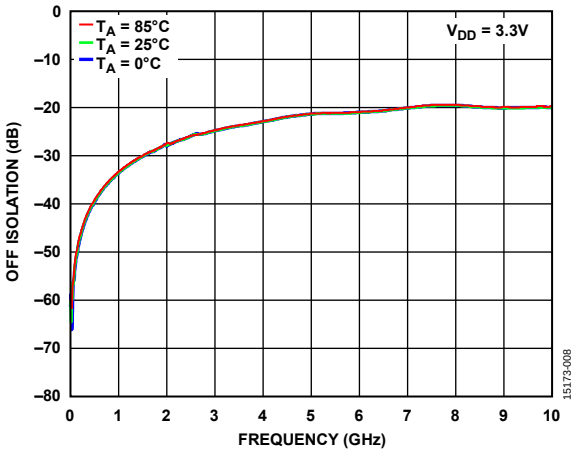


Figure 19. Off Isolation vs. Frequency over Temperature, All Channels Off (V_{DD} = 3.3 V, RF1 to RFC)

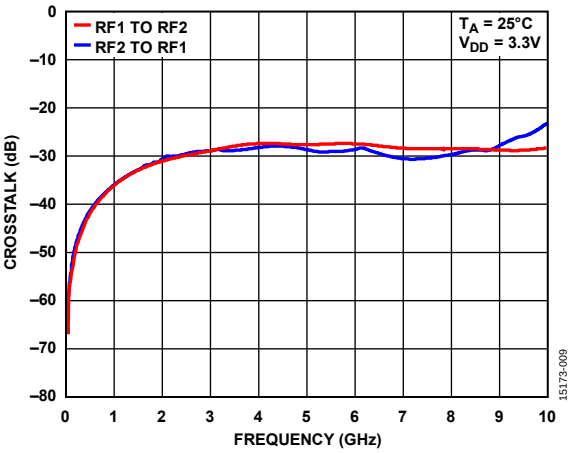


Figure 22. Crosstalk vs. Frequency (V_{DD} = 3.3 V)

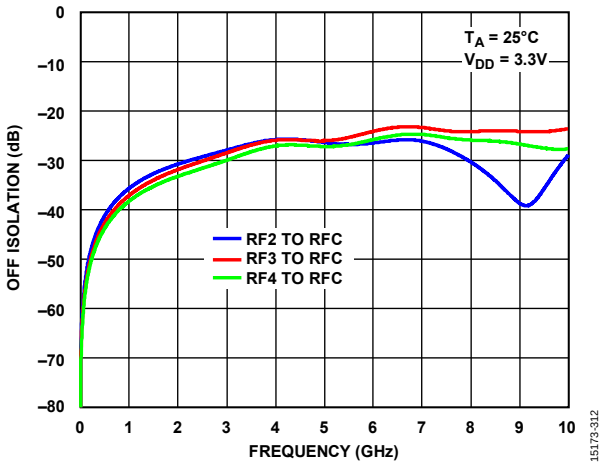


Figure 20. Off Isolation vs. Frequency, RF1 to RFC On (V_{DD} = 3.3 V)

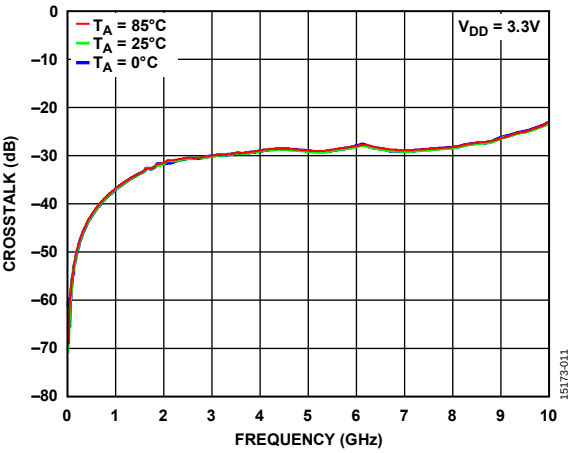


Figure 23. Crosstalk vs. Frequency over Temperature (V_{DD} = 3.3 V, RF2 to RF1)

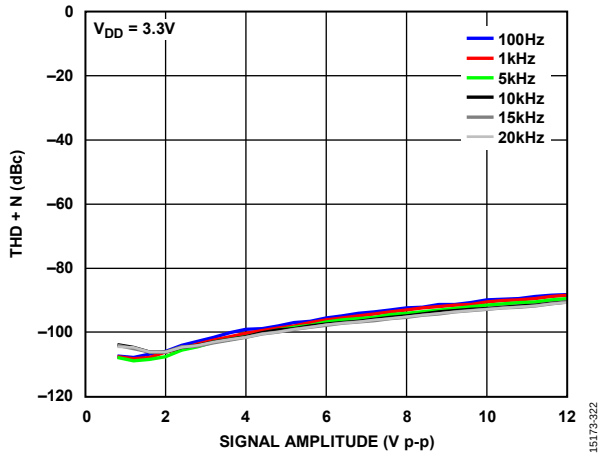


Figure 24. THD + N vs. Signal Amplitude (V_{DD} = 3.3 V, R_{LOAD} = 300 Ω, T_A = 25°C, Signal Source Impedance = 20 Ω)

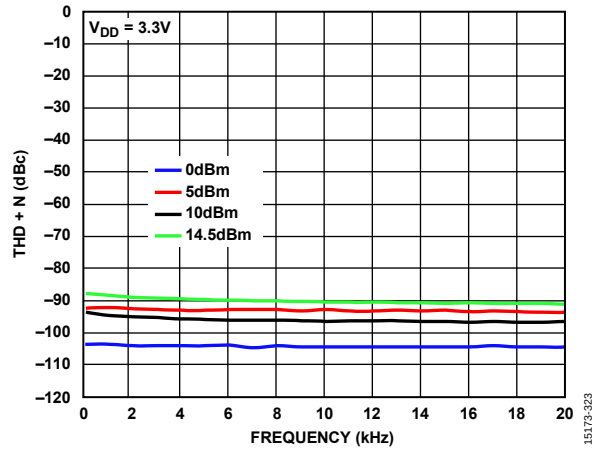


Figure 25. THD + N vs. Frequency (V_{DD} = 3.3 V, R_{LOAD} = 300 Ω, T_A = 25°C, Signal Source Impedance = 20 Ω

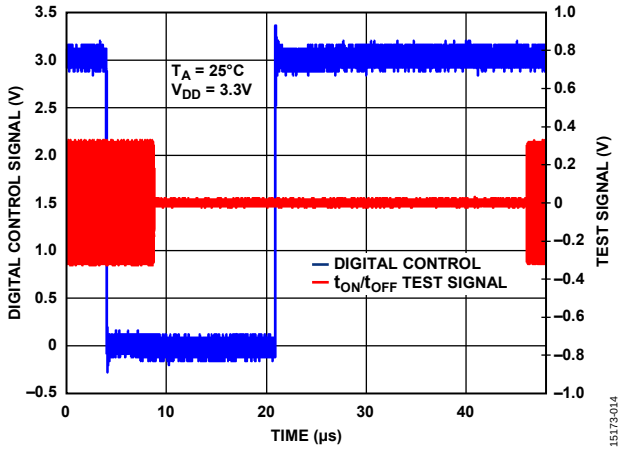


Figure 26. Digital Control Signal and Test Signal vs. Time (V_{DD} = 3.3 V)

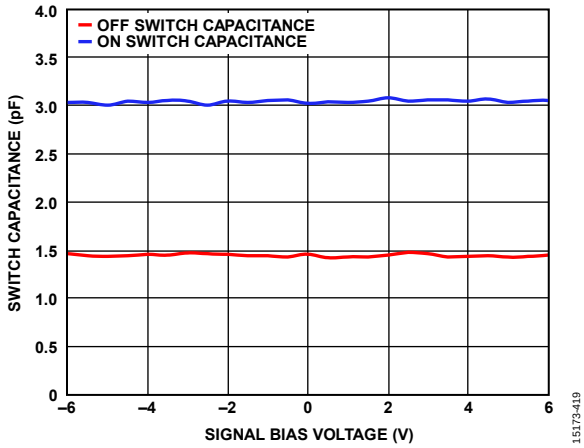


Figure 27. Switch Capacitance vs. Signal Bias Voltage

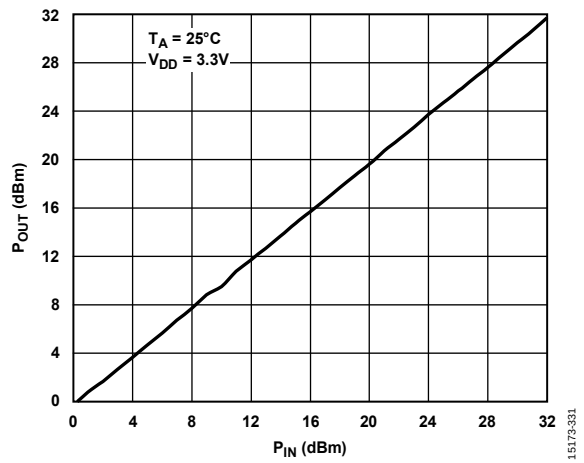


Figure 28. Output Power (P_{OUT}) vs. Input Power (P_{IN}) (V_{DD} = 3.3 V, Signal Frequency = 4 GHz)

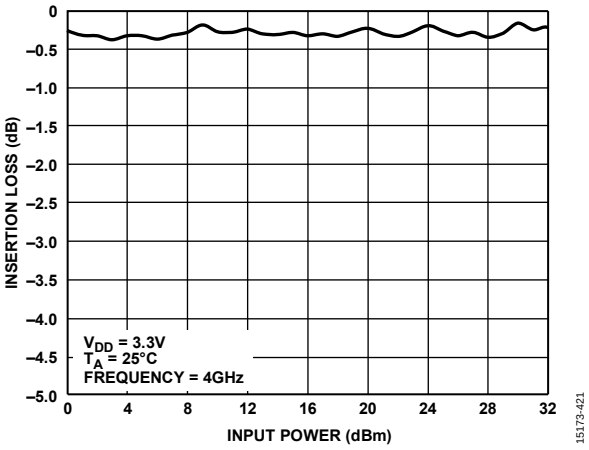


Figure 29. Insertion Loss vs. Input Power

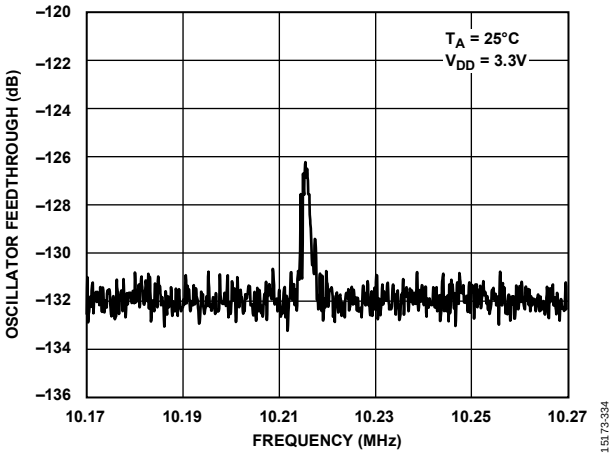


Figure 30. Oscillator Feedthrough vs. Frequency, Zoomed in at 10.2 MHz (V_{DD} = 3.3 V)

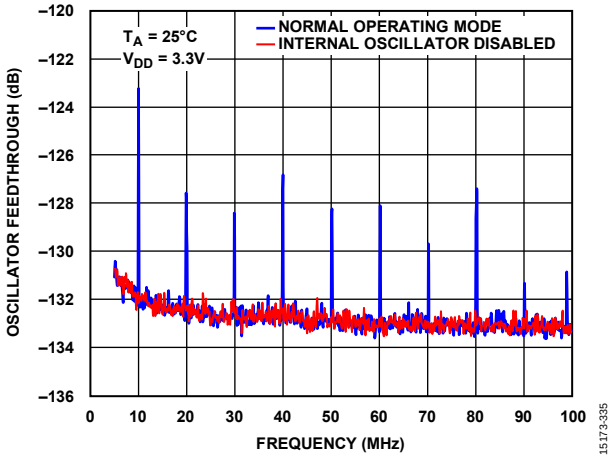


Figure 31. Oscillator Feedthrough vs. Frequency, Wide Bandwidth (V_{DD} = 3.3 V)

TEST CIRCUITS

The test circuits shown in Figure 32 to Figure 43 are applicable to all channels. Additional pins are omitted for clarity and V_S is the source voltage.

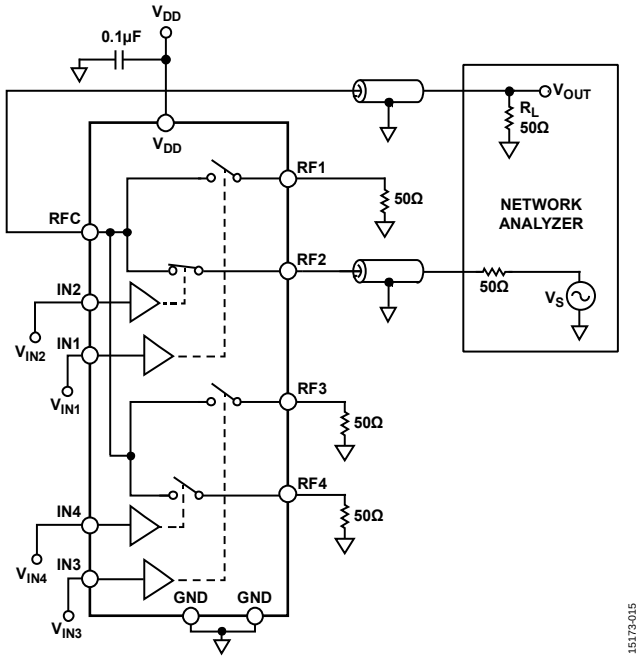


Figure 32. Insertion Loss and Return Loss

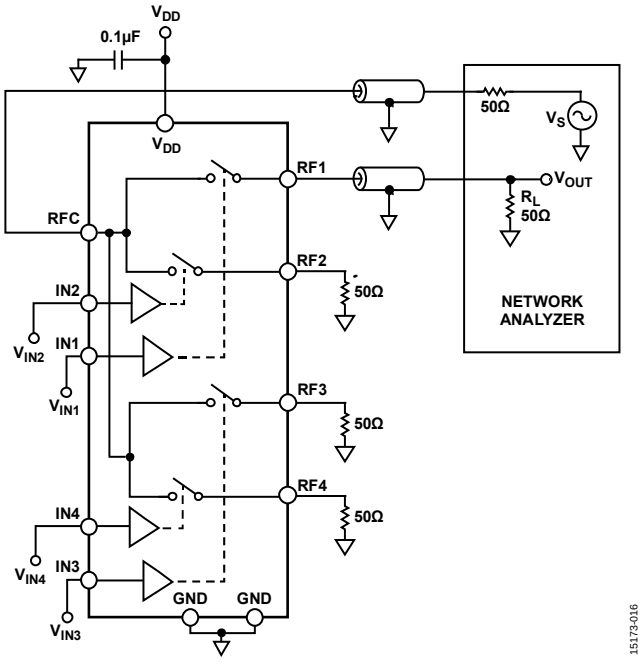


Figure 33. Isolation (All Switches Off)

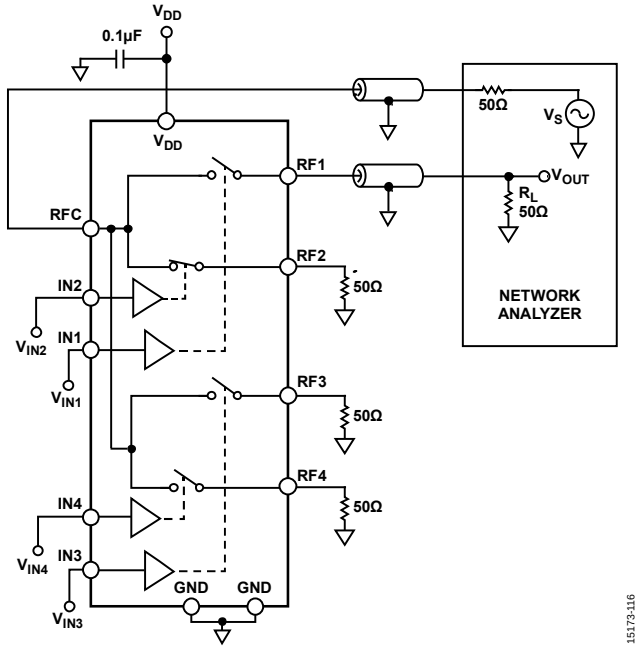


Figure 34. Isolation (RF2 to RFC On, RF1 to RFC Off)

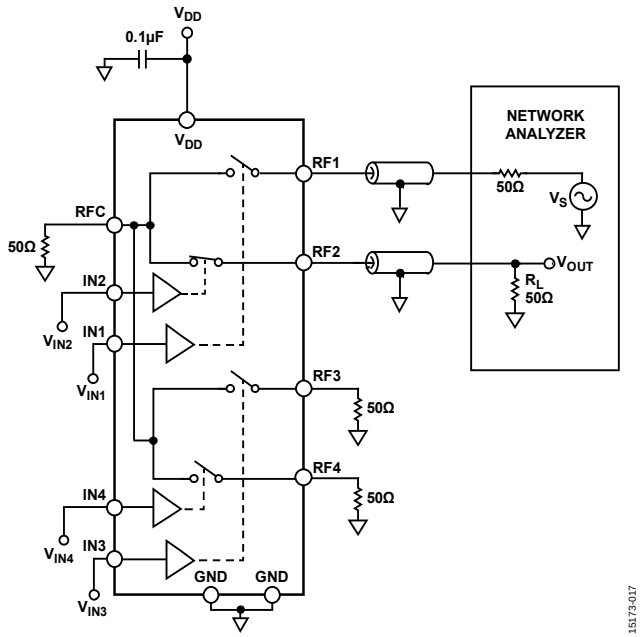


Figure 35. Crosstalk

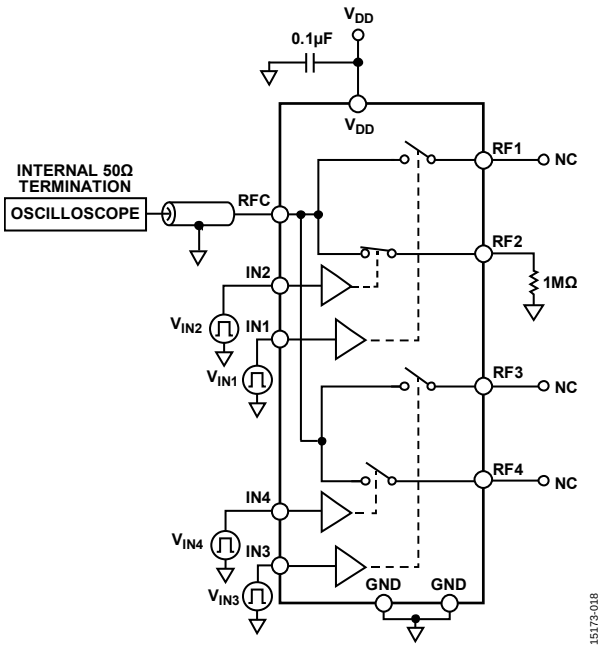


Figure 36. Video Feedthrough

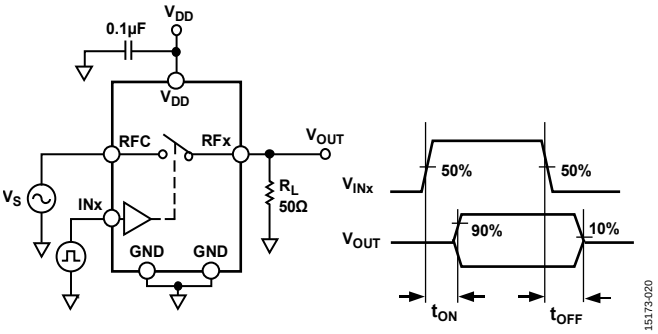


Figure 38. Switch Timing, t_{ON} and t_{OFF} (All RFx Terminals Connected to 50 Ω Termination)

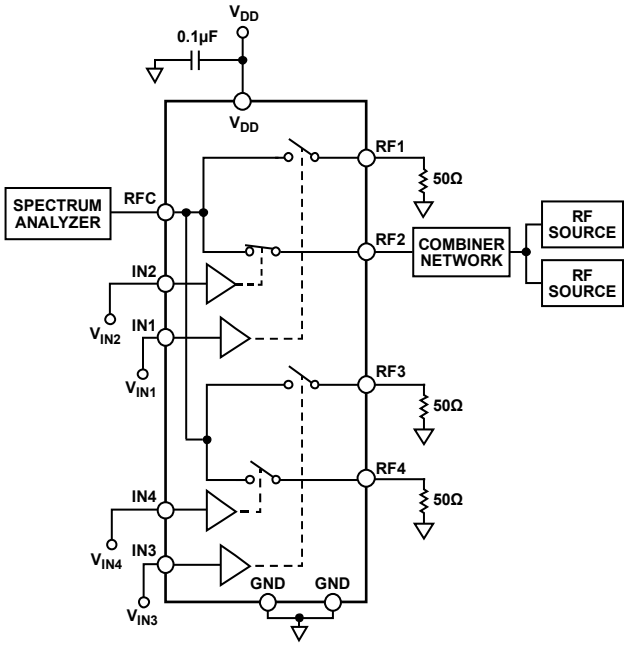


Figure 37. IP2 and IP3

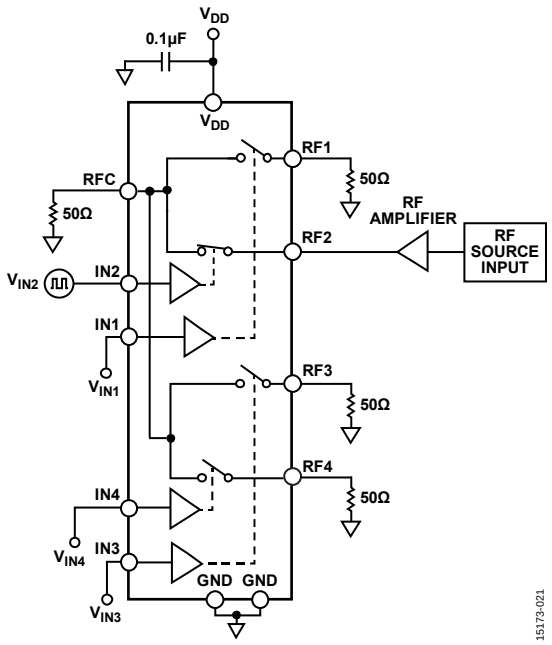


Figure 39. Hot Switching Evaluation Setup, 2 GHz RF Source, 50% Duty Cycle, 5 kHz Switching Actuation Speed

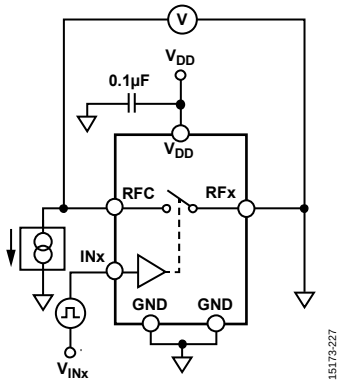


Figure 40. On Resistance

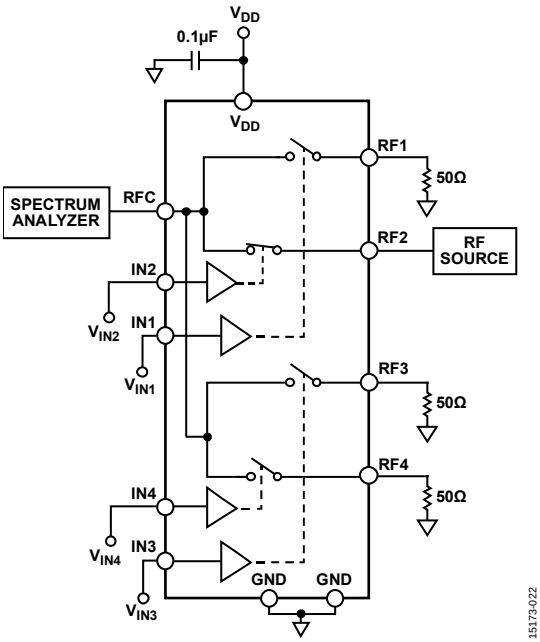


Figure 42. Second and Third Harmonics, RF Power

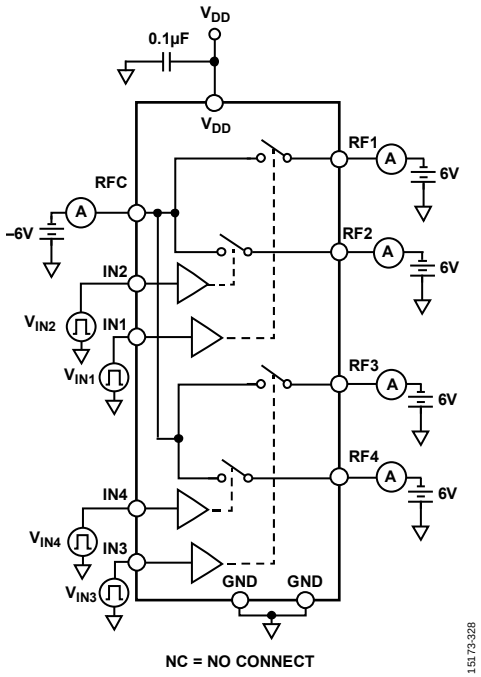


Figure 41. Off Leakage

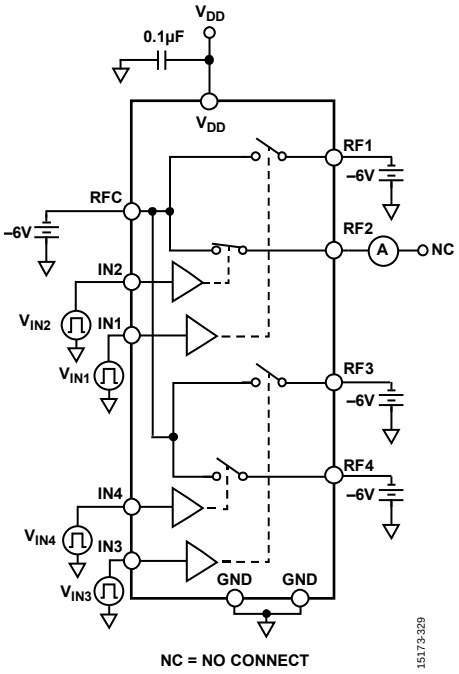


Figure 43. On Leakage

TERMINOLOGY

Insertion Loss
Insertion loss is the amount of signal attenuation between the input and output ports of the switch when the switch is in the on state. Expressed in decibels, ensure that insertion loss is as small as possible for maximum power transfer.

An example calculation of insertion loss based on the setup in Figure 32 is as follows:

$$Insertion\ Loss\ (\text{dB}) = -20\log_{10}|S_{RF2RFC}|$$

where S_{RF2RFC} is the transmission coefficient measured from RF2 to RFC with RF2 in the on position. All unused switches are in the off position and terminated in a purely resistive load of 50 Ω.

Isolation
Isolation is the amount of signal attenuation between the input and output ports of the switch when the switch is in the off state. Expressed in decibels, ensure that isolation is as large as possible.

An example calculation of isolation based on the setup in Figure 33 is as follows:

$$Isolation\ (\text{dB}) = -20\log_{10}|S_{RFCRF1}|$$

where S_{RFCRF1} is the transmission coefficient measured from RFC to RF1 with RF1 in the off position. All unused switches are in the off position and terminated in a purely resistive load of 50 Ω.

Crosstalk
Crosstalk is a measure of unwanted signals coupled through from one channel to another because of parasitic capacitance.

An example calculation of crosstalk based on the setup in Figure 35 is as follows:

$$Crosstalk\ (\text{dB}) = -20\log_{10}|S_{RF1RF2}|$$

where S_{RF1RF2} is the transmission coefficient measured from RF1 to RF2 with RF1 in the off position and RF2 in the on position. All unused switches are in the off position and terminated in a purely resistive load of 50 Ω.

Return Loss
Return Loss is the magnitude of the reflection coefficient expressed in decibels, and the amount of reflected signal relative to the incident signal.

An example calculation of return loss based on the setup in Figure 32 is as follows:

$$Return\ Loss\ (\text{dB}) = -20\log_{10}|S_{11}|$$

where S_{11} is the reflection coefficient of the port under test.

Third-Order Intermodulation Intercept (IP3)
IP3 is the intersection point of the fundamental P_{OUT} vs. P_{IN} extrapolated line and the third-order intermodulation products extrapolated line of a two-tone test. IP3 is a figure of merit that characterizes the switch linearity.

Second-Order Intermodulation Intercept (IP2)
IP2 is the intersection point of the fundamental P_{OUT} vs. P_{IN} extrapolated line and the second-order intermodulation products extrapolated line of a two-tone test. IP2 is a figure of merit that characterizes the switch linearity.

Second Distortion Harmonic (HD2)
HD2 is the amplitude of the second distortion harmonic, where, for a signal whose fundamental frequency is f, the second distortion harmonic has a frequency of 2 f. This measurement is a single-tone test expressed with reference to the carrier signal (dBc).

Third Distortion Harmonic (HD3)
HD3 is the amplitude of the third distortion harmonic, where, for a signal whose fundamental frequency is f, the third distortion harmonic has a frequency of 3 f. This measurement is a single tone test expressed with reference to the carrier signal (dBc).

On Switching Time (t_{ON})
t_{ON} is the time it takes for the switch to turn on. t_{ON} is measured from 50% of the control signal (INx) to 90% of the on level. No power was applied through the switch during this test (cold switched). The switch was terminated into a 50 Ω load.

Off Switching Time (t_{OFF})
t_{OFF} is the time it takes for the switch to turn off. t_{OFF} is measured from 50% of the control signal (INx) to 10% of the on level. No power was applied through the switch during this test (cold switched). The switch was terminated into a 50 Ω load.

Actuation Frequency
The actuation frequency refers to the speed at which the ADGM1004 can be switched on and off. The actuation frequency is dependent on both the settling times and the on and off switching times.

Power-Up Time
The power-up time is a measure of the time required for the device to power up and start to pass 90% of an RF input signal after the V_{DD} pin reaches 95%.

Video Feedthrough
Video feedthrough is a measure of the spurious signals present at the RFx ports of the switch when the control voltage is switched from high to low or from low to high without an RF signal present.

Internal Oscillator Frequency
The internal oscillator frequency is the value of the on-board oscillator that drives the gate control chip of the ADGM1004.

Internal Oscillator Feedthrough
The internal oscillator feedthrough is the amount of internal oscillator signal that feeds through to the RFx and RFC pins of the switch. This signal appears as a noise spur on the RFx and RFC pins of the switch at the frequency the oscillator is operating at and the harmonics thereof.

On Resistance (R_{ON})
R_{ON} is the resistance of a switch in the closed/on state measured between the RFx and RFC package pins. Measure resistance in 4-wire mode to null out any cabling or PCB series resistances.

On Resistance Drift
On resistance drift is the change in the R_{ON} of the switch over the specified criteria in Table 1.

Continuously On Lifetime
The continuously on lifetime parameter measures how long the switch is left in a continuously on state. If the switch is left in the on position for an extended period, this parameter affects the turn off mechanism of the device.

Actuation Lifetime
Actuation lifetime is the number of consecutive open, close, and open cycles that the device can complete without the R_{ON} exceeding a specified limit and no occurrence of failures to open (FTO) or failures to close (FTC).

Cold Switching
Cold switching operates the switch in a mode so that no voltage differential exists between the source and the drain when the switch is closed and/or no current is flowing from the source to the drain when the switch opens. All switches have longer lives when cold switched.

Hot Switching
Hot switching is operating the switch in a mode where a voltage differential exists between the source and the drain when the switch is closed and/or current is flowing from RFx to RFC when the switch opens. Hot switching results in a reduced switch life, depending on the magnitude of the open circuit voltage between the source and the drain.

Input High Voltage (V_{INH})
V_{INH} is the minimum input voltage for Logic 1.

Input Low Voltage (V_{INL})
V_{INL} is the maximum input voltage for Logic 0.

Input Current (I_{INL}, I_{INH})
I_{INL} and I_{INH} are the low and high input currents of the digital inputs.

Low Power Mode Current ($I_{DD\ EXT\ VCP}$)
$I_{DD\ EXT\ VCP}$ is the amount of supply current used by the gate driver circuity when the internal oscillator and the charge pump circuitry are disabled by setting the EXTD_EN pin high.

External Drive Current ($I_{CP\ EXT\ VCP}$)
$I_{CP\ EXT\ VCP}$ is the amount of current used by the ADGM1004 from the external 80 V power supply when the internal oscillator and the charge pump circuitry are turned off by setting EXTD_EN pin high.

THEORY OF OPERATION

The ADGM1004 is a wideband SP4T switch fabricated using Analog Devices MEMS switch technology. This technology enables high power, low loss, low distortion GHz switches for use in demanding RF applications.

The MEMS switch simultaneously brings together high frequency RF performance and 0 Hz/dc precision performance. This combination, coupled with superior reliability and a tiny surface-mountable form factor, makes the MEMS switch an ideal switching solution for all RF and precision signal instrumentation needs.

Figure 44 shows a cross section of the switch with dimensions. The switch is an electrostatically actuated cantilever beam connected in a 3-terminal configuration. Functionally, the switch is analogous to a field effect transistor (FET). The terminals can be used as a source, gate, or drain.

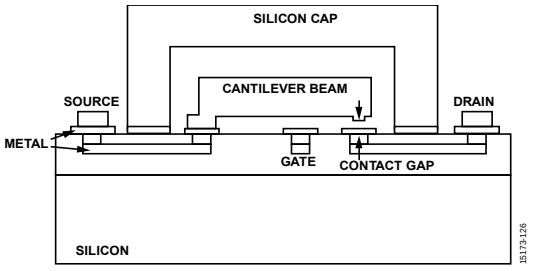


Figure 44. Cross Section of the MEMS Switch Design Showing the Cantilever Switch Beam (Not to Scale)

When a dc actuation voltage is applied between the gate electrode and the source (the switch beam), an electrostatic force is generated, resulting in attracting the beam toward the substrate. A separate on-board driver IC generates the 80 V bias voltage used for actuation.

When the bias voltage between the gate and the source exceeds the threshold voltage of the switch (V_{TH}) the contacts on the beam touch the drain, which completes the circuit between the source and the drain and turns the switch on. When the bias voltage is removed, that is, the 0 V on the gate electrode, the beam acts as a spring generating a sufficient restoring force to open the connection between the source and the drain, thus breaking the circuit and turning the switch off.

The silicon cap covering the switch die is shown in Figure 44. This cap hermetically seals the switch, which improves reliability. The switch contacts do not suffer from dry switching or low power switching lifetime degradation.

PARALLEL DIGITAL INTERFACE

The ADGM1004 is controlled via a parallel digital interface. Standard complimentary metal-oxide semiconductor (CMOS)/ low voltage transistor to transistor logic (LVTTL) signals applied through this interface control the actuation or release of all ADGM1004 switch channels. Gate signals applied are boosted to provide the required voltages required to actuate the MEMS switch.

Setting the $\overline{\text{PIN}}$/SPI pin low enables the parallel digital interface in 4-wire SP4T mode. In parallel mode, Pin 1 to Pin 4 (IN1 to IN4) control the switching functions of the ADGM1004. When a Logic 1 is applied to one of these pins, the gate of the corresponding switch is activated and the switch turns on. Conversely, when a Logic 0 is applied to one of these pins, the switch turns off. Note that it is possible to connect more than one RFx input to RFC at a time. See Table 6 for the ADGM1004 truth table.

Table 6. Truth Table When in Parallel Digital Interface Mode

IN1	IN2	IN3	IN4	RF1 to RFC	RF2 to RFC	RF3 to RFC	RF4 to RFC
0	0	0	0	Off	Off	Off	Off
0	0	0	1	Off	Off	Off	On
0	0	1	0	Off	Off	On	Off
0	0	1	1	Off	Off	On	On
0	1	0	0	Off	On	Off	Off
0	1	0	1	Off	On	Off	On
0	1	1	0	Off	On	On	Off
0	1	1	1	Off	On	On	On
1	0	0	0	On	Off	Off	Off
1	0	0	1	On	Off	Off	On
1	0	1	0	On	Off	On	Off
1	0	1	1	On	Off	On	On
1	1	0	0	On	On	Off	Off
1	1	0	1	On	On	Off	On
1	1	1	0	On	On	On	Off
1	1	1	1	On	On	On	On

SPI DIGITAL INTERFACE

The ADGM1004 can be controlled via a digital SPI when the $\overline{PIN}$/SPI pin is high. The SPI is compatible with SPI Mode 0 (clock polarity (CPOL) = 0, clock phase (CPHA) = 0) and Mode 3 (CPOL = 1, CPHA = 1) and it operates with SCLK frequencies up to 10 MHz. When the SPI is active, the default mode is addressable, in which, the device registers are accessed by a 16-bit SPI command that is bound by the state of the $\overline{CS}$ pin. The ADGM1004 can also operate in daisy-chain mode.

The SPI interface pins of the ADGM1004 are $\overline{CS}$, SCLK, SDI, and SDO. Hold the $\overline{CS}$ pin low when using the SPI. The data on the SDI pin is captured on the rising edge of SCLK, and data is propagated out on the SDO pin on the falling edge of SCLK. The SDO pin has a push pull output driver architecture. Therefore, the ADGM1004 does not require pull-up resistors. The two modes of SPI operation are: addressable and daisy-chain.

Addressable Mode

Addressable mode is the default mode for the ADGM1004 upon power-up. A single SPI frame in addressable mode is bound by a $\overline{CS}$ falling edge and the succeeding $\overline{CS}$ rising edge. The frame is comprised of 16 SCLK cycles. The timing diagram for addressable mode is shown in Figure 45. The first SDI signal bit indicates if the SPI command is a read or write command. The next seven bits determine the target register address. The remaining eight bits provide the data to the addressed register. The first eight bits are ignored during a read command because the SDO pin propagates out the data contained in the addressed register during these clock cycles.

The target register address of an SPI command is determined on the eighth SCLK rising edge. Data from this register propagates out on the SDO pin from the 9th to the 16th SCLK falling edge during SPI reads. A register write occurs on the 16th SCLK rising edge during SPI writes. During any SPI command, the SDO pin sends out eight alignment bits on the first eight SCLK falling edges. The alignment bits observed at the SDO pin are 0x25.

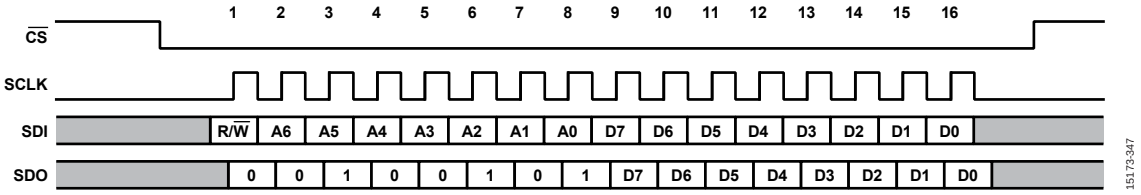


Figure 45. Addressable Mode Timing Diagram

Daisy-Chain Mode

The connection of several ADGM1004 devices in a daisy-chain configuration is possible. All devices share the same $\overline{CS}$ and SCLK lines while the SDO pin of one device forms a connection to the SDI pin of the next device, creating a shift register. In daisy-chain mode, the SDO signal is an 8-cycle delayed version of the SDI signal (see Figure 47).

The ADGM1004 can only enter daisy-chain mode from addressable mode by sending the 16-bit SPI command, 0x2500. See Figure 47 for an example of this command. When the ADGM1004 receives this command, the SDO pin of the devices sends out the same command because the alignment bits at the SDO pin are 0x25. This command allows multiple daisy-chained devices to enter daisy-chain mode in a single SPI frame. A hardware reset is required to exit daisy-chain mode.

For the timing diagram of a typical daisy-chain SPI frame, see Figure 48. When the $\overline{CS}$ pin goes high, Device 1 writes Command 0, Bits[7:0], to the SWITCH_DATA register, Device 2 writes Command 1, Bits[7:0], to the switches, and so on. The SPI block uses the last eight bits received through the SDI pin to update the switches. After entering daisy-chain mode, the first eight bits sent out by the SDO pin are 0x00. When $\overline{CS}$ goes high, the internal shift register value does not reset back to 0.

An SCLK rising edge reads in data on the SDI pin while data is propagated out of the SDO pin on an SCLK falling edge. The expected number of SCLK cycles are a multiple of eight before the $\overline{CS}$ pin goes high. When this is not the case, the SPI interface sends the last eight bits received to the SWITCH_DATA register.

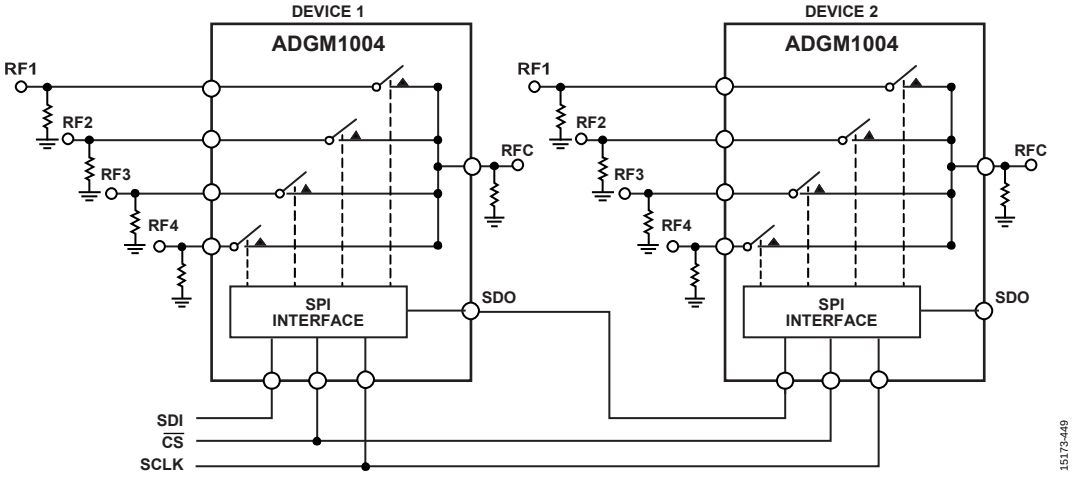


Figure 46. Two SPI Controlled ADGM1004 Switches Connected in Daisy-Chain Configuration

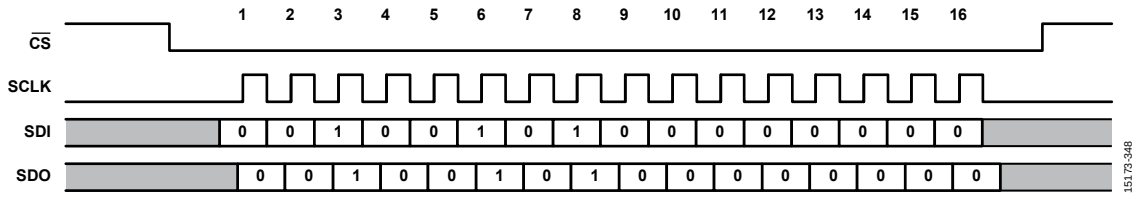


Figure 47. SPI Command to Enter Daisy-Chain Mode

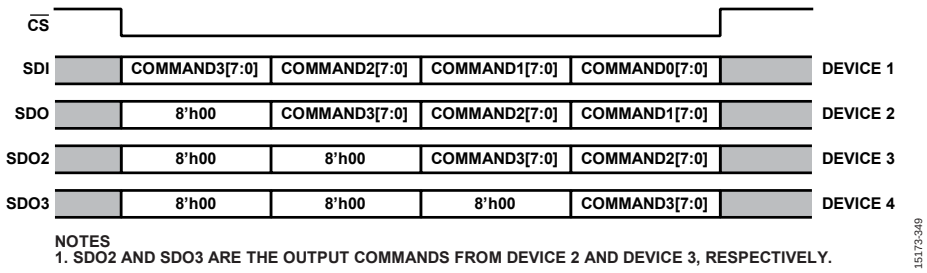


Figure 48. Example of SPI Frame with Three ADGM1004 Switches Connected in Daisy-Chain Mode

Hardware Reset

The digital section of the ADGM1004 goes through an initialization phase during V_{DD} power-up. To hardware reset the device, power cycle the V_{DD} input. After power-up or a hardware reset, ensure that there is a minimum of 10 µs from the time of power-up or reset before any SPI command is issued. Ensure that V_{DD} does not drop out during the 10 µs initialization phase because V_{DD} dropout can result in incorrect operation of the ADGM1004.

Internal Error Status

When an internal error is detected in the device, the internal error is flagged by the INTERNAL_ERROR bits (Bits[7:6]) of the SWITCH_DATA register (Register 0x20), as shown in Table 9. An internal error results from an error in the configuration of the device at power up.

INTERNAL OSCILLATOR FEEDTHROUGH

The ADGM1004 has an internal oscillator running at a nominal 10 MHz. This oscillator drives the charge pump circuitry that provides the actuation voltage for each switch gate electrode. Although this oscillator is low power, the 10 MHz signal is coupled to the switch and is considered a noise spur on the switch channels. The magnitude of this feedthrough noise spur is specified in Table 1 and is typically −123 dBm or −146 dBm/Hz when one switch is on. When all four switches are simultaneously on, the feedthrough goes up to −120 dBm. V_{DD} level and temperature changes affect the frequency of the noise spur. For the maximum and minimum frequency range over temperature and voltage supply range, see Table 1.

INTERNAL OSCILLATOR FEEDTHROUGH MITIGATION

In normal operation, the 80 V actuation voltage is supplied by the driver IC. Setting the EXTD_EN pin low enables the built in 10 MHz oscillator. This setting enables the charge pump circuitry to generate the 80 V required for MEMS switch actuation. The internal oscillator is a source of noise that couples through to the RF ports. The magnitude of this feedthrough noise spur is specified in Table 1 and is typically −123 dBm or −146 dBm/Hz when one switch is on. To eliminate the internal oscillator feedthrough, set the EXTD_EN pin high to disable the internal oscillator and charge pump circuitry. When the internal oscillator and charge pump circuitry is disabled, the V_{CP} pin must be driven with 80 V dc (VCP_{EXT}) from an external voltage supply required for MEMS switch actuation, as shown in Table 5. The switch can still be controlled via the digital logic interface pins.

LOW POWER MODE

Setting the EXTD_EN pin high shuts down the internal oscillator. The ADGM1004 enters a low power quiescent state, drawing only 50 µA maximum supply current.

TYPICAL OPERATING CIRCUIT

Figure 49 shows the typical operating circuit for the ADGM1004 as used in the EVAL-ADGM1004SDZ evaluation board. A 47 pF (100 V rated) external capacitor (C_{CP}) is required on the V_{CP} pin. This capacitor is a holding capacitor for the 80 V dc gate drive voltage.

In the circuit shown in Figure 49, V_{DD} is connected to 3.3 V. EP1 connects to EP2 internally. Typically, one large GND pad on the PCB is used to short together EP1 and EP2. Figure 49 shows the ADGM1004 configured to use the internal oscillator as the reference clock to the driver IC control circuit. Alternatively, set the EXTD_EN pin high and apply 80 V dc directly to the V_{CP} pin to disable the internal oscillator and eliminate all oscillator feedthrough. The switches can then be controlled normally via the logic control interface, IN1 to IN4.

To avoid any floating nodes, connect a 10 MΩ shunt resistor to GND on all RFx pins (RF1 to RF4, and RFC), as shown in Figure 49. See the Floating Node section for more information.

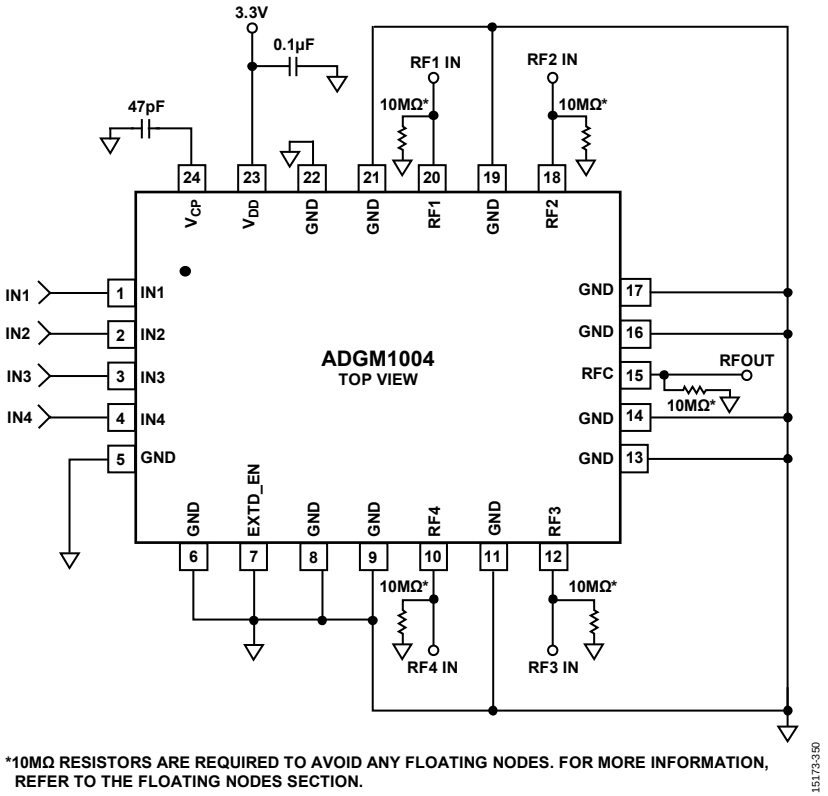


Figure 49. Typical Operating Circuit

APPLICATIONS INFORMATION

SWITCHABLE RF ATTENUATOR

RF attenuator networks are commonly used in RF instrumentation equipment, such as vector network analyzers, spectrum analyzers, and signal generators. Routing RF signals through an attenuator can enable the equipment to accept higher power signals and, therefore, increase the dynamic range of the instrument. In RF attenuation applications like the vector network analyzers, spectrum analyzers, and signal generators, maintaining the bandwidth of the signal after the signal passes through the network is critical. Any degradation of the signal reduces the performance of the equipment. Therefore, the RF characteristics of the switches used for routing are an integral part of the quality of an attenuator network.

The ADGM1004 MEMS switch with low flat insertion loss, wide RF bandwidth, and high reliability is suited for use as a switchable RF attenuator. The ADGM1004, as an SP4T switch, also brings added flexibility. Figure 50 shows an example attenuation network configuration using two ADGM1004 switches and three different attenuators. The fourth channel of the switches is used as a nonattenuated route in Figure 50.

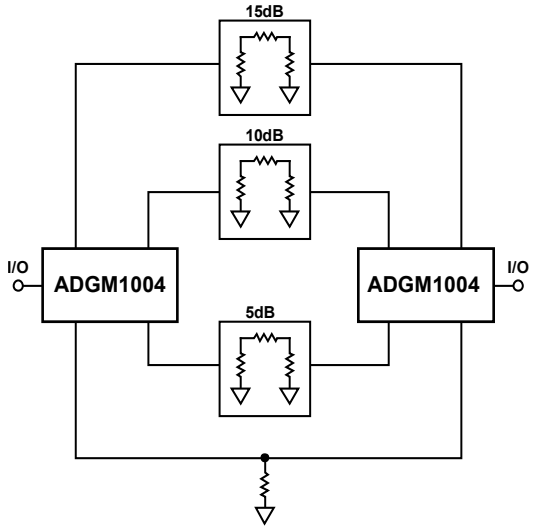


Figure 50. Switching RF Attenuators Using Two ADGM1004 MEMS Switches

RECONFIGURABLE RF FILTER

A reconfigurable RF filter is advantageous in many RF front-end applications. A reconfigurable RF filter provides more saved space. As space becomes more constrained in applications, the option to have an economical reconfigurable RF filter instead of individual frequency dependent filters is preferred.

The ADGM1004 low flat insertion loss, wide RF bandwidth, low parasitic, low capacitance, and high linearity are required to turn on the lump components (capacitor and inductor), which make the MEMS switch suited for reconfigurable filter application.

In applications such as wireless communications or mobile radios, the number of bands and/or modes constantly increases. A reconfigurable RF filter allows more bands and/or modes to be covered using the same components.

Figure 51 shows an example of a reconfigurable band-pass filter. The topology shown is of a generalized, two section, inductively coupled, single-ended band-pass filter, nominally centered on a 400 MHz ultrahigh frequency (UHF) band. The MEMS switches are positioned in series with each shunt inductor.

The function of the switches includes or omits a shunt inductor from the circuit. Changing the shunt inductor value affects the bandwidth and center frequency of the filter. Using inductance values from 15 nH to 30 nH significantly alters the bandwidth and center frequency, allowing the filter to dynamically configure to operate in the UHF bands or very high frequency (VHF) bands while preserving the 50 Ω match on the input and output ports. The low R_{ON} value and wide bandwidth of the MEMS switch makes the switch an ideal choice for this application. The low R_{ON} reduces the negative effect a series resistance has on the quality factor of the shunt inductor. The large bandwidth enables higher frequency band-pass filters.

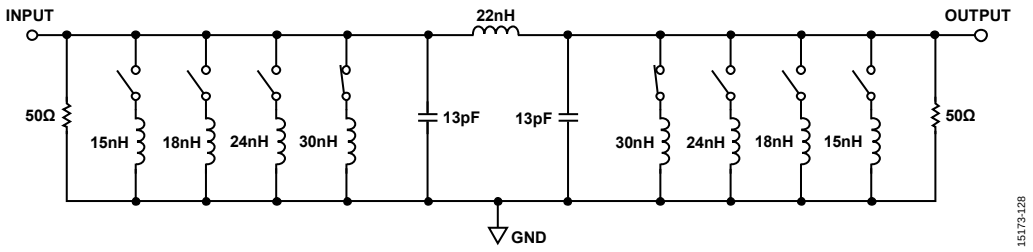


Figure 51. Reconfigurable Band-Pass Filter Achieved Using Two ADGM1004 MEMS Switches

CRITICAL OPERATIONAL REQUIREMENTS

SYSTEM ERROR CONSIDERATIONS DUE TO ON-RESISTANCE DRIFT

The R_{ON} performance of the ADGM1004 is affected by part to part variation, channel to channel variation, cycle actuations, settling time post turn on, bias voltage, and temperature changes (see Figure 6 to Figure 13).

In a 50 Ω system, the on-resistance drift over switch actuations (ΔR_{ON}) can introduce system inaccuracy. Figure 52 shows the ADGM1004 connected with the load in a 50 Ω system, where R_S is the source impedance. TO calculate the system error caused by the ADGM1004 on-resistance drift, use the following equation:

$$System\ Error\ (\%) = \Delta R/R_{LOAD}$$

where:
ΔR is the ADGM1004 on-resistance drift.
R_{LOAD} is the load impedance.

The ADGM1004 on-resistance drift also affects insertion loss, which must be considered when using the device. To calculate the on-resistance impact on insertion loss, use the following equation:

$$Insertion\ Loss = 10\log(1 + (\Delta R/R_{LOAD}))$$

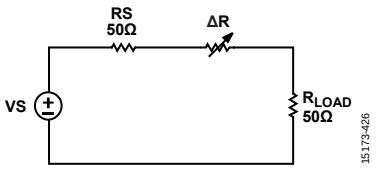


Figure 52. 50 Ω System Representation Where the ADGM1004 is Connected with the Load

Table 7. System Error and Insertion Loss Error Due to ADGM1004 R_{ON} Drift

On-Resistance Drift	System Error (%)	Insertion Loss Error (dB)
4.75	9.5	0.39
5	10	0.41

FLOATING NODE

The ADGM1004 has no internal impedance to ground, and charges can develop on the switch terminals leading to unreliable switch behavior To mitigate this behavior, provide a discharge path to all switch nodes. Figure 53 to Figure 56 show examples of cases to avoid where floating nodes can occur when using the switch. Conditions to avoid include the following:

- Leaving the RFx pins open circuit (see Figure 53).
- Connecting a series capacitor directly to the switch (see Figure 54).
- Connecting the RFx pin of two switches together directly or connecting the RFC pin to the RFx pin (see Figure 55 and Figure 56).

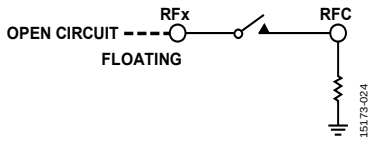


Figure 53. RFx Pins Left Open Circuit

Figure 54. Series Capacitor Directly Connected to MEMS Switch

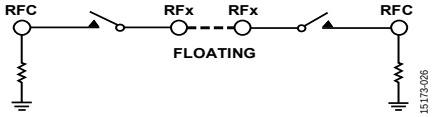


Figure 55. RFx Pins of Two MEMS Switches Directly Connected

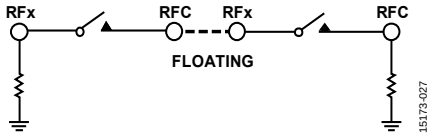


Figure 56. RFC Connected to RFx

Provide a discharge path to the switch nodes to avoid floating nodes. In a typical application, a 50 Ω termination connected to the switch provides this path. Driving switch nodes with a device of adequate impedance (<10 MΩ) provides a discharge path. If there is no discharge path in the application circuit, add a 10 MΩ shunt resistor or inductor on the source RFx pin of the MEMS switch to provide the discharge path. Note that the shunt resistors introduce leakage. Figure 57 shows an example of a configuration providing a discharge path.

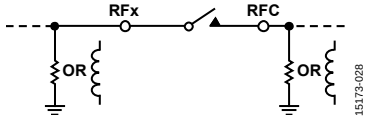


Figure 57. Switch Configuration Providing a Discharge Path

Figure 58 and Figure 59 illustrate typical cascaded switch use cases and the corresponding schemes to mitigate floating node risks.

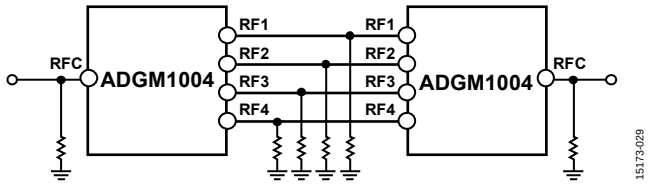


Figure 58. Two ADGM1004 Devices Connected in Path Selection Configuration with 10 MΩ Shunt Resistors to Mitigate Floating Nodes

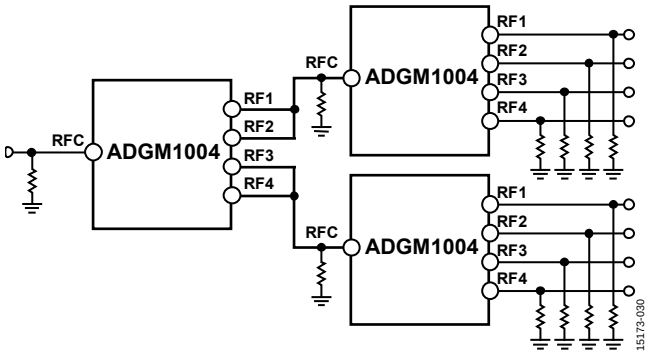


Figure 59. Three ADGM1004 Devices Connected in Fanout Configuration with 10 MΩ Shunt Resistors to Mitigate Floating Nodes

Avoid connecting shunt capacitors directly to the switch. A capacitor can store a charge and potentially lead to hot switching events when the switch opens or closes if there are no alternative discharge paths. These events affect the cycle lifetime of the switch.

CUMULATIVE ON SWITCH LIFETIME

Leaving the switch in an on state for a long period affects the lifetime of the switch because of mechanical degradation effects. These effects can result in the switch failing to turn off. Figure 60 shows a failure rate at 50°C where the mean time to failure is 7.2 years (2628 days), resulting in 50% of the sample lot failing at this point.

Temperatures above 50°C further reduce the switch lifetime. The cumulative on switch lifetime specification is also duty cycle dependent. If the user operates the MEMS switch with a duty cycle of less than 50% the lifetime of the MEMS switch improves.

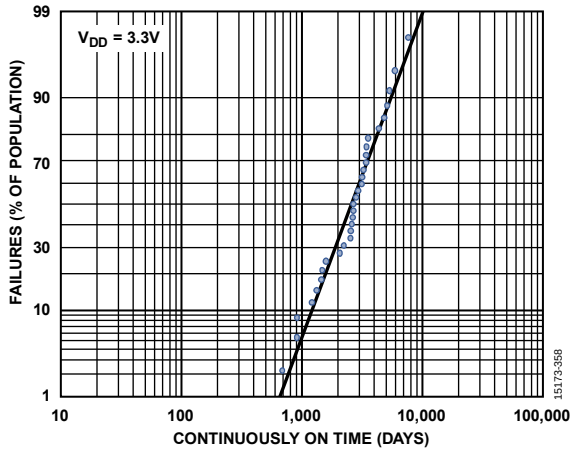


Figure 60. Cumulative On Switch Lifetime at 50°C, V_{DD} = 3.3 V, Sample Size 31 Parts

HANDLING PRECAUTIONS

Electrical Overstress (EOS) Precautions

The ADGM1004 is susceptible to EOS. Therefore, take the following precautions:

- The ADGM1004 is an ESD sensitive device. Ensure to take all of the normal handling precautions, including working only on static dissipative surfaces, wearing wrist straps or other ESD control devices, and storing unused devices in conductive foam.
- Avoid running measurement instruments, such as digital multimeters (DMMs), in autorange modes. Some instruments generate large transient compliance voltages when switching between ranges.
- Use the highest practical DMM range setting (the lowest resolution) for resistance measurements to minimize compliance voltages, particularly during switching.
- Discharge coaxial cables before connecting directly to the switch. Note that coaxial cables can store charge and lead to EOS when directly connected to the switch.
- Avoid connecting large capacitive terminations directly to the switch, as shown in Figure 61. A shunt capacitor can store a charge that potentially leads to hot switching events when the switch opens or closes, affecting the lifetime of the switch.

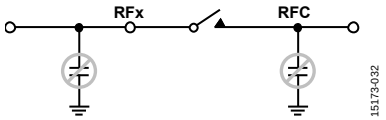


Figure 61. Avoid Having a Large Capacitor Directly Connected to the MEMS Switch

Mechanical Shock Precautions

The ADGM1004 passes extensive mechanical shock qualification tests, as described in Table 8. These tests validate the robustness of the device when exposed to normal mechanical shocks.

Table 8. Mechanical Qualification Summary

Parameter	Qualification
Mechanical Shock	Powered (PMS) IEC 60068-2-27
Random Drop	AEC-Q100 Test G5, five drops from 0.6 m
Vibration Testing	MIL-STD-883, M2007.3, Condition B, 20 Hz to 2000 Hz at 50 g
Group D, Sub 4, MIL-STD-883, M5005	Mechanical shock, 1500 g, 0.5 ms; vibration 50 g sine sweep, 20 Hz to 2000 Hz; acceleration 30,000 g

Do not use the ADGM1004 if dropped. Ensure minimal mechanical shocks during the handling and manufacturing of the device.

Figure 62 shows examples of loose device handling situations to avoid for risk of mechanical shock and ESD events.

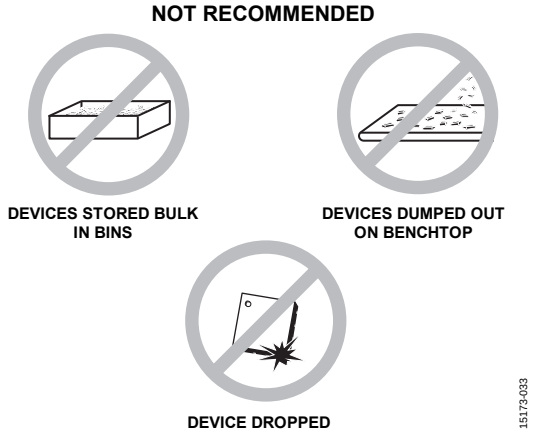


Figure 62. Situations to Avoid During Handling

REGISTER DETAILS

SWITCH DATA REGISTER

Address: 0x20, Reset: 0x00, Name: SWITCH_DATA

The switch data register controls the status of the four ADGM1004 switches.

Table 9. Bit Descriptions for SWITCH_DATA

Bits	Bit Name	Description	Reset	Access
[7:6]	INTERNAL_ERROR	Internal Error Detection. These bits determine if an internal error has occurred. 00: no error detected. 01: error detected. 10: error detected. 11: error detected.	0x0	R
[5:4]	RESERVED	Reserved. These bits are reserved. Set these bits to 0.	0x0	R
3	SW4_EN	Enable for Switch 4. 0: Switch 4 open. 1: Switch 4 closed.	0x0	R/W
2	SW3_EN	Enable for Switch 3. 0: Switch 3 open. 1: Switch 3 closed.	0x0	R/W
1	SW2_EN	Enable for Switch 2. 0: 00: Switch 2 open. 1: Switch 2 closed.	0x0	R/W
0	SW1_EN	Enable for Switch 1. 0: Switch 1 open. 1: Switch 1 closed.	0x0	R/W

OUTLINE DIMENSIONS

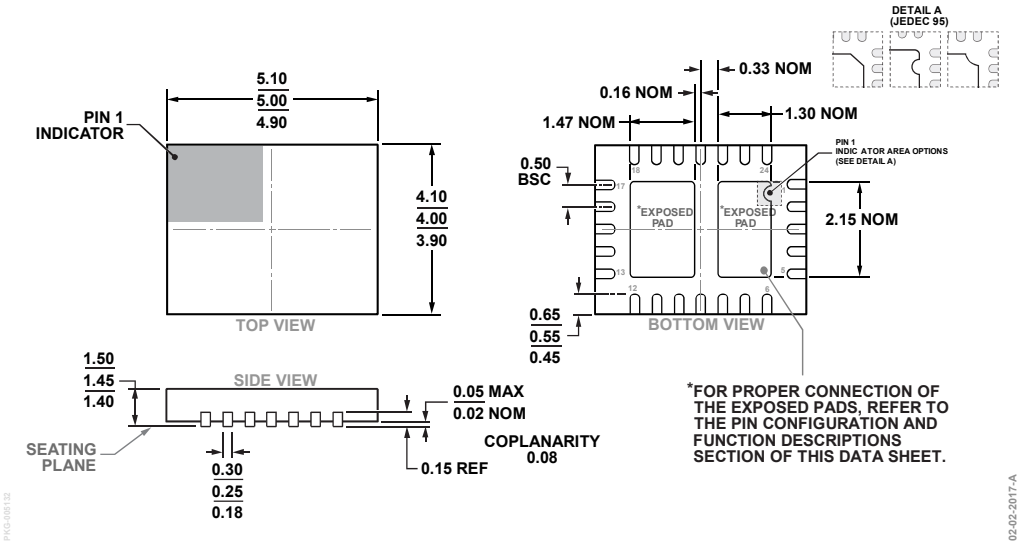


Figure 63. 24-Lead Lead Frame Chip Scale Package [LFCSP]
5 mm × 4 mm Body, and 1.45 mm Package Height
(CP-24-4)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADGM1004JCPZ-R2	0°C to 85°C	24-Lead Lead Frame Chip Scale Package [LFCSP]	CP-24-4
ADGM1004JCPZ-RL7	0°C to 85°C	24-Lead Lead Frame Chip Scale Package [LFCSP]	CP-24-4
EVAL-ADGM1004SDZ		Evaluation Board	

[1] Z = RoHS Compliant Part.

D15173-0-11/19(D)