MOTOROLA

Semiconductor Products Sector

MMC2001

Product Brief

MMC2001 M•CORE™ Integrated Microcontroller

The MMC2001 microcontroller is the first member of the M•CORE family of single-chip control systems. The M•CORE architecture is targeted for high-performance and cost-sensitive embedded control applications, with particular emphasis on reduced system power consumption, making the MMC2001 suitable for battery-operated products.

The MMC2001 incorporates the following functional units:

- M•CORE Integer Processor
  - 32-bit RISC architecture, 16-bit instructions
  - Low power, high performance
- OnCE™ Debug Module
- On-chip SRAM, 32 kbytes with battery backup supply support
- On-Chip ROM, 256 kbytes
- Interrupt Controller with support for up to 32 Interrupt sources
- External Interface Module
  - External interface with 20 address lines and 16 data lines
  - Chip select and wait state generation
  - Bus watchdog timer
- Timer/Reset Module
  - Crystal oscillator generates on-chip clock signal from a 32.768 kHz crystal
  - Time-of-day timer provides real-time event information
  - Watchdog timer resets the chip to recover from system failure
  - Reset unit provides low voltage detection and backup power switching
  - Periodic interrupt timer
- Serial Communication Port (UART)
  - Two independent UART channels
  - Asynchronous Operation
  - Baud Rate Generation
- 16-bit General Purpose I/O Port with support for Keyboard Scan / Encode
- 8-bit General Purpose I/O Port with support for Edge/ Level sensitive external interrupts
- Pulse Width Modulation Module
  - Six independent PWM channels
  - Pins can also be configured for general purpose I/O
- Serial Peripheral Interface (ISPI)
  - Interval-mode SPI operation
  - Efficient communication with slower serial peripherals
  - Designed for master/slave SPI operation
- DC to 33 MHz Operation
- Low Voltage — 1.8 to 3.6 Volt operation with separate input/output and core supplies

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Figure 1 is a block diagram of the MMC2001 microcontroller. The paragraphs that follow describe the functional components of the integrated control system.

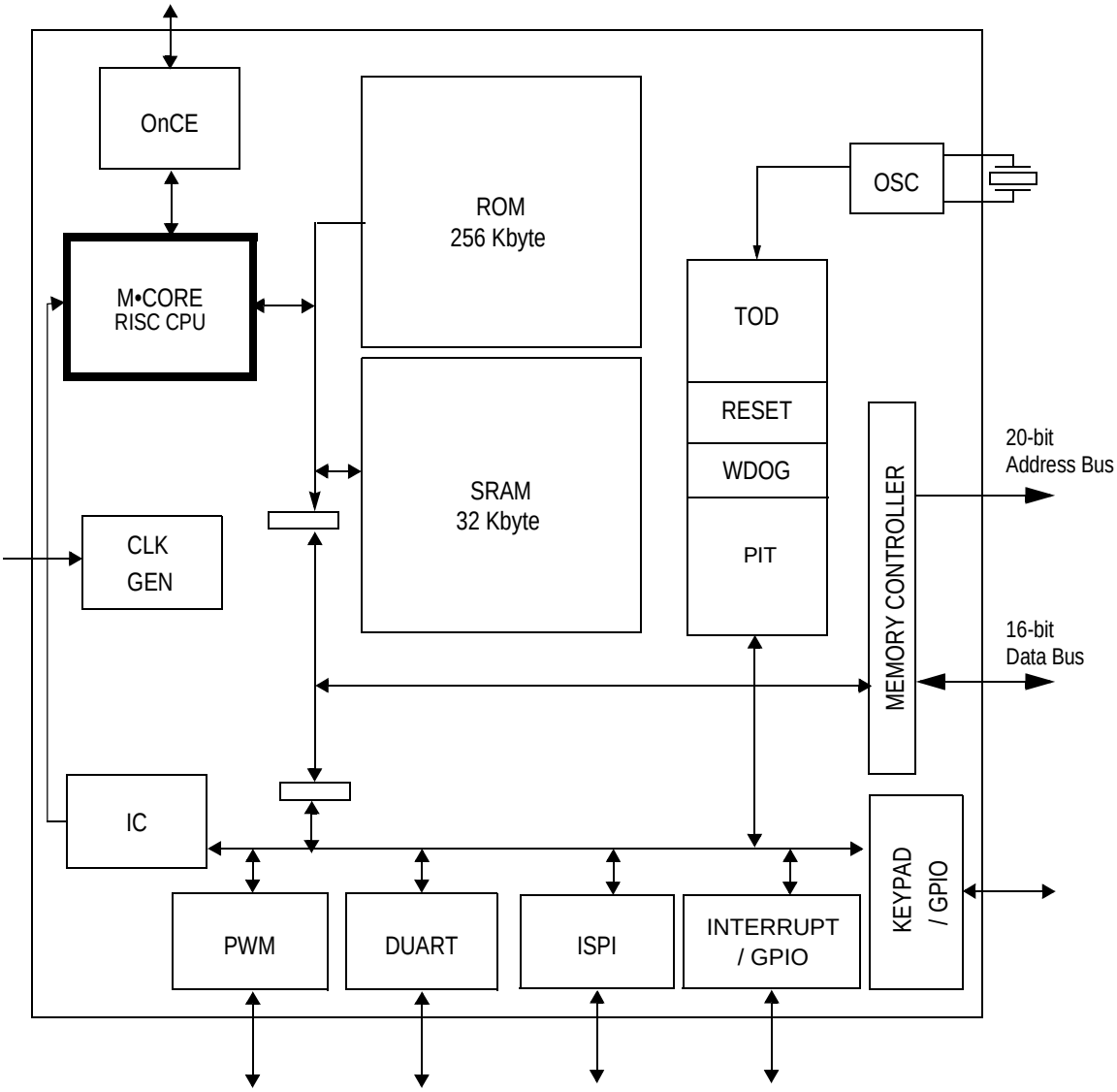


Figure 1. MMC2001 Block Diagram

M•CORE PROCESSOR CORE

The 32-bit M•CORE microRISC Engine is the first of a new line of Motorola microprocessor products designed expressly for embedded control applications. M•CORE is a streamlined execution engine that uses many of the same performance enhancements as mainstream RISC computer designs to minimize system complexity and overhead. A 16-bit instruction encoding is used to lower memory bandwidth and sustain a high rate of instruction execution.

The M•CORE processor utilizes a four-stage pipeline for instruction execution. The Instruction Fetch, Instruction Decode/Register File Read, Execute, and Register File Writeback stages operate in an overlapped fashion, allowing single clock instruction execution for most instructions.

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Sixteen general purpose registers are provided for source operands and instruction results. Register R15 is used as the Link Register to hold the return address for subroutine calls and Register R0 is used as the current Stack Pointer by convention.

The execution unit consists of a 32-bit Arithmetic/Logic Unit (ALU), a 32-bit Barrel Shifter (Shifter), Find-First-One unit (FFO), Result Feed-Forward hardware, and miscellaneous support hardware for multiplication, division, and multiple register load and stores. Arithmetic and Logical operations are executed in a single cycle with the exception of multiply and divide. Multiply is implemented with a 2-bit per clock, overlapped-scan, modified Booth algorithm with early-out capability to reduce execution time for operations with small multipliers. Divide is implemented with a 1-bit per clock early-in algorithm. The Find-First-One unit operates in a single clock cycle.

The Program Counter Unit has a PC incrementer and a dedicated Branch Address Adder to minimize delays during change of flow operations. Branch target addresses are calculated in parallel with branch instruction decode, with a single pipeline bubble for taken branches and jumps, resulting in an execution time of two clocks. Conditional Branches which are not taken execute in a single clock.

Memory load and store operations are provided for byte, halfword and word (32-bit) data with automatic zero extension of byte and halfword load data. These instructions can execute in two clock cycles. Load and store multiple register instructions allow low overhead context save and restore operations; these instructions can execute in (N+1) clock cycles, where N is the number of registers to transfer.

A single Condition/Code Carry (C) bit is provided for condition testing and for use in implementing arithmetic and logical operations greater than 32-bits. Typically, the C bit is set only by explicit test/comparison operations, not as a side-effect of normal instruction operation. Exceptions to this rule occur for specialized operations where it is desirable to combine condition setting with actual computation.

A 16-entry Alternate register file is provided to support low overhead interrupt exception processing, and both vectored and autovectored interrupts are supported by the CPU.

DEBUG INTERFACE

The M•CORE architecture includes on-chip emulation (OnCE) circuitry. A JTAG interface provides the means of interacting with the M•CORE processor and on-chip peripherals. A user can examine processor and on-chip peripheral registers, memory, and instruction execution to facilitate hardware/software development. Debug status and control registers are accessible during OnCE operation. Special circuitry and interface pins are provided to support non-intrusive debug and efficient use of on-chip resources.

INTERNAL STANDBY RAM

The 32 kbyte on-chip SRAM supports single-clock access by the M•CORE processor. SRAM supports byte, half-word and word accesses. The RAM array is divided into two separate blocks that can be independently activated in order to conserve power.

ON-CHIP ROM

The 256-kbyte ROM is pre-programmed with development support code, including.

- Floating Point Routines
  - M•CORE ABI compliant routines to implement floating-point computation
- MBUG™ Motorola Monitor Debugger program with the following features:

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- Assembly and disassembly of M•CORE instructions for modification and display of code
- Single-step trace and continued execution from a specified address
- Modification, display, and movement of system memory
- Setting, displaying, and removing breakpoints
- Extensive on-line help
- Ability to execute user-assembled and/or downloaded software in a controlled environment
- Automatic decompression of compressed S-record files while downloading
- Logging function for generating a transcript of a debugging session

EXTERNAL INTERFACE MODULE

The EIM provides 20 address lines and 16 data lines. It supports aligned byte, halfword, and word transfers via 8-bit and 16-bit ports. The upper or lower byte of the data bus can be used for 8-bit transfers. The EIM incorporates four chip-select circuits for external devices. Each chip select has a match address range of 16 mbytes, programmable wait state, selectable protection, and programmable data port size. Each unused chip-select pin can be programmed four use as a general-purpose output. The EIM also includes the logic for external/internal Boot ROM select and a bus watchdog for all internal and external bus cycles. Show cycles are available for external visibility of internal bus cycles.

CLOCK GENERATION MODULE

This module controls system clock signals and implements low-power operation. There are two system clock signals. The HI_REFCLK signal for the processor is provided via an external clock input pin (CLKIN). The LOW_REFCLK signal is driven by an external crystal oscillator connected to the VOSC, XOSX, and EXOSC pins. On-chip peripherals can use LOW_REFCLK, HI_REFCLK, a prescaled LOW_REFCLK, or a combination of these, but must be properly synchronized when different clock sources are used. On-chip peripherals can be shut down independently of the processor. The CLKOUT pin can be driven by either HI_REFCLK or LOW_REFCLK, or it can be de-activated.

There are four operating modes: RUN, WAIT, DOZE, STOP. Different output encodings on the LMPD pins inform external devices which mode is in use. RUN mode is for normal full operation, with all system clocks operating. The remaining modes are for power conservation; each has an associated CPU instruction.

All low power modes halt the CPU, which then must be awakened by an interrupt request or a reset. The TOD timer is unaffected by any low-power mode. In WAIT mode, only the CPU is halted, and it can be wakened by any interrupt request. Individual on-chip peripherals are pre-programmed for DOZE operation; some shut down, while some remain active. Peripherals that remain active can generate interrupt requests and wake up the CPU. In STOP mode, most system clocks are halted, but the programmable interrupt and watchdog timers can be used to wake up the system (both can also be stopped). Most on-chip peripherals retain control register values during STOP mode, but peripheral operations must be properly terminated before STOP in order to assure orderly re-activation when normal mode operation resumes.

TIMER/RESET MODULE

The Timer/Reset module contains four timer sub-modules and the device reset control logic. The reset logic provides reset source status and controls the CLKOUT pin. There are four possible sources of system reset (Low-voltage monitor signal, external reset signal, power-on, and watchdog); there is a status bit for each of the reset sources. The CLKOUT signal is disabled during reset, to assure proper synchronization of external devices that use it as a clock reference. It must be re-enabled as a part of system initialization.

Timer functions include:

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- Time-of-Day with Alarm (TOD)
  - Free-running, clocked at LOW_REFCLK/128.
  - Two 32-bit registers count seconds and fractions (1/256) of seconds
  - Unaffected by low power modes
  - Alarm interrupt can be used to exit from any low power state
- Periodic Interrupt Timer (PIT)
  - Clocked at LOW_REFCLK/4
  - Count down from modulus latch value (set-and-forget) or free-running
  - Polled or interrupt-driven operation
- Watch-Dog Timer (WD)
  - Clocked at LOW_REFCLK/16384
  - Time-out period determined by 6-bit count value
  - Count register re-loaded by each service sequence

INTERRUPT CONTROLLER MODULE

The IC module performs interrupt masking and priority support. Absolute priority of interrupt service requests is determined by the processor. The IC manages requests from multiple sources and provides an interface to the processor. It can manage up to 32 interrupt sources, indicates pending interrupt requests, enables/disables interrupt sources, and determines whether an interrupt is a normal or fast mode interrupt (fast mode interrupts always have priority). The IC also provides a mechanism for software to schedule interrupt requests.

DUAL UART MODULE

This module provides two independent and nearly identical (UART0 includes modem RTS and CTS support, while UART1 does not) serial communications interfaces. Both UARTs support standard serial communications at normal baud rates and are also compatible with the HPSIR/IrDA Physical Communication Protocol. Each UART contains independent receivers and transmitters clocked by an independent clock generator. The generator can be clocked by system clock HI_REFCLK or by an external clock source on the $\overline{\text{DTR}}$ pin. A 12-bit programmable prescaler is used to generate the baud clock.

The UARTs support full duplex, auto-echo loopback, local loopback, and remote loopback modes. Data formats are 5, 6, 7, or 8 bits with even, odd, or no parity, and up to 2 stop bits. Four-byte receive buffers and two-byte transmit buffers minimize CPU service overhead. The module also provides error-detection and maskable-interrupt capabilities. Each UART can generate an interrupt service request when operational or error-condition events occur. Interrupts support wake up from low power modes.

INTERVAL MODE SERIAL PERIPHERAL INTERFACE

The ISPI supports a standard, multimaster serial peripheral interface bus, including interrupt-driven operation, and also supports transfers at programmable intervals to implement timed-event protocols.

The ISPI has three operating modes:

- Manual Mode -- typical SPI Master mode operation
- Interval Mode -- Manual Mode plus the ability to exchange data at programmed periodic intervals.
- Slave Mode -- typical SPI Slave mode operation

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EXTERNAL INTERRUPT/GPIO MODULE

This module, also called the Edge Port, controls eight external interrupt request pins. Each pin is configurable for level-sensitive or edge (rising, falling, or both) detection. To enable external interrupts, this module must be configured to recognize the appropriate interrupt request signal, and the Interrupt Control Module must be configured to enable the interrupt request to the processor. The eight pins can also be configured for use as general-purpose I/O pins.

KEYPAD/GPIO MODULE

The Keypad module provides keypad matrix scanning functions. The module controls 16 pins, and can perform row and column monitoring functions for any keypad configuration up to eight rows by eight columns. Polled and interrupt-driven operation are supported, and there are interrupt request signals for both key depress and key release. If fewer than 64 keys are used, unused pins can be individually configured for use as general-purpose I/O. Pins [7:0] have internal pullups enabled when configured as inputs. Pins [15:8] can be configured as open drain outputs, but normally have totem-pole style output drive. Pins [7:0] are always totem-pole driven when configured as outputs.

PULSE WIDTH MODULATOR MODULE

The PWM module contains six identical PWM output channels. Each channel consists of a free-running counter, a period-compare register, a width-compare register, and an associated pin. Width and period registers are double buffered to allow for next cycle loading. All channels share a single pre-scaler that divides HI_REFCLK by eight predetermined values in the range 4 to 65536, but each channel can independently select a pre-scaler tap point. Each channel can make an independent maskable interrupt service request. Any unused pin can be used for general-purpose I/O. Channels can be configured as periodic interrupt sources, and the associated pin can be used for general-purpose I/O at the same time.

DEVICE AVAILABILITY

Packages and operating frequencies currently available for the MMC2001.

Package	Frequency
Plastic Low-Profile Quad Flat Pack 144 lead	33 MHz

TECHNICAL DOCUMENTATION

Detailed technical information is available from Motorola literature distribution centers.

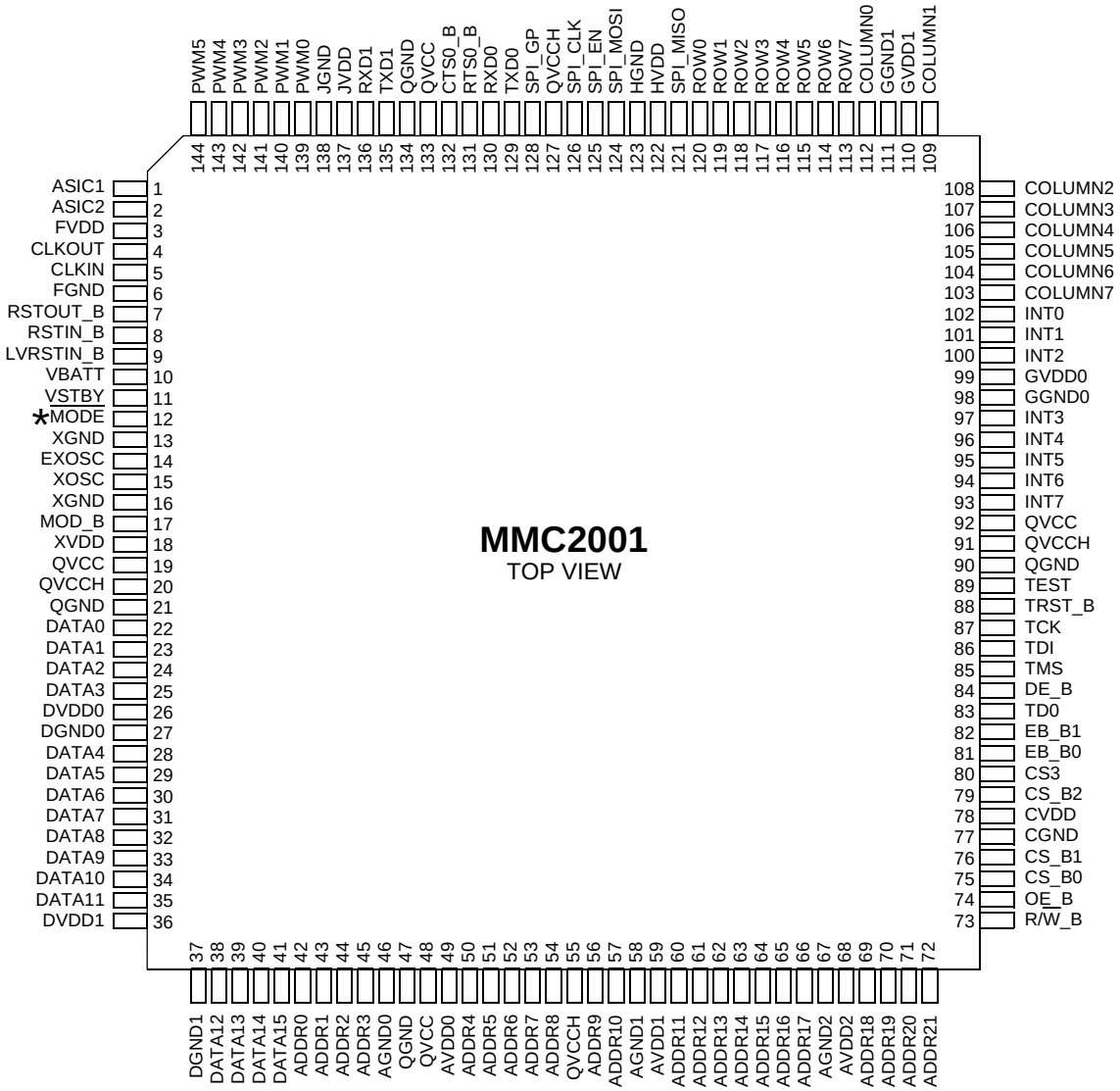
Document Number	Document Title	Availability
MMC2001RM/D	MMC2001 Reference Manual	2Q98
MCORERM/AD	M•CORE Programmer's Reference Manual	now

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MMC2001 PINOUT

Figure 2 is the pinout for an MMC2001 device in a 144-pin Plastic Low-Profile Quad Flat Pack (LQFP).



*Pin 12 ($\overline{\text{MODE}}$) must be grounded for proper operation but is NOT a system ground.

DEVELOPMENT TOOLS

A complete suite of compilers and debuggers for the MMC2001 is available from third-party developers, as shown below. Any development tool that generates code for the Motorola M•CORE Processor can do the same for the MMC2001 processor.

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Company Name	Company Phone Number	Availability
Compilers/Debuggers		
Cosmic	www.std.com/cosmic	4Q98
Diab Data	650-571-1700	now
Metrowerks	512-873-4740	4Q98
Motorola GNU	www.motorola.com/mcore	now
Software Development Systems	630-368-0400	now
RTOS		
Embedded System Products	281-561-9990	now
Integrated Systems	408-542-1781	now
Microware	515-327-2337	4Q98
Microtec	408-487-7336	now
Motorola RTEK	800-262-5486	now
Wind River Systems	510-748-4100	4Q98
Instruction Set Simulators		
Software Development Systems	630-368-0400	now
Software/Hardware Verification		
Summit	512-343-3686	now
Mentor Graphics	503-685-1575	3Q98
ViewLogic/Eagle Design	503-520-2328	now
Logic Analyzers		
Hewlett-Packard (Processor Probe)	719-590-2558	now
Tektronix (Logic Analyzer)	503-627-6836	now
Development Boards		
MMCEVB1200	800-521-6274	2Q98
MMCEVD1200	800-521-6274	2Q98
Axiom CMB2001	www.axman.com	2Q98

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