

FEATURES

- ESD Protection for RS-232 Bus Pins
 - ± 15 -kV Human-Body Model (HBM)
 - ± 8 -kV IEC 61000-4-2, Contact Discharge
 - ± 15 -kV IEC 61000-4-2, Air-Gap Discharge
- Meets or Exceeds the Requirements of TIA/EIA-232-F and ITU v.28 Standards
- Operates With 3-V to 5.5-V V_{CC} Supply
- Operates up to 1000 kbit/s
- Two Drivers and Two Receivers
- Low Standby Current . . . 1 μ A Typ
- External Capacitors . . . $4 \times 0.1 \mu$ F
- Accepts 5-V Logic Input With 3.3-V Supply

APPLICATIONS

- Battery-Powered Systems
- PDAs
- Notebooks
- Laptops
- Palmtop PCs
- Hand-Held Equipment

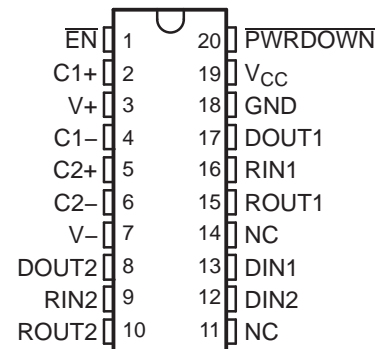
DESCRIPTION/ ORDERING INFORMATION

The TRSF3222E consists of two line drivers, two line receivers, and a dual charge-pump circuit with ± 15 -kV ESD protection pin to pin (serial-port connection pins, including GND).

The TRSF3222E meets the requirements of TIA/EIA-232-F and provides the electrical interface between an asynchronous communication controller and the serial-port connector. The charge pump and four small external capacitors allow operation from a single 3-V to 5.5-V supply. The TRSF3222E operates at typical data signaling rates up to 1000 kbit/s and is an improved drop-in replacement for industry-popular '3222 two-driver, two-receiver functions.

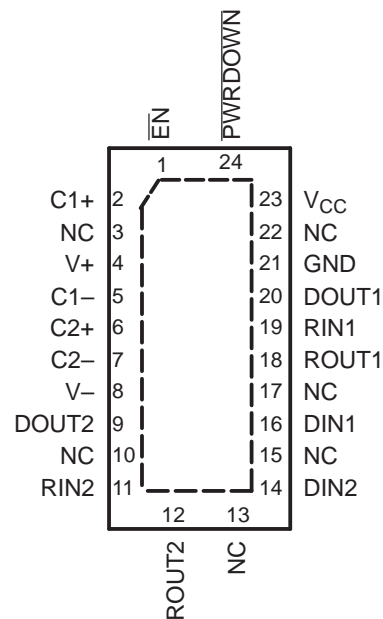
The TRSF3222E can be placed in the power-down mode by setting the power-down ($\overline{\text{PWRDOWN}}$) input low, which draws only 1 μ A from the power supply. When the device is powered down, the receivers remain active while the drivers are placed in the high-impedance state. Also, during power down, the onboard charge pump is disabled; $V+$ is lowered to V_{CC} , and $V-$ is raised toward GND. Receiver outputs also can be placed in the high-impedance state by setting enable ($\overline{\text{EN}}$) high.

DB, DW, OR PW PACKAGE
(TOP VIEW)



NC – No internal connection

RHL PACKAGE
(TOP VIEW)



NC – No internal connection



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

TRSF3222E
3-V TO 5.5-V MULTICHANNEL RS-232 LINE DRIVER/RECEIVER
WITH ±15-kV ESD PROTECTION

SLLS823–JULY 2007

ORDERING INFORMATION

T _A	PACKAGE ⁽¹⁾⁽²⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	SOIC – DW	Tube of 25	TRSF3222ECDW	TRSF3222EC
		Reel of 2000	TRSF3222ECDWR	
	SSOP – DB	Tube of 70	TRSF3222ECDB	RT22EC
		Reel of 2000	TRSF3222ECDBR	
	TSSOP – PW	Tube of 70	TRSF3222ECPW	RT22EC
		Reel of 2000	TRSF3222ECPWR	
–40°C to 85°C	SOIC – DW	Tube of 25	TRSF3222EIDW	TRSF3222EI
		Reel of 2000	TRSF3222EIDWR	
	SSOP – DB	Tube of 70	TRSF3222EIDB	RT22EI
		Reel of 2000	TRSF3222EIDBR	
	TSSOP – PW	Tube of 70	TRSF3222EIPW	RT22EI
		Reel of 2000	TRSF3222EIPWR	

- (1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.
- (2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

FUNCTION TABLES

Each Driver⁽¹⁾

INPUTS		OUTPUT DOUT
DIN	PWRDOWN	
X	L	Z
L	H	H
H	H	L

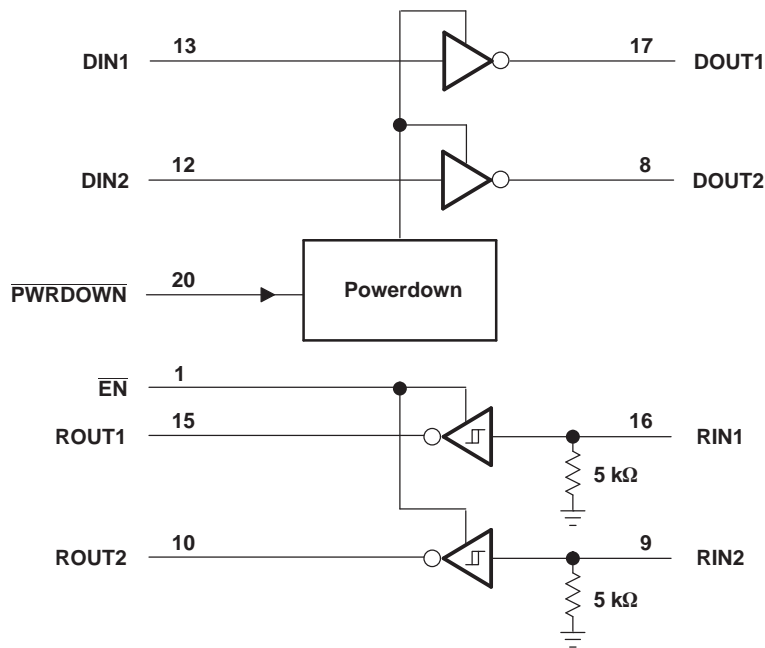
- (1) H = high level, L = low level, X = irrelevant, Z = high impedance

Each Receiver⁽¹⁾

INPUTS		OUTPUT ROUT
RIN	$\overline{\text{EN}}$	
L	L	H
H	L	L
X	H	Z
Open	L	H

- (1) H = high level, L = low level, X = irrelevant,
Z = high impedance (off),
Open = input disconnected or connected driver off

LOGIC DIAGRAM (POSITIVE LOGIC)⁽¹⁾



(1) Pin numbers shown are for the DB, DW, and PW packages.

Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{CC}	Supply voltage range ⁽²⁾	-0.3	6	V
V+	Positive-output supply voltage range ⁽²⁾	-0.3	7	V
V-	Negative-output supply voltage range ⁽²⁾	0.3	-7	V
V+ - V-	Supply voltage difference ⁽²⁾		13	V
V_I	Input voltage range	Driver (EN, PWRDOWN)		V
V_O	Output voltage range	Driver		V
θ_{JA}	Package thermal impedance ⁽³⁾⁽⁴⁾	DB package		°C/W
		DW package		
		PW package		
		RHL package		
T_J	Operating virtual junction temperature		150	°C
T_{stg}	Storage temperature range	-65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages are with respect to network GND.
- (3) Maximum power dissipation is a function of $T_J(\max)$, θ_{JA} , and T_A . The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(\max) - T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
- (4) The package thermal impedance is calculated in accordance with JESD 51-7.

TRSF3222E
3-V TO 5.5-V MULTICHANNEL RS-232 LINE DRIVER/RECEIVER
WITH ± 15 -kV ESD PROTECTION

SLLS823–JULY 2007

Recommended Operating Conditions⁽¹⁾

See [Figure 5](#)

			MIN	NOM	MAX	UNIT
Supply voltage		$V_{CC} = 3.3\text{ V}$	3	3.3	3.6	V
		$V_{CC} = 5\text{ V}$	4.5	5	5.5	
V_{IH}	Driver and control high-level input voltage	DIN, \overline{EN} , $\overline{PWRDOWN}$	$V_{CC} = 3.3\text{ V}$	2		V
			$V_{CC} = 5\text{ V}$	2.4		
V_{IL}	Driver and control low-level input voltage	DIN, \overline{EN} , $\overline{PWRDOWN}$			0.8	V
V_I	Driver and control input voltage	DIN, \overline{EN} , $\overline{PWRDOWN}$	0		5.5	V
V_I	Receiver input voltage		-25		25	V
T_A	Operating free-air temperature	TRSF3222EC	0		70	°C
		TRSF3222EI	-40		85	

(1) Test conditions are C1–C4 = 0.1 μF at $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$; C1 = 0.047 μF , C2–C4 = 0.33 μF at $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$.

Electrical Characteristics⁽¹⁾

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [Figure 5](#))

PARAMETER		TEST CONDITIONS	MIN	TYP ⁽²⁾	MAX	UNIT
I_I	Input leakage current (\overline{EN} , $\overline{PWRDOWN}$)			± 0.01	± 1	μA
I_{CC}	Supply current	No load, $\overline{PWRDOWN}$ at V_{CC}		0.3	1	mA
	Supply current (powered off)	No load, $\overline{PWRDOWN}$ at GND		1	10	μA

(1) Test conditions are C1–C4 = 0.1 μF at $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$; C1 = 0.047 μF , C2–C4 = 0.33 μF at $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$.

(2) All typical values are at $V_{CC} = 3.3\text{ V}$ or $V_{CC} = 5\text{ V}$, and $T_A = 25^\circ\text{C}$.

DRIVER SECTION

Electrical Characteristics⁽¹⁾

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [Figure 5](#))

PARAMETER		TEST CONDITIONS		MIN	TYP ⁽²⁾	MAX	UNIT
V _{OH}	High-level output voltage	DOUT at R _L = 3 k Ω to GND, DIN = GND		5	5.4		V
V _{OL}	Low-level output voltage	DOUT at R _L = 3 k Ω to GND, DIN = V _{CC}		-5	-5.4		V
I _{IH}	High-level input current	V _I = V _{CC}			± 0.01	± 1	μ A
I _{IL}	Low-level input current	V _I at GND			± 0.01	± 1	μ A
I _{OS}	Short-circuit output current ⁽³⁾	V _{CC} = 3.6 V	V _O = 0 V		± 35	± 60	mA
		V _{CC} = 5.5 V					
r _o	Output resistance	V _{CC} , V+, and V- = 0 V, V _O = ± 2 V		300	10M		Ω
I _{OZ}	Output leakage current	$\overline{\text{PWRDOWN}}$ = GND	V _{CC} = 3 V to 3.6 V, V _O = ± 12 V			± 25	μ A
			V _{CC} = 4.5 V to 5.5 V, V _O = ± 10 V			± 25	

(1) Test conditions are C1–C4 = 0.1 μ F at V_{CC} = 3.3 V \pm 0.3 V; C1 = 0.047 μ F, C2–C4 = 0.33 μ F at V_{CC} = 5 V \pm 0.5 V.

(2) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

(3) Short-circuit durations should be controlled to prevent exceeding the device absolute power dissipation ratings, and not more than one output should be shorted at a time.

Switching Characteristics⁽¹⁾

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [Figure 5](#))

PARAMETER		TEST CONDITIONS		MIN	TYP ⁽²⁾	MAX	UNIT
Maximum data rate (See Figure 1)	R _L = 3 k Ω , One DOUT switching	C _L = 1000 pF			250		kbit/s
		C _L = 250 pF,	V _{CC} = 3 V to 4.5 V		1000		
		C _L = 1000 pF,	V _{CC} = 4.5 V to 5.5 V		1000		
t _{sk(p)}	Pulse skew ⁽³⁾	C _L = 150 pF to 2500 pF,	R _L = 3 k Ω to 7 k Ω , See Figure 2		300		ns
SR(tr)	Slew rate, transition region (see Figure 1)	R _L = 7 k Ω ,	C _L = 150 pF to 1000 pF		8	90	V/ μ s
			C _L = 1000 pF		12	60	
		R _L = 3 k Ω	C _L = 150 pF to 250 pF		24	150	

(1) Test conditions are C1–C4 = 0.1 μ F at V_{CC} = 3.3 V \pm 0.3 V; C1 = 0.047 μ F, C2–C4 = 0.33 μ F at V_{CC} = 5 V \pm 0.5 V.

(2) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

(3) Pulse skew is defined as |t_{PLH} - t_{PHL}| of each channel of the same device.

TRSF3222E

3-V TO 5.5-V MULTICHANNEL RS-232 LINE DRIVER/RECEIVER

WITH ± 15 -kV ESD PROTECTION

SLLS823–JULY 2007

RECEIVER SECTION

Electrical Characteristics⁽¹⁾

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [Figure 5](#))

PARAMETER		TEST CONDITIONS	MIN	TYP ⁽²⁾	MAX	UNIT
V _{OH}	High-level output voltage	I _{OH} = -1 mA	V _{CC} - 0.6	V _{CC} - 0.1		V
V _{OL}	Low-level output voltage	I _{OL} = 1.6 mA			0.4	V
V _{IT+}	Positive-going input threshold voltage	V _{CC} = 3.3 V		1.5	2.4	V
		V _{CC} = 5 V		1.8	2.4	
V _{IT-}	Negative-going input threshold voltage	V _{CC} = 3.3 V	0.6	1.2		V
		V _{CC} = 5 V	0.8	1.5		
V _{hys}	Input hysteresis (V _{IT+} - V _{IT-})			0.3		V
I _{OZ}	Output leakage current	$\overline{\text{EN}} = 1$		± 0.05	± 10	μA
r _i	Input resistance	V _I = ± 3 V to ± 25 V	3	5	7	k Ω

(1) Test conditions are C1–C4 = 0.1 μF at V_{CC} = 3.3 V \pm 0.3 V; C1 = 0.047 μF , C2–C4 = 0.33 μF at V_{CC} = 5 V \pm 0.5 V.

(2) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

Switching Characteristics⁽¹⁾

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

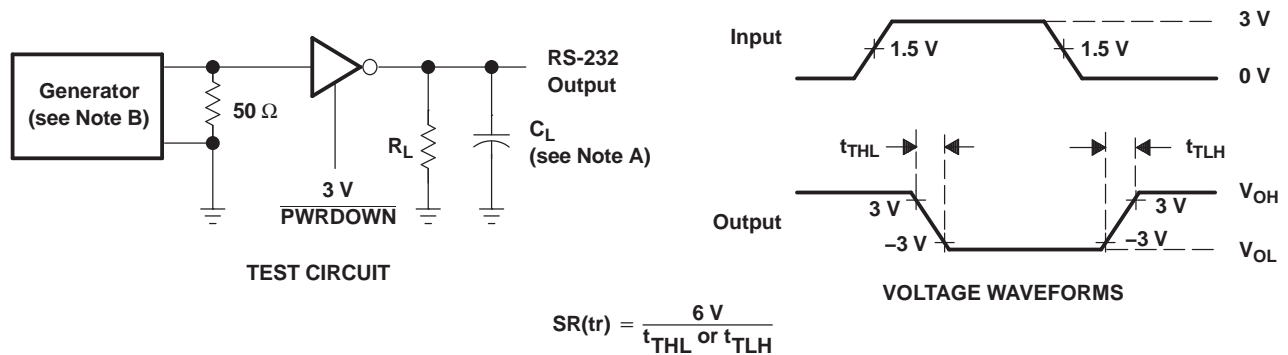
PARAMETER		TEST CONDITIONS	TYP ⁽²⁾	UNIT
t _{PLH}	Propagation delay time, low- to high-level output	C _L = 150 pF, See Figure 3	300	ns
t _{PHL}	Propagation delay time, high- to low-level output	C _L = 150 pF, See Figure 3	300	ns
t _{en}	Output enable time	C _L = 150 pF, R _L = 3 k Ω , See Figure 4	200	ns
t _{dis}	Output disable time	C _L = 150 pF, R _L = 3 k Ω , See Figure 4	200	ns
t _{sk(p)}	Pulse skew ⁽³⁾	See Figure 3	300	ns

(1) Test conditions are C1–C4 = 0.1 μF at V_{CC} = 3.3 V \pm 0.3 V; C1 = 0.047 μF , C2–C4 = 0.33 μF at V_{CC} = 5 V \pm 0.5 V.

(2) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

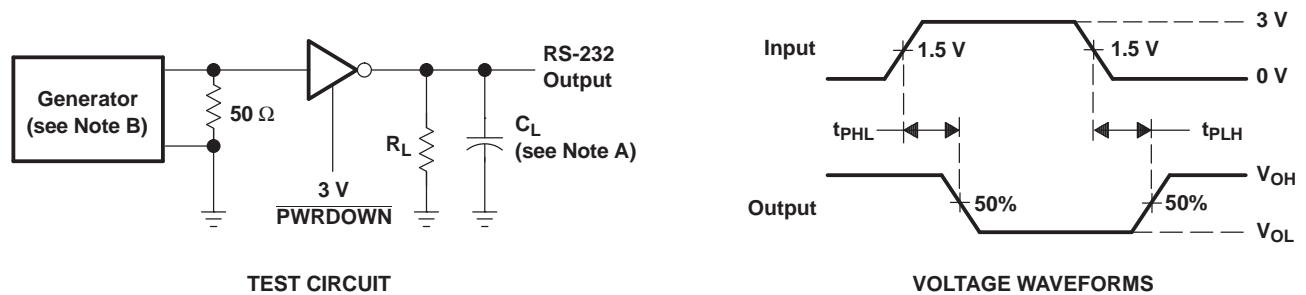
(3) Pulse skew is defined as |t_{PLH} - t_{PHL}| of each channel of the same device.

PARAMETER MEASUREMENT INFORMATION



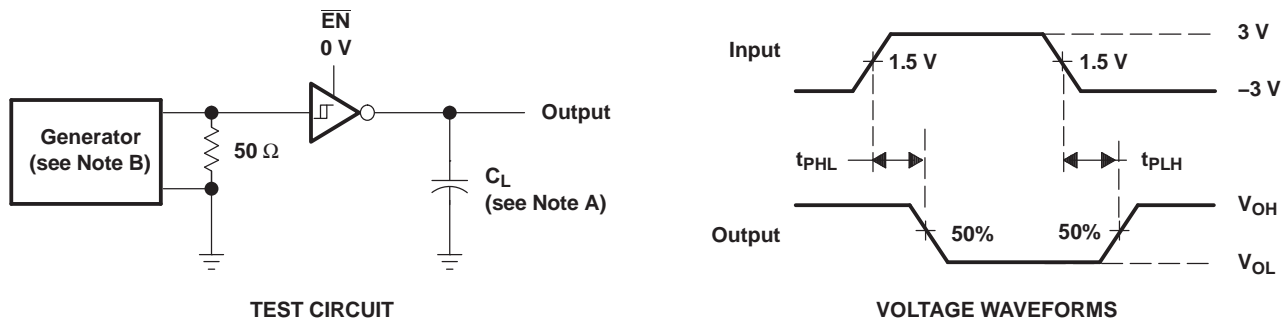
- A. C_L includes probe and jig capacitance.
- B. The pulse generator has the following characteristics: PRR = 250 kbit/s, $Z_O = 50\ \Omega$, 50% duty cycle, $t_r \leq 10\text{ ns}$, $t_f \leq 10\text{ ns}$.

Figure 1. Driver Slew Rate



- A. C_L includes probe and jig capacitance.
- B. The pulse generator has the following characteristics: PRR = 250 kbit/s, $Z_O = 50\ \Omega$, 50% duty cycle, $t_r \leq 10\text{ ns}$, $t_f \leq 10\text{ ns}$.

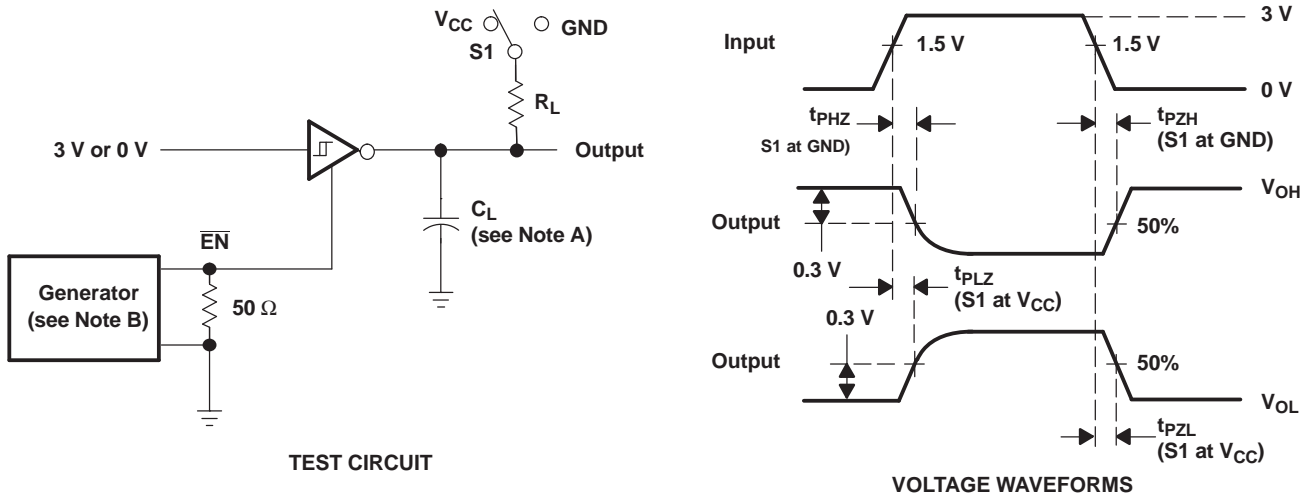
Figure 2. Driver Pulse Skew



- A. C_L includes probe and jig capacitance.
- B. The pulse generator has the following characteristics: $Z_O = 50\ \Omega$, 50% duty cycle, $t_r \leq 10\text{ ns}$, $t_f \leq 10\text{ ns}$.

Figure 3. Receiver Propagation Delay Times

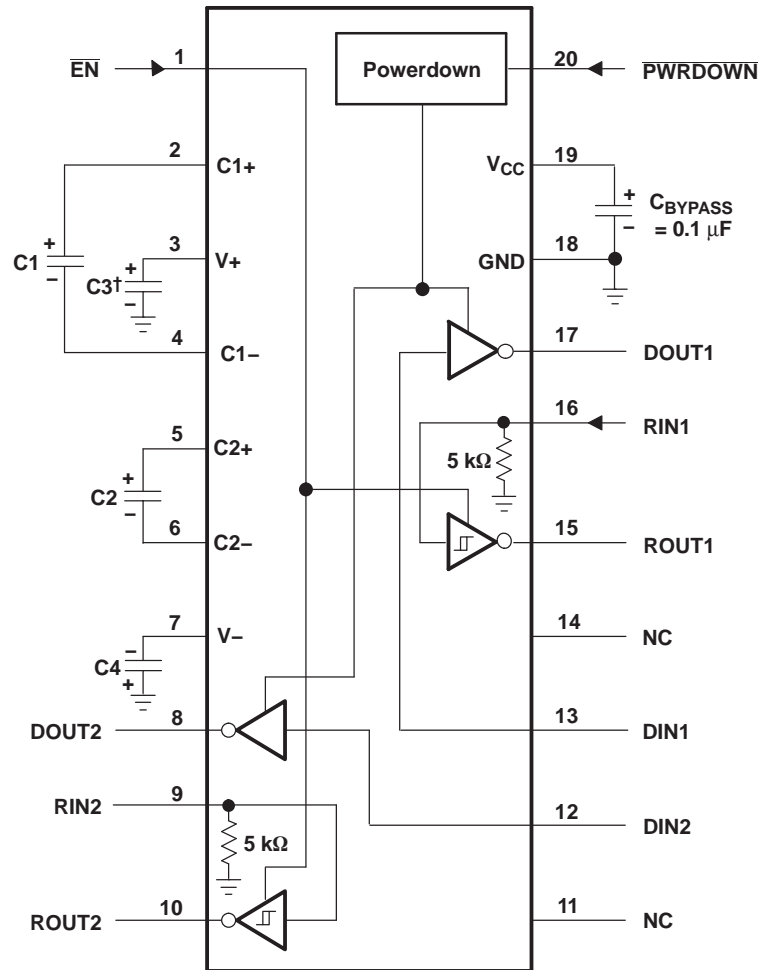
PARAMETER MEASUREMENT INFORMATION (continued)



- A. C_L includes probe and jig capacitance.
- B. The pulse generator has the following characteristics: $Z_O = 50 \Omega$, 50% duty cycle, $t_r \leq 10$ ns, $t_f \leq 10$ ns.

Figure 4. Receiver Enable and Disable Times

APPLICATION INFORMATION



† C3 can be connected to V_{CC} or GND.

NOTES: A. Resistor values shown are nominal.

B. NC – No internal connection

C. Nonpolarized ceramic capacitors are acceptable. If polarized tantalum or electrolytic capacitors are used, they should be connected as shown.

V_{CC} vs CAPACITOR VALUES

V_{CC}	C1	C2, C3, and C4
3.3 V \pm 0.3 V	0.1 μ F	0.1 μ F
5 V \pm 0.5 V	0.047 μ F	0.33 μ F
3 V to 5.5 V	0.1 μ F	0.47 μ F

Figure 5. Typical Operating Circuit and Capacitor Values

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TRSF3222ECDB	ACTIVE	SSOP	DB	20	70	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	RT22EC	Samples
TRSF3222ECDWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	TRSF3222EC	Samples
TRSF3222ECPWR	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	RT22EC	Samples
TRSF3222EIDWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TRSF3222EI	Samples
TRSF3222EIPW	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	RT22EI	Samples
TRSF3222EIPWG4	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	RT22EI	Samples
TRSF3222EIPWR	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	RT22EI	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=100ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TRSF3222ECDWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
TRSF3222ECPWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
TRSF3222EIDWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
TRSF3222EIPWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TRSF3222ECDWR	SOIC	DW	20	2000	367.0	367.0	45.0
TRSF3222ECPWR	TSSOP	PW	20	2000	367.0	367.0	38.0
TRSF3222EIDWR	SOIC	DW	20	2000	367.0	367.0	45.0
TRSF3222EIPWR	TSSOP	PW	20	2000	367.0	367.0	38.0

DB0020A



PACKAGE OUTLINE

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



4214851/B 08/2019

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.

EXAMPLE BOARD LAYOUT

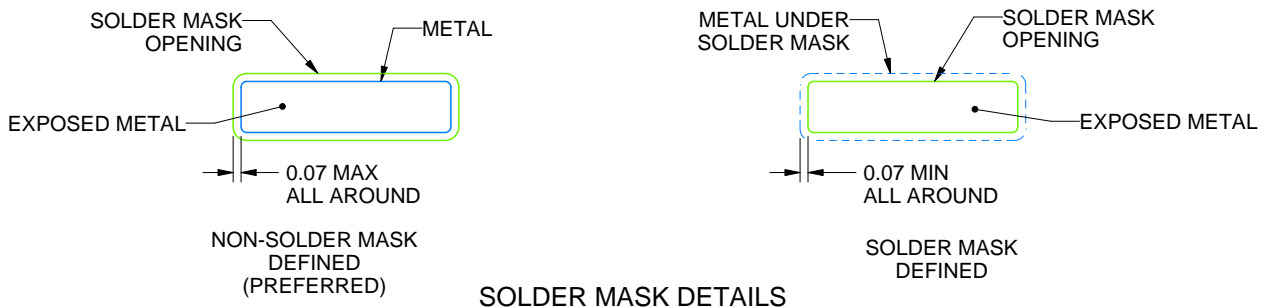
DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4214851/B 08/2019

NOTES: (continued)

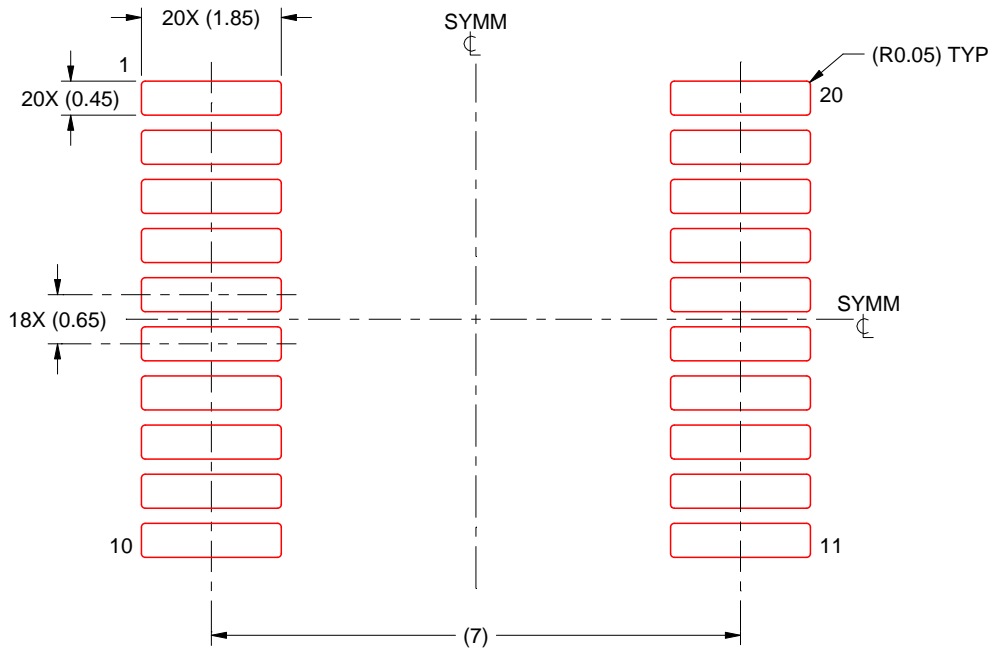
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4214851/B 08/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate design.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

DW0020A



PACKAGE OUTLINE

SOIC - 2.65 mm max height

SOIC



4220724/A 05/2016

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

EXAMPLE BOARD LAYOUT

DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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