Application Note 111

General PCB Design and Layout Guidelines

Micrel 10/100 Switches and PHYs

General Description

This application note assists in designing products that comply with both EMI and ESD standards using Micrel's 10/100 family of switches and PHYs.

The printed circuit board (PCB) is the single most important factor affecting EMI, ESD, and overall performance. Meeting these requirements depends on good PCB design practices. The goal here is to minimize digital and common mode noise as well as to provide shielding between the PCB's internal circuitry and the external environment. These PCB design practices should apply to the entire PCB design, not just to Micrel's Ethernet products.

General Rules

- Position components so as to avoid long loop traces.
- Choose a metal box to shield the circuit board.
- Use a ferrite core on the DC power cord to reduce EMI.
- Follow layout guidelines for differential pairs, ground plane, and high-speed signals.
- Provide termination on clock lines and high-speed digital signals.
- Provide impedance matching on high-speed signal traces to prevent reflections.
- Keep power and ground noise under 50mV peak-to-peak.
- Ensure that the power supply is rated for the application.
- Ensure that switching converters are filtered and properly shielded as these power converters can produce a great deal of EMI noise.

Power and Ground Planes

- Do not split the ground plane into separate planes for analog, digital, and power pins. A single ground plane is recommended for Micrel's 10/100 Ethernet products.
- Route high-speed signals above a continuous unbroken ground plane.
- Fill copper in the unused area of signal planes, and connect these copper fills to the ground plane with vias.
- Stagger the placement of vias to avoid creating long gaps in the planes due to via voids.

Analog V_{CC} Planes

- Place and route the analog components within the analog V_{CC} plane.

Digital V_{CC} Planes

- Place and route the digital components within the digital V_{CC} plane.

Signal Ground

The signal ground region should be one continuous, unbroken plane.

- Connect GNDD, GNDA, and GNDS directly to the signal ground plane for Micrel's 10/100 Ethernet products.

Chassis Ground

The chassis ground and magnetics serve two purposes: they help to reduce EMI noise emissions from the signal ground plane to the PCB's external environment and also act as a shield to protect the PCB components from ESD.

- Place the chassis ground on all PCB layers except for the power plane layer(s).

  Use super vias to join the chassis ground on different PCB layers.
- Connect the chassis ground at multi-points to the external chassis and/or metal frame.
- Use a trench/moat to isolate the chassis ground plane from the signal ground plane.

  The chassis ground region extends from the front edge of the PCB board (RJ-45 connectors) to the magnetics and around the edge of the board. See Figure 1.

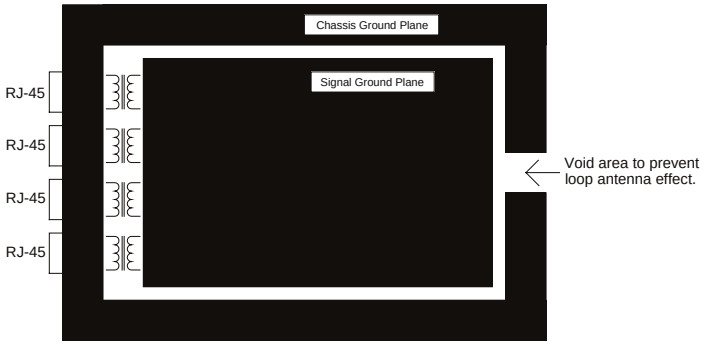

Figure 1. Ground Planes

Magnetic Noise Zone

- Void power and ground planes on all PCB layers directly under the magnetics.
- Extend the chassis ground from the magnetics to the RJ-45 connectors.
- Do not route any digital signals between the PHY and RJ-45 connectors.

Differential Signal Layout

- Route differential pairs close together and away from all other signals.
- Route each differential pair on the same PCB layer.
- Keep both traces of each differential pair as identical to each other as possible.
- Keep transmit (TX) and receive (RX) pairs at least three times the distance from each other.
- Route TX and RX differential pairs using 5-mil trace width and 5-mil spacing. See Figure 2.

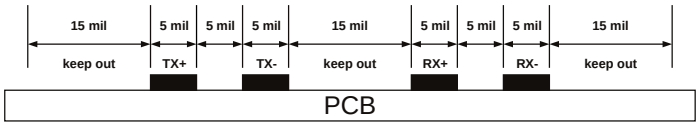

Figure 2. Transmit/Receive Differential Pair

PCB Layer Stacking

6-Layer Example

– Layer 1 component side (short traces), 1-oz copper
– Layer 2 ground plane, 1-oz copper
– Layer 3 signal, 1-oz copper
– Layer 4 signal, 1-oz copper
– Layer 5 power plane, 1-oz copper
– Layer 6 signal, 1-oz copper

Keep Layers 3 and 4 as far apart as possible.

4-Layer Example

– Layer 1 component side, 1-oz copper
– Layer 2 ground plane, 1-oz copper
– Layer 3 power plane, 1-oz copper
– Layer 4 signal, 1-oz copper

Clock Layout Guidelines

- Keep clock traces as short as possible.
- Ensure that all clock traces have an unbroken reference ground plane.
- Use a clock driver when driving multiple loads from a single oscillator.
- Terminate all clock signals.

  For example, place a 33Ω – 50Ω series resistor close to the clock source.

ESD Protection

Various ESD protection methods and devices can be used. The level of ESD protection provided by each method varies and depends on the type of protection device used. Consult the specific manufacturer's data sheet to determine the level of ESD protection and proper connection. Figures 3 and 4 show examples of two ESD protection methods.

- Place transient voltage suppressor (TVS) devices on the TX and RX differential pair I/Os to help increase ESD protection.

  These devices are connected in parallel with the I/O lines to be protected.
- Connect all unused inputs to either ground with a 1K resistor or power with a 10K resistor, depending on the desired strap-in setting of the chip.
- Place termination resistors for the TX and RX differential pairs close to the Micrel chip. See Figure 5.
- During FCC or ESD tests, remove all unused headers pins, jumpers, test point pins, etc. These parts act as antennas and can degrade test results.

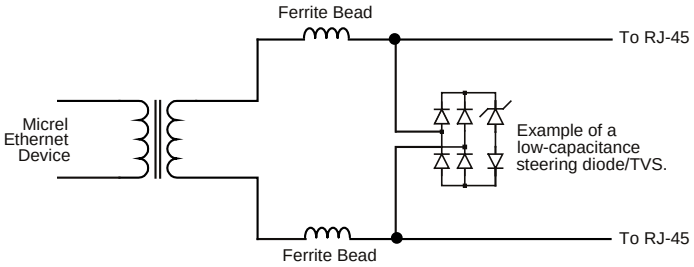

Figure 3. ESD Protection on the RJ-45 Side

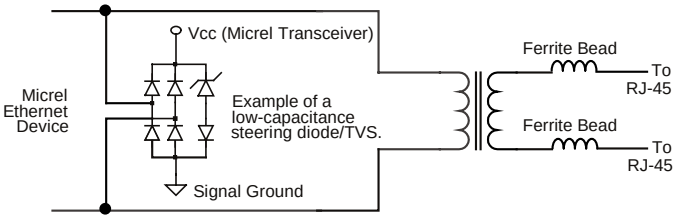

Figure 4. ESD Protection on Micrel's Ethernet Device Side

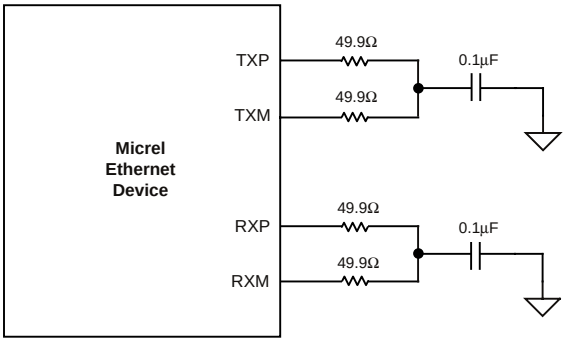

Figure 5. Termination of TX and RX Differential Pairs

For additional support, contact your local Micrel Field Application Engineer or salesperson.

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