KSZ8873MLL 64LQFP reference design Revision 1.0

REVISION HISTORY

DATE:	DESCRIPTION	REVISION
04/30/2009	Initial release	1.0

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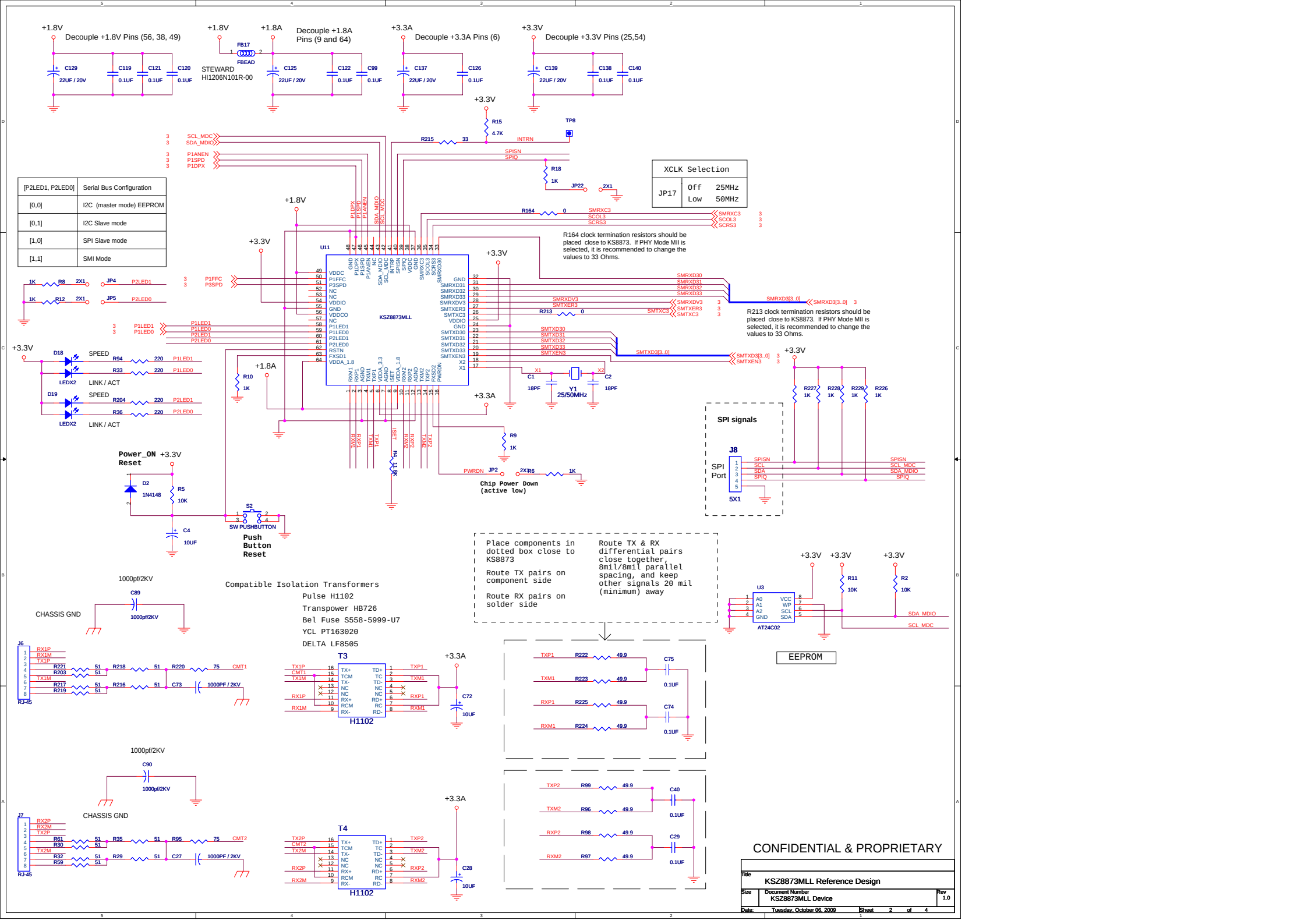
+1.8V
Decouple +1.8V Pins (56, 38, 49)
C129 22UF / 20V
C119 0.1UF
C121 0.1UF
C120 0.1UF
+1.8V
FB17
FBEAD
STEWARD
HI1206N101R-00
+1.8A
Decouple +1.8A Pins (9 and 64)
C125 22UF / 20V
C122 0.1UF
C99 0.1UF
+3.3A
Decouple +3.3A Pins (6)
C137 22UF / 20V
C126 0.1UF
+3.3V
Decouple +3.3V Pins (25,54)
C139 22UF / 20V
C138 0.1UF
C140 0.1UF
+3.3V
R15 4.7K
TP8
INTRN
R215 33
SPISN
SPIQ
R18 1K
JP22 2X1
SCL_MDC
SDA_MDIO
P1ANEN
P1SPD
P1DPX
XCLK Selection
JP17 Off 25MHz
Low 50MHz
[P2LED1, P2LED0] Serial Bus Configuration
[0,0] I2C (master mode) EEPROM
[0,1] I2C Slave mode
[1,0] SPI Slave mode
[1,1] SMI Mode
R164 clock termination resistors should be placed close to KS8873. If PHY Mode MII is selected, it is recommended to change the values to 33 Ohms.
R213 clock termination resistors should be placed close to KS8873. If PHY Mode MII is selected, it is recommended to change the values to 33 Ohms.
U11
KSZ8873MLL
R164 0
R213 0
1K R8 2X1 JP4 P2LED1
1K R12 2X1 JP5 P2LED0
P1FFC
P3SPD
P1LED1
P1LED0
P2LED1
P2LED0
RSTN
FXSD1
D18 SPEED R94 220 P1LED1
LEDX2 R33 220 P1LED0 LINK / ACT
D19 SPEED R204 220 P2LED1
LEDX2 R36 220 P2LED0 LINK / ACT
R10 1K
C1 18PF
Y1 25/50MHz
C2 18PF
R9 1K
R4 1.18K
PWRDN JP2 2X1 R6 1K
Chip Power Down (active low)
Power_ON Reset
D2 1N4148
R5 10K
C4 10UF
S2 SW PUSHBUTTON
Push Button Reset
SPI signals
J8 SPI Port 5X1
R227 1K
R228 1K
R229 1K
R226 1K
Place components in dotted box close to KS8873
Route TX pairs on component side
Route RX pairs on solder side
Route TX & RX differential pairs close together, 8mil/8mil parallel spacing, and keep other signals 20 mil (minimum) away
U3 AT24C02
R11 10K
R2 10K
EEPROM
1000pf/2KV
C89 1000pf/2KV
CHASSIS GND
Compatible Isolation Transformers
Pulse H1102
Transpower HB726
Bel Fuse S558-5999-U7
YCL PT163020
DELTA LF8505
J6 RJ-45
R221 51
R203 51
R218 51
R220 75 CMT1
R217 51
R219 51
R216 51
C73 1000PF / 2KV
T3 H1102
C72 10UF
R222 49.9
R223 49.9
R225 49.9
R224 49.9
C75 0.1UF
C74 0.1UF
1000pf/2KV
C90 1000pf/2KV
CHASSIS GND
J7 RJ-45
R61 51
R30 51
R35 51
R95 75 CMT2
R32 51
R59 51
R29 51
C27 1000PF / 2KV
T4 H1102
C28 10UF
R99 49.9
R96 49.9
R98 49.9
R97 49.9
C40 0.1UF
C29 0.1UF
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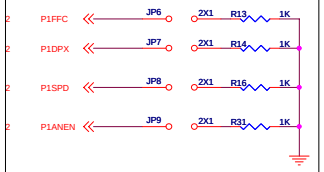
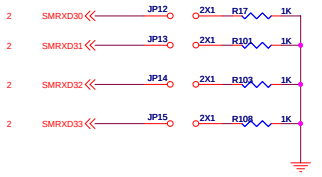
PORT 1



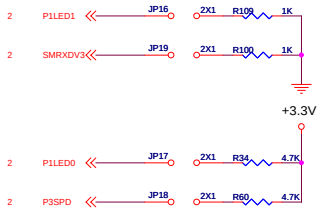
JP6	Force Flow Control Off = ENABLE Low = DISABLE
JP7	Force Full/Half Off = Full Duplex Low = Half Duplex
JP8	Force Speed Off = 100BaseTX Low = 10BaseT
JP9	Auto-negotiation Off = Enable Low = Disable

PORT 2



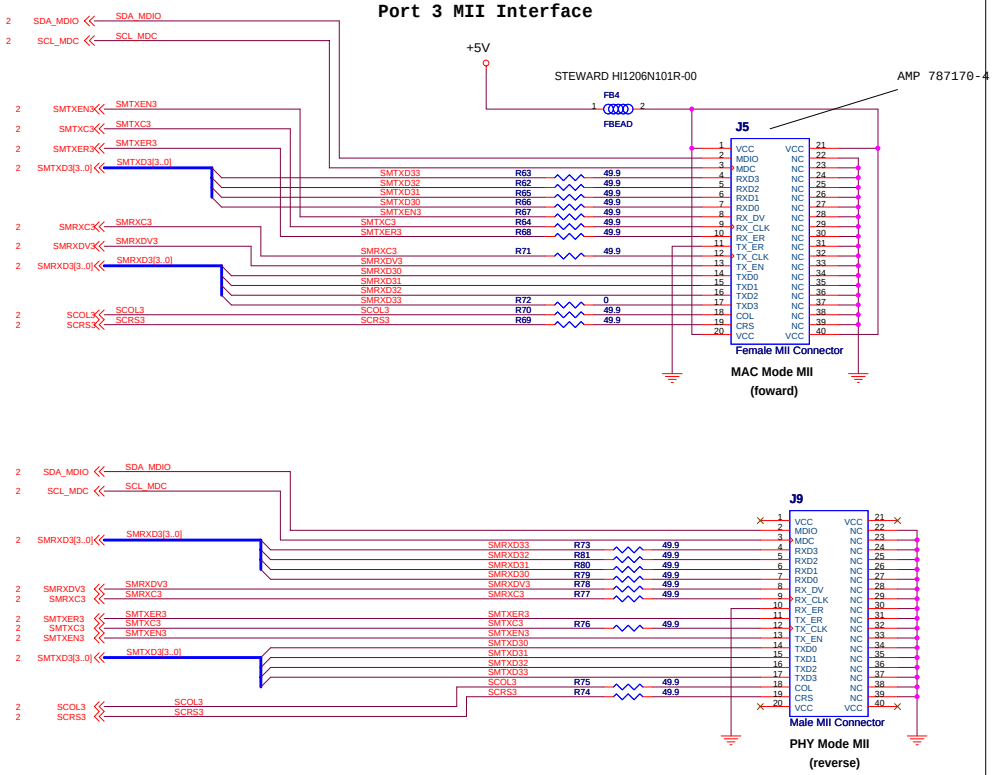
JP12	Force Flow Control Off = ENABLE Low = DISABLE
JP13	Force Full/Half Off = Full Duplex Low = Half Duplex
JP14	Force Speed Off = 100BaseTX Low = 10BaseT
JP15	Auto-negotiation Off = ENABLE Low = DISABLE

PORT 3



JP16	Force Flow Control Off = ENABLE Low = DISABLE
JP17	Force Full/Half High = Half Duplex Off = Full Duplex
JP18	Force Speed High = 10BaseT Off = 100BaseTX
JP19	MII Mode Selection Off = PHY mode Low = MAC mode

Port 3 MII Interface



MICREL
KENDIN OPERATIONS

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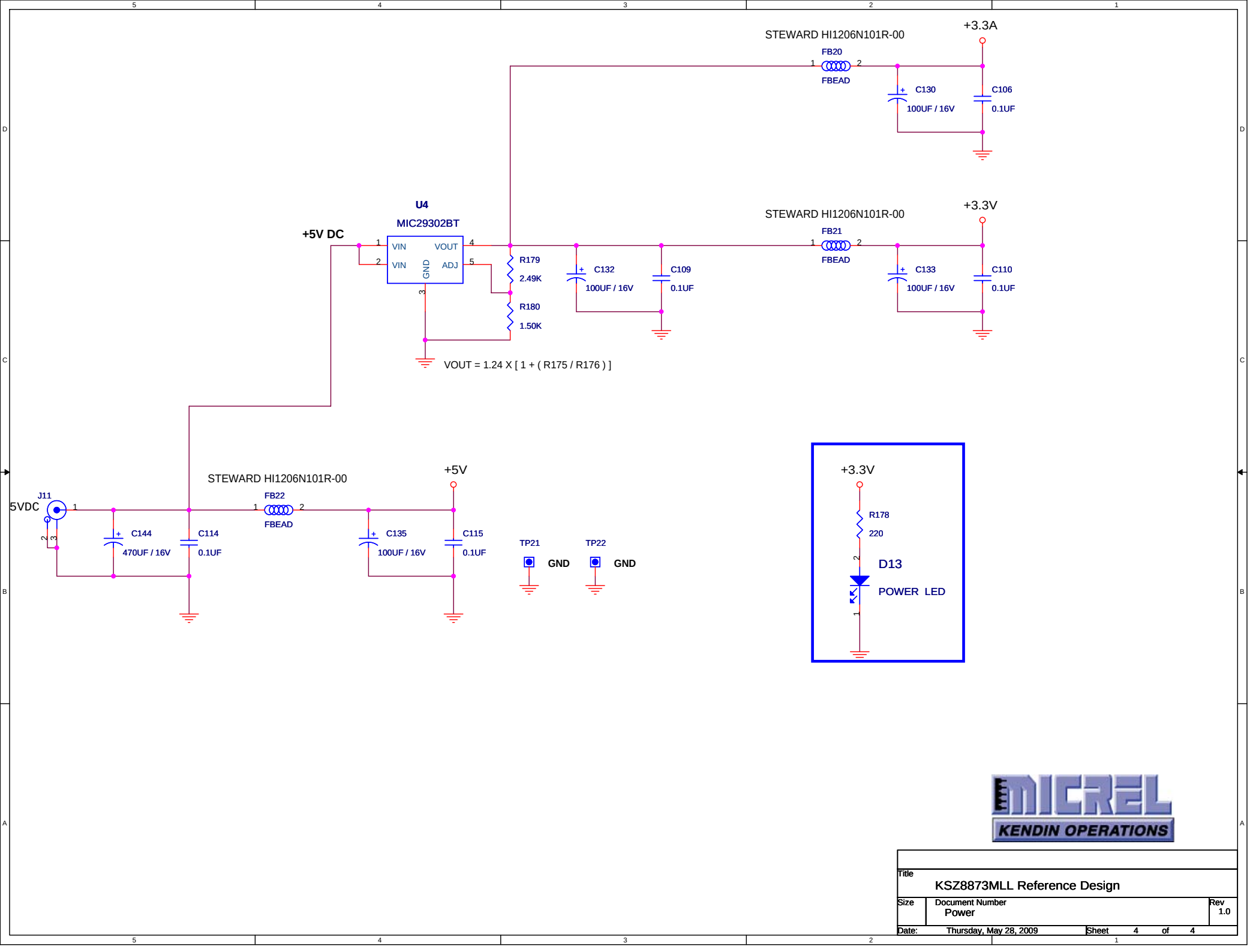
STEWARD HI1206N101R-00
+3.3A
FB20
FBEAD
C130
100UF / 16V
C106
0.1UF
U4
MIC29302BT
+5V DC
VIN
VIN
GND
VOUT
ADJ
R179
2.49K
R180
1.50K
C132
100UF / 16V
C109
0.1UF
STEWARD HI1206N101R-00
+3.3V
FB21
FBEAD
C133
100UF / 16V
C110
0.1UF
VOUT = 1.24 X [1 + (R175 / R176)]
STEWARD HI1206N101R-00
+5V
J11
5VDC
FB22
FBEAD
C144
470UF / 16V
C114
0.1UF
C135
100UF / 16V
C115
0.1UF
TP21
GND
TP22
GND
+3.3V
R178
220
D13
POWER LED
MICREL
KENDIN OPERATIONS
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