KSZ8873FLL/MLL/RLL_LQFP Demo Board Revision 1.0

REVISION HISTORY

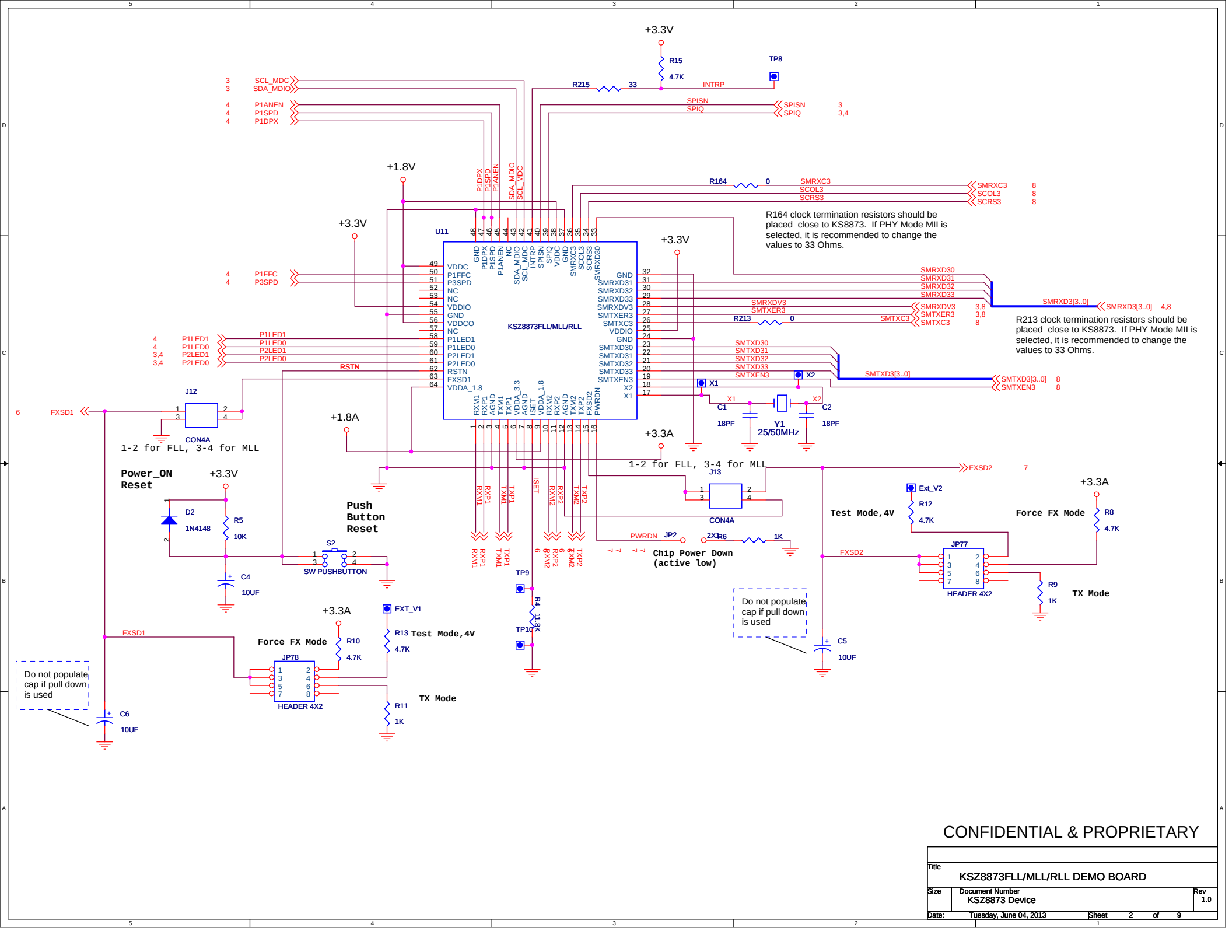
DATE:	DESCRIPTION	REVISION
04/30/2009	Initial release	1.0

Table of Contents

PAGE 01: Revision History
PAGE 02: KSZ8873FLL/MLL/RLL_LQFP Device
PAGE 03: Device Configuration /
PAGE 04: Device Configuration and LEDs
PAGE 05: Ethernet Interface
PAGE 06: Fiber interface1
PAGE 07: Fiber Interface2
PAGE 08: MII / RMII / SNI Interface
PAGE 09: Power

CONFIDENTIAL & PROPRIETARY

Title: KS8873FLL/MLL/RLL DEMO BOARD		
Size	Document Number: Revision History	Rev: 1.0
Date: Tuesday, June 04, 2013	Sheet 1 of 9	

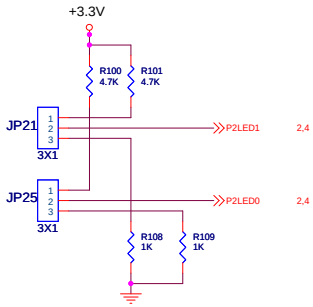

+3.3V
R15
4.7K
TP8
R215
33
INTRP
SPISN
SPIQ
SCL_MDC
SDA_MDIO
P1ANEN
P1SPD
P1DPX
+1.8V
+3.3V
U11
KSZ8873FLL/MLL/RLL
R164
0
SMRXC3
SCOL3
SCRS3
R164 clock termination resistors should be placed close to KS8873. If PHY Mode MII is selected, it is recommended to change the values to 33 Ohms.
SMRXD30
SMRXD31
SMRXD32
SMRXD33
SMRXD3[3..0]
SMRXDV3
SMTXER3
SMTXC3
R213
0
R213 clock termination resistors should be placed close to KS8873. If PHY Mode MII is selected, it is recommended to change the values to 33 Ohms.
P1FFC
P3SPD
P1LED1
P1LED0
P2LED1
P2LED0
RSTN
SMTXD30
SMTXD31
SMTXD32
SMTXD33
SMTXEN3
SMTXD3[3..0]
X1
X2
C1
C2
18PF
Y1
25/50MHz
J12
CON4A
1-2 for FLL, 3-4 for MLL
+1.8A
+3.3A
Power_ON Reset
D2
1N4148
R5
10K
C4
10UF
Push Button Reset
S2
SW PUSHBUTTON
J13
CON4A
PWRDN
JP2
R6
1K
Chip Power Down (active low)
TP9
TP10
R4
11.8K
Test Mode,4V
Ext_V2
R12
4.7K
Force FX Mode
R8
4.7K
JP77
HEADER 4X2
R9
1K
TX Mode
FXSD1
FXSD2
EXT_V1
R13
4.7K
R10
4.7K
JP78
HEADER 4X2
R11
1K
Do not populate cap if pull down is used
C6
10UF
C5
10UF
CONFIDENTIAL & PROPRIETARY
Title
KSZ8873FLL/MLL/RLL DEMO BOARD
Size
Document Number
KSZ8873 Device
Rev
1.0
Date:
Tuesday, June 04, 2013
Sheet
2
of
9

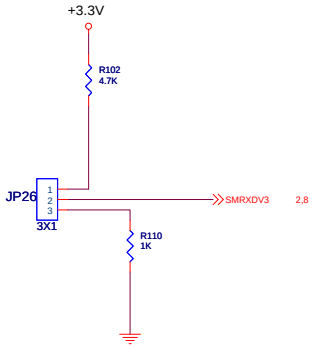
[P2LED1, P2LED0]	Serial Bus Configuration
[0,0]	I2C (master mode) EEPROM
[0,1]	I2C Slave mode
[1,0]	SPI Slave mode
[1,1]	SMI Mode

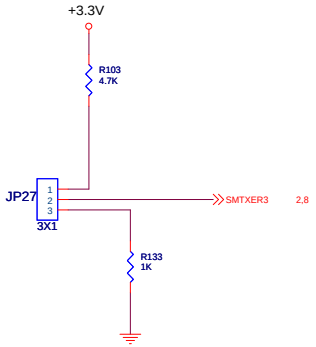
SMRXDV3	Switch MII Configuration
1	PHY mode MII
0	MAC mode MII

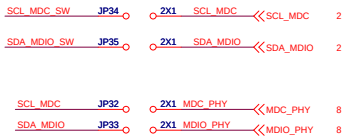
SMTXER3	SWITCH MII Configuration (For test only)
1	MII no link in PHY mode
0	Tie to GND in RMII mode

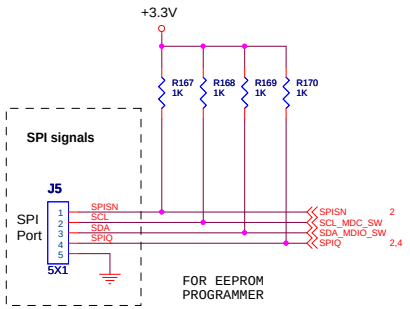
Bus Selection	Jumper Setting
SMI / MIIM (SW)	open JP32 and JP33. close JP34 and JP35.
I2C Master / I2C Slave / SPI Slave	open JP32 and JP33 close JP34 and JP35.
MIIM (PHY only)	close JP32 and JP33 open JP34 and JP35.

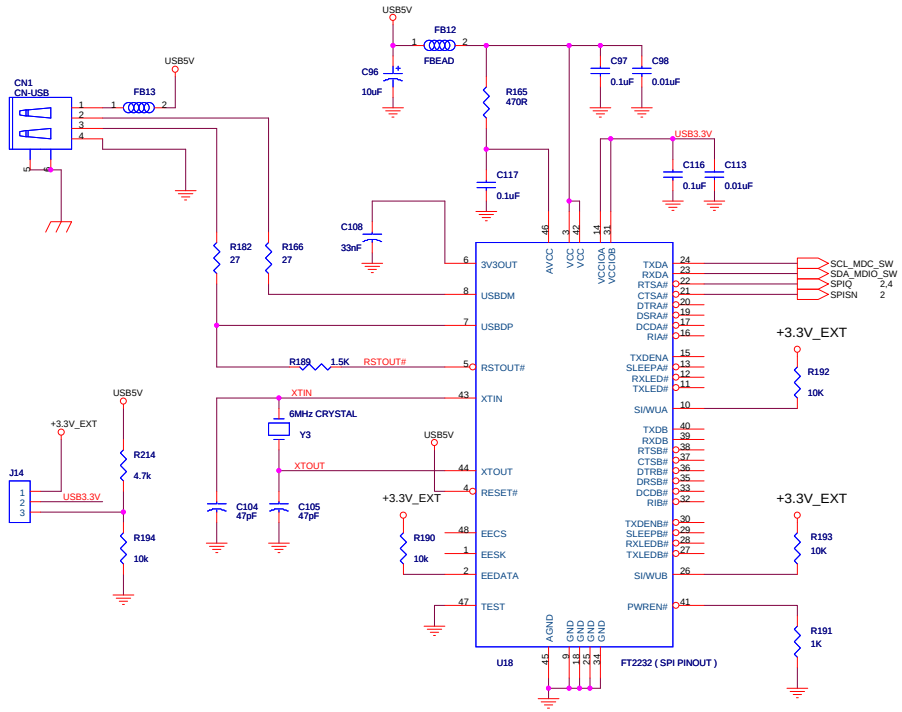








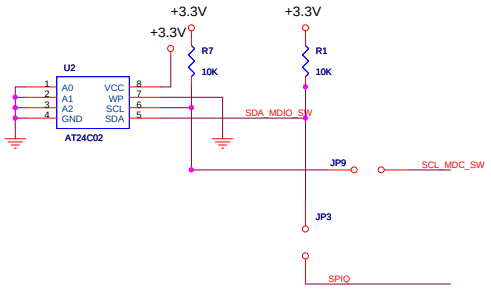




1-2 Close for default

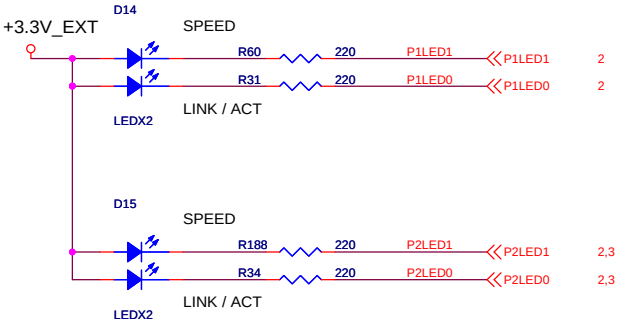
1-2	USB 3.3V from LDO
2-3	USB 3.3V from USB port Not Recomment

	EEPROM I2C master	SPI, I2C Slave SMI
JP3	CLOSE	CLOSE
JP9	CLOSE	OPEN

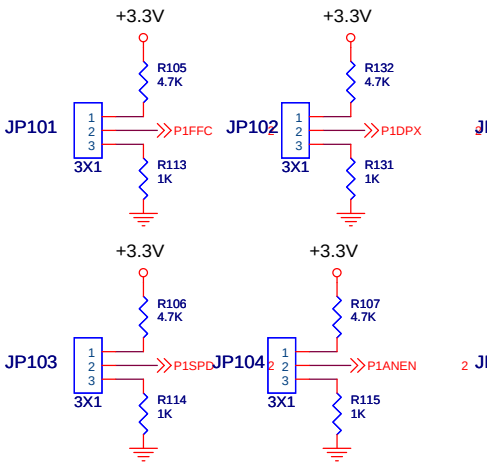


CONFIDENTIAL & PROPRIETARY

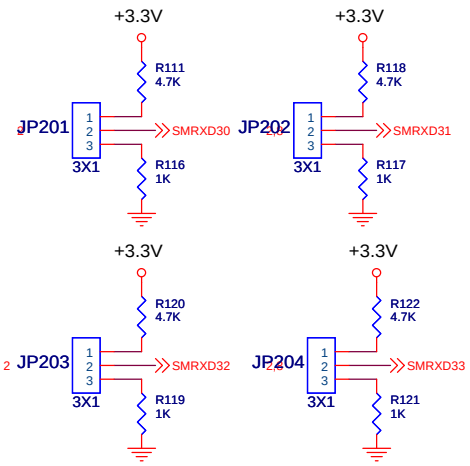
Title	KSZ8873FLL/MLL/RLL DEMO BOARD	
Size	Document Number: Device Configuration	Rev: 1.0
Date: Tuesday, June 04, 2013	Sheet 3 of 9	



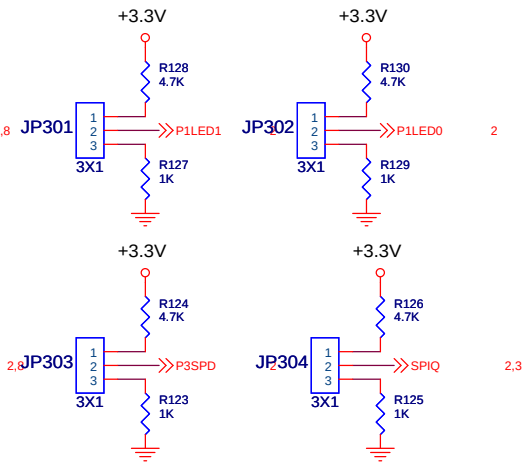
PORT 1



PORT 2



PORT 3



JP101	Force Flow Control Pull Up = ENABLE Pull Down = DISABLE
JP102	Force Full/Half Pull Up = Full Duplex Pull Down = Half Duplex
JP103	Force Speed Pull Up = 100BaseTX Pull Down = 10BaseT
JP104	Auto-negotiation Pull Up = ENABLE Pull Down = DISABLE

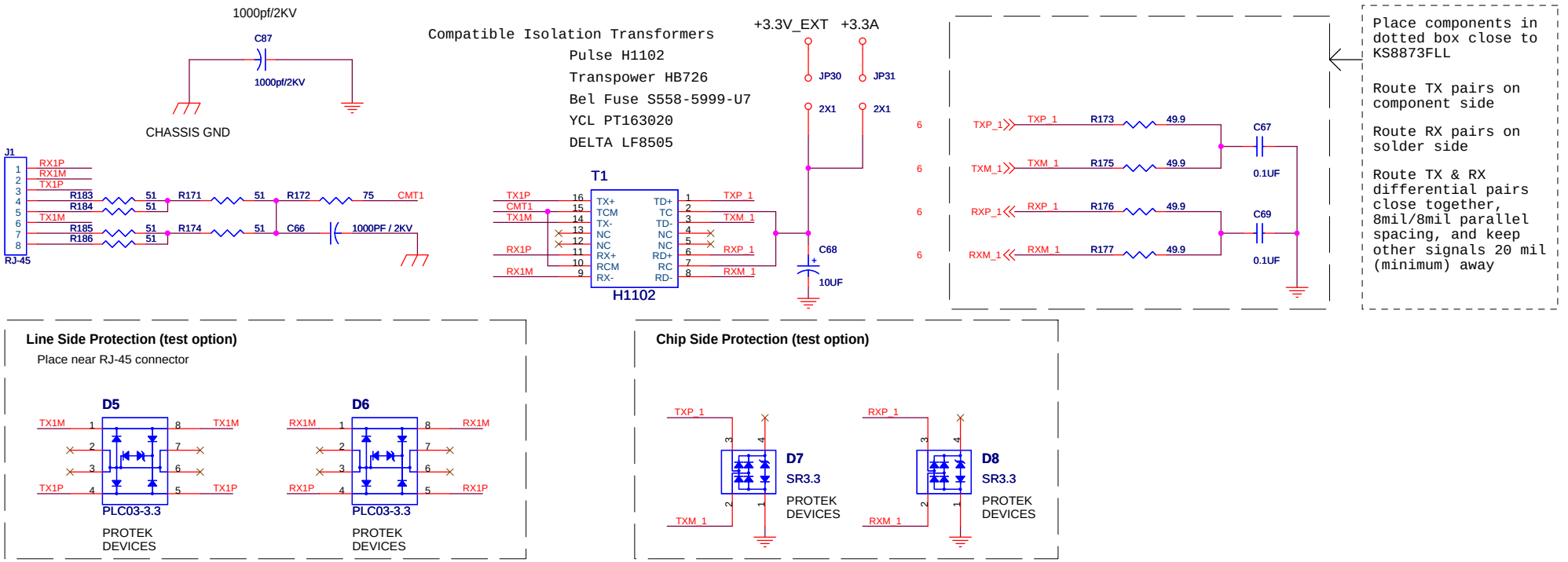
JP201	Force Flow Control Pull Up = ENABLE Pull Down = DISABLE
JP202	Force Full/Half Pull Up = Full Duplex Pull Down = Half Duplex
JP203	Force Speed Pull Up = 100BaseTX Pull Down = 10BaseT
JP204	Auto-negotiation Pull Up = ENABLE Pull Down = DISABLE

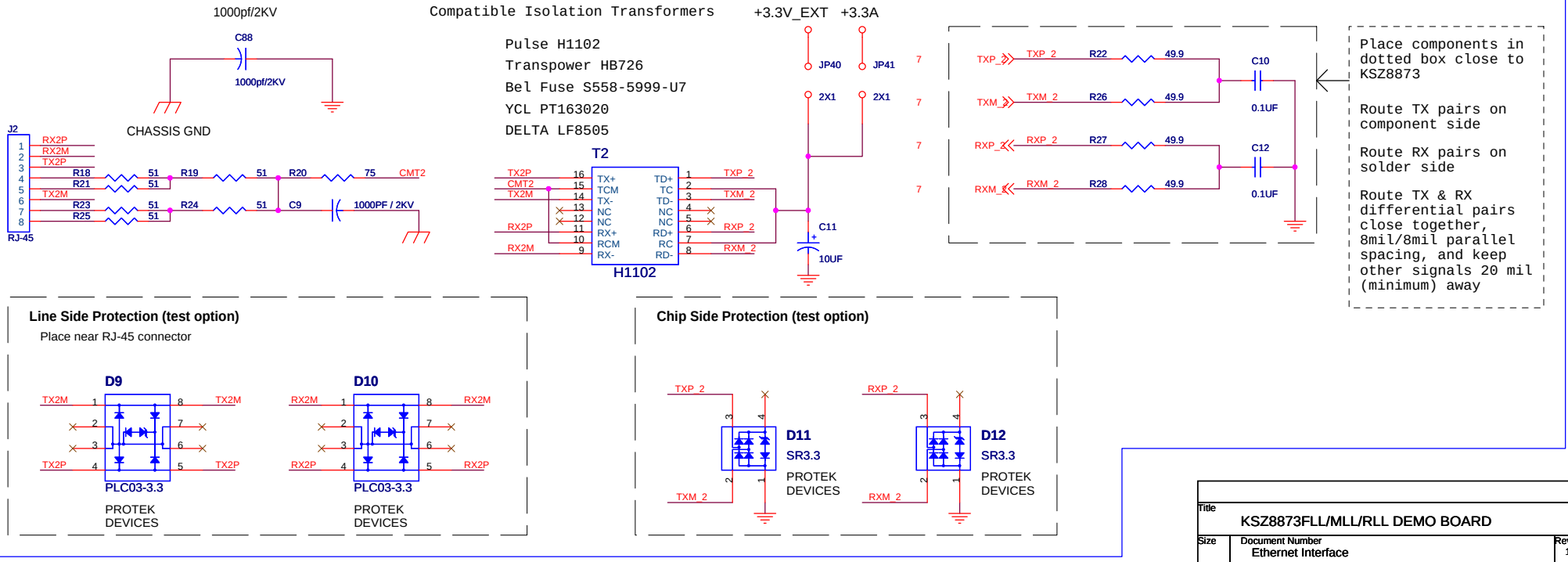
JP301	Force Flow Control Pull Up = ENABLE Pull Down = DISABLE
JP302	Force Full/Half Pull Down = Full Duplex Pull Up = Half Duplex
JP303	Force Speed Pull Down = 100BaseTX Pull Up = 10BaseT
JP304	XCLK Frequency Pull Up/Off = 25MHz Pull Down = 50MHz

MICREL
KENDIN OPERATIONS

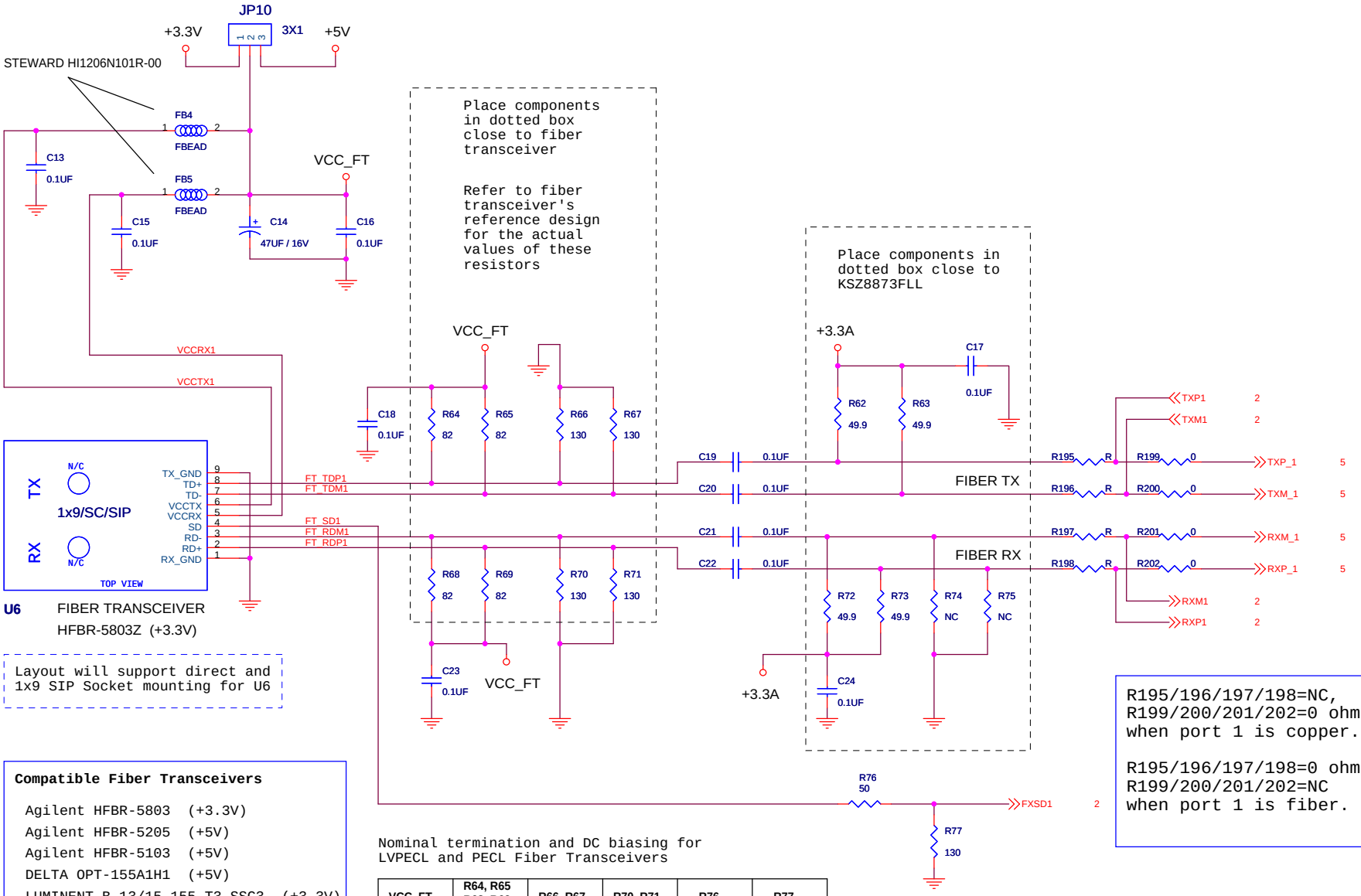
CONFIDENTIAL & PROPRIETARY

Title: KSZ8873FLL/MLL/RLL DEMO BOARD		
Size	Document Number: Device Configuration and LEDs	Rev: 1.0
Date: Tuesday, June 04, 2013	Sheet 4 of 9	





Title	KSZ8873FLL/MLL/RLL DEMO BOARD	
Size	Document Number: Ethernet Interface	Rev: 1.0
Date: Tuesday, June 04, 2013	Sheet 5 of 9	

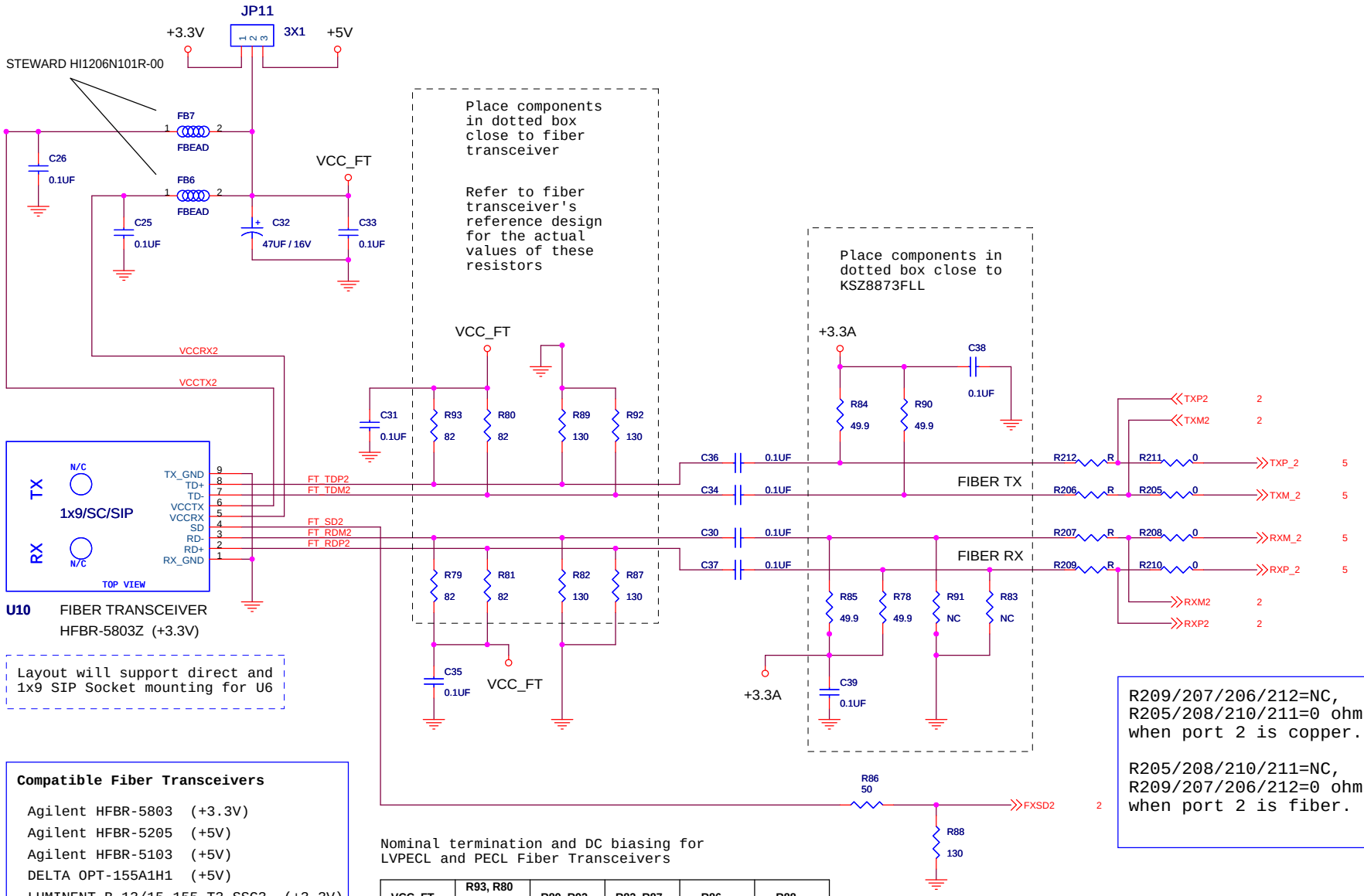


VCC_FT	R64, R65 R68, R69	R66, R67	R70, R71	R76	R77
+3.3V	82 Ohms	130 Ohms	130 Ohms	O Ohm	130 Ohms
+5V	68 Ohms	191 Ohms	270 Ohms	4.75K 1%	5.62K 1%

KENDIN OPERATIONS

CONFIDENTIAL & PROPRIETARY

Title: KSZ8873FLL/MLL/RLL DEMO BOARD		
Size	Document Number: Fiber Interface	Rev: 1.0
Date: Tuesday, June 04, 2013	Sheet 6 of 9	



Compatible Fiber Transceivers

- Agilent HFBR-5803 (+3.3V)
- Agilent HFBR-5205 (+5V)
- Agilent HFBR-5103 (+5V)
- DELTA OPT-155A1H1 (+5V)
- LUMINENT B-13/15-155-T3-SSC3 (+3.3V)
- LUMINENT B-13/15-155-T-SSC3 (+5V)

Nominal termination and DC biasing for LVPECL and PECL Fiber Transceivers

VCC_FT	R93, R80 R79, R81	R89, R92	R82, R87	R86	R88
+3.3V	82 Ohms	130 Ohms	130 Ohms	O Ohm	130 Ohms
+5V	68 Ohms	191 Ohms	270 Ohms	4.75K 1%	5.62K 1%

KENDIN OPERATIONS

CONFIDENTIAL & PROPRIETARY

Title	KSZ8873FLL/MLL/RLL DEMO BOARD		
Size	Document Number: Fiber Interface		Rev: 1.0
Date: Tuesday, June 04, 2013	Sheet 7 of 9		

RMII option

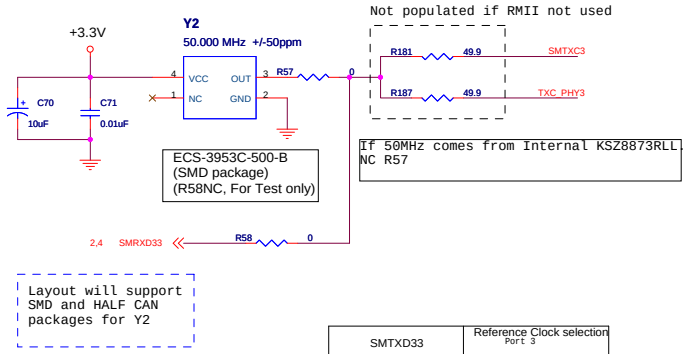
KS8873RLL provides RMII signals with respect to both PHY and MAC sides.

For this board, the KS8873RLL provides RMII signals with respect to MAC side only. The RMII signal connections between KS8873RLL and external PHY are shown in the table to the right.

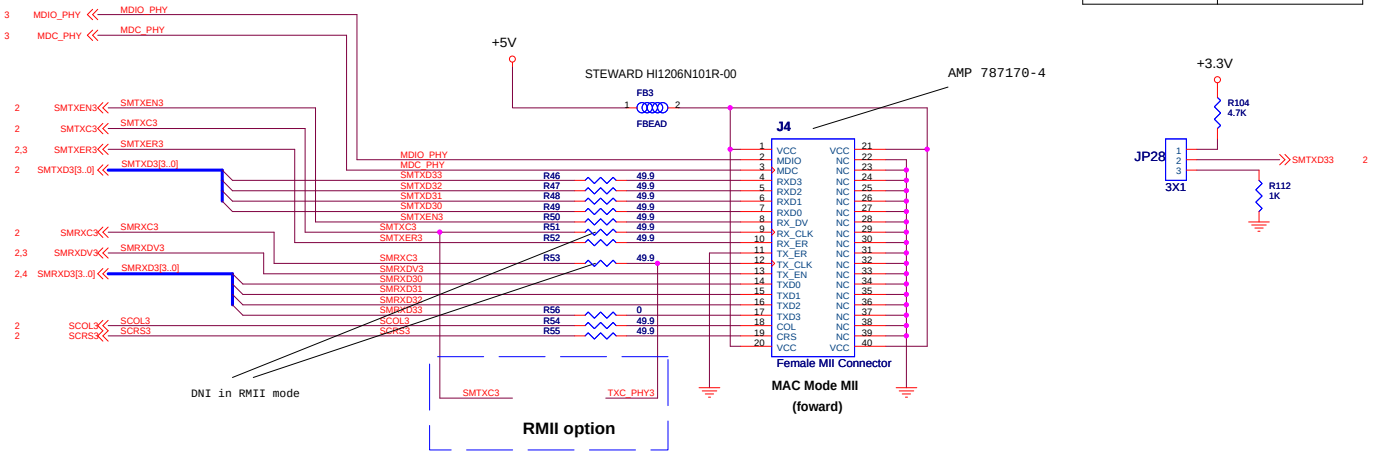
The KSZ8873RLL can provide the 50MHz reference clock by disconnect JP19 to enable REFCLKO. Remove R 51 and R53.

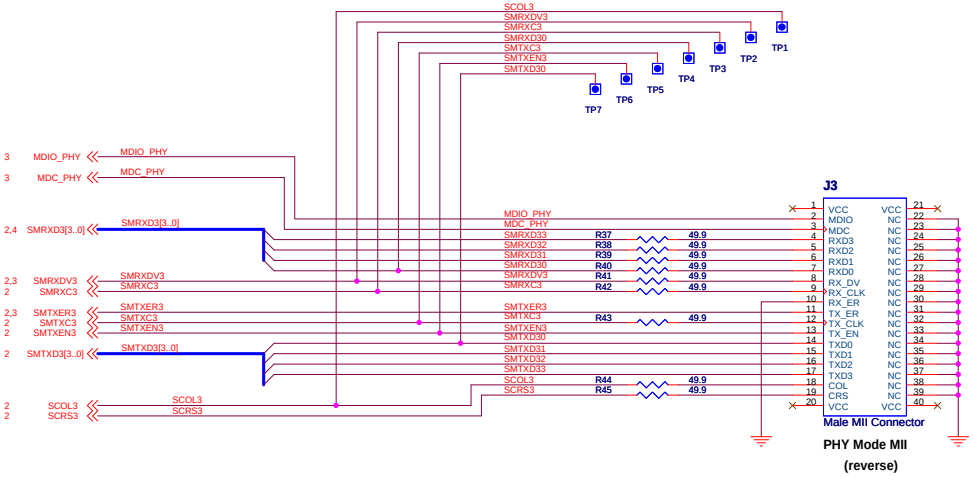
The KSZ8873RLL can use internal or external reference clock which is selected by register 198 bit 3.
For external, it is set to 1, vice reverse.

External PHY RMII (with respect to PHY)		KSZ8873RLL RMII (with respect to MAC)		
Signal	Type	Signal	Pin #	Type
REF_CLK	Input	SMTXC3	26	Input
CRS_DV	Output	SMTXEN3	19	Input
RXD[1]	Output	SMTXD31	22	Input
RXD[0]	Output	SMTXD30	23	Input
TX_EN	Input	SMRXDV3	28	Output
TXD[1]	Input	SMRXD31	31	Output
TXD[0]	Input	SMRXD30	33	Output
RX_ER	Output	SMTXER3	27	Input

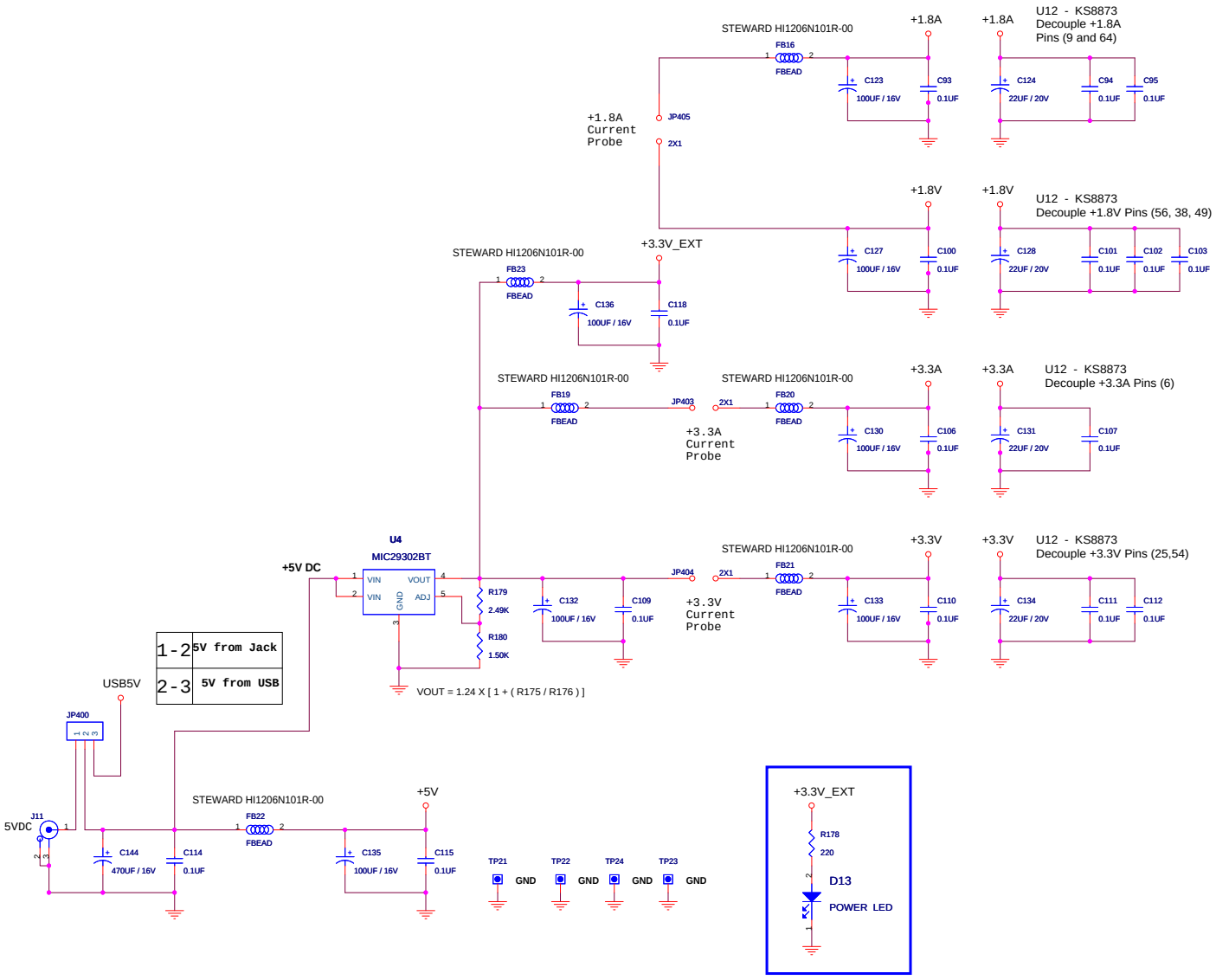


SMTXD33 Port 3	Reference Clock selection
1	Enable REFCLKO Output
0	Disable REFCLKO Output





Title	KSZ8873FLL/MLL/RLL DEMO BOARD		
Size	Document Number: MII / RMII Interface		Rev: 1.0
Date: Tuesday, June 04, 2013	Sheet 8 of 9		



KENDIN OPERATIONS

CONFIDENTIAL & PROPRIETARY

Title	KSZ8873FLL/MLL/RLL DEMO BOARD	
Size	Document Number: Power	Rev: 1.0
Date: Tuesday, June 04, 2013	Sheet 9 of 9	