

# KSZ8873FLL 64LQFP reference design Revision 1.0

## REVISION HISTORY

DATE:	DESCRIPTION	REVISION
04/30/2009	Initial release	1.0

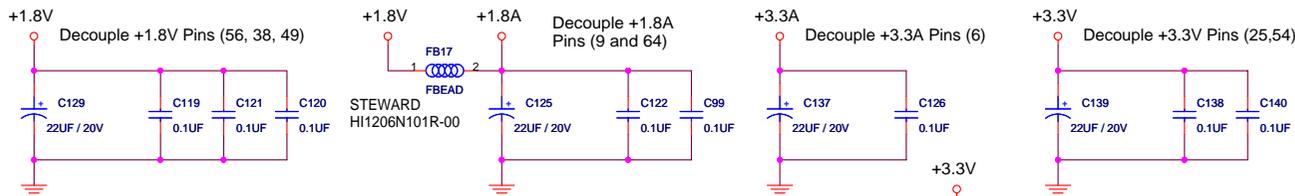
### Table of Contents

PAGE 01: Revision History  
PAGE 02: KSZ8873FLL\_LQFP Device  
PAGE 03: Device Configuration/Strap and MII Interface  
PAGE 04: Fiber Interface  
PAGE 05: Power



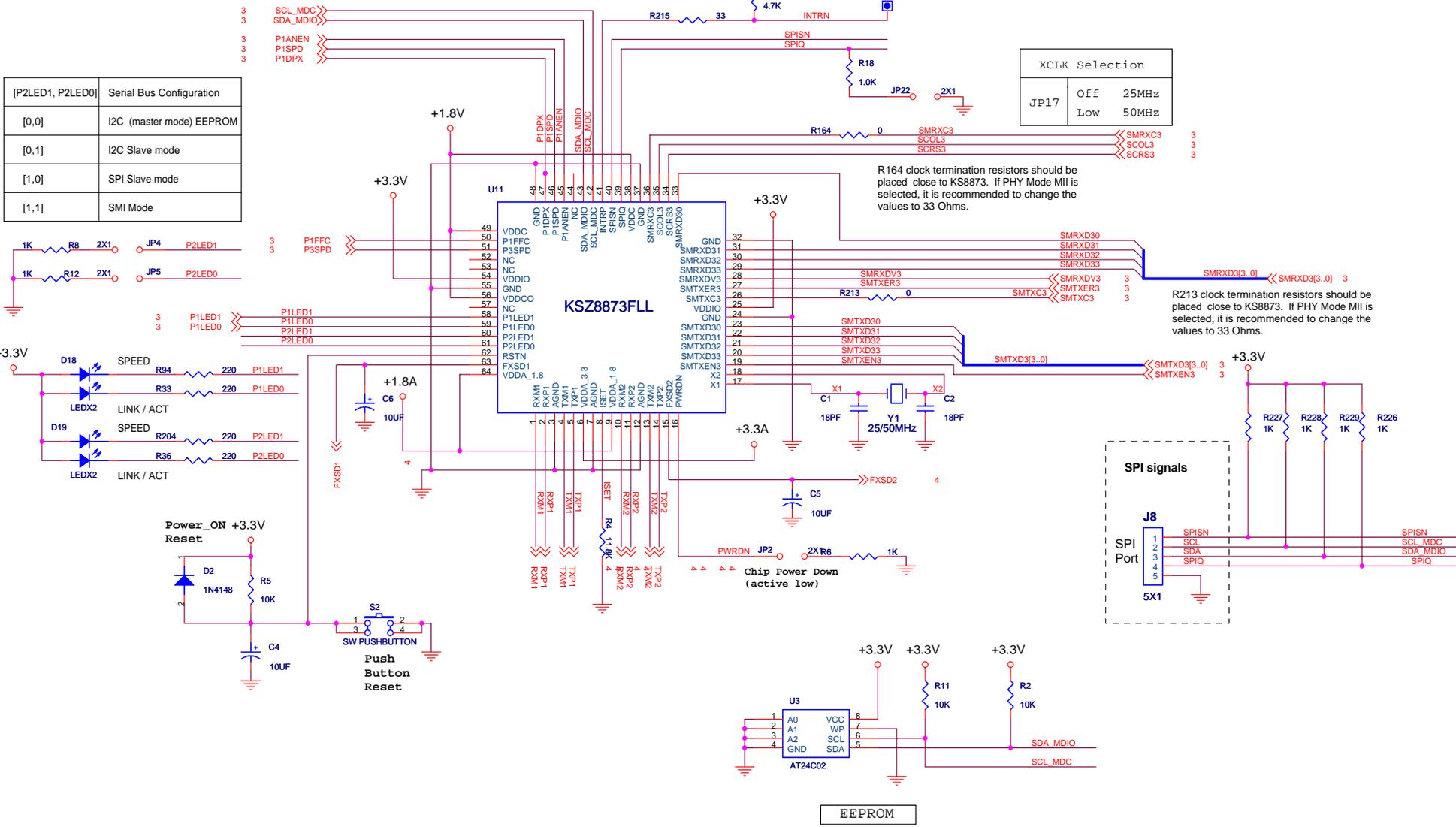
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Title		
KS8873FLL Reference Design		
Size	Document Number Revision History	Rev 1.0
Date:	Thursday, May 28, 2009	Sheet 1 of 5



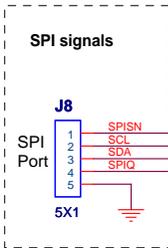
[P2LED1, P2LED0]	Serial Bus Configuration
[0,0]	I2C (master mode) EEPROM
[0,1]	I2C Slave mode
[1,0]	SPI Slave mode
[1,1]	SMI Mode

XCLK Selection		
JP17	Off	25MHz
	Low	50MHz



R164 clock termination resistors should be placed close to KS8873. If PHY Mode MII is selected, it is recommended to change the values to 33 Ohms.

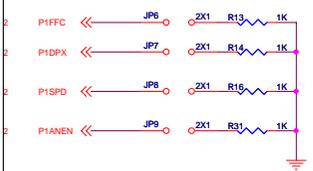
R213 clock termination resistors should be placed close to KS8873. If PHY Mode MII is selected, it is recommended to change the values to 33 Ohms.



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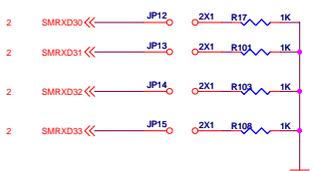
Title			
KSZ8873FLL Reference Design			
Size	Document Number	Rev	
	KSZ8873FLL Device	1.0	
Date:	Tuesday, October 06, 2009	Sheet	2 of 4

### PORT 1



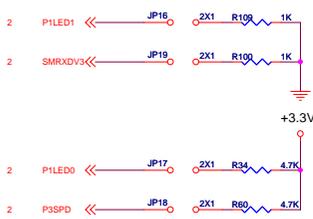
JP6	Force Flow Control Off = ENABLE Low = DISABLE
JP7	Force Full/Half Off = Full Duplex Low = Half Duplex
JP8	Force Speed Off = 100BaseTX Low = 10BaseT
JP9	Auto-negotiation Off = Enable Low = Disable

### PORT 2



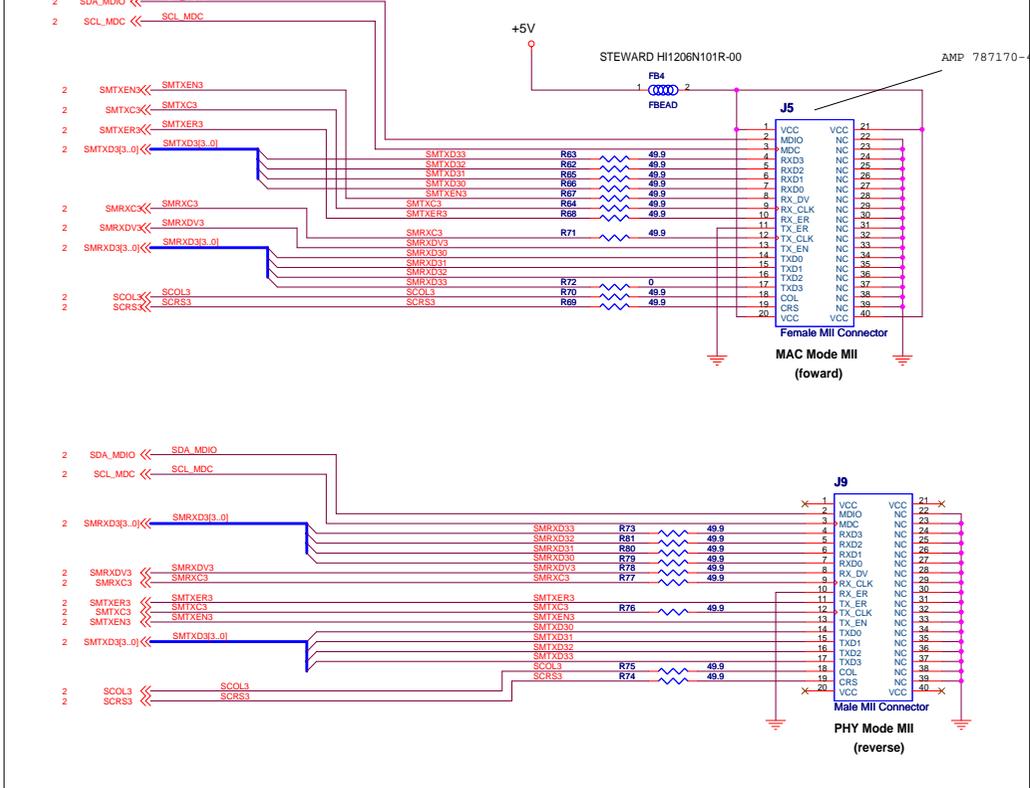
JP12	Force Flow Control Off = ENABLE Low = DISABLE
JP13	Force Full/Half Off = Full Duplex Low = Half Duplex
JP14	Force Speed Off = 100BaseTX Low = 10BaseT
JP15	Auto-negotiation Off = ENABLE Low = DISABLE

### PORT 3



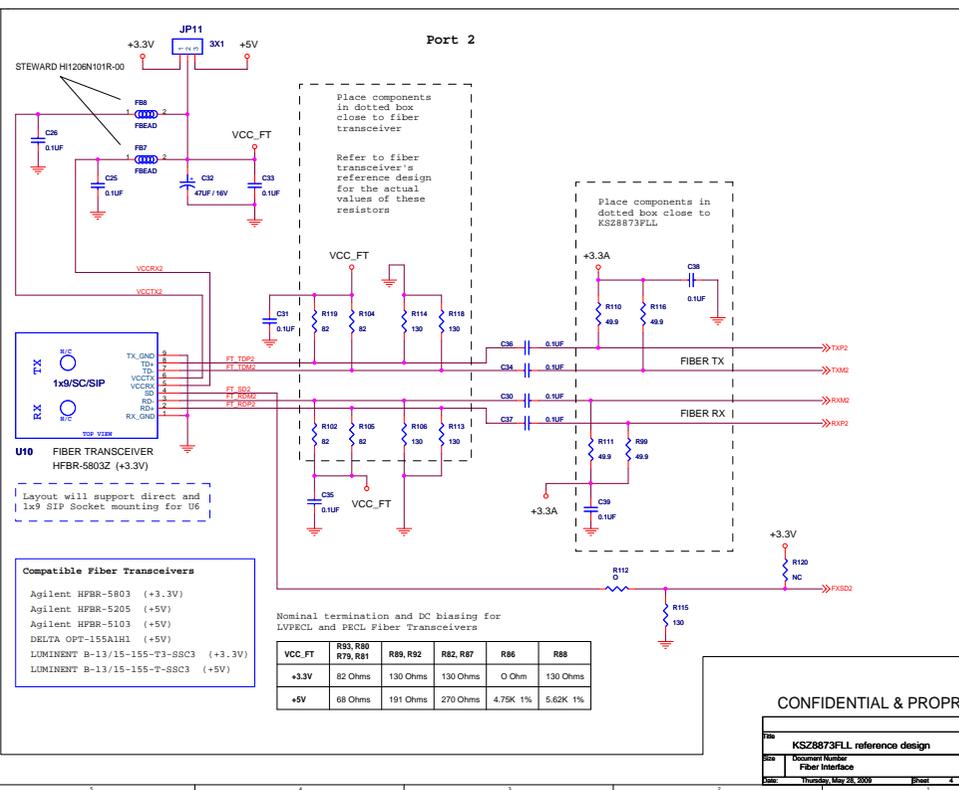
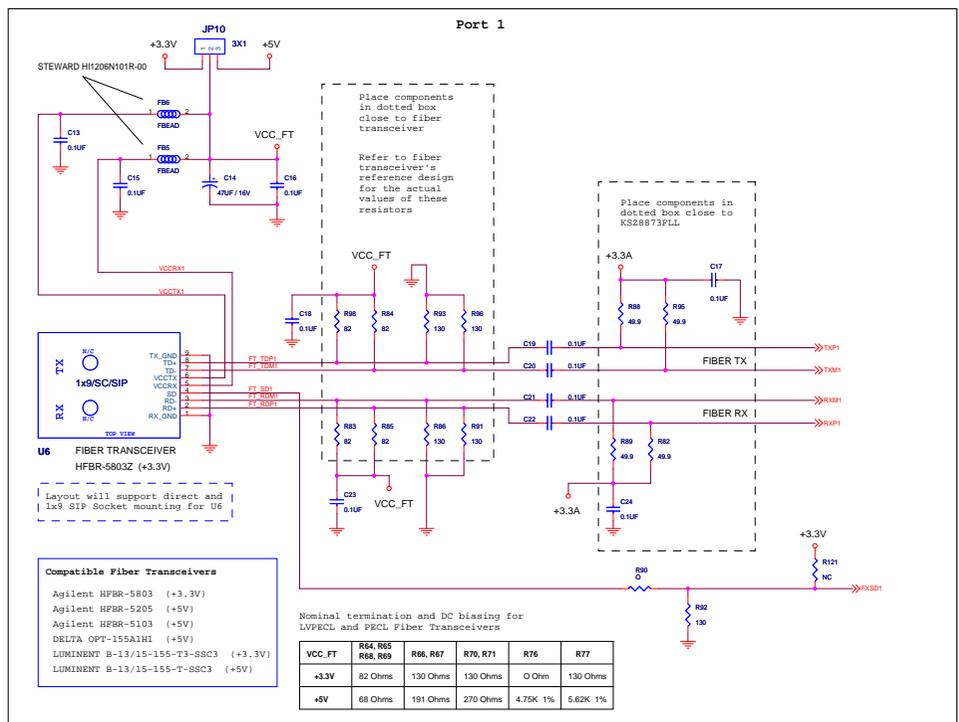
JP16	Force Flow Control Off = ENABLE Low = DISABLE
JP17	Force Full/Half High = Half Duplex Off = Full Duplex
JP18	Force Speed High = 100BaseT Off = 100BaseTX
JP19	MII Mode Selection Off = PHY mode Low = MAC mode

### Port 3 MII Interface

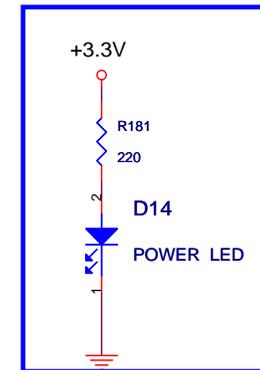
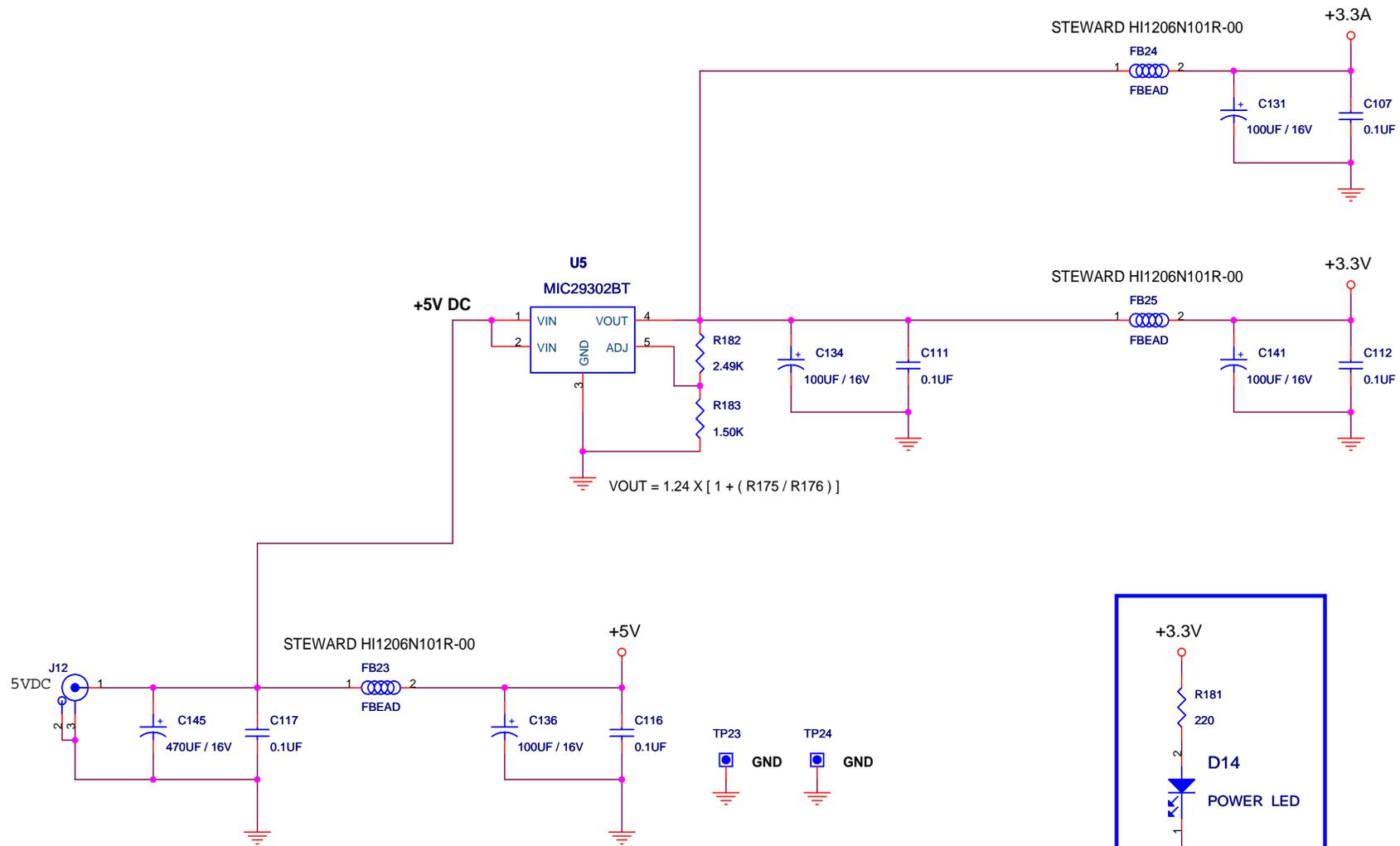


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File	KSZ8873FLL Reference Design	
Size	Document Number	Rev
	Device Config/Strap and MII Interface	1.0
Date:	Tuesday, October 06, 2009	Sheet 3 of 4



CONFIDENTIAL & PROPRIETARY



Title		
KSZ8873FLL Reference Design		
Size	Document Number	Rev
	Power	1.0
Date:	Thursday, May 28, 2009	Sheet 5 of 5