Application Note
KSZ8873/63 MLL Demo Board
Current Consumption

Introduction

This application note provides the procedure required to measure the power of the 8873/63MLL in 4 modes of operation using the KSZ8873/63/MLL/FLL/RLL Demo board. The numbers reported on the data sheet are typical numbers. The current numbers actually measured can vary up to +- 10% from those reported on the data sheet due to process variation. Also note that the data sheet numbers are at 25C and nominal voltage

These numbers are useful in creating a power budget and designing the power circuit

Operation and Measurement conditions

The KSZ8873/63MLL operates using 3 different voltage inputs as listed below:

- VDDIO can be 3.3, 2.5 or 1.8V (3.3V is used for this AN)
- VDDA_3.3 is the analog 3.3V input
- VDDC powers the internal digital core and must be 1.8V
- VDDA_1.8 is the analog 1.8 input

Note the part has one on board 1.8V regulator that can supply both 1.8V inputs. This regulator output is called VDDCO. All measurements assume the onboard regulator is used.

The tests below will describe the voltage measurement under 5 conditions

- 100BT running traffic on port 1, port 2 and port 3
- 10BT running traffic on port 1, port 2 and port 3
- Power saving mode
- Soft power down mode
- Energy Detect mode

See KSZ8873/63MLL_FLL_RLL data sheet for explanation of power modes

Test Equipment Required

- 8873/63MLL/FLL/RLL Evaluation board kit. Including Evaluation board populated with 8873/63MLL
- PC with USB port and Win2000/XP operating system
- Micrel Switch Configuration SW installed onto your PC
- USB cable
- 5 Volt power supply provided with Evaluation kit
- Fluke 173 Multi-meter or similar, need 2

General Setup

Figure 1 shows the overall setup. Figure 2 shows the power detail. Table 1 shows the jumper configurations.

Power to the part is isolated as 3.3V and 3.3A and is measured across JP 404 and 403 respectively.

Register setting are default except as otherwise noted below.

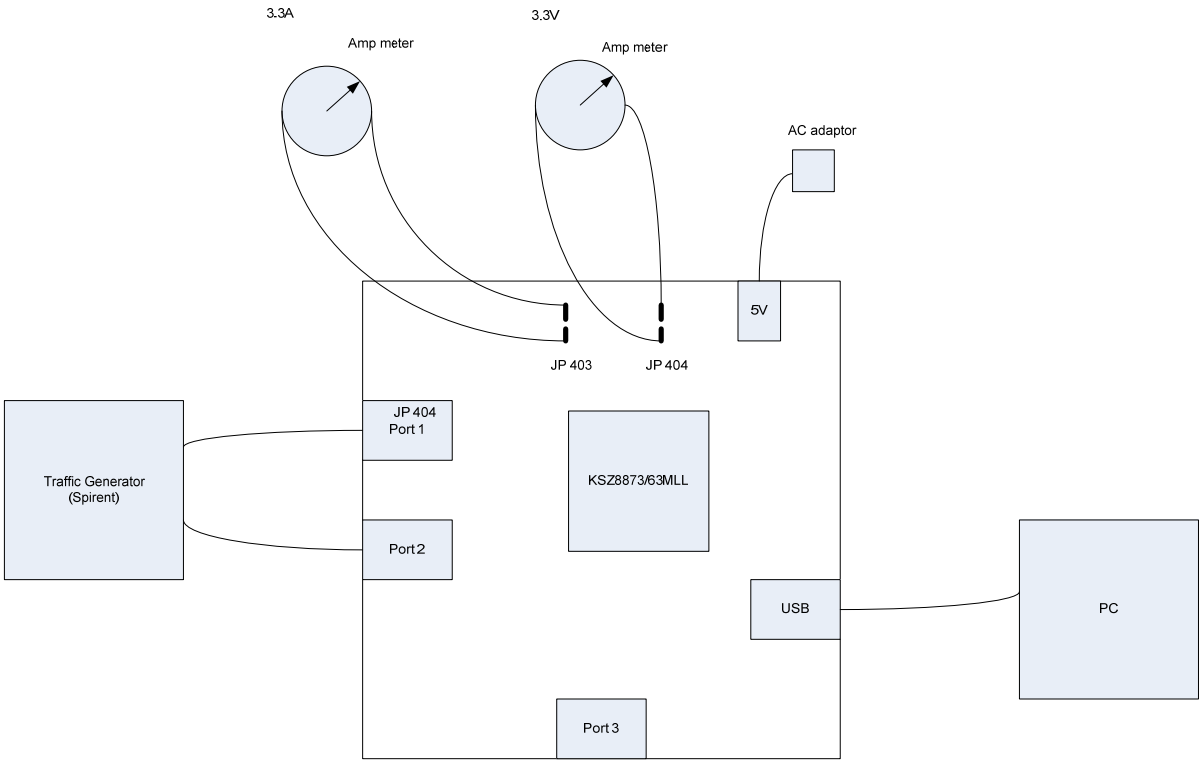

Figure 1. General Setup

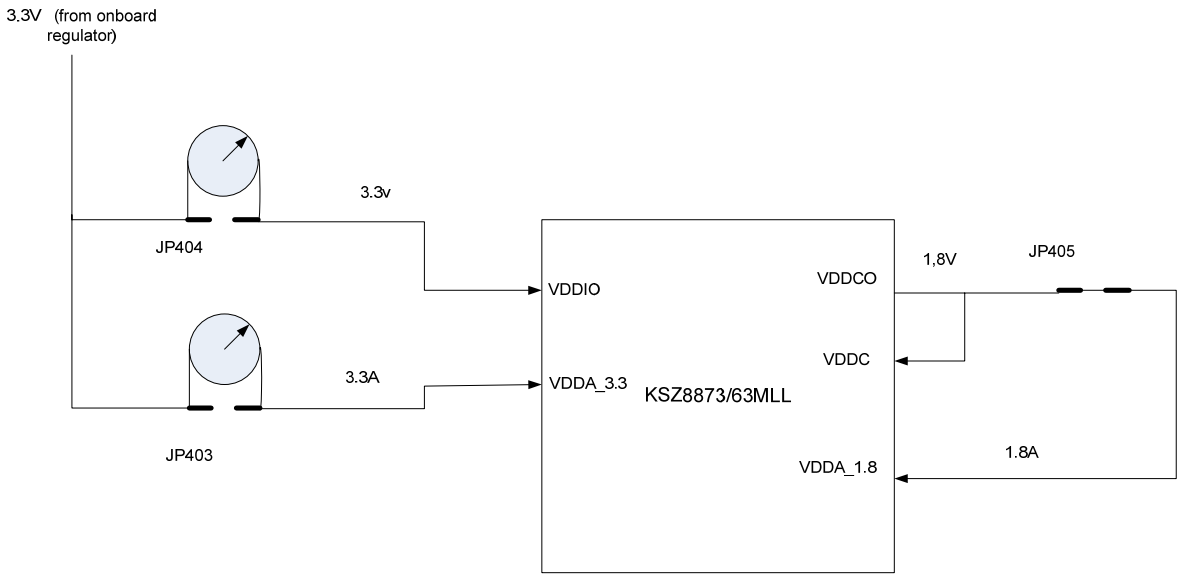

Figure 2. Power measurement detail

Jumper(JP)	Pin to	Pin	Comments
405	1	2	
40	1	2	
30	1	2	
12	4	3	
13	1	2	
26(Only for KSZ8873)	2	3	MII MAC mode
	1	2	MII PHY mode
34	1	2	
35	1	2	
21	1	2	
25	2	3	
5	1	1	
external	TP6	JP27-3	Need to tie TXEN low since non PHY tied to MII connector

Table 1. Jumper setting in Evaluation Board (All other jumper open except listed in the table)

Measurement in 100/10 Base TX all Ports Linked at 100% Line-Rate

Normal operating
Register 0xC3=0x00
MII in MAC mode (register 0x35 bit 7 =1)
Switch clock = 31.25MHz (register 0x0B bit [7:6] = [0,0])
CPU interface clock = 31.25MHz (register 0x0B bit [5:4] = [0,0])

1. Connect the Evaluation Board to the Smartbits as below

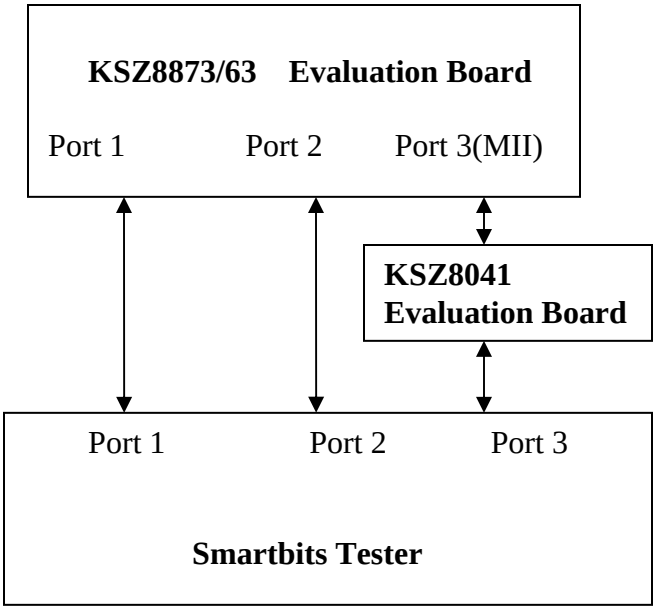

Figure 3. System connection

2. Set up the Smartbits as below:

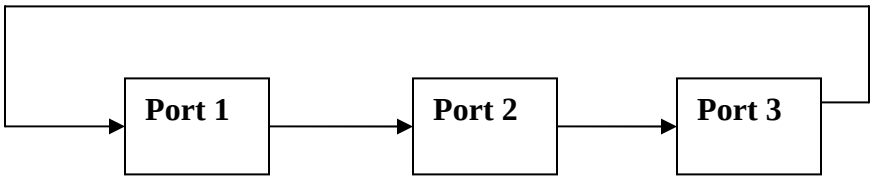

Figure 4. Smartbits setup

Transmit Mode: Single Burst 10,000
Data Length : Random
Load (IPG) : 100% (0.96uS)
Background : Random

3. Results:

	KSZ8863	**KSZ8873**
100 Base	**108mA (112mA in DS)**	**105mA (123mA in DS)**
10 Base	**78mA (92mA in DS)**	**78mA (88mA in DS)**

Measurement in Power Saving Mode

Register 0xC3=0x03
100BT with auto-negotiation enable
MII in MAC mode (register 0x35 bit 7 =1)
Switch clock = 31.25MHz (register 0x0B bit [7:6] = [0,0])
CPU interface clock = 31.25MHz (register 0x0B bit [5:4] = [0,0])

Results:

	KSZ8863	**KSZ8873**
No Cable on All ports	**84 mA (89mA in DS)**	**80mA (90mA in DS)**
Only port 1 connected	95 mA	89mA
Only port 2 connected	92 mA	89mA
Both port 1 and port 2 connected	105 mA	99mA

Measurement in Soft Power Down Mode

Register 0xC3 =0x02
Result:

KSZ8863	**KSZ8873**
8.7mA (6.2mA in DS)	**6.5mA (6.5mA in DS)**

Measurement in Energy Detect Mode

Register 0xC3=0x05
100BT with auto-negotiation enable
MII in **MAC mode** (register 0x35 bit 7 =1)
Switch clock = 31.25MHz (register 0x0B bit [7:6] = [0,0])
CPU interface clock = 31.25MHz (register 0x0B bit [5:4] = [0,0])

	KSZ8863			**KSZ8873**		
	Switch OFF(24s)	Switch ON(8s)	**Average**	Switch OFF(24s)	Switch ON(8s)	**Average**
No Cable on All ports	48 mA	66 mA	**53 mA**	44mA	62mA	**46mA**
Only port 1 connected	68 mA	87 mA	**73 mA**	62mA	80mA	**67mA**
Only port 2 connected	66 mA	84 mA	**71 mA**	63mA	81mA	**68mA**
Both port 1 and port 2 connected	84 mA	106 mA	**106 mA**	81mA	99mA	**86mA**

Register 0xC3=0x05
100BT with auto-negotiation enable
MII in **PHY mode** (register 0x35 bit 7 =0), SMTXER3 connect to HIGH

Switch clock = 31.25MHz (register 0x0B bit [7:6] = [0,0])
CPU interface clock = 31.25MHz (register 0x0B bit [5:4] = [0,0])

	KSZ8863	**KSZ8873**
	Switch is OFF(24s)/ON(8s)	Switch is OFF(24s)/ON(8s)
No Cable on All ports	17/69mA (Off/On) **30mA(average)** **(42mA in DS)**	10/63mA (Off/On) **24mA(Average)** **(35mA in DS)**
Only port 1 connected	92mA	85mA
Only port 2 connected	89mA	86mA
Both port 1 and port 2 connected	110mA	104mA