KSZ8873 Rev.A2 Errata Sheet

Dear Customer,

The following is the errata for the currently sampling KSZ8873, 3-Port Switch family. The following issues currently exhibited on the Revision-A2 silicon.

Item	Symptom	Comment	Solution/Workaround
1	**LinkMD not working in the Port 1**	Can not get the right LinkMD status in the register.	Will be fixed in next revision
2	**The rate will be double with tag insertion**	In the egress port rate limiting with tag insertion, the rate will be double	Will be fixed in next revision
3	**MDC/MDIO can't write MIIM register 0 bit 8, 12, 13**	Those bits are reserved in current datasheet.	Will be fixed in next revision
4	**RMII transmit timing is out of max delay time specification in the KSZ8873RLL**	The data delay time is 18ns, it is doesn't affect to transfer data on RMII	Will be fixed in next revision
5	**Upon reset or warm reset, the start switch bit in Register 1 is cleared to '0' in I2C master mode.**	As the result, the switch doesn't work in the I2C master mode.	Workaround solution: Set Register 78 (0x4E) bit 0 = '1' when program the EEPROM. The I2C master mode will work fine.
6	**Port 1 Receiving Flow Control doesn't take effect when port 1 receives Pause frame.**	As the result, the port 1 still transmit normal packets when receive pause frame.	Workaround solution: Set Register 21 Port 1 Control 5 bit [7] = '1' (this is a reserved bit). Port 1 Receiving Flow Control will work fine.