25-W STEREO CLASS-D AUDIO POWER AMPLIFIER

FEATURES

- **25-W/ch into a 4-Ω Load from a 27-V Supply**
- **20-W/ch into a 4-Ω Load from a 24-V Supply**
- **Operates from 10 V to 30 V**
- **Efficient Class-D Operation Eliminates Need for Heat Sinks**
- **Four Selectable, Fixed-Gain Settings**
- **Internal Oscillator (No External Components Required)**
- **Single-Ended Analog Inputs**
- **Thermal and Short-Circuit Protection With Auto Recovery**
- **Space-Saving Surface-Mount 24-Pin TSSOP Package**

APPLICATIONS

- **Televisions**

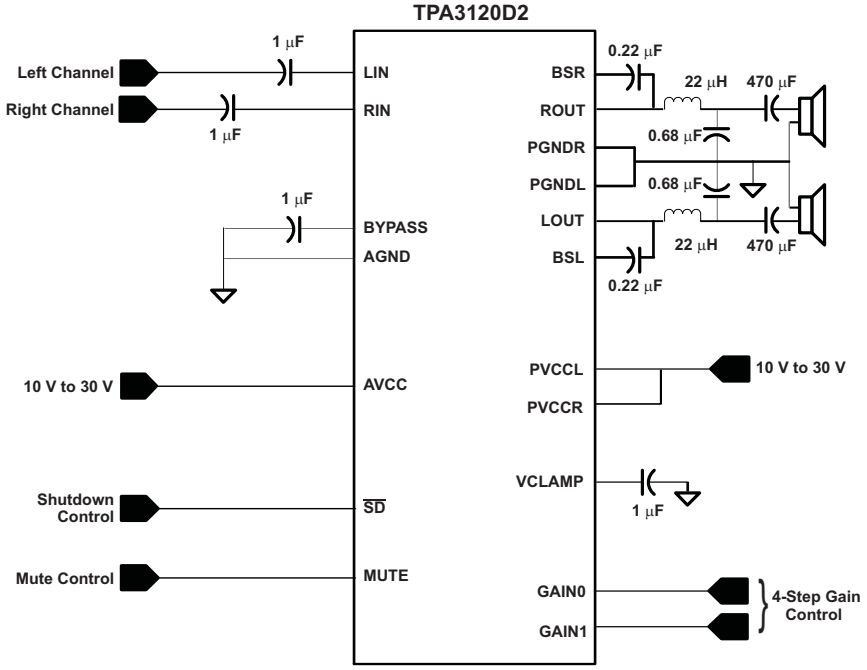
DESCRIPTION

The TPA3120D2 is a 25-W (per channel) efficient, Class-D audio power amplifier for driving stereo speakers in a single-ended configuration or a mono bridge-tied speaker. The TPA3120D2 can drive stereo speakers as low as 4 Ω. The efficiency of the TPA3120D2 eliminates the need for an external heat sink when playing music.

The gain of the amplifier is controlled by two gain select pins. The gain selections are 20, 26, 32, 36 dB.

The patented start-up and shut-down sequences minimize *pop* noise in the speakers without additional circuitry.

SIMPLIFIED APPLICATION CIRCUIT



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

PWP (TSSOP) PACKAGE
(TOP VIEW)

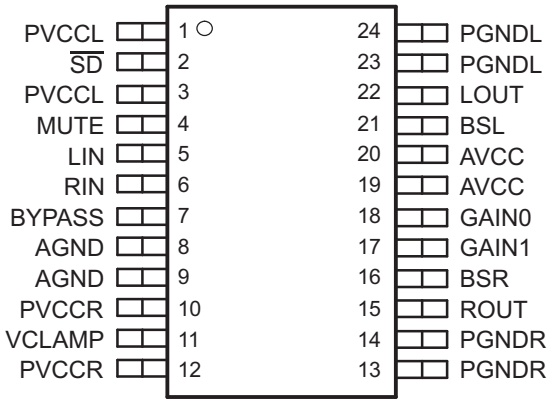


Table 1. TERMINAL FUNCTIONS

TERMINAL		I/O/P	DESCRIPTION
NAME	24-PIN (PWP)		
$\overline{SD}$	2	I	Shutdown signal for IC (low = disabled, high = operational). TTL logic levels with compliance to AVCC
RIN	6	I	Audio input for right channel
LIN	5	I	Audio input for left channel
GAIN0	18	I	Gain select least-significant bit. TTL logic levels with compliance to AVCC
GAIN1	17	I	Gain select most-significant bit. TTL logic levels with compliance to AVCC
MUTE	4	I	Mute signal for quick disable/enable of outputs (high = outputs switch at 50% duty cycle, low = outputs enabled). TTL logic levels with compliance to AVCC
BSL	21	I/O	Bootstrap I/O for left channel
PVCCL	1, 3	P	Power supply for left-channel H-bridge, not internally connected to PVCCR or AVCC
LOUT	22	O	Class-D 1/2-H-bridge positive output for left channel
PGNDL	23, 24	P	Power ground for left-channel H-bridge
VCLAMP	11	P	Internally generated voltage supply for bootstrap capacitors
BSR	16	I/O	Bootstrap I/O for right channel
ROUT	15	O	Class-D 1/2-H-bridge negative output for right channel
PGNDR	13, 14	P	Power ground for right-channel H-bridge.
PVCCR	10, 12	P	Power supply for right-channel H-bridge, not connected to PVCCL or AVCC
AGND	9	P	Analog ground for digital/analog cells in core
AGND	8	P	Analog ground for analog cells in core
BYPASS	7	O	Reference for preamplifier inputs. Nominally equal to AVCC/8. Also controls start-up time via external capacitor sizing.
AVCC	19, 20	P	High-voltage analog power supply. Not internally connected to PVCCR or PVCCL
Thermal pad	Die pad	P	Connect to ground. Thermal pad should be soldered down on all applications to secure the device properly to the printed wiring board.

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ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) (1)

			VALUE	UNIT
V_{CC}	Supply voltage	AVCC, PVCC	–0.3 to 36	V
V_I	Logic input voltage	$\overline{SD}$, MUTE, GAIN0, GAIN1	–0.3 to V_{CC} + 0.3	V
V_{IN}	Analog input voltage	RIN, LIN	–0.3 to 7	V
	Continuous total power dissipation		See *Dissipation Ratings* table	
T_A	Operating free-air temperature range		–40 to 85	°C
T_J	Operating junction temperature range		–40 to 150	°C
T_{stg}	Storage temperature range		–65 to 150	°C
R_L	Load resistance (minimum value)		3.2	Ω
ESD	Electrostatic Discharge	Human-body model (all pins)	± 2	kV
		Charged-device model (all pins)	± 500	V

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operations of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATINGS

PACKAGE(1)(2)	$T_A \le 25°C$	DERATING FACTOR	$T_A = 70°C$	$T_A = 85°C$
24-pin TSSOP	4.16 W	33.3 mW/°C	2.67 W	2.16 W

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
(2) This data was taken using 1 oz trace and copper pad that is soldered directly to a JEDEC standard high-k PCB. The thermal pad must be soldered to a thermal land on the printed-circuit board. See the *PowerPAD Thermally Enhanced Package* application note (SLMA002).

RECOMMENDED OPERATING CONDITIONS

			MIN	MAX	UNIT
V_{CC}	Supply voltage	PVCC, AVCC	10	30	V
V_{IH}	High-level input voltage	$\overline{SD}$, MUTE, GAIN0, GAIN1	2		V
V_{IL}	Low-level input voltage	$\overline{SD}$, MUTE, GAIN0, GAIN1		0.8	V
I_{IH}	High-level input current	$\overline{SD}$, $V_I = V_{CC}$, V_{CC} = 30 V		125	μA
		MUTE, $V_I = V_{CC}$, V_{CC} = 30 V		125	
		GAIN0, GAIN1, $V_I = V_{CC}$, V_{CC} = 24 V		125	
I_{IL}	Low-level input current	$\overline{SD}$, V_I = 0, V_{CC} = 30 V		1	μA
		MUTE, V_I = 0 V, V_{CC} = 30 V		1	
		GAIN0, GAIN1, V_I = 0 V, V_{CC} = 24 V		1	
T_A	Operating free-air temperature		–40	85	°C

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DC CHARACTERISTICS

T_A = 25°C, V_{CC} = 24 V, R_L = 4 Ω (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
| V_{OS} |	Class-D output offset voltage (measured differentially in BTL mode as shown in Fig 30)	V_I = 0 V, A_V = 36 dB			7.5	50	mV
$V_{(BYPASS)}$	Bypass output voltage	No load			AVCC/8		V
$I_{CC(q)}$	Quiescent supply current	$\overline{SD}$ = 2 V, MUTE = 0 V, No load			23	37	mA
$I_{CC(q)}$	Quiescent supply current in mute mode	MUTE = 0.8 V, No load			23		mA
$I_{CC(q)}$	Quiescent supply current in shutdown mode	$\overline{SD}$ = 0.8 V , No load			0.39	1	mA
$r_{DS(on)}$	Drain-source on-state resistance				200		mΩ
G	Gain	GAIN1 = 0.8 V	GAIN0 = 0.8 V	18	20	22	dB
			GAIN0 = 2 V	24	26	28	
		GAIN = 2 V	GAIN0 = 0.8 V	30	32	34	
			GAIN0 = 2 V	34	36	38	
	Mute Attenuation	V_I = 1Vrms			–82		dB

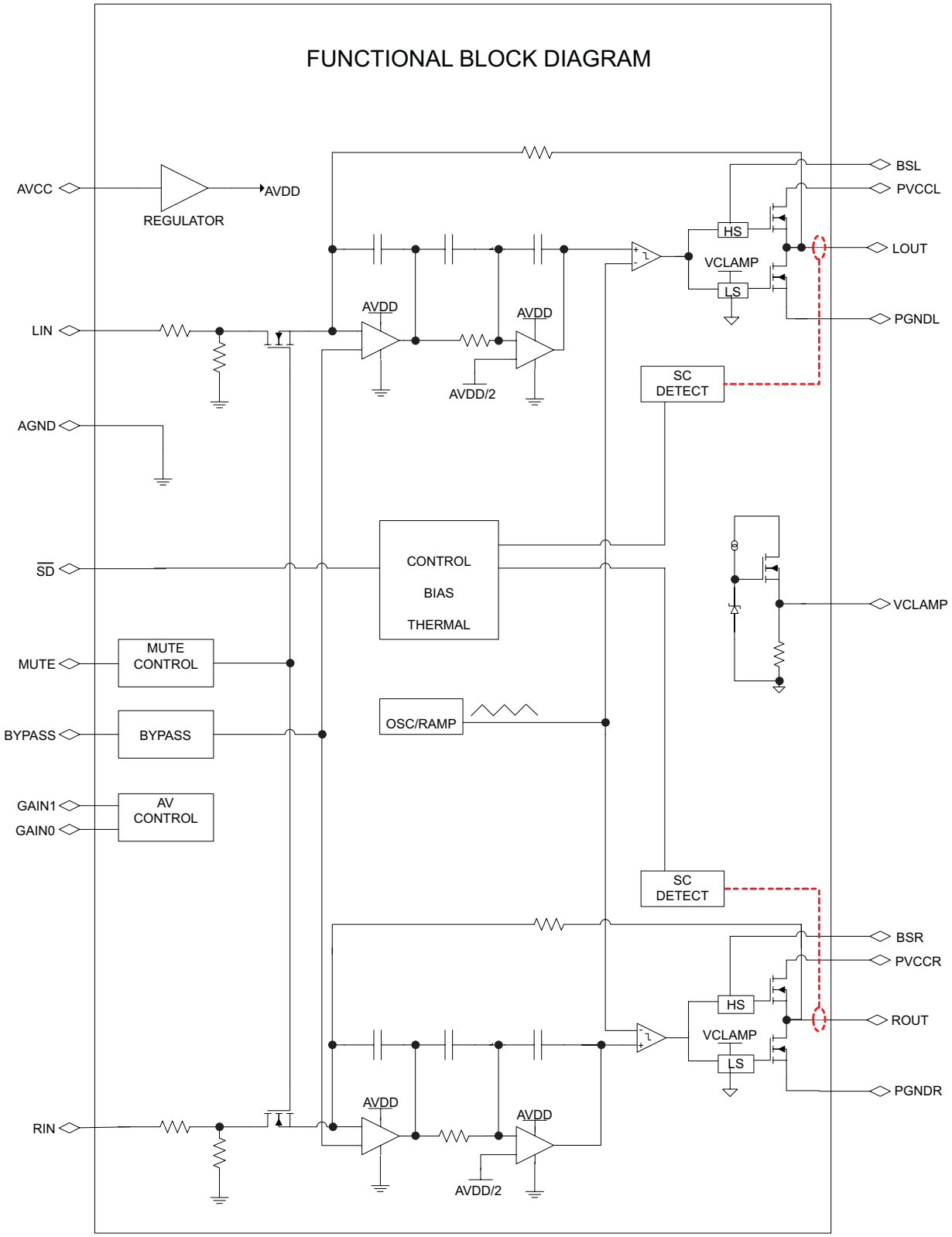
AC CHARACTERISTICS

T_A = 25°C, V_{CC} = 24 V, R_L = 4Ω (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
ksvr	Supply ripple rejection	V_{CC} = 24, V_{ripple} = 200 mV_{PP} Gain = 20 dB	100 Hz		–48		dB
			1 kHz		–52		
P_O	Output power at 1% THD+N	V_{CC} = 24 V, R_L = 4 Ω, f = 1 kHz			16		W
		V_{CC} = 24 V, R_L = 8 Ω, f = 1 kHz			8		
	Output power at 10% THD+N	V_{CC}= 24 V, R_L = 4 Ω, f = 1 kHz			20		
		V_{CC} = 24 V, R_L = 8 Ω, f = 1 kHz			10		
THD+N	Total harmonic distortion + noise	R_L = 4 Ω, f = 1 kHz, P_O = 10 W			0.08%		
		R_L = 8 Ω, f = 1 kHz, P_O = 5 W			0.08%		
V_n	Output integrated noise floor	20 Hz to 22 kHz, A-weighted filter, Gain = 20 dB			85		μV
					–80		dBV
	Crosstalk	P_O = 1 W, f = 1 kHz; Gain = 20 dB			–60		dB
SNR	Signal-to-noise ratio	Max output at THD+N < 1%, f = 1 kHz, Gain = 20 dB			99		dB
	Thermal trip point				150		°C
	Thermal hysteresis				30		°C
f_{OSC}	Oscillator frequency			230	250	270	kHz

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FUNCTIONAL BLOCK DIAGRAM



TYPICAL CHARACTERISTICS

All tests are made at frequency = 1 kHz unless otherwise noted.

TOTAL HARMONIC DISTORTION + NOISE
vs
FREQUENCY

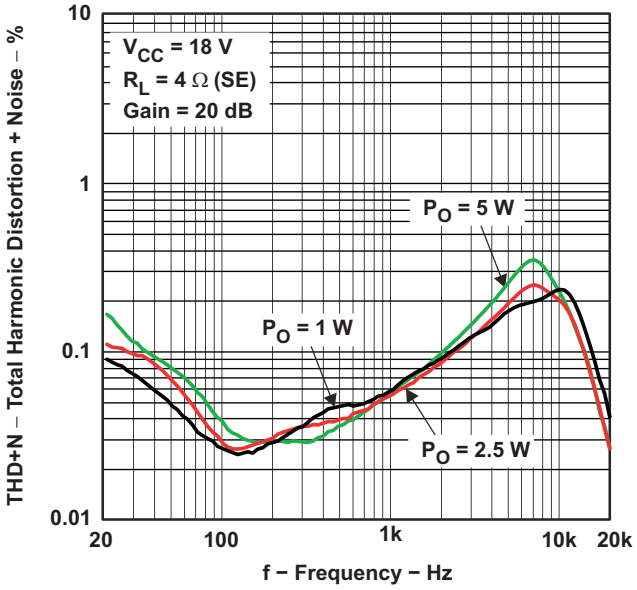


Figure 1.

TOTAL HARMONIC DISTORTION + NOISE
vs
FREQUENCY

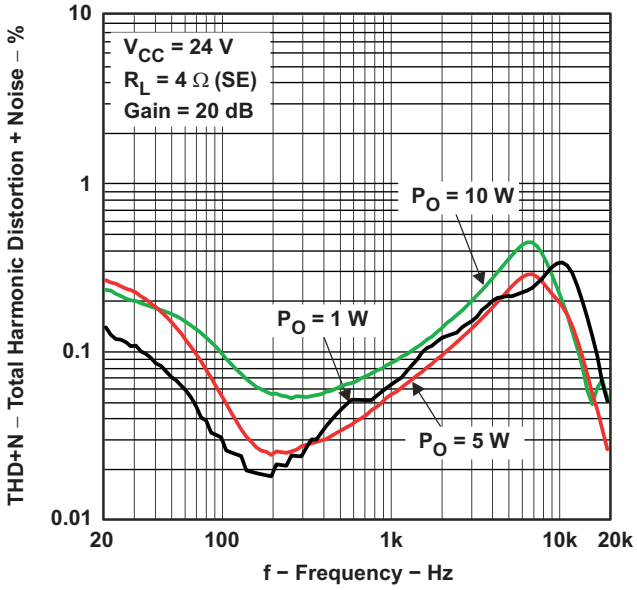


Figure 2.

TOTAL HARMONIC DISTORTION + NOISE
vs
FREQUENCY

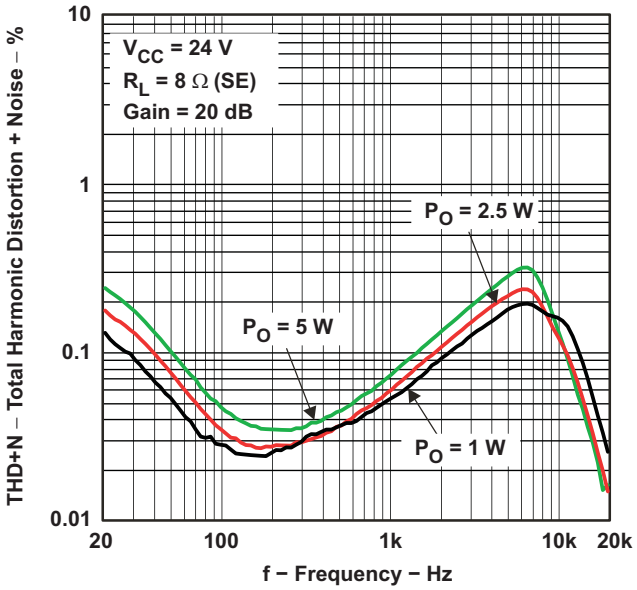


Figure 3.

TOTAL HARMONIC DISTORTION + NOISE
vs
OUTPUT POWER

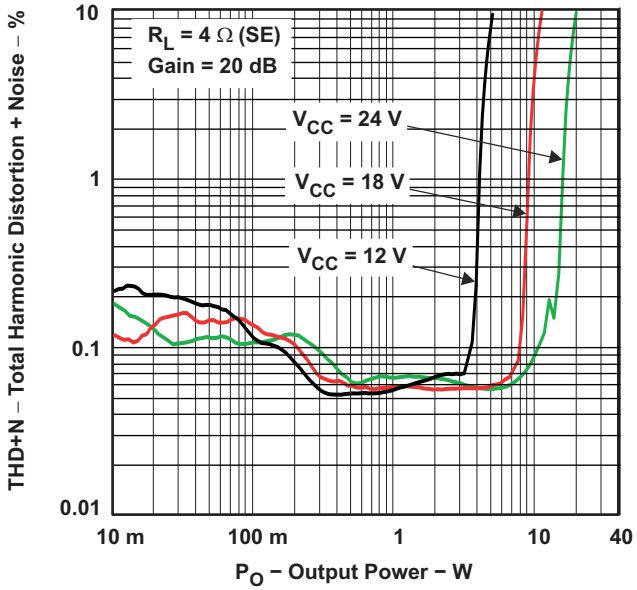


Figure 4.

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TYPICAL CHARACTERISTICS (continued)

All tests are made at frequency = 1 kHz unless otherwise noted.

TOTAL HARMONIC DISTORTION + NOISE
vs
OUTPUT POWER

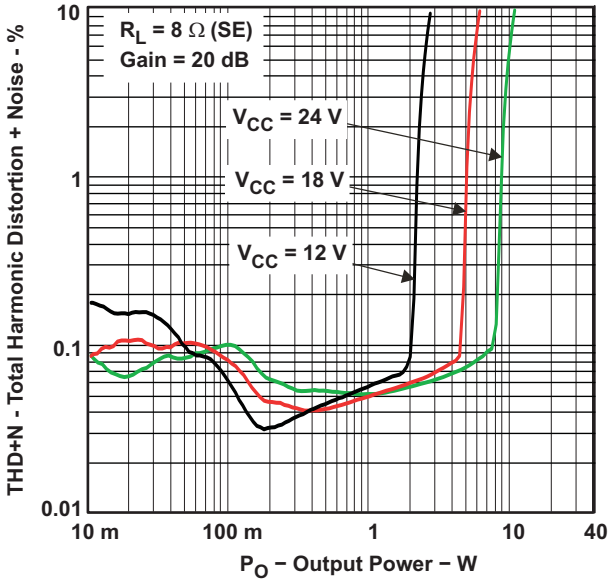


Figure 5.

CROSSTALK
vs
FREQUENCY

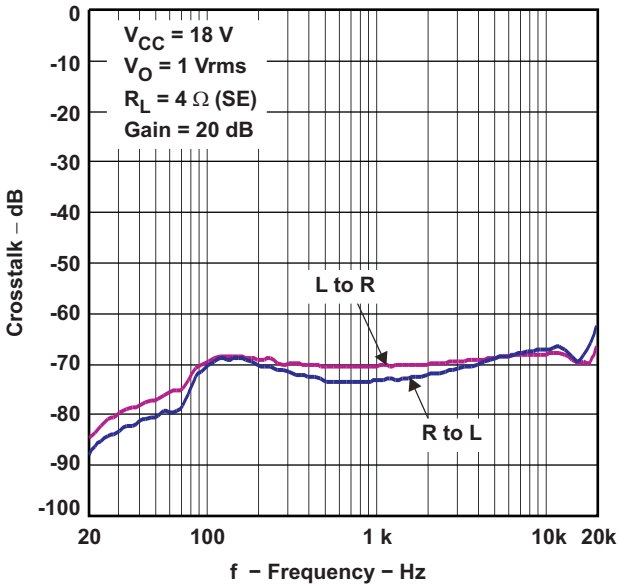


Figure 6.

CROSSTALK
vs
FREQUENCY

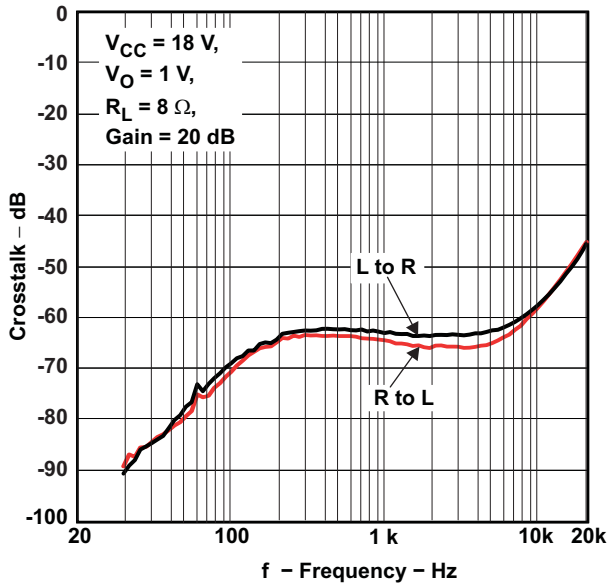


Figure 7.

GAIN/PHASE
vs
FREQUENCY

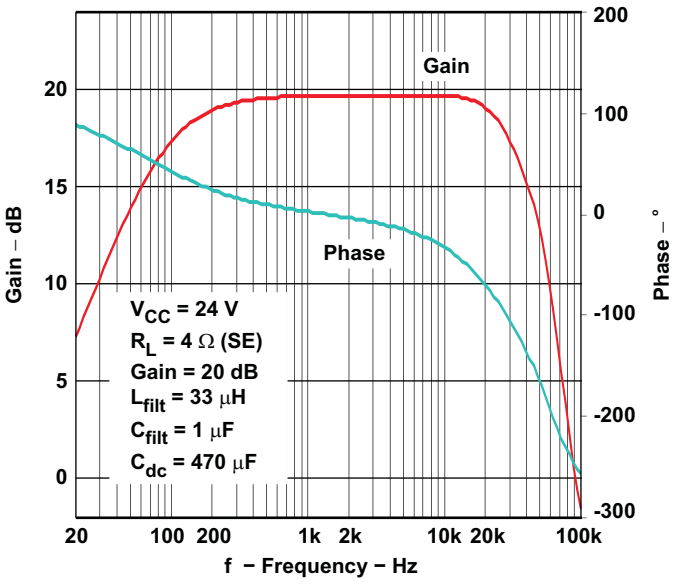


Figure 8.

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TYPICAL CHARACTERISTICS (continued)

All tests are made at frequency = 1 kHz unless otherwise noted.

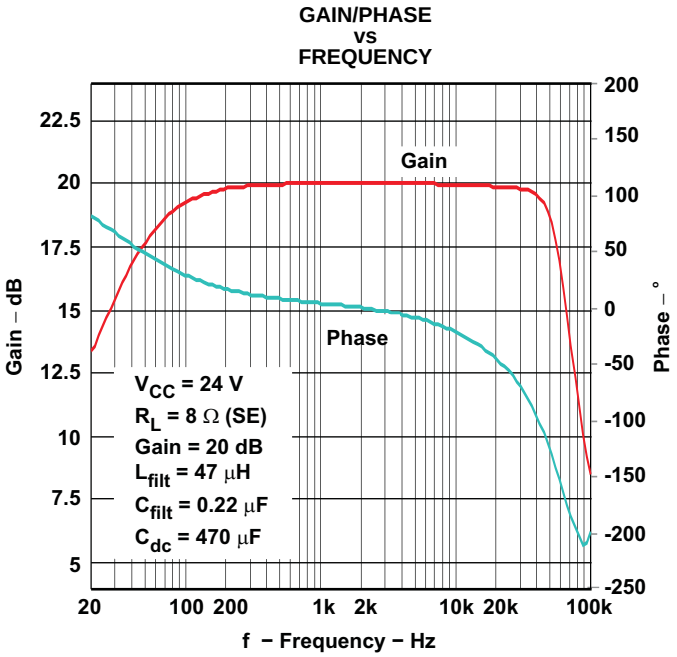
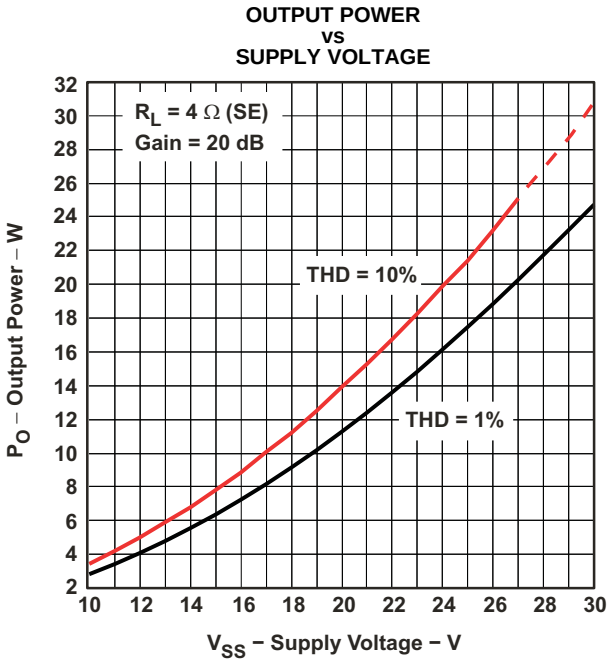


Figure 9.



A. Dashed line represents thermally limited region.

Figure 10.

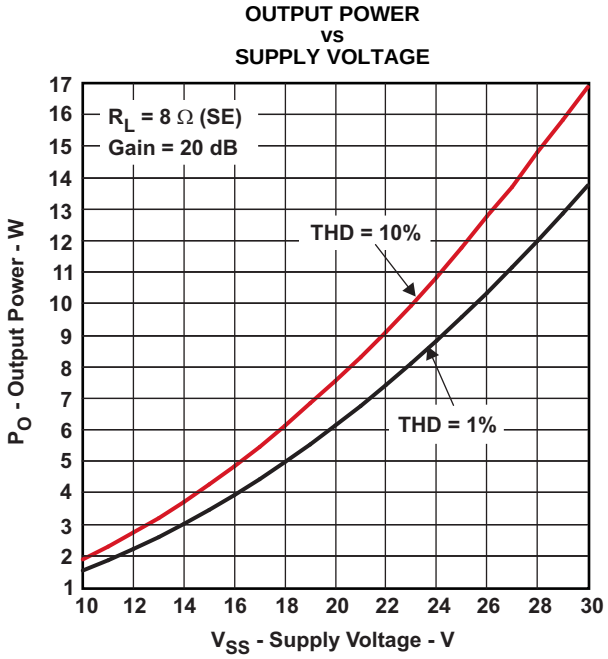


Figure 11.

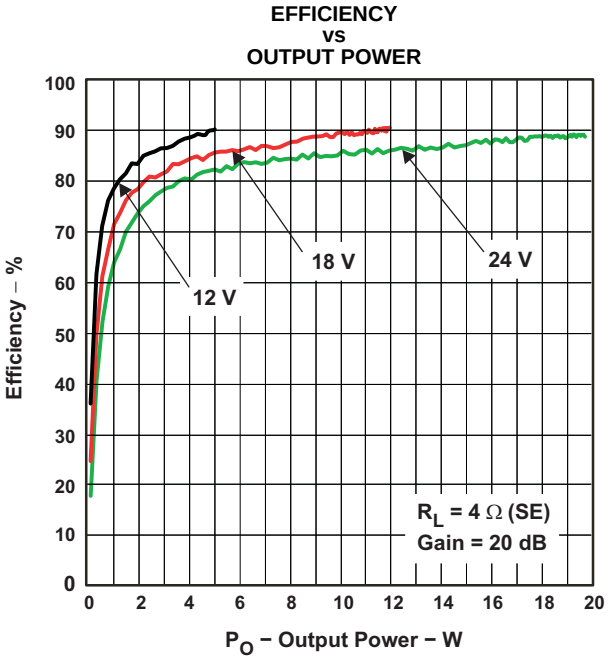


Figure 12.

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TYPICAL CHARACTERISTICS (continued)

All tests are made at frequency = 1 kHz unless otherwise noted.

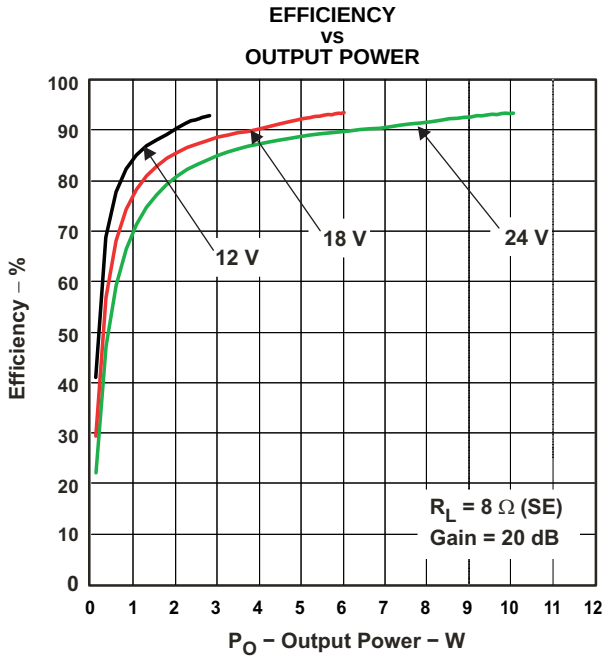


Figure 13.

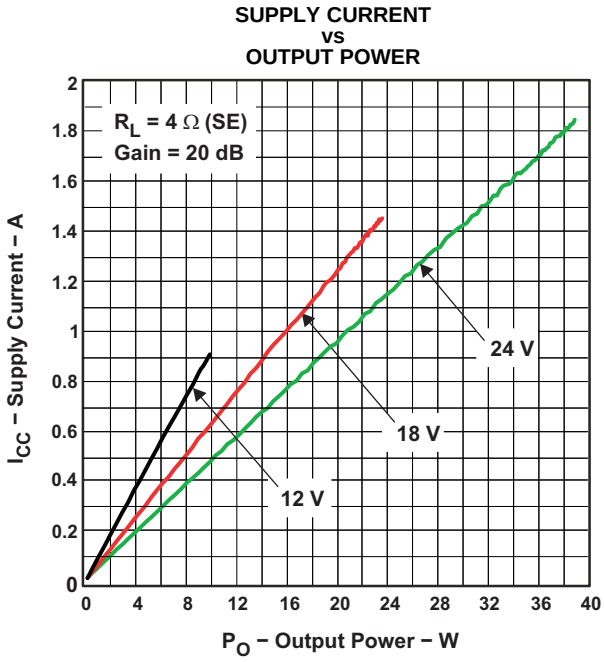


Figure 14.

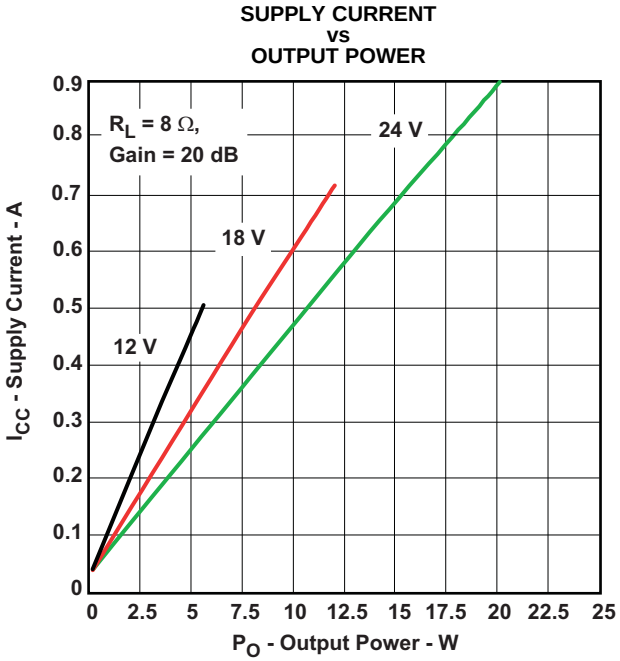


Figure 15.

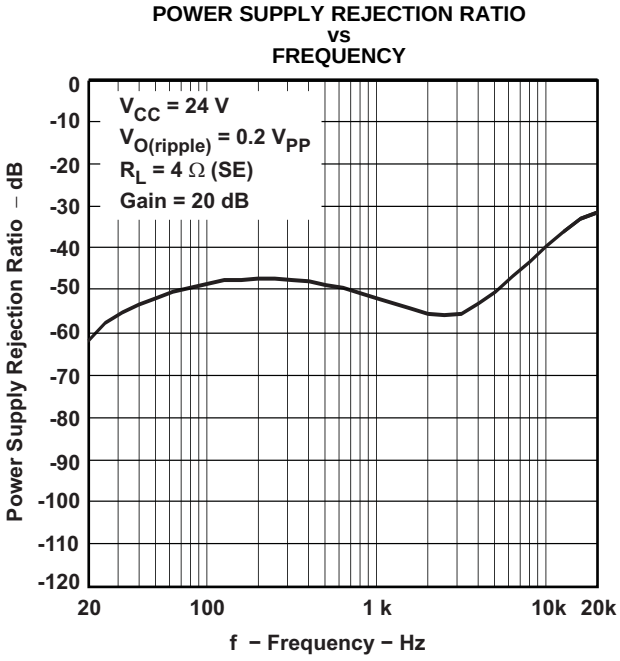


Figure 16.

TYPICAL CHARACTERISTICS (continued)

All tests are made at frequency = 1 kHz unless otherwise noted.

TOTAL HARMONIC DISTORTION + NOISE
vs
FREQUENCY

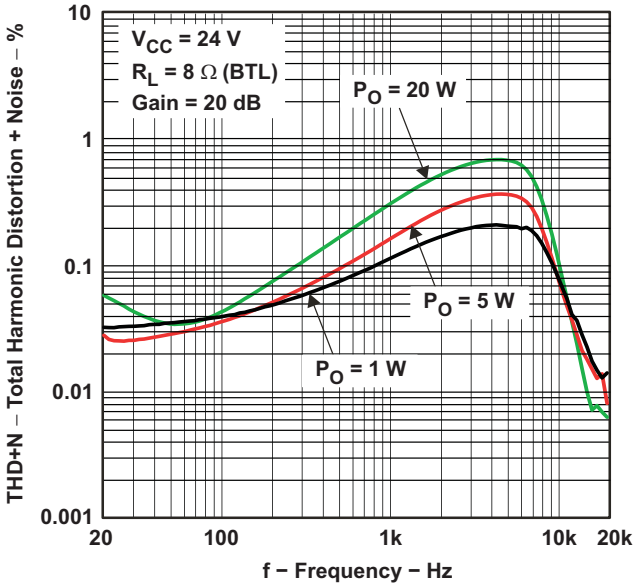


Figure 17.

TOTAL HARMONIC DISTORTION + NOISE
vs
OUTPUT POWER

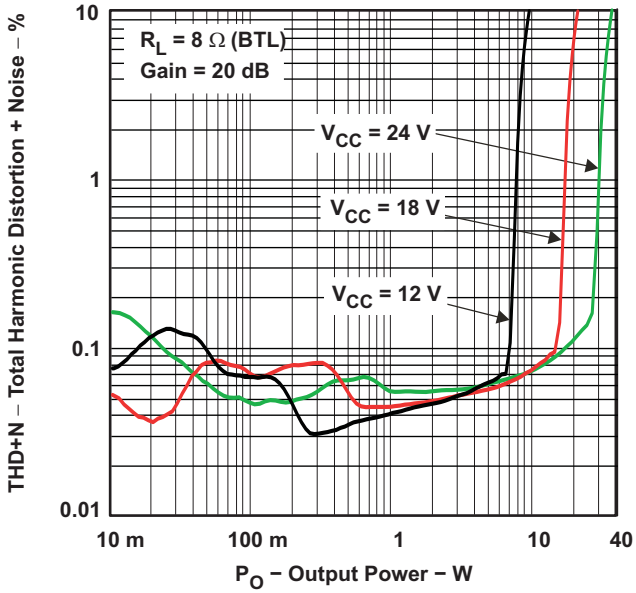


Figure 18.

GAIN/PHASE
vs
FREQUENCY

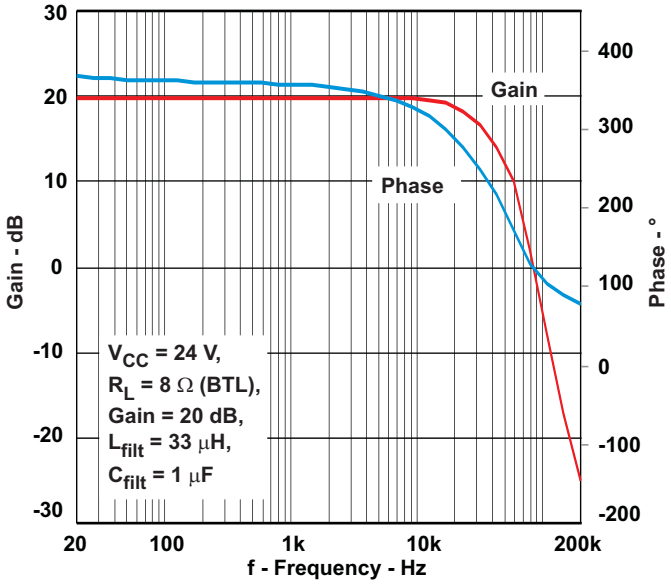
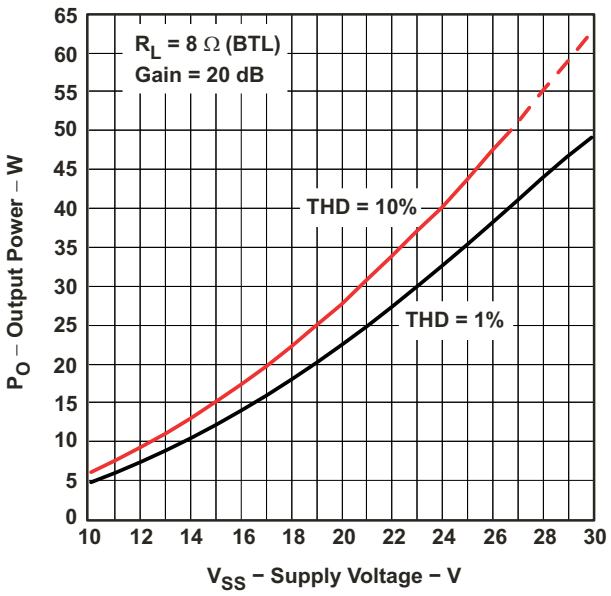


Figure 19.

OUTPUT POWER
vs
SUPPLY VOLTAGE



A. Dashed line represents thermally limited region.

Figure 20.

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TYPICAL CHARACTERISTICS (continued)

All tests are made at frequency = 1 kHz unless otherwise noted.

EFFICIENCY vs OUTPUT POWER

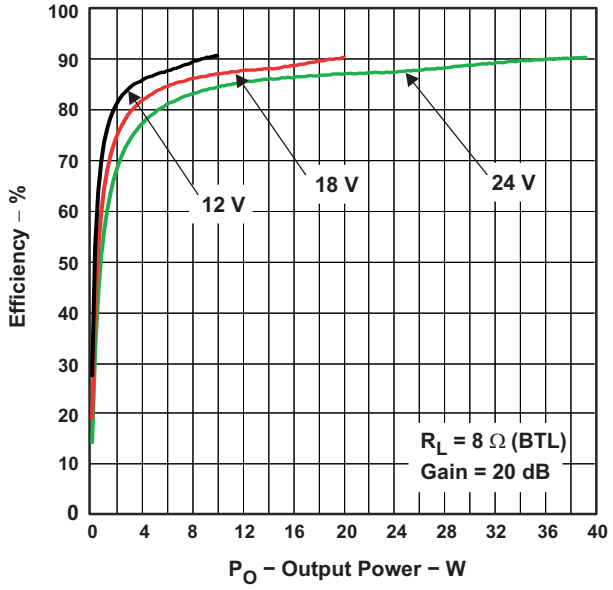


Figure 21.

POWER SUPPLY REJECTION RATIO vs FREQUENCY

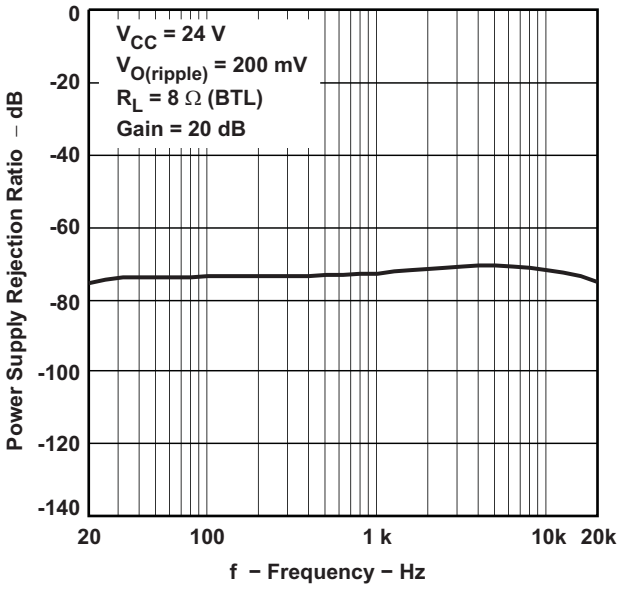


Figure 22.

APPLICATION INFORMATION

CLASS-D OPERATION

This section focuses on the class-D operation of the TPA3120D2.

Traditional Class-D Modulation Scheme

The TPA3120D2 operates in AD mode. There are two main configurations that may be used. For stereo operation, the TPA3120D2 should be configured in a single-ended (SE) half-bridge amplifier. For mono applications, TPA3120D2 may be used as a bridge-tied-load (BTL) amplifier. The traditional class-D modulation scheme, which is used in the TPA3120D2 BTL configuration, has a differential output where each output is 180 degrees out of phase and changes from ground to the supply voltage, V_{CC}. Therefore, the differential prefiltered output varies between positive and negative V_{CC}, where filtered 50% duty cycle yields 0 V across the load. The class-D modulation scheme with voltage and current waveforms is shown in Figure 23 and Figure 24.

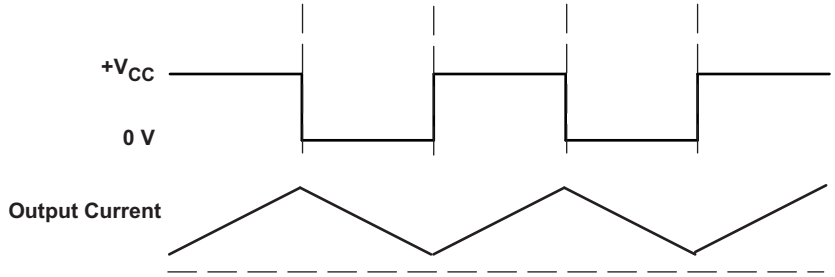


Figure 23. Class-D Modulation for TPA3120D2 SE Configuration

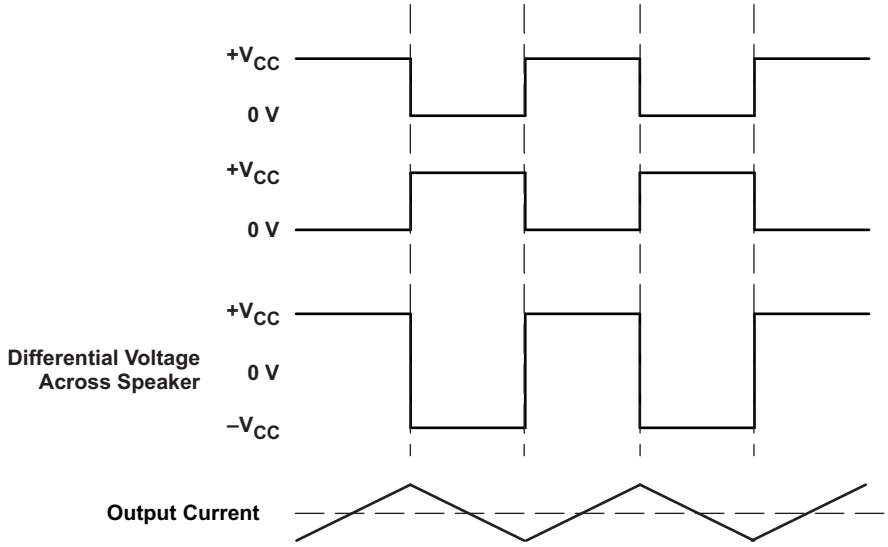


Figure 24. Class-D Modulation for TPA3120D2 BTL Configuration

Supply Pumping

One issue encountered in single-ended (SE) class-D amplifier designs is supply pumping. Power-supply pumping is a rise in the local supply voltage due to energy being driven back to the supply by operation of the class-D amplifier. This phenomenon is most evident at low audio frequencies and when both channels are operating at the same frequency and phase. At low levels, power-supply pumping results in distortion in the audio output due to fluctuations in supply voltage. At higher levels, pumping can cause the overvoltage protection to operate, which temporarily shuts down the audio output.

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Several things can be done to relieve power-supply pumping. The lowest impact is to operate the two inputs out of phase 180° and reverse the speaker connections. Because most audio is highly correlated, this causes the supply pumping to be out of phase and not as severe. If this is not enough, the amount of bulk capacitance on the supply must be increased. Also, improvement is realized by hooking other supplies to this node, thereby, sinking some of the excess current. Power-supply pumping should be tested by operating the amplifier at low frequencies and high output levels.

Gain Setting via GAIN0 and GAIN1 Inputs

The gain of the TPA3120D2 is set by two input terminals, GAIN0 and GAIN1.

The gains listed in Table 2 are realized by changing the taps on the input resistors and feedback resistors inside the amplifier. This causes the input impedance (Z_i) to be dependent on the gain setting. The actual gain settings are controlled by ratios of resistors, so the gain variation from part-to-part is small. However, the input impedance from part-to-part at the same gain may shift by ±20% due to shifts in the actual resistance of the input resistors.

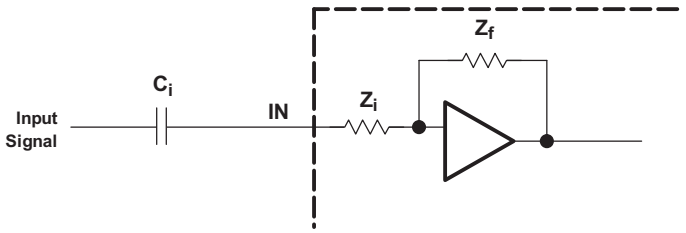
For design purposes, the input network (discussed in the next section) should be designed assuming an input impedance of 8 kΩ, which is the absolute minimum input impedance of the TPA3120D2. At the higher gain settings, the input impedance could increase as high as 72 kΩ.

Table 2. Gain Setting

GAIN1	GAIN0	AMPLIFIER GAIN (dB), TYPICAL	INPUT IMPEDANCE (kΩ), TYPICAL
0	0	20	60
0	1	26	30
1	0	32	15
1	1	36	9

INPUT RESISTANCE

Changing the gain setting can vary the input resistance of the amplifier from its smallest value, 10 kΩ ±20%, to the largest value, 60 kΩ ±20%. As a result, if a single capacitor is used in the input high-pass filter, the –3-dB cutoff frequency may change when changing gain steps.



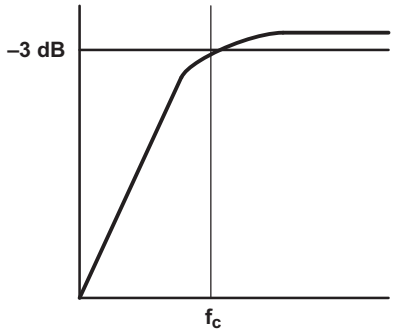
The –3-dB frequency can be calculated using Equation 1. Use the Z_i values given in Table 2.

$$f = \frac{1}{2\pi Z_i C_i} \quad (1)$$

INPUT CAPACITOR, C_i

In the typical application, an input capacitor (C_i) is required to allow the amplifier to bias the input signal to the proper dc level for optimum operation. In this case, C_i and the input impedance of the amplifier (Z_i) form a high-pass filter with the corner frequency determined in Equation 2.

$$f_c = \frac{1}{2\pi Z_i C_i} \quad (2)$$



The value of C_i is important, as it directly affects the bass (low-frequency) performance of the circuit. Consider the example where Z_i is 20 kΩ and the specification calls for a flat bass response down to 20 Hz. Equation 2 is reconfigured as Equation 3.

$$C_i = \frac{1}{2\pi Z_i f_c} \quad (3)$$

In this example, C_i is 0.4 µF; so, one would likely choose a value of 0.47 µF as this value is commonly used. If the gain is known and is constant, use Z_i from Table 2 to calculate C_i. A further consideration for this capacitor is the leakage path from the input source through the input network (C_i) and the feedback network to the load. This leakage current creates a dc offset voltage at the input to the amplifier that reduces useful headroom, especially in high-gain applications. For this reason, a low-leakage tantalum or ceramic capacitor is the best choice. When polarized capacitors are used, the positive side of the capacitor should face the amplifier input in most applications as the dc level there is held at 2 V, which is likely higher than the source dc level. Note that it is important to confirm the capacitor polarity in the application. Additionally, lead-free solder can create dc offset voltages, and it is important to ensure that boards are cleaned properly.

Single-Ended Output Capacitor, C_O

In single-ended (SE) applications, the dc blocking capacitor forms a high-pass filter with the speaker impedance. The frequency response rolls of with decreasing frequency at a rate of 20 dB/decade. The cutoff frequency is determined by

$$f_c = 1/2\pi C_O Z_L$$

Table 3 shows some common component values and the associated cutoff frequencies:

Table 3. Common Filter Responses

Speaker Impedance (Ω)	C_{SE} – DC Blocking Capacitor (µF)		
	f_c = 60 Hz (–3 dB)	f_c = 40 Hz (–3 dB)	f_c = 20 Hz (–3 dB)
4	680	1000	2200
8	330	470	1000

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Output Filter and Frequency Response

For the best frequency response, a flat-passband output filter (second-order Butterworth) may be used. The output filter components consist of the series inductor and capacitor to ground at the LOUT and ROUT pins. There are several possible configurations, depending on the speaker impedance and whether the output configuration is single-ended (SE) or bridge-tied load (BTL). Table 4 lists the recommended values for the filter components. It is important to use a high-quality capacitor in this application. A rating of at least X7R is required.

Table 4. Recommended Filter Output Components

Output Configuration	Speaker Impedance (Ω)	Filter Inductor (µH)	Filter Capacitor (nF)
Single Ended (SE)	4	22	680
	8	47	390
Bridge Tied Load (BTL)	4	10	1500
	8	22	680

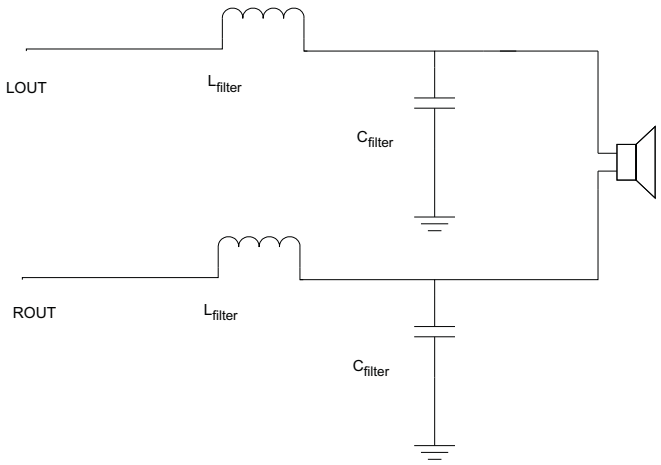


Figure 25. BTL Filter Configuration

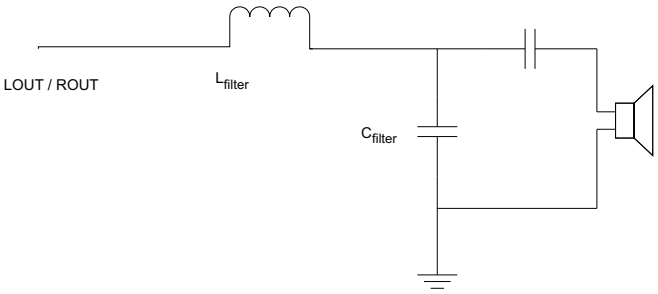


Figure 26. SE Filter Configuration

Power-Supply Decoupling, C_S

The TPA3120D2 is a high-performance CMOS audio amplifier that requires adequate power-supply decoupling to ensure that the output total harmonic distortion (THD) is as low as possible. Power-supply decoupling also prevents oscillations for long lead lengths between the amplifier and the speaker. The optimum decoupling is achieved by using two capacitors of different types that target different types of noise on the power-supply leads. For higher-frequency transients, spikes, or digital hash on the line, a good low equivalent-series-resistance (ESR) ceramic capacitor, typically 0.1 µF to 1 µF, placed as close as possible to the device V_{CC} lead works best. For filtering lower frequency noise signals, a larger aluminum electrolytic capacitor of 470 µF or greater placed near the audio power amplifier is recommended. The 470-µF capacitor also serves as local storage capacitor for supplying current during large signal transients on the amplifier outputs. The PVCC terminals provide the power to the output transistors, so a 470-µF or larger capacitor should be placed on each PVCC terminal. A 10-µF capacitor on the AVCC terminal is adequate. These capacitors must be properly derated for voltage and ripple-current rating to ensure reliability.

BSN and BSP Capacitors

The half H-bridge output stages use only NMOS transistors. Therefore, they require bootstrap capacitors for the high side of each output to turn on correctly. A 220-nF ceramic capacitor, rated for at least 25 V, must be connected from each output to its corresponding bootstrap input. Specifically, one 220-nF capacitor must be connected from LOUT to BSL, and one 220-nF capacitor must be connected from ROUT to BSR.

The bootstrap capacitors connected between the BSx pins and their corresponding outputs function as a floating power supply for the high-side N-channel power MOSFET gate-drive circuitry. During each high-side switching cycle, the bootstrap capacitors hold the gate-to-source voltage high enough to keep the high-side MOSFETs turned on.

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VCLAMP Capacitor

To ensure that the maximum gate-to-source voltage for the NMOS output transistors is not exceeded, one internal regulator clamps the gate voltage. One 1-µF capacitor must be connected from VCLAMP (pin 11) to ground and must be rated for at least 16 V. The voltages at the VCLAMP terminal may vary with V_{CC} and may not be used for powering any other circuitry.

VBYP Capacitor Selection

The scaled supply reference (VBYP) nominally provides an AVCC/8 internal bias for the preamplifier stages. The external capacitor for this reference (C_{BYP}) is a critical component and serves several important functions. During start-up or recovery from shutdown mode, C_{BYP} determines the rate at which the amplifier starts. The start up time is proportional to 0.5 s per microfarad. Thus, the recommended 1-µF capacitor results in a start-up time of approximately 500 ms. The second function is to reduce noise produced by the power supply caused by coupling with the output drive signal. This noise could result in degraded power-supply rejection and THD+N.

The circuit is designed for a C_{BYP} value of 1 µF for best pop performance. The input capacitors should have the same value. A ceramic or tantalum low-ESR capacitor is recommended.

$\overline{\text{SHUTDOWN}}$ OPERATION

The TPA3120D2 employs a shutdown mode of operation designed to reduce supply current (I_{CC}) to the absolute minimum level during periods of nonuse for power conservation. The $\overline{\text{SHUTDOWN}}$ input terminal should be held high (see specification table for trip point) during normal operation when the amplifier is in use. Pulling $\overline{\text{SHUTDOWN}}$ low causes the outputs to mute and the amplifier to enter a low-current state. Never leave $\overline{\text{SHUTDOWN}}$ unconnected, because amplifier operation would be unpredictable.

For the best power-up *pop* performance, place the amplifier in the shutdown or mute mode prior to applying the power-supply voltage.

MUTE Operation

The MUTE pin is an input for controlling the output state of the TPA3120D2. A logic high on this terminal causes the outputs to run at a constant 50% duty cycle. A logic low on this pin enables the outputs. This terminal may be used as a quick disable/enable of outputs when changing channels on a television or transitioning between different audio sources.

The MUTE terminal should never be left floating. For power conservation, the $\overline{\text{SHUTDOWN}}$ terminal should be used to reduce the quiescent current to the absolute minimum level.

USING LOW-ESR CAPACITORS

Low-ESR capacitors are recommended throughout this application section. A real (as opposed to ideal) capacitor can be modeled simply as a resistor in series with an ideal capacitor. The voltage drop across this resistor minimizes the beneficial effects of the capacitor in the circuit. The lower the equivalent value of this resistance, the more the real capacitor behaves like an ideal capacitor.

SHORT-CIRCUIT PROTECTION

The TPA3120D2 has short-circuit protection circuitry on the outputs that prevents damage to the device during output-to-output shorts and output-to-GND shorts after the filter and output capacitor (at the speaker terminal.) Directly at the device terminals, the protection circuitry prevents damage to device during output-to-output, output-to-ground, and output-to-supply. When a short circuit is detected on the outputs, the part immediately disables the output drive. This is an unlatched fault. Normal operation is restored when the fault is removed.

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THERMAL PROTECTION

Thermal protection on the TPA3120D2 prevents damage to the device when the internal die temperature exceeds 150°C. There is a ±15°C tolerance on this trip point from device to device. Once the die temperature exceeds the thermal set point, the device enters into the shutdown state and the outputs are disabled. This is not a latched fault. The thermal fault is cleared once the temperature of the die is reduced by 30°C. The device begins normal operation at this point with no external system interaction.

PRINTED-CIRCUIT BOARD (PCB) LAYOUT

Because the TPA3120D2 is a class-D amplifier that switches at a high frequency, the layout of the printed-circuit board (PCB) should be optimized according to the following guidelines for the best possible performance.

- Decoupling capacitors—The high-frequency 0.1-µF decoupling capacitors should be placed as close to the PVCC (pins 1, 3, 10, and 12) and AVCC (pins 19 and 20) terminals as possible. The VBYP (pin 7) capacitor and VCLAMP (pin 11) capacitor should also be placed as close to the device as possible. Large (220-µF or greater) bulk power-supply decoupling capacitors should be placed near the TPA3120D2 on the PVCCL and PVCCR terminals.
- Grounding—The AVCC (pins 19 and 20) decoupling capacitor and VBYP (pin 7) capacitor should each be grounded to analog ground (AGND, pins 8 and 9). The PVCCx decoupling capacitors and VCLAMP capacitors should each be grounded to power ground (PGND, pins 13, 14, 23, and 24). Analog ground and power ground should be connected at the thermal pad, which should be used as a central ground connection or star ground for the TPA3120D2.
- Output filter—The reconstruction filter (L1, L2, C9, and C16) should be placed as close to the output terminals as possible for the best EMI performance. The capacitors should be grounded to power ground.
- Thermal pad—The thermal pad must be soldered to the PCB for proper thermal performance and optimal reliability. The dimensions of the thermal pad and thermal land are described in the mechanical section at the back of the data sheet. See TI Technical Briefs SLMA002 and SLOA120 for more information about using the thermal pad. For recommended PCB footprints, see figures at the end of this data sheet.

For an example layout, see the TPA3120D2 Evaluation Module (TPA3120D2EVM) User Manual, (SLOU189). Both the EVM user manual and the thermal pad application note are available on the TI Web site at http://www.ti.com.

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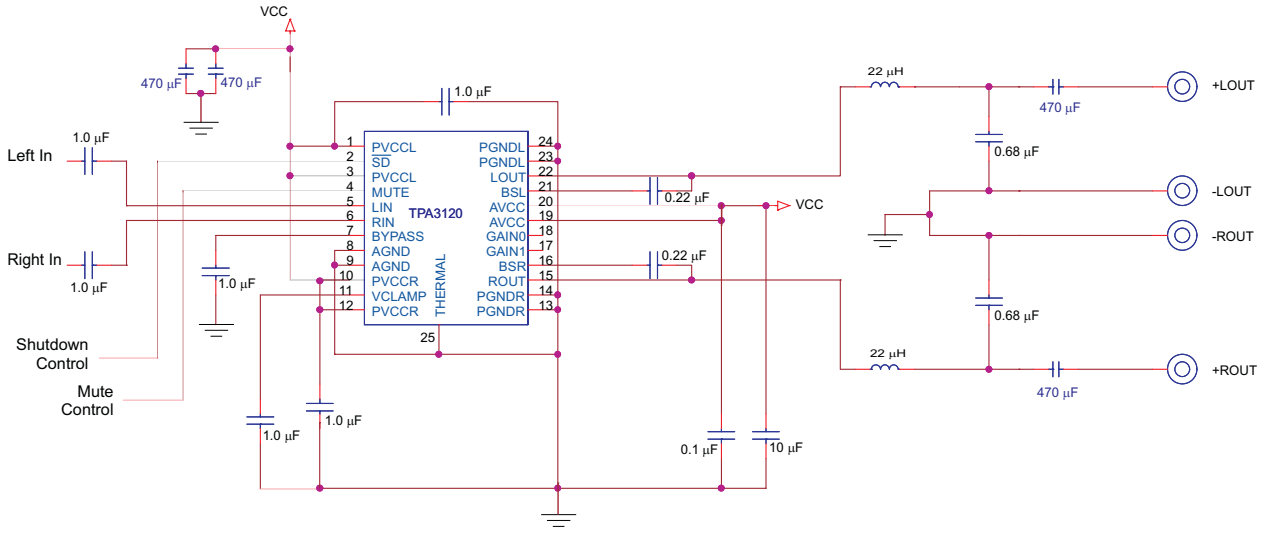


Figure 27. Schematic for Single-Ended (SE) Configuration

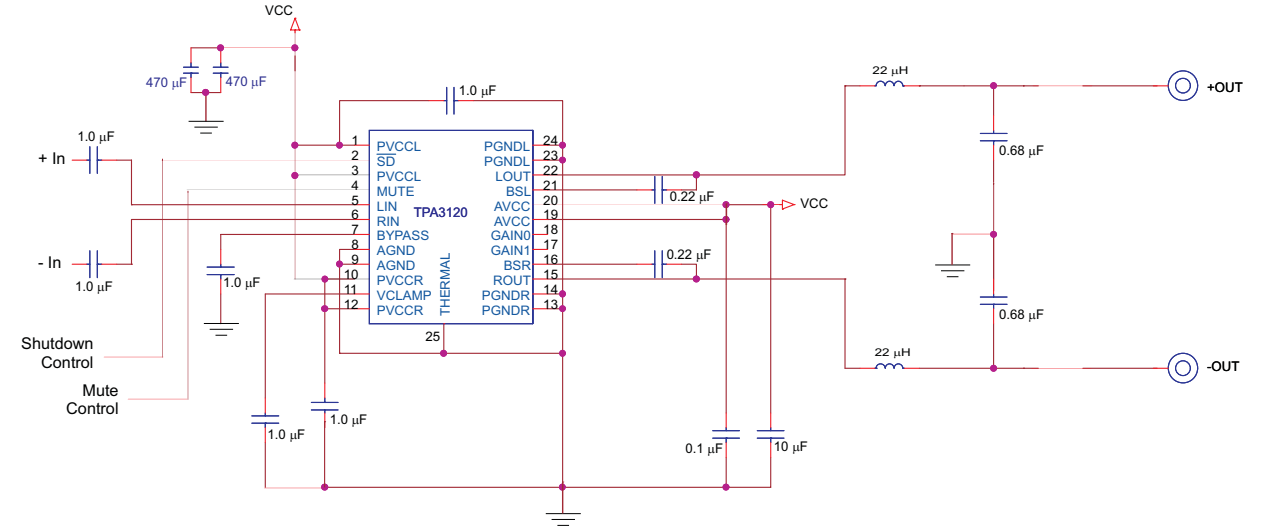


Figure 28. Schematic for Bridge-Tied (BTL) Configuration

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BASIC MEASUREMENT SYSTEM

This section focuses on methods that use the basic equipment listed below:

- Audio analyzer or spectrum analyzer
- Digital multimeter (DMM)
- Oscilloscope
- Twisted-pair wires
- Signal generator
- Power resistor(s)
- Linear regulated power supply
- Filter components
- EVM or other complete audio circuit

Figure 29 shows the block diagrams of basic measurement systems for class-AB and class-D amplifiers. A sine wave is normally used as the input signal because it consists of the fundamental frequency only (no other harmonics are present). An analyzer is then connected to the audio power amplifier (APA) output to measure the voltage output. The analyzer must be capable of measuring the entire audio bandwidth. A regulated dc power supply is used to reduce the noise and distortion injected into the APA through the power pins. A System Two™ audio measurement system (AP-II) by Audio Precision™ includes the signal generator and analyzer in one package.

The generator output and amplifier input must be ac-coupled. However, the EVMs already have the ac-coupling capacitors, (C_{IN}), so no additional coupling is required. The generator output impedance should be low to avoid attenuating the test signal, and is important because the input resistance of APAs is not high. Conversely, the analyzer input impedance should be high. The output resistance, R_{OUT}, of the APA is normally in the hundreds of milliohms and can be ignored for all but the power-related calculations.

Figure 29(a) shows a class-AB amplifier system. It takes an analog signal input and produces an analog signal output. This amplifier circuit can be directly connected to the AP-II or other analyzer input.

This is not true of the class-D amplifier system shown in Figure 29(b), which requires low-pass filters in most cases in order to measure the audio output waveforms. This is because it takes an analog input signal and converts it into a pulse-width modulated (PWM) output signal that is not accurately processed by some analyzers.

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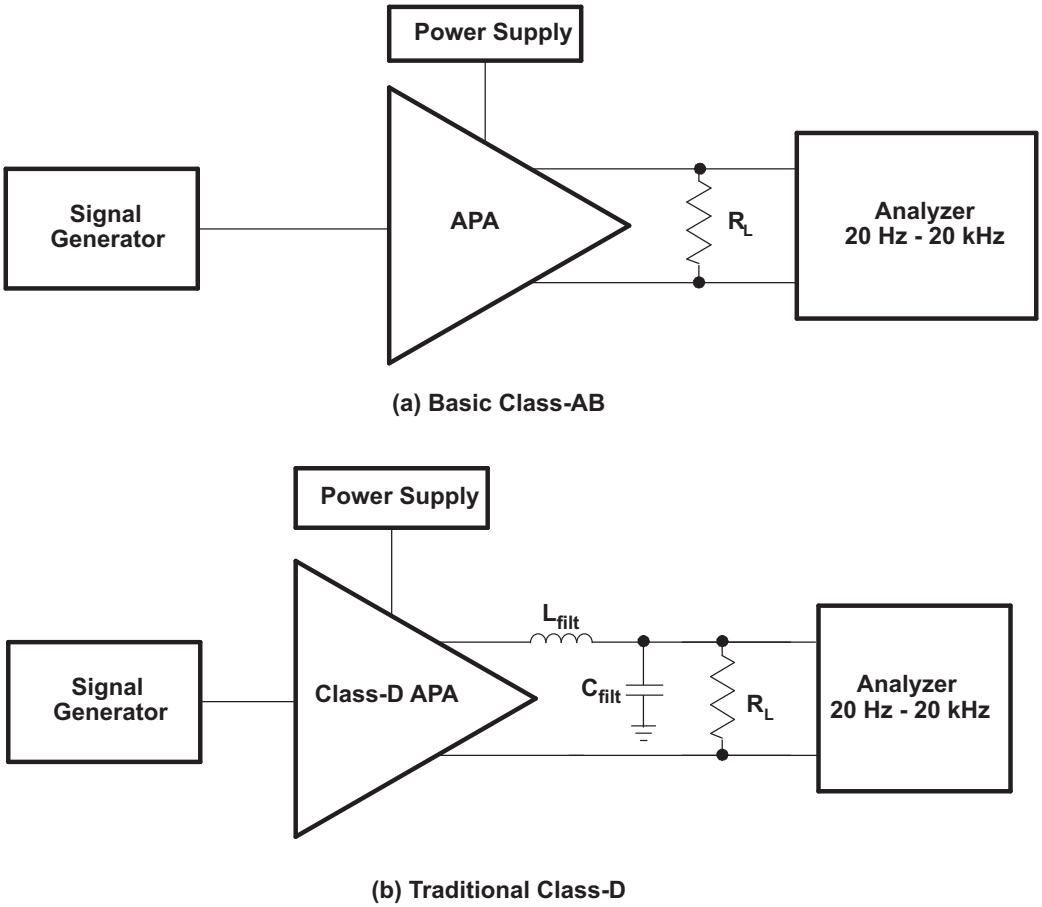


Figure 29. Audio Measurement Systems

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SE Input and SE Output (TPA3120D2 Stereo Configuration)

The SE input and output configuration is used with class-AB amplifiers. A block diagram of a fully SE measurement circuit is shown in Figure 30. SE inputs normally have one input pin per channel. In some cases, two pins are present; one is the signal and the other is ground. SE outputs have one pin driving a load through an output ac-coupling capacitor and the other end of the load is tied to ground. SE inputs and outputs are considered to be unbalanced, meaning one end is tied to ground and the other to an amplifier input/output.

The generator should have unbalanced outputs, and the signal should be referenced to the generator ground for best results. Unbalanced or balanced outputs can be used when floating, but they may create a ground loop that affects the measurement accuracy. The analyzer should have balanced inputs to cancel out any common-mode noise in the measurement.

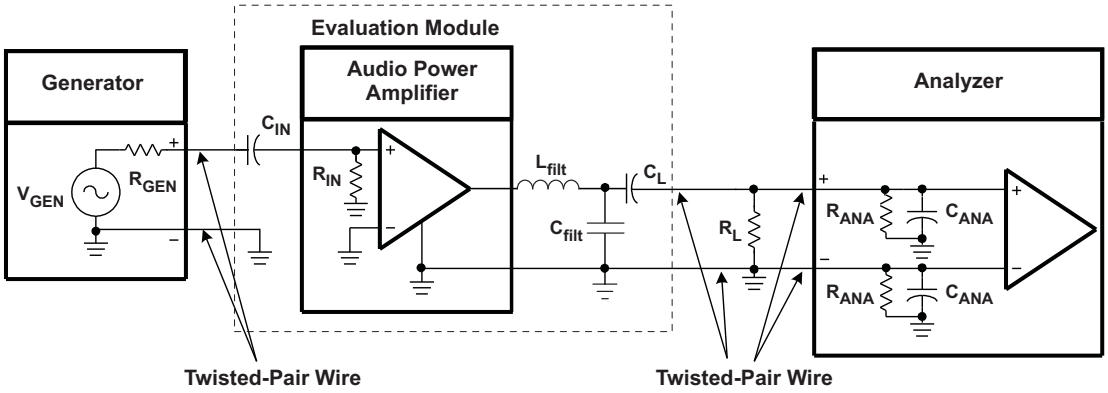


Figure 30. SE Input—SE Output Measurement Circuit

The following general rules should be followed when connecting to APAs with SE inputs and outputs:

- Use an unbalanced source to supply the input signal.
- Use an analyzer with balanced inputs.
- Use twisted-pair wire for all connections.
- Use shielding when the system environment is noisy.
- Ensure the cables from the power supply to the APA, and from the APA to the load, can handle the large currents (see Table 5).

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DIFFERENTIAL INPUT AND BTL OUTPUT (TPA3120D2 Mono Configuration)

Many of the class-D APAs and many class-AB APAs have differential inputs and bridge-tied-load (BTL) outputs. Differential inputs have two input pins per channel and amplify the difference in voltage between the pins. Differential inputs reduce the common-mode noise and distortion of the input circuit. BTL is a term commonly used in audio to describe differential outputs. BTL outputs have two output pins providing voltages that are 180° out of phase. The load is connected between these pins. This has the added benefits of quadrupling the output power to the load and eliminating a dc-blocking capacitor.

A block diagram of the measurement circuit is shown in Figure 31. The differential input is a balanced input, meaning the positive (+) and negative (–) pins have the same impedance to ground. Similarly, the SE output equates to a balanced output.

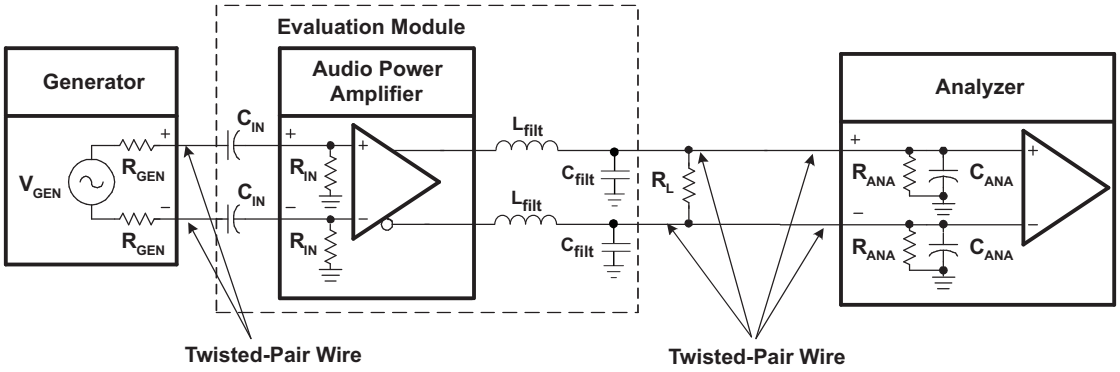


Figure 31. Differential Input, BTL Output Measurement Circuit

The generator should have balanced outputs, and the signal should be balanced for best results. An unbalanced output can be used, but it may create a ground loop that affects the measurement accuracy. The analyzer must also have balanced inputs for the system to be fully balanced, thereby cancelling out any common-mode noise in the circuit and providing the most accurate measurement.

The following general rules should be followed when connecting to APAs with differential inputs and BTL outputs:

- Use a balanced source to supply the input signal.
- Use an analyzer with balanced inputs.
- Use twisted-pair wire for all connections.
- Use shielding when the system environment is noisy.
- Ensure that the cables from the power supply to the APA, and from the APA to the load, can handle the large currents (see Table 5).

Table 5 shows the recommended wire size for the power supply and load cables of the APA system. The real concern is the dc or ac power loss that occurs as the current flows through the cable. These recommendations are based on 12-inch (30.5-cm)-long wire with a 20-kHz sine-wave signal at 25°C.

Table 5. Recommended Minimum Wire Size for Power Cables

P_{OUT} (W)	R_L(Ω)	AWG Size		DC POWER LOSS (mW)		AC POWER LOSS (mW)	
10	4	18	22	16	40	18	42
2	4	18	22	3.2	8	3.7	8.5
1	8	22	28	2	8	2.1	8.1
< 0.75	8	22	28	1.5	6.1	1.6	6.2

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPA3120D2PWP	NRND	HTSSOP	PWP	24	60	Green (RoHS & no Sb/Br)	NIPDAU	Level-3-260C-168 HR	-40 to 85	TPA3120D2	
TPA3120D2PWPR	NRND	HTSSOP	PWP	24	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-3-260C-168 HR	-40 to 85	TPA3120D2	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

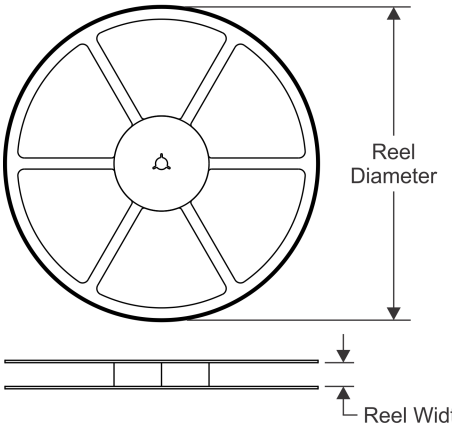
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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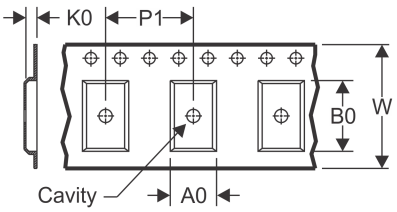
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

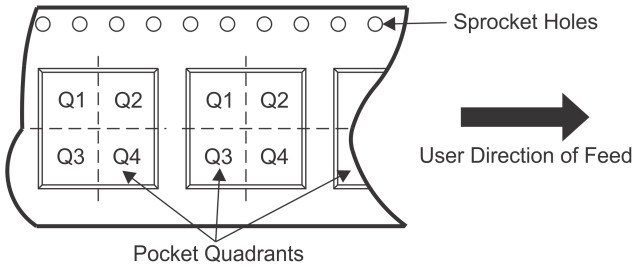


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

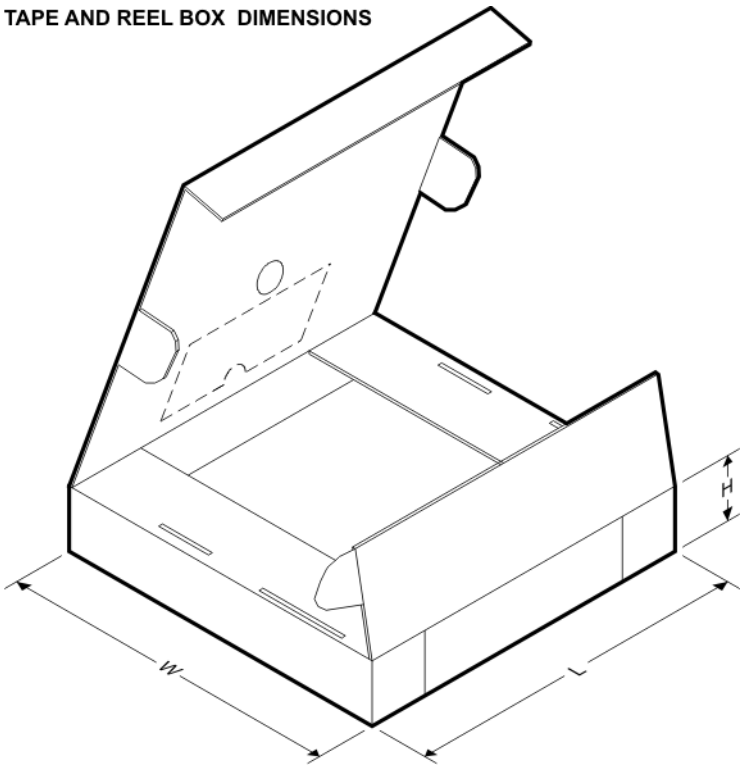
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPA3120D2PWPR	HTSSOP	PWP	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPA3120D2PWPR	HTSSOP	PWP	24	2000	350.0	350.0	43.0

GENERIC PACKAGE VIEW

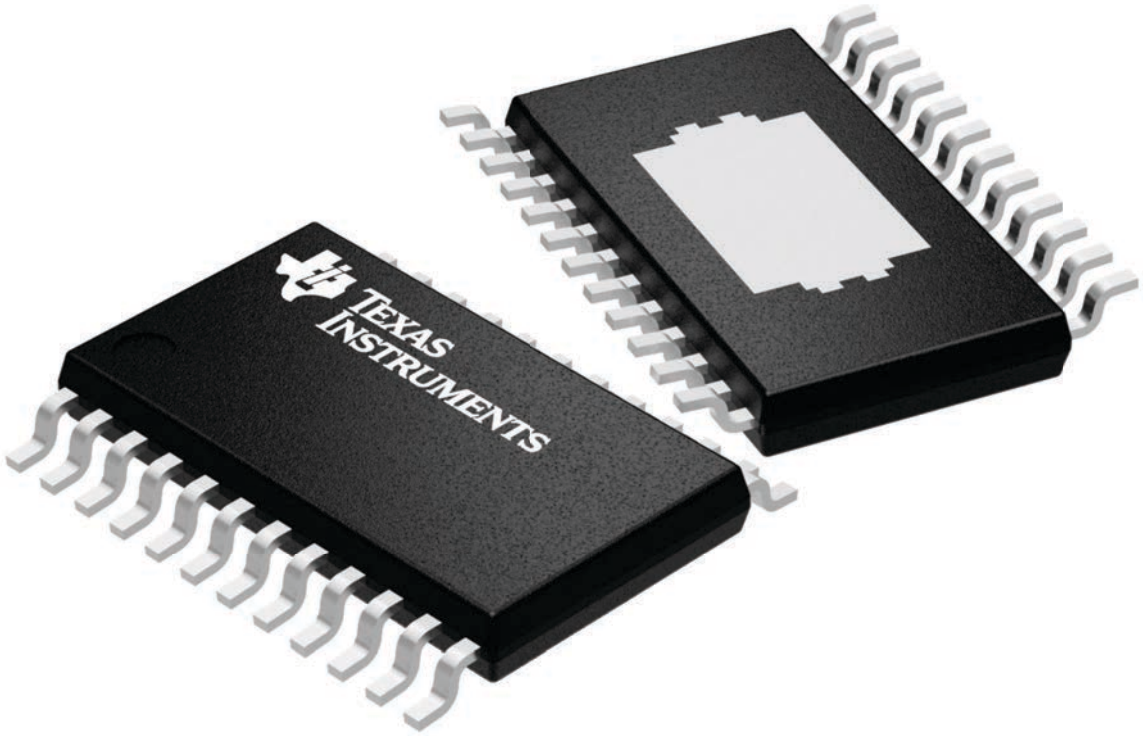
PWP 24

PowerPAD™ TSSOP - 1.2 mm max height

4.4 x 7.6, 0.65 mm pitch

PLASTIC SMALL OUTLINE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



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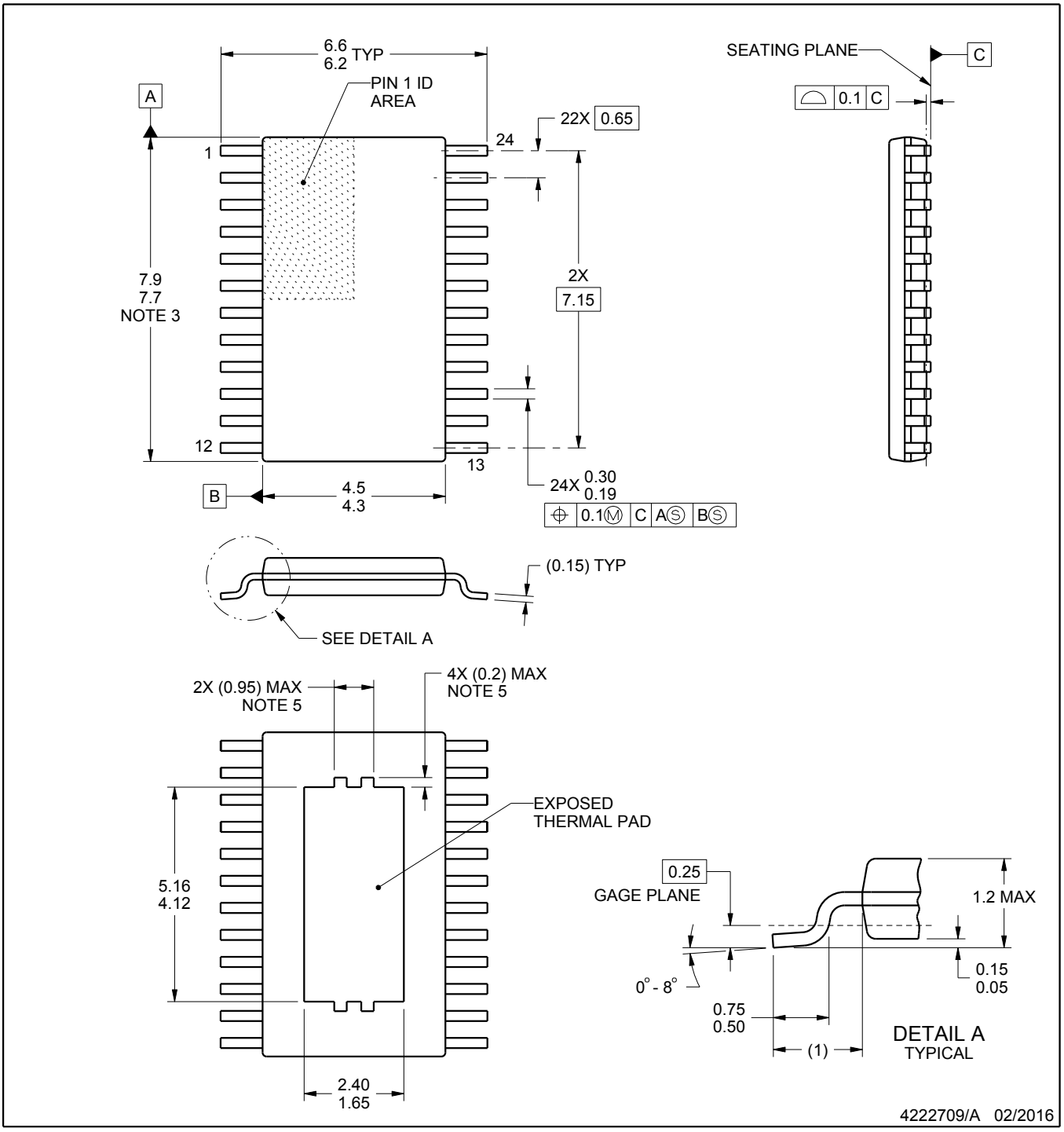


PACKAGE OUTLINE

PWP0024B

PowerPAD™ TSSOP - 1.2 mm max height

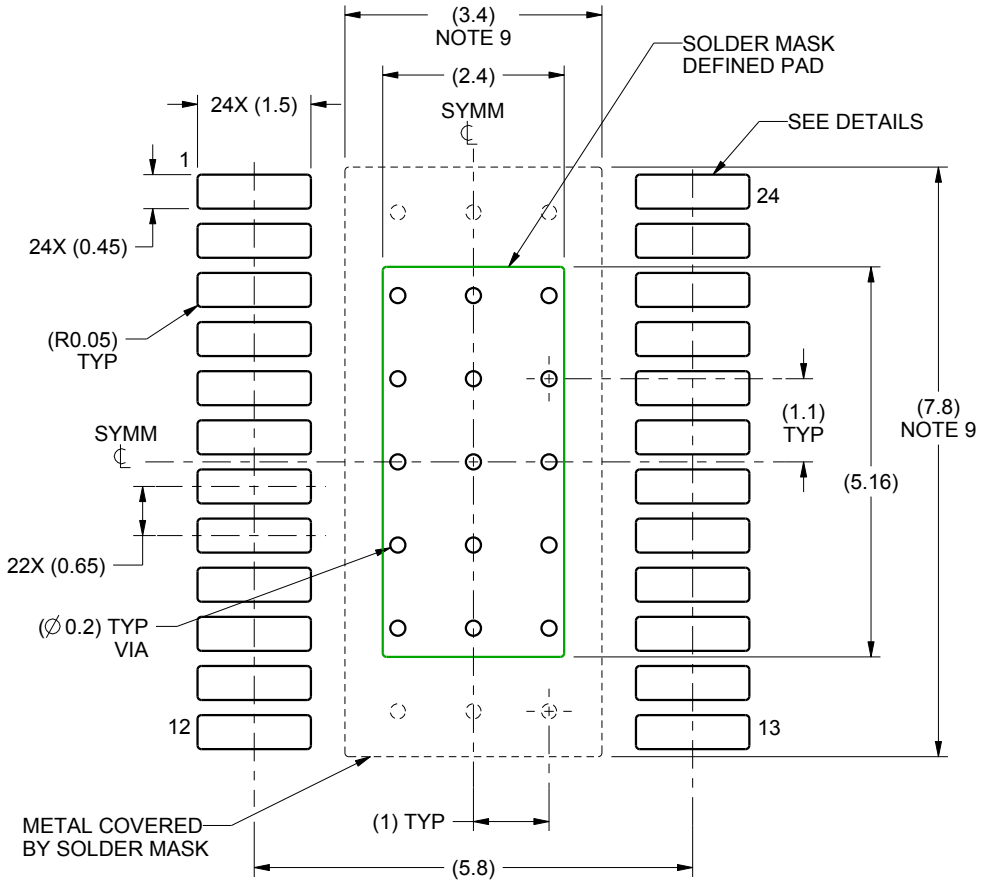
PLASTIC SMALL OUTLINE



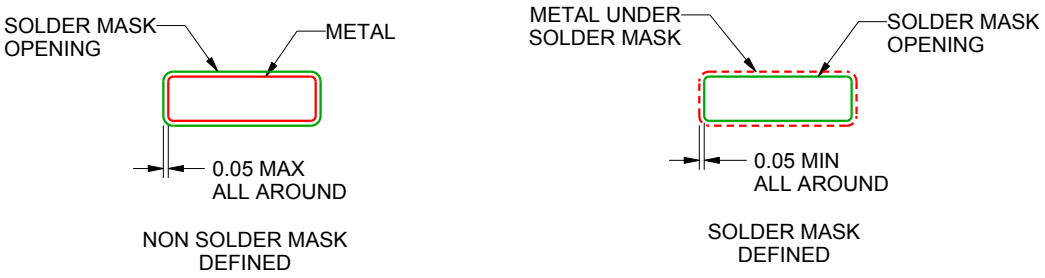
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may not be present and may vary.



LAND PATTERN EXAMPLE
SCALE:10X

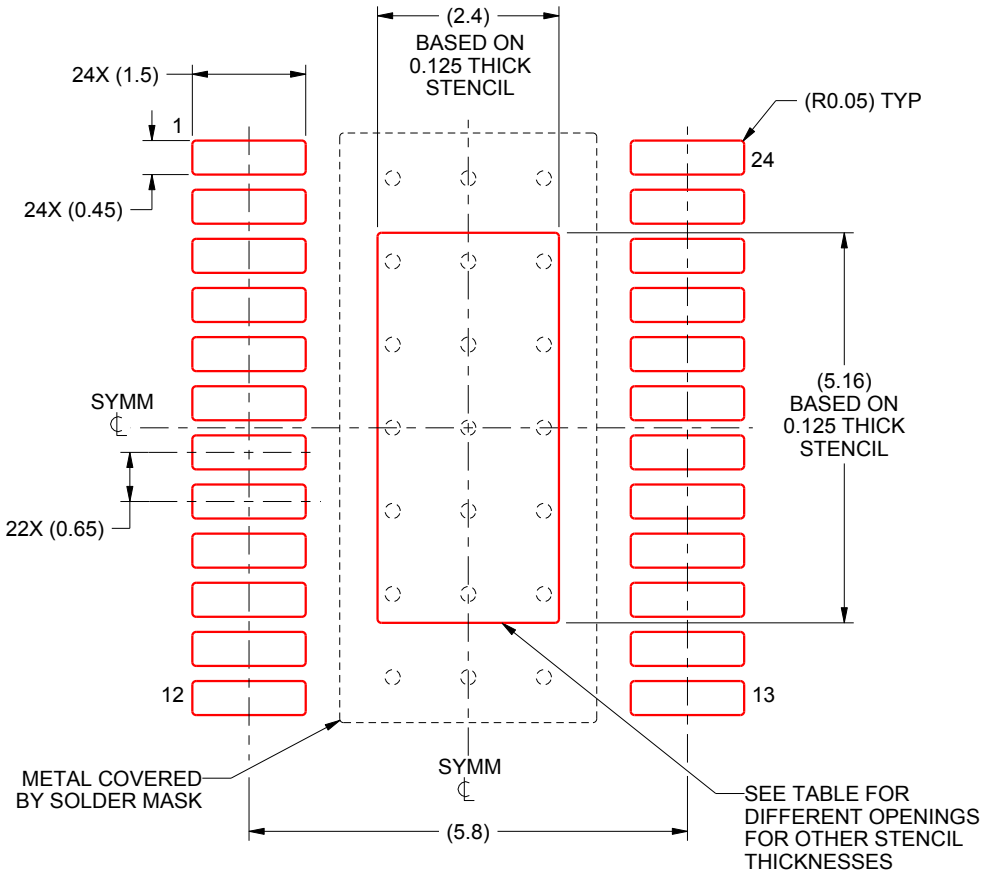


SOLDER MASK DETAILS
PADS 1-24

4222709/A 02/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:10X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	2.68 X 5.77
0.125	2.4 X 5.16 (SHOWN)
0.15	2.19 X 4.71
0.175	2.03 X 4.36

4222709/A 02/2016

NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

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