

Automotive grade N-channel 500 V, 0.23 Ω , 17 A, Zener-protected SuperMESH™ Power MOSFET in a D²PAK package

Datasheet - production data

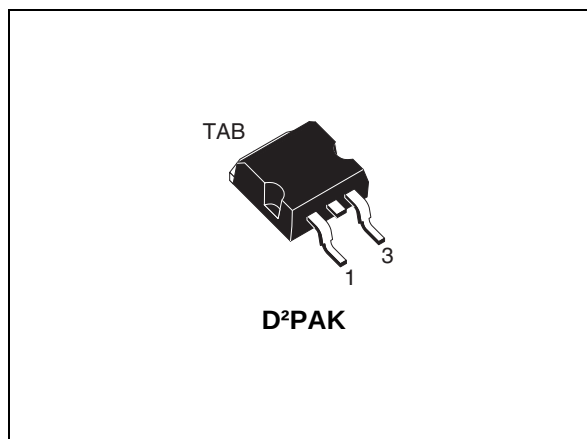
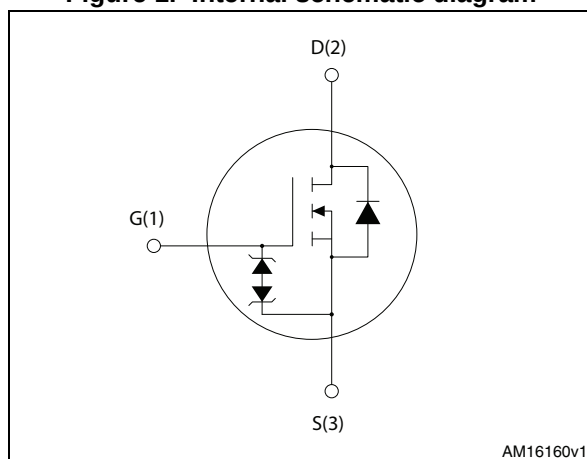


Figure 1. Internal schematic diagram



Features

Order code	V _{DS}	R _{DS(on)} max	I _D	P _W
STB21NK50Z	500 V	0.27 Ω	17 A	190 W

- Designed for automotive applications and AEC-Q101 qualified
- Extremely high dv/dt capability
- 100% avalanche tested
- Gate charge minimized
- Very low intrinsic capacitances
- Very good manufacturing repeatability

Applications

- Switching applications

Description

This device is an N-channel Zener-protected Power MOSFET developed using STMicroelectronics' SuperMESH™ technology, achieved through optimization of ST's well established strip-based PowerMESH™ layout. In addition to a significant reduction in on-resistance, this device is designed to ensure a high level of dv/dt capability for the most demanding applications.

Table 1. Device summary

Order code	Marking	Packages	Packaging
STB21NK50Z	21NK50Z	D ² PAK	Tape and reel

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1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage ($V_{GS} = 0$)	500	V
V_{GS}	Gate-source voltage	± 30	V
I_D	Drain current (continuous) at $T_C = 25\text{ }^{\circ}\text{C}$	17	A
I_D	Drain current (continuous) at $T_C=100\text{ }^{\circ}\text{C}$	10.71	A
$I_{DM}^{(1)}$	Drain current (pulsed)	68	A
P_{TOT}	Total dissipation at $T_C = 25\text{ }^{\circ}\text{C}$	190	W
	Derating Factor	1.51	W/ $^{\circ}\text{C}$
$V_{esd}(G-S)$	G-S ESD (HBM $C=100\text{ pF}$, $R=1.5\text{ k}\Omega$)	6000	V
$dv/dt^{(2)}$	Peak diode recovery voltage slope	4.5	V/ns
T_{stg}	Storage temperature	-55 to 150	$^{\circ}\text{C}$
T_J	Max operating junction temperature	150	$^{\circ}\text{C}$

1. Pulse width limited by safe operating area

2. $I_{SD} \leq 17\text{ A}$, $di/dt \leq 200\text{ A}/\mu\text{s}$, $V_{DD} \leq V_{(BR)DSS}$, $T_J \leq T_{JMAX}$

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case max	0.66	$^{\circ}\text{C}/\text{W}$
$R_{thj-amb}$	Thermal resistance junction-ambient max	62.5	$^{\circ}\text{C}/\text{W}$
T_I	Maximum lead temperature for soldering purpose	300	$^{\circ}\text{C}$

Table 4. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by T_{jmax})	17	A
E_{AS}	Single pulse avalanche energy (starting $T_J=25\text{ }^{\circ}\text{C}$, $I_D=I_{AR}$, $V_{DD}=50\text{ V}$)	850	mJ

2 Electrical characteristics

($T_{CASE} = 25\text{ °C}$ unless otherwise specified)

Table 5. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 1\text{ mA}$, $V_{GS} = 0$	500			V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = 500\text{ V}$			1	μA
		$V_{DS} = 500\text{ V}$, $T_C = 125\text{ °C}$			50	μA
I_{GSS}	Gate body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 20\text{ V}$			± 10	μA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 100\text{ }\mu\text{A}$	3	3.75	4.5	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$, $I_D = 8.5\text{ A}$		0.23	0.27	Ω

Table 6. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 25\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0$	-	2600		pF
C_{oss}	Output capacitance		-	328		pF
C_{rss}	Reverse transfer capacitance		-	72		pF
$C_{oss\text{ eq}}^{(1)}$	Equivalent output capacitance	$V_{GS} = 0$, $V_{DS} = 0$ to 400 V	-	187		pF
Q_g	Total gate charge	$V_{DD} = 400\text{ V}$, $I_D = 17\text{ A}$ $V_{GS} = 10\text{ V}$ (see Figure 15)	-	85	119	nC
Q_{gs}	Gate-source charge		-	15.5		nC
Q_{gd}	Gate-drain charge		-	42		nC

1. $C_{oss\text{ eq}}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 7. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD}=250\text{ V}$, $I_D=8.5\text{ A}$, $R_G=4.7\Omega$, $V_{GS}=10\text{ V}$ (see Figure 16)	-	28	-	ns
t_r	Rise time		-	20	-	ns
$t_{d(off)}$	Turn-off delay time	$V_{DD}=250\text{ V}$, $I_D=8.5\text{ A}$, $R_G=4.7\Omega$, $V_{GS}=10\text{ V}$ (see Figure 16)	-	70	-	ns
t_f	Fall time		-	15	-	ns

Table 8. Gate-source Zener diode

Symbol	Parameter	Test conditions	Min	Typ.	Max.	Unit
$V_{(BR)GSO}$	Gate-source breakdown voltage	$I_{GS} = \pm 1\text{ mA}$, $I_D=0$	30	-	-	V

The built-in back-to-back Zener diodes have been specifically designed to enhance the ESD capability of the device. The Zener voltage is appropriate for efficient and cost-effective intervention to protect the device integrity. These integrated Zener diodes thus eliminate the need for external components.

Table 9. Source drain diode

Symbol	Parameter	Test conditions	Min	Typ.	Max	Unit
I_{SD}	Source-drain current		-		17	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		68	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD}=17\text{ A}$, $V_{GS}=0$	-		1.6	V
t_{rr}	Reverse recovery time	$I_{SD}=17\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_R=100\text{ V}$ (see Figure 16)	-	355		ns
Q_{rr}	Reverse recovery charge		-	3.90		μC
I_{RRM}	Reverse recovery current		-	22		A
t_{rr}	Reverse recovery time	$I_{SD}=17\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_R=100\text{ V}$, $T_j=150\text{ }^\circ\text{C}$ (see Figure 16)	-	440		ns
Q_{rr}	Reverse recovery charge		-	5.72		μC
I_{RRM}	Reverse recovery current		-	25		A

1. Pulse width limited by safe operating area

2. Pulsed: pulse duration=300 μs , duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

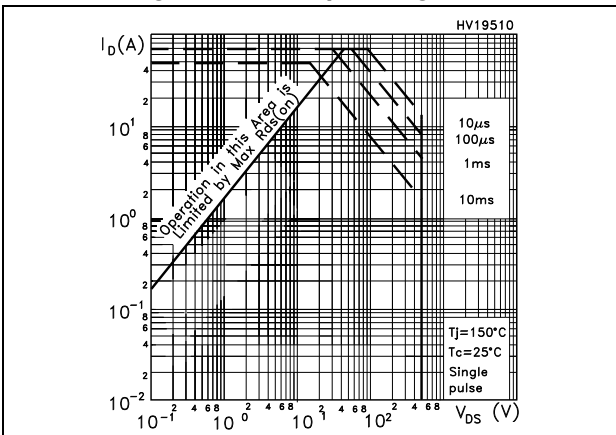


Figure 3. Thermal impedance

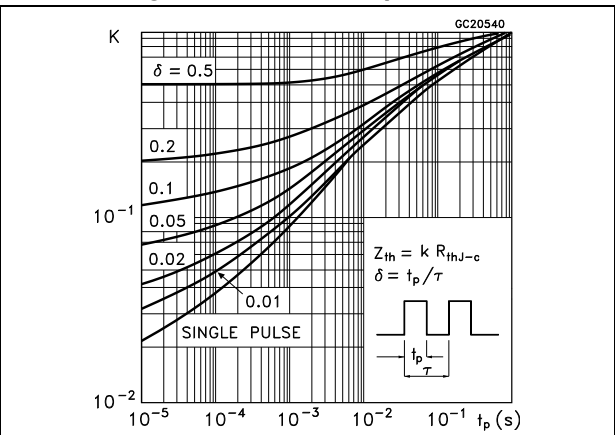


Figure 4. Output characteristics

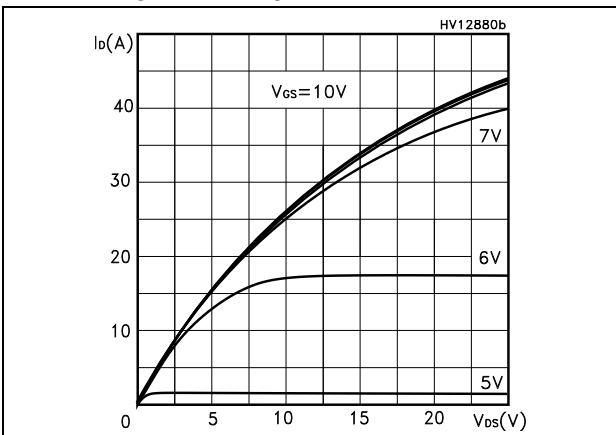


Figure 5. Transfer characteristics

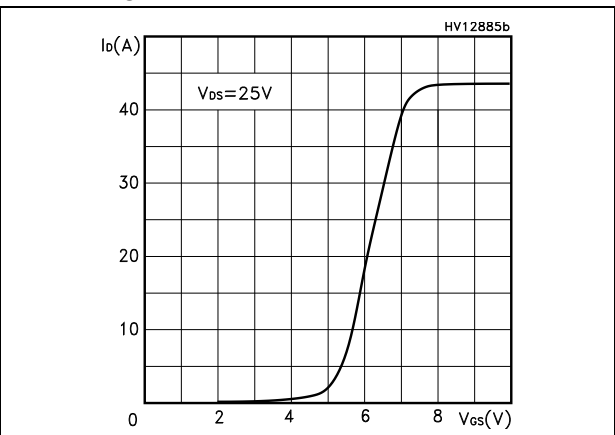


Figure 6. Normalized $B_{V_{DS}}$ vs temperature

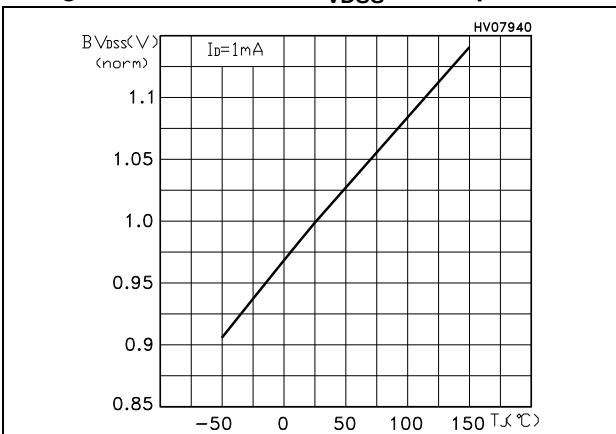


Figure 7. Static drain-source on-resistance

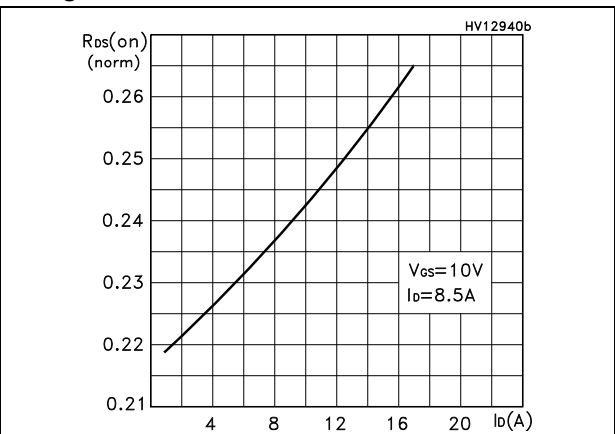


Figure 8. Gate charge vs gate-source voltage

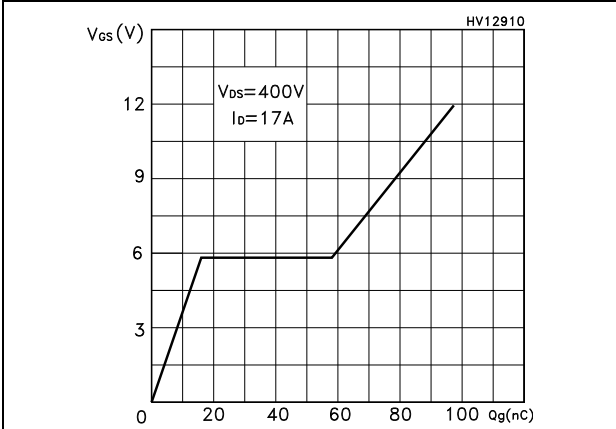


Figure 9. Capacitance variations

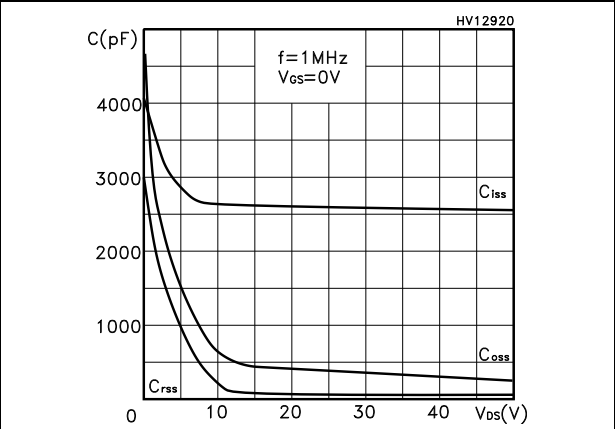


Figure 10. Normalized gate threshold voltage vs temperature

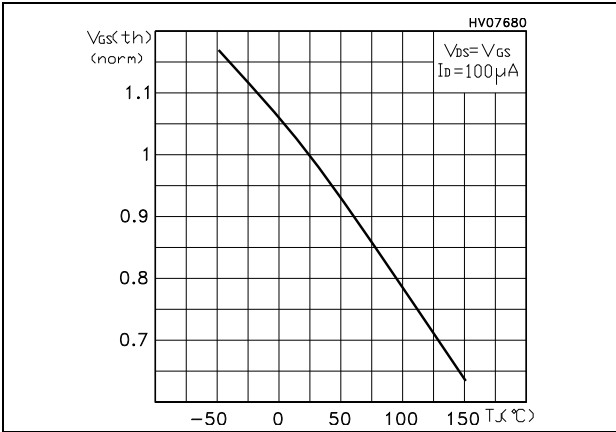


Figure 11. Normalized on-resistance vs temperature

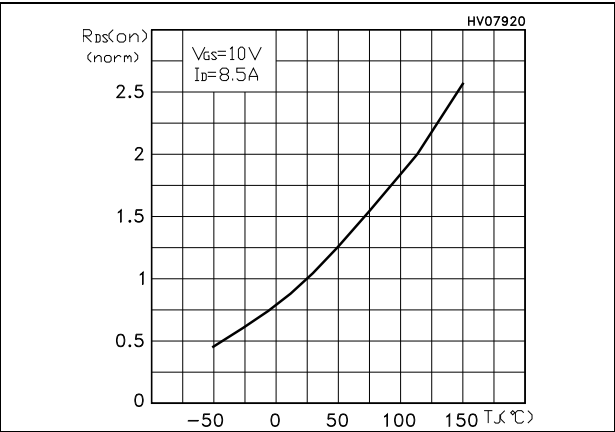


Figure 12. Source-drain diode forward characteristics

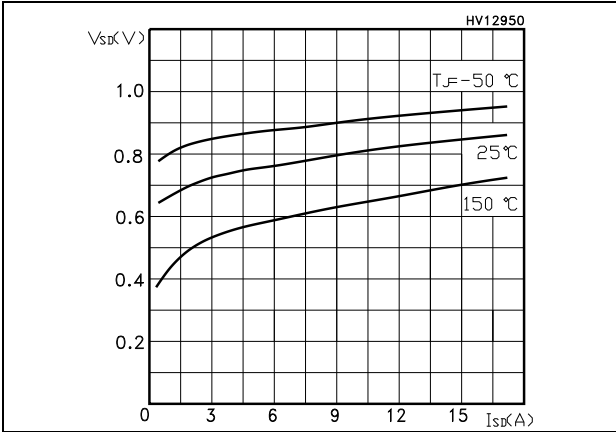
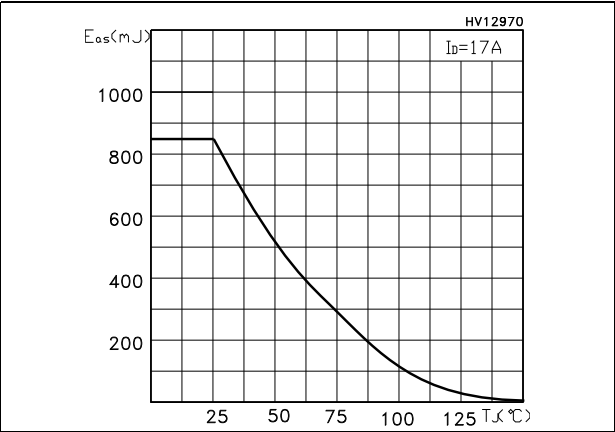


Figure 13. Maximum avalanche energy vs temperature



3 Test circuits

Figure 14. Switching times test circuit for resistive load

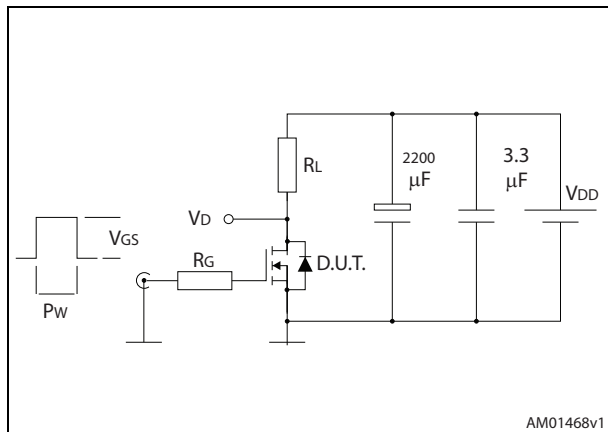


Figure 15. Gate charge test circuit

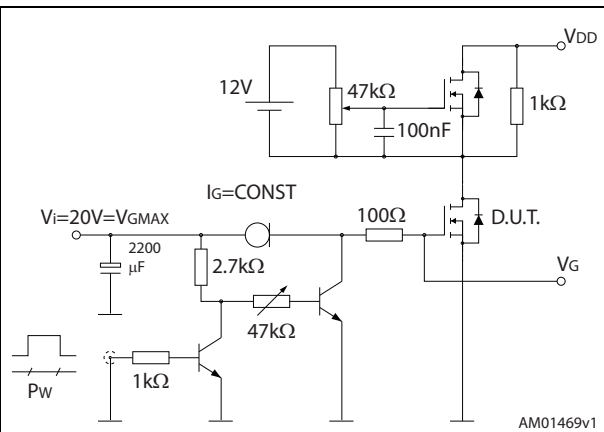


Figure 16. Test circuit for inductive load switching and diode recovery times

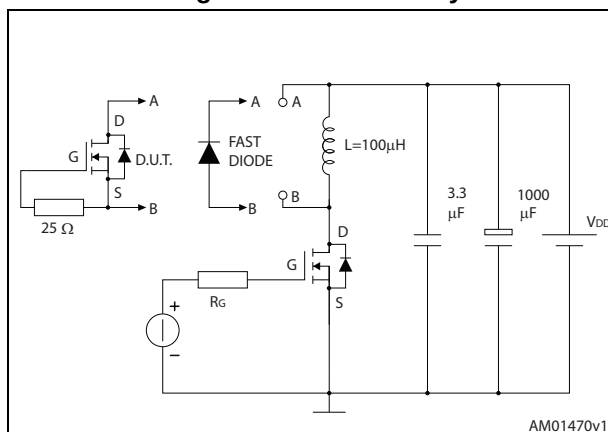


Figure 17. Unclamped inductive load test circuit

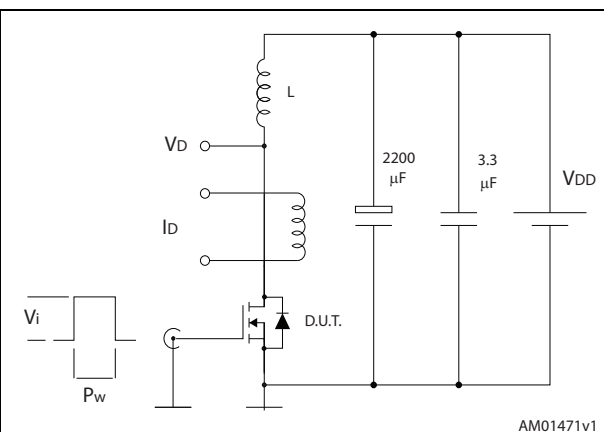


Figure 18. Unclamped inductive waveform

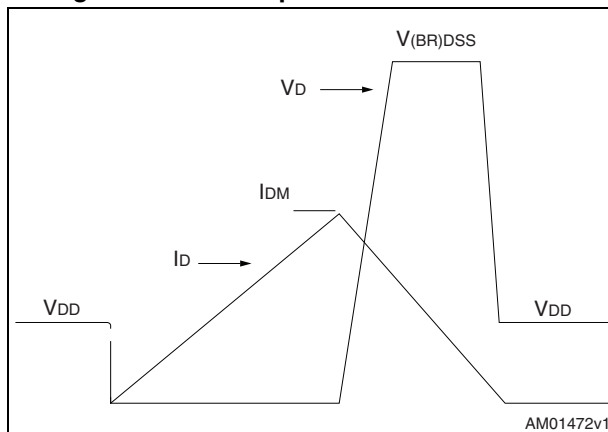
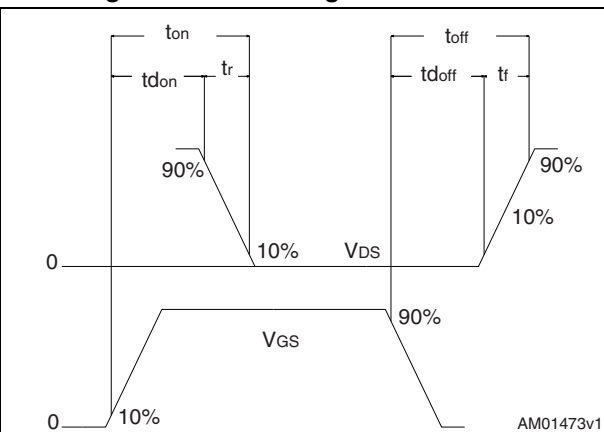


Figure 19. Switching time waveform



4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

Figure 20. D²PAK (TO-263) drawing

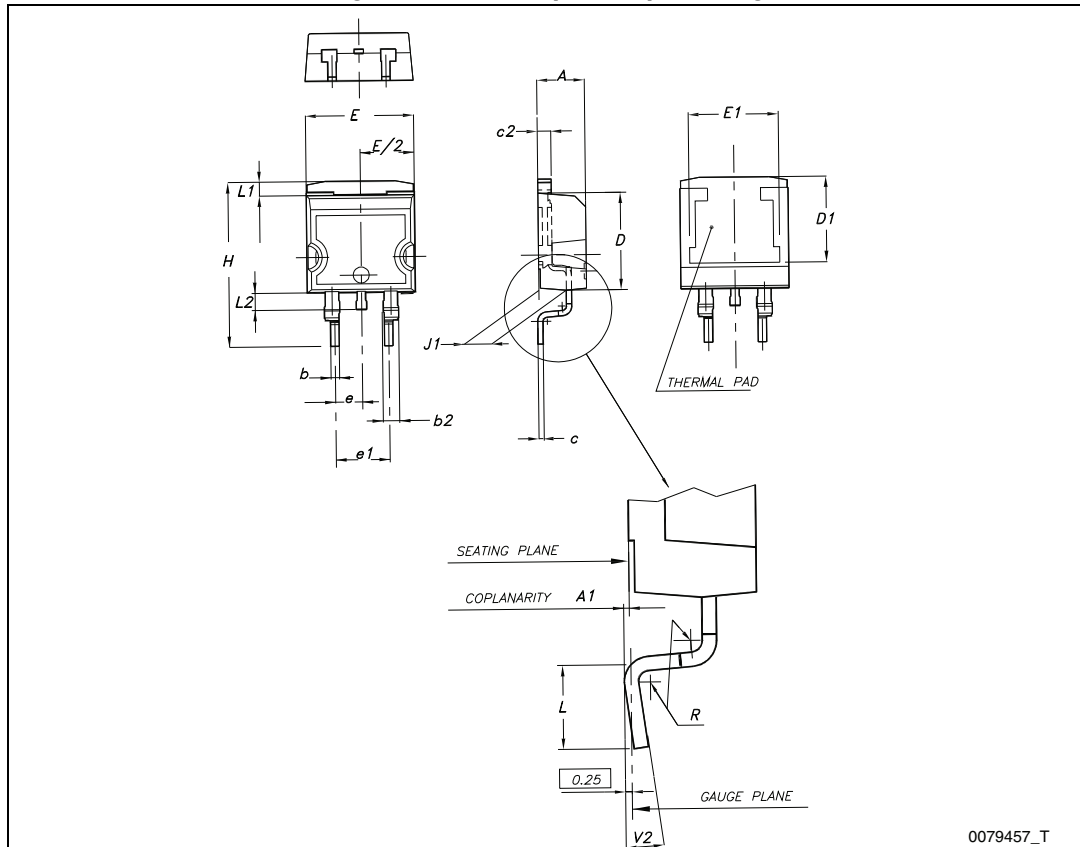
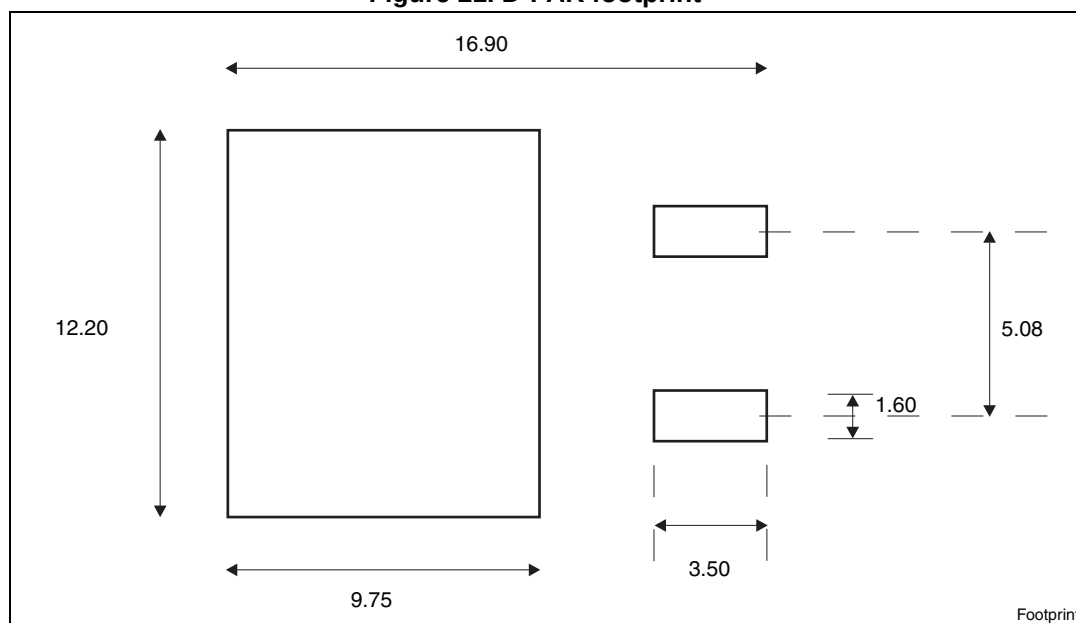


Table 10. D²PAK (TO-263) mechanical data

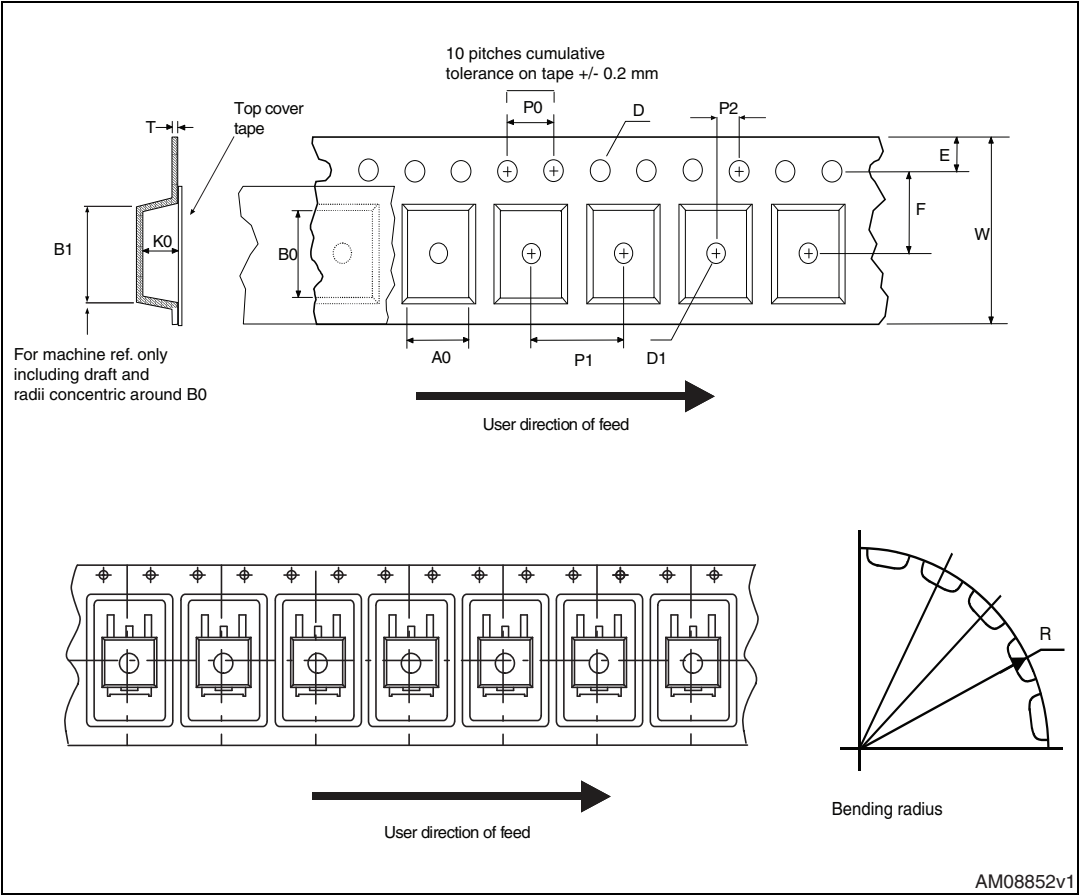
Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
A1	0.03		0.23
b	0.70		0.93
b2	1.14		1.70
c	0.45		0.60
c2	1.23		1.36
D	8.95		9.35
D1	7.50		
E	10		10.40
E1	8.50		
e		2.54	
e1	4.88		5.28
H	15		15.85
J1	2.49		2.69
L	2.29		2.79
L1	1.27		1.40
L2	1.30		1.75
R		0.4	
V2	0°		8°

Figure 21. D²PAK footprint^(a)

a. All dimension are in millimeters

5 Packaging mechanical data

Figure 22. Tape



6 Revision history

Table 12. Document revision history

Date	Revision	Changes
16-Sep-2008	1	First issue
19-Sep-2014	2	– Updated: title and features in cover page – Updated: Section 4: Package mechanical data and Section 5: Packaging mechanical data – Minor text changes

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