100V, 0.6A Synchronous Micropower Step-Down High Efficiency Switching Regulator

FEATURES

- **Ultrawide Input Voltage Range: 3V to 100V**
- **Boundary Mode Switching for Highest Efficiency**
- **Output Voltage Range: 0.8V to 60V**
- **Internal Synchronous Switches**
- **Burst Mode® Operation:**
  - **16µA I_Q at 12V_{IN} to 5V_{OUT}**
  - **7µA I_Q at 48V_{IN} to 5V_{OUT}**
- **Low Dropout: 99% Maximum Duty Cycle**
- **Peak Current Mode Control**
- **Programmable Undervoltage Lockout**
- **Power Good Flag**
- Flexible Output Voltage Tracking
- Short-Circuit Protection
- Low Shutdown Current: 5µA
- Tolerates Pin Open/Short Faults
- Thermally Enhanced 20-Lead TSSOP with High Voltage Lead Spacing

APPLICATIONS

- Automotive Supplies
- Telecom Supplies
- Distributed Supply Regulation

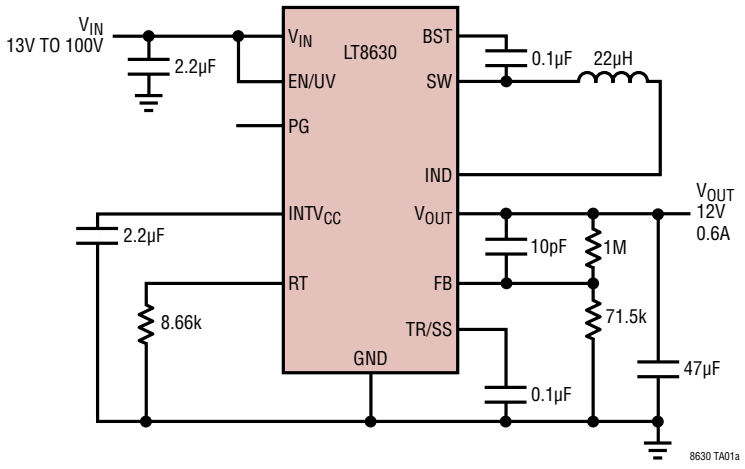
DESCRIPTION

The LT®8630 is a current mode PWM step-down DC/DC converter with internal synchronous switches that provide current for output loads up to 0.6A. The wide input range of 3V to 100V makes the LT8630 suitable for regulating power from a wide variety of sources, including automotive and industrial systems and 36V to 72V telecom supplies. Variable frequency boundary mode switching maximizes efficiency across a wide range of input voltages. Low ripple Burst Mode operation enables high efficiency operation down to very low output currents while keeping the output ripple below 5mV. The soft-start feature controls the ramp rate of the output voltage, eliminating input current surge during start-up, while also providing output tracking. A power good flag signals when the output voltage is within ±7.5% of the regulated output. Undervoltage lockout can be programmed using the EN/UV pin. Shutdown mode reduces the total quiescent current to < 5µA. The LT8630 is available in a 20-lead TSSOP package with exposed pad for low thermal resistance and high voltage lead spacing.

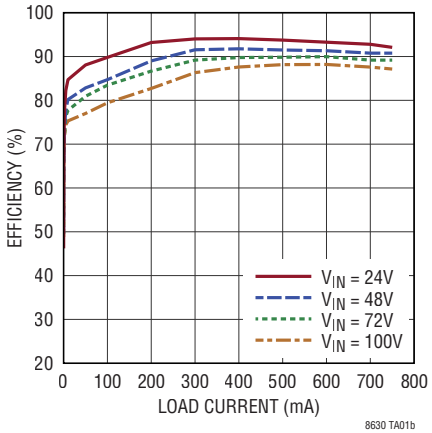
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TYPICAL APPLICATION

12V, 0.6A Step-Down Converter



Efficiency at V_{OUT} = 12V

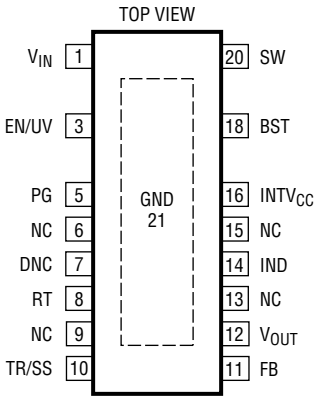


ABSOLUTE MAXIMUM RATINGS

(Note 1)

V_{IN}, EN/UV, PG 100V
IND, V_{OUT}, ... 60V/–0.3V
FB, TR/SS 4V
Operating Junction Temperature Range
LT8630EFE (Note 2) ..... –40°C to 125°C
LT8630IFE (Note 2) ..... –40°C to 125°C
Storage Temperature Range ..... –65°C to 150°C

PIN CONFIGURATION



FE PACKAGE
VARIATION FE20(16)
20-LEAD PLASTIC TSSOP

θ_{JA} = 40°C/W, $\theta_{JC(PAD)}$ = 10°C/W
EXPOSED PAD (PIN 21) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

(http://www.linear.com/product/LTC8630#orderinfo)

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LT8630EFE#PBF	LT8630EFE#TRPBF	8630PE	20-Lead Plastic TSSOP	–40°C to 125°C
LT8630IFE#PBF	LT8630IFE#TRPBF	8630PE	20-Lead Plastic TSSOP	–40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_J = 25°C. V_{IN} = 15V, $V_{EN/UV}$ = 2V, unless otherwise specified. (Note 2)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
EN/UV Voltage Threshold	$V_{EN/UV}$ Rising	●	1.14	1.19	1.24	V
EN/UV Voltage Hysteresis			10	17	26	mV
EN/UV Input Current				5	100	nA
V_{IN} Undervoltage Lockout	V_{FB} = 0.9V	●	2.74	2.8	3.05	V
Quiescent Current from V_{IN}	$V_{EN/UV}$ = 0V V_{FB} = 0.9V, V_{VOUT} = 0V V_{FB} = 0.9V, V_{VOUT} = 5V	● ● ●		5 16 3.6	15 50 10	µA µA µA
Quiescent Current from V_{OUT}	V_{FB} = 0.9V, V_{VOUT} = 5V	●		10	45	µA
V_{IN} Current in Regulation	V_{VOUT} = 5V, I_{LOAD} = 100µA V_{VOUT} = 5V, I_{LOAD} = 1mA			90 475	180 650	µA µA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_J = 25°C. V_{IN} = 15V, $V_{EN/UV}$ = 2V, unless otherwise specified. (Note 2)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Feedback Bias Current	V_{FB} = 0.8V		–25	–15		nA
Feedback Voltage (V_{FBREF})	V_{VOUT} = 5V, I_{LOAD} = 100mA	●	796	808	820	mV
Feedback Voltage Regulation	V_{IN} = 7V to 100V, I_{LOAD} = 0.1A to 0.75A, V_{VOUT} = 5V		792	808	824	mV
Track/Soft-Start Source Current	V_{FB} = 0.9V, $V_{TR/SS}$ = 0		–6.5	–4.5	–2.5	µA
Track/Soft-Start VOH	V_{FB} = 0.9V		2.9	3.0	3.4	V
Track/Soft-Start Sink Current	V_{FB} = 0.7V, $V_{TR/SS}$ = 1V		15	30	45	µA
Track/Soft-Start VOL	V_{FB} = 0V			50	75	mV
Track/Soft-Start to Feedback Offset	$V_{TR/SS}$ = 0.4V, V_{VOUT} = 5V, I_{LOAD} = 100mA		–30	5	30	mV
Track/Soft-Start Sink Current POR (Note 4)	V_{FB} = 0.9V, $V_{TR/SS}$ = 0.2V		180	230		µA
PG Leakage Current	V_{FB} = 0V, V_{PG} = 100V		–200	0	200	nA
PG Lower Threshold % of V_{FBREF} (Note 5)	V_{FB} Rising	●	–11.5	–7.5	–4.5	%
PG Upper Threshold % of V_{FBREF} (Note 5)	V_{FB} Falling	●	4.5	7.5	11.5	%
PG Hysteresis			1.4	1.9	2.3	%
PG Sink Current	V_{FB} = 0.7V, V_{PG} = 0.2V			900		µA
Minimum Switch ON Time	V_{IN} = 95V, V_{VOUT} = 5V, I_{LOAD} = 0A			150		ns
Minimum Switch OFF Time	V_{IN} = 5V, V_{VOUT} = 5V, I_{LOAD} = 500mA, L = 15µH			2.1		µs
IND to V_{OUT} Peak Current (Note 6)	V_{IN} = 6V		1.6	2.0	2.7	A
Maximum V_{OUT} Current in Regulation	V_{IN} = 10V, V_{VOUT} = 5V, L = 15µH V_{IN} = 50V, V_{VOUT} = 5V, L = 15µH	 ●	0.8 0.6	1.1 0.9	1.4 2.0	A A
Switch Pin Leakage Current	V_{SW} = 0V, V_{IN} = 100V, V_{EN} = 0V V_{SW} = 100V, V_{IN} = 100V, V_{EN} = 0V			50 0.5	500 2.0	nA µA
Top Switch On-Resistance				775		mΩ
Bottom Switch On-Resistance				550		mΩ
BST Pin Current	V_{BST} = 18V			180		µA
BST Pin Threshold (Note 7)				2.4		V

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LT8630EFE is guaranteed to meet performance specifications from 0°C to 125°C junction temperature. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LT8630IFE is guaranteed over the full –40°C to 125°C operating junction temperature range.

Note 3: The LT8630 includes overtemperature protection that is intended to protect the device during thermal overload conditions. Internal junction temperature will exceed 150°C before the overtemperature circuitry becomes active.

Note 4: An internal power on reset (POR) latch is set on the positive transition of the EN/UV pin through its threshold or thermal shutdown. The output of the latch activates a current source on the TR/SS pin which typically sinks 230µA while discharging the TR/SS capacitor. The latch is reset when the TR/SS pin is driven below the soft-start POR threshold or the EN/UV pin is taken below its threshold.

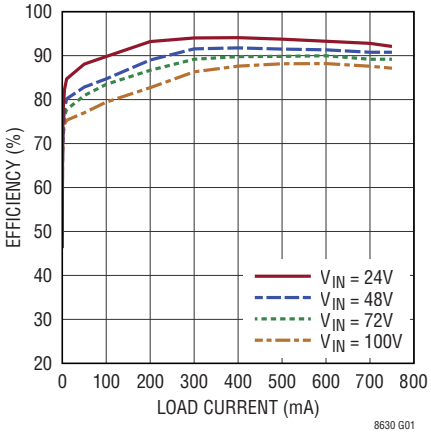
Note 5: The threshold is expressed as a percentage of the feedback reference voltage.

Note 6: The IND to V_{OUT} peak current is defined as the maximum value of current flowing from the IND pin to the V_{OUT} during a switch cycle.

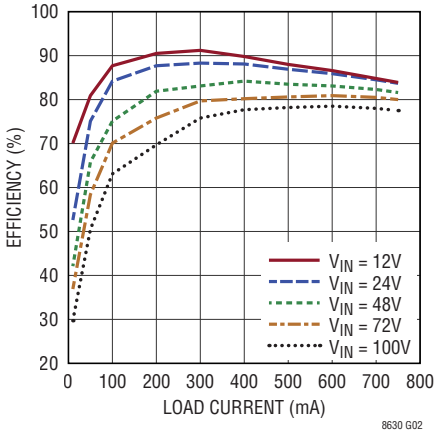
Note 7: The BST pin threshold is defined as the minimum voltage between the BST and SW pins to keep the top switch on. If the the voltage falls below the threshold when the top switch is on, a minimum switch off pulse will be generated.

TYPICAL PERFORMANCE CHARACTERISTICS

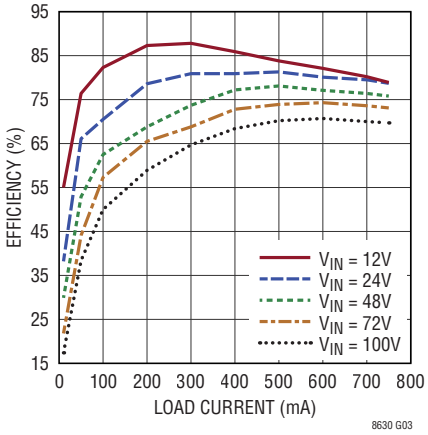
Efficiency at V_{OUT} = 12V



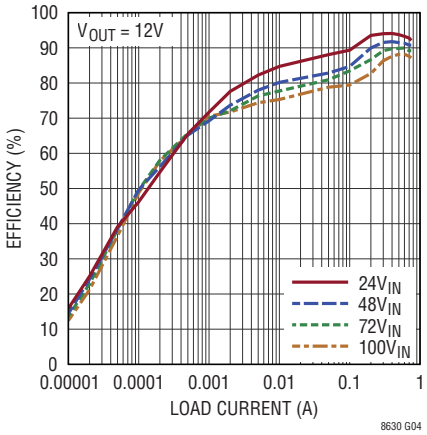
Efficiency at V_{OUT} = 5V



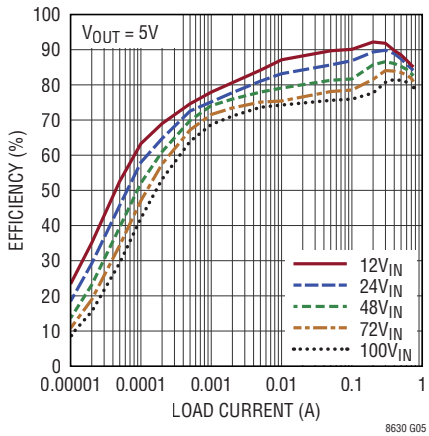
Efficiency at V_{OUT} = 3.3V



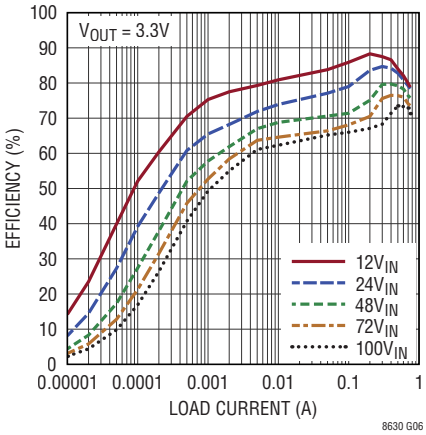
Efficiency at Load



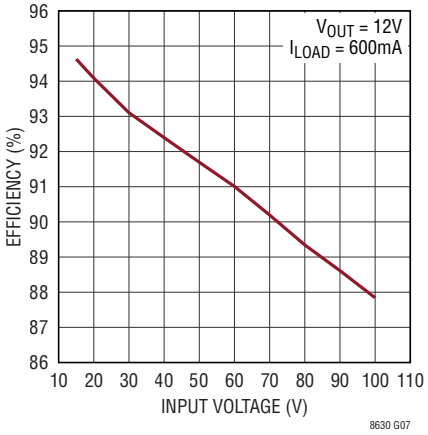
Efficiency at Load



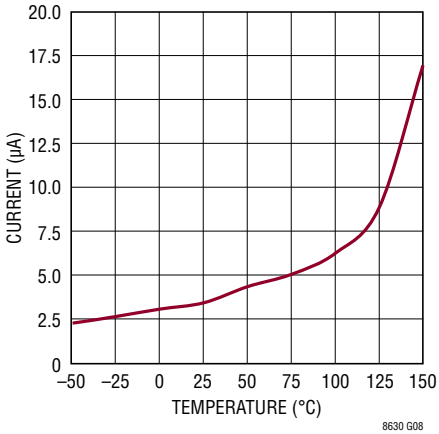
Efficiency at Load



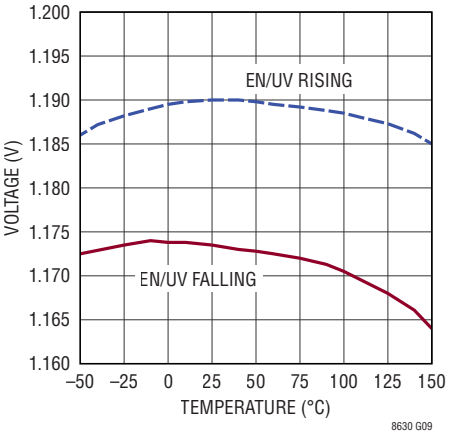
Efficiency vs Input Voltage



Shutdown Supply Current

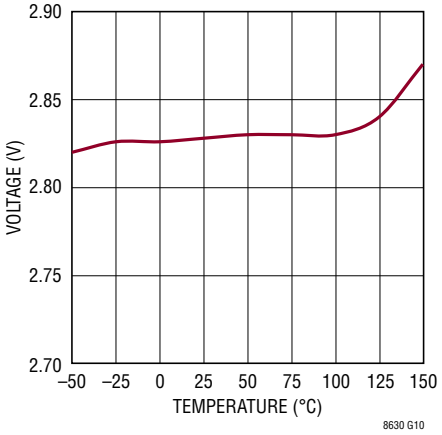


EN/UV Thresholds

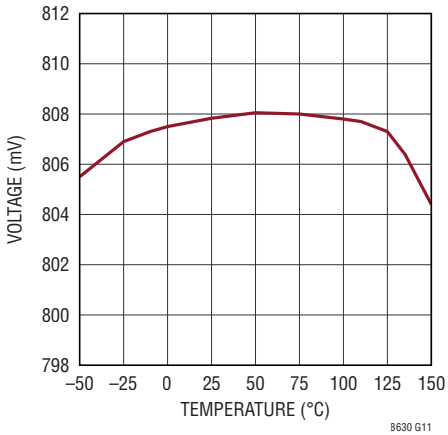


TYPICAL PERFORMANCE CHARACTERISTICS

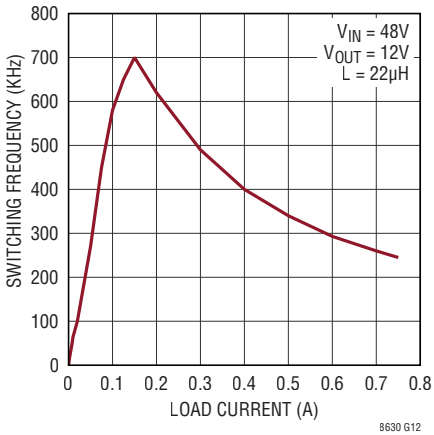
V_{IN} Undervoltage Lockout



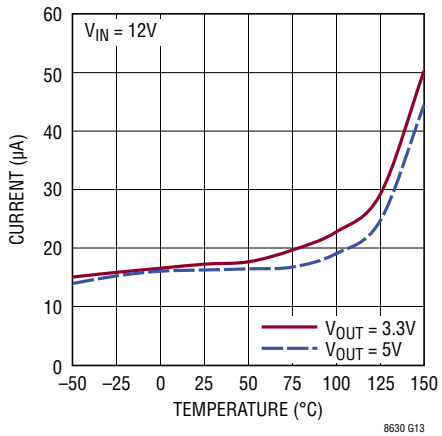
Reference Voltage



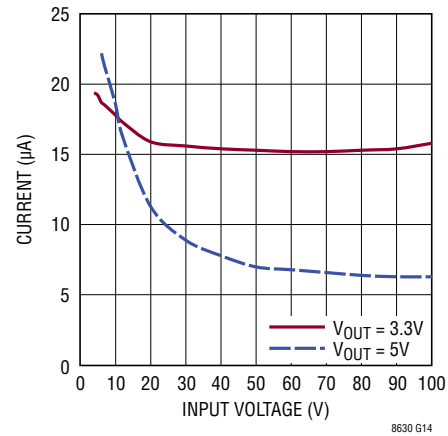
Frequency vs Load Current



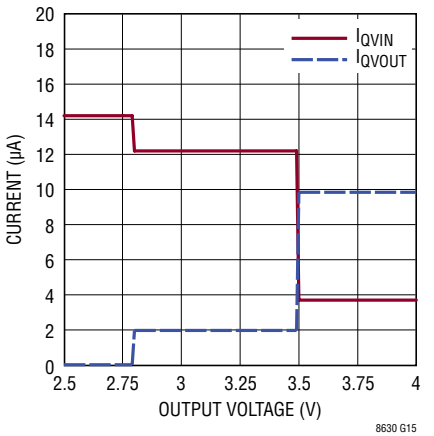
No Load Supply Current



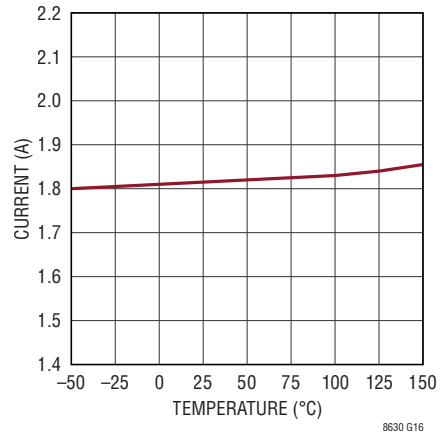
No Load Supply Current



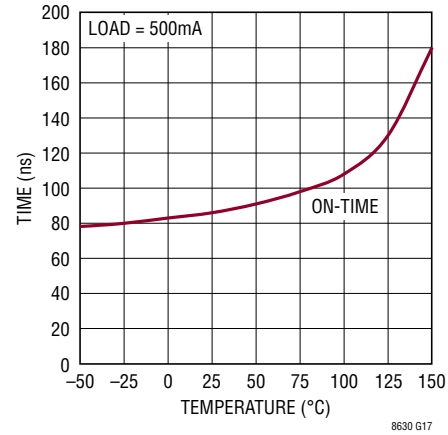
Sleep Quiescent Currents



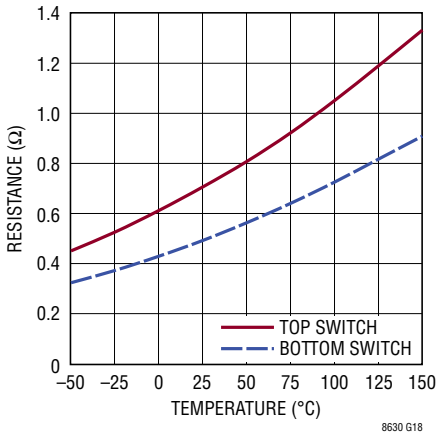
Peak Switch Current



Minimum On-Time

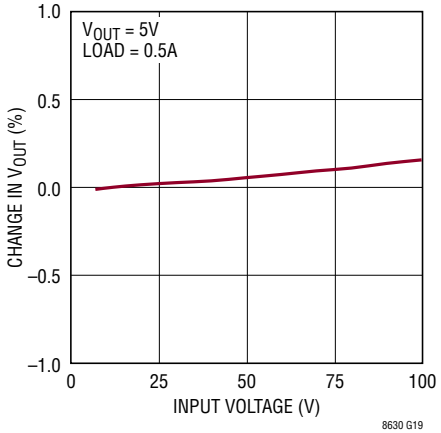


Switch Resistance

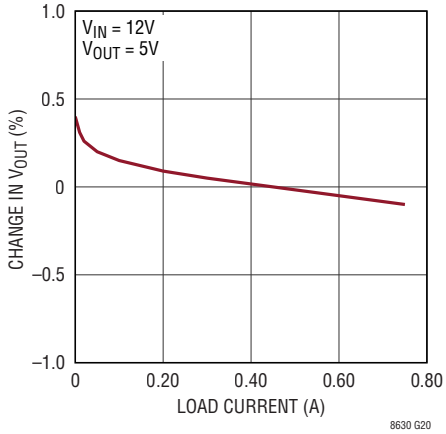


TYPICAL PERFORMANCE CHARACTERISTICS

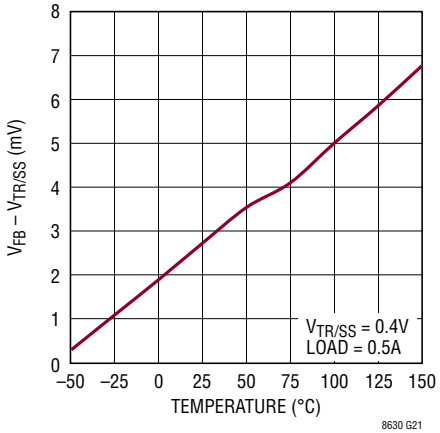
Line Regulation



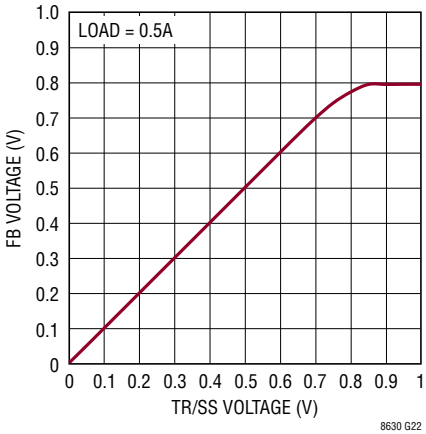
Load Regulation



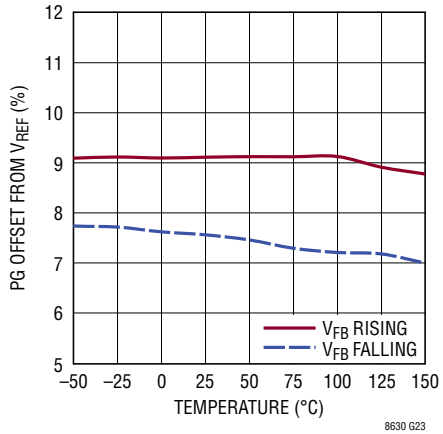
FB to TR/SS Offset Voltage



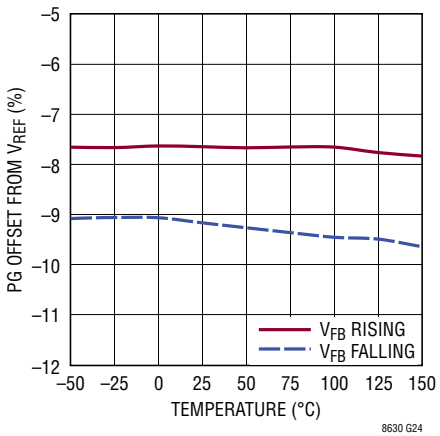
Soft-Start Tracking



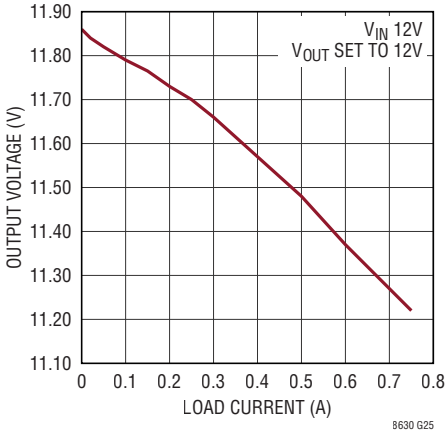
PG High Thresholds



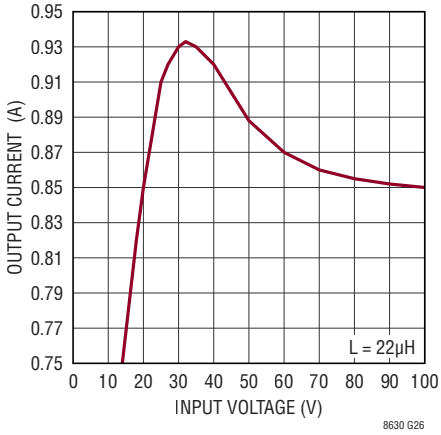
PG Low Thresholds



Dropout Voltage

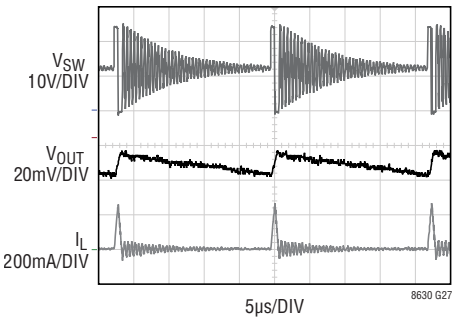


Output Current Limit



FRONT PAGE APPLICATION

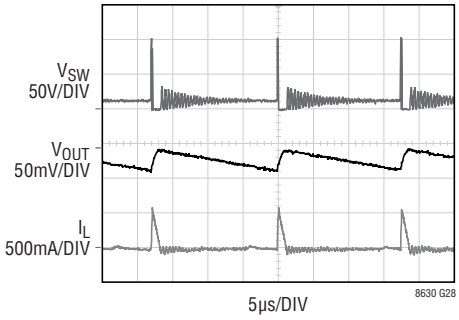
Burst Waveforms



FRONT PAGE APPLICATION
V_{IN} = 24V
LOAD = 10mA

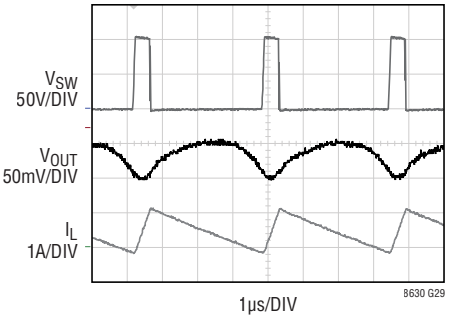
TYPICAL PERFORMANCE CHARACTERISTICS

Burst Waveforms



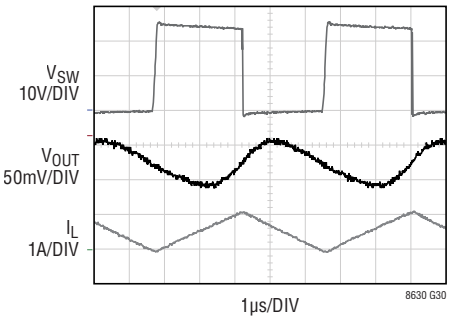
FRONT PAGE APPLICATION
V_{IN} = 100V
LOAD = 50mA

Switching Waveforms



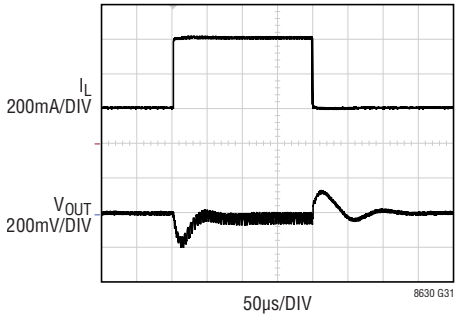
FRONT PAGE APPLICATION
V_{IN} = 100V
LOAD = 500mA

Switching Waveforms



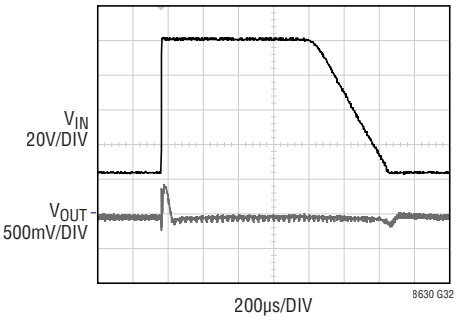
FRONT PAGE APPLICATION
V_{IN} = 24V
LOAD = 500mA

Load Transient Response



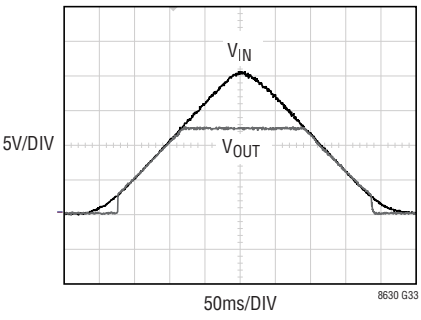
FRONT PAGE APPLICATION
200mA TO 600mA LOAD TRANSIENT
V_{IN} = 48V

Input Voltage Transient Response



FRONT PAGE APPLICATION
I_{LOAD} = 500mA

Start-Up Dropout Performance



FRONT PAGE APPLICATION
I_{LOAD} = 500mA

PIN FUNCTIONS

V_{IN} (Pin 1): The V_{IN} pin powers the internal control circuitry and is monitored by an undervoltage lockout comparator. The V_{IN} pin is also connected to the drain of the on chip power switch. The V_{IN} pin has high dI/dt edges and must be decoupled to the GND pin of the device. The input decouple capacitor should be placed as close as possible to the V_{IN} and GND pins.

EN/UV (Pin 3): The EN/UV pin is used to enable the LT8630 or to program the undervoltage lockout threshold with external resistors. The LT8630 is in shutdown mode(I_Q < 5µA) when the EN/UV pin voltage is below 1.18V and active mode when the voltage exceeds 1.18V. Tie EN/UV to the V_{IN} pin if the EN/UV feature isn't required.

PG (Pin 5): The PG pin is an open drain output that sinks current when the feedback voltage deviates from the regulation point by ±7.5%. The PG pin has 1.6% of hysteresis.

NC6 (Pin 6): No Internal Connection. Leave this pin open or connect to GND.

DNC (Pin 7): Do Not Connect. Do not connect this pin, allow it to float.

RT (Pin 8): A 8.66k resistor must be connected between the RT pin and GND. The R_T resistor sets an internal clock reference. Do not leave pin floating.

NC9 (Pin 9): No Internal Connection. Leave this pin open or connect to GND.

TR/SS (Pin 10): A capacitor with a minimum value of 100pF must be connected between the TR/SS pin and the GND pin. The voltage ramp rate on the TR/SS pin determines the output voltage ramp rate. This pin can also be used for voltage tracking. Do not leave this pin floating.

FB (Pin 11): The FB pin is the negative input to the error amplifier. The output switches to regulate this pin to 0.808V with respect to the GND pin.

V_{OUT} (Pin 12): The V_{OUT} pin is the output to the internal sense resistor that measures current flowing in the inductor. Connect the output capacitor from the V_{OUT} pin to the GND pin.

NC13 (Pin 13): No Internal Connection. Leave this pin open or connect to GND.

IND (Pin 14): The IND pin is the input to the internal sense resistor that measures current flowing in the inductor.

NC15 (Pin 15): No Internal Connection. Leave this pin open or connect to GND.

$INTV_{CC}$ (Pin 16): The $INTV_{CC}$ pin is the bypass pin for the internal 3V regulator. Connect a 2.2µF bypass capacitor from the $INTV_{CC}$ pin to the GND pin. Do not load the $INTV_{CC}$ pin with external circuitry.

BST (Pin 18): The BST pin is used to provide a drive voltage, higher than the V_{IN} voltage, to the topside power switch. Place a 0.1µF capacitor between the BST and SW pins as close as possible to the device.

SW (Pin 20): The SW pin is the output of the internal power switches. Place the inductor and BST capacitor as close as possible to keep the SW PCB trace short.

GND (Exposed Pad Pin 21): The exposed pad GND pin is the *ONLY GROUND CONNECTION* for the device. The exposed pad should be soldered to a large copper area to reduce thermal resistance. The GND pin also serves as small signal ground. For ideal operation all small signal ground paths should connect to the GND pin at a single point avoiding any high current ground returns.

BLOCK DIAGRAM

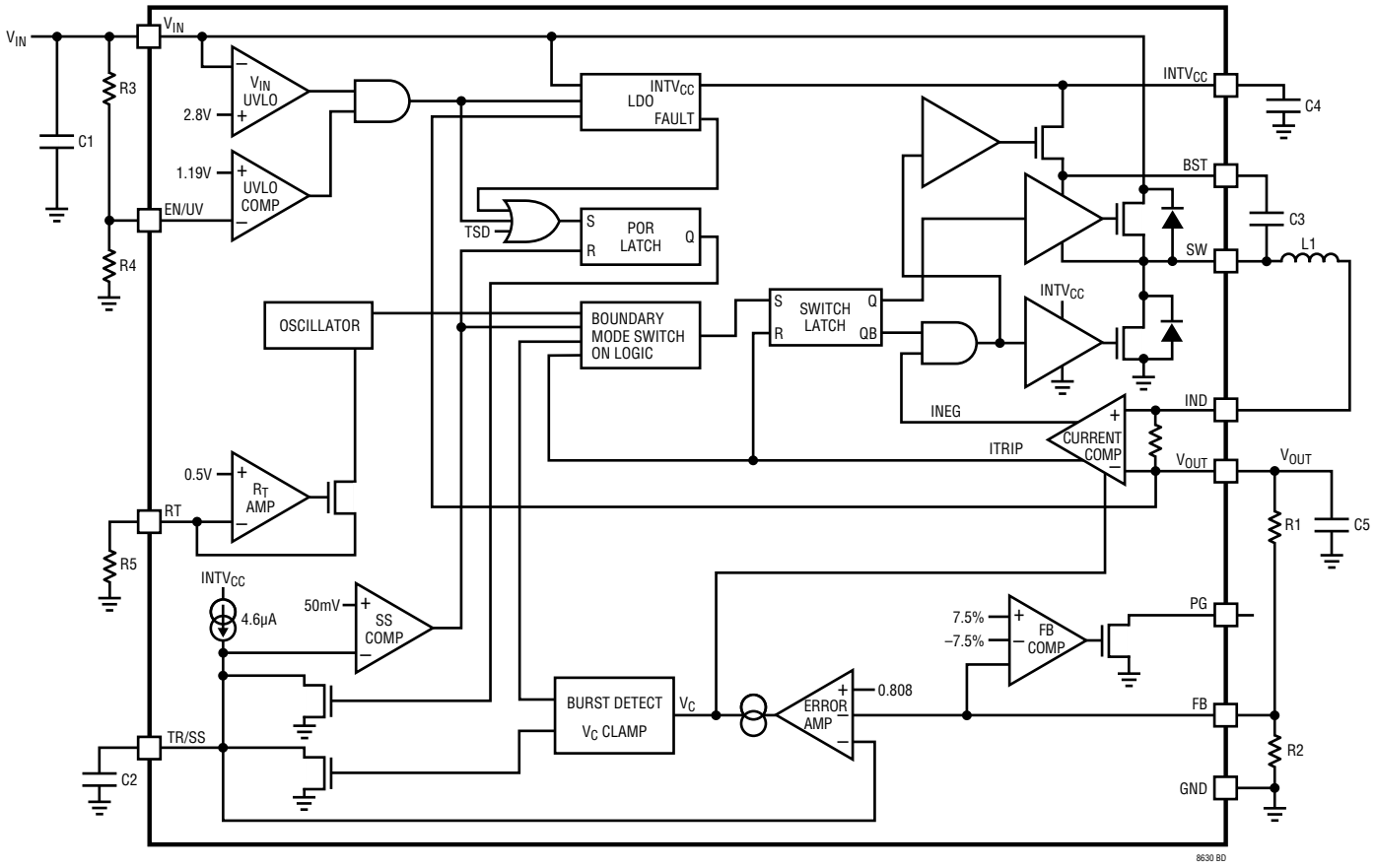


Figure 1. Block Diagram

OPERATION

The LT8630 is a monolithic, variable frequency, current mode step-down DC/DC converter. When the voltage on the EN/UV pin is below its 1.19V threshold, the LT8630 is shutdown and draws less than 5µA from the input supply. When the EN/UV pin is driven above 1.19V, the internal bias circuits turn on generating an internal regulated voltage, 0.808V feedback reference, a 4.5µA soft-start current reference, and a power on reset (POR) signal.

During power-up the POR signal is set and in turn sets the soft-start latch. When the soft-start latch is set, the TR/SS pin will be discharged to ground to ensure proper start-up operation. When the TR/SS pin drops below 50mV, the soft-start latch is reset. Once the latch is reset the soft-start capacitor starts to charge with a typical value of 4.5µA.

The error amplifier is a transconductance amplifier that compares the FB pin voltage to the lowest voltage present at either the TR/SS pin or an internal 0.808V reference. Since the TR/SS pin is driven by a constant current source, a single capacitor on the soft-start pin will generate a controlled linear ramp on the output voltage. The voltage on the output of the error amplifier (internal VC node in Figure 1) sets the peak current of each switch cycle and also determines when to enable low quiescent current Burst Mode operation.

When the voltage on the VC node rises above the switching threshold, the internal clock set-pulse sets the driver flip-flop, which turns on the internal top power switch. This causes current from V_{IN}, through the top switch, inductor, and internal sense resistor, to increase. When the voltage drop across the internal sense resistor exceeds a predetermined level set by the voltage on the internal VC node, the flip-flop is reset and the internal top switch is turned off. Once the top switch is turned off the inductor will drive the voltage on the SW pin low. The synchronous power switch will turn on, decreasing the current in the inductor until the reverse current comparator trips, indicating that the inductor current is close to zero. If the VC voltage is still above the switching threshold, the top power switch is turned on again and another cycle commences.

Comparators monitoring the FB pin voltage will pull the PG pin low if the output voltage varies more the ±7.5% from the feedback reference voltage. The PG comparators have 1.9% of hysteresis.

Provided that the output voltage is in regulation (as determined by the PG comparators), the LT8630 maximizes efficiency across a wide range of input voltages by employing a boundary mode switching scheme that minimizes switching losses. The boundary mode switching cycle is comprised of three stages: a top-switch ON phase, a bottom-switch ON phase, and a discontinuous ring phase. Figure 2 shows an example of boundary mode operation. At the beginning of a switch cycle, the internal top side power switch is turned on at the peak of the SW node discontinuous ring. The current then flows from V_{IN}, through the top switch, inductor, and internal sense resistor to the output. Once the voltage drop across the internal sense resistor exceeds a predetermined level set by the voltage on the internal VC node, the top switch is turned off. Inductor current ceases to flow through the top switch; instead, inductor current discharges the switch node capacitance. The switch node voltage is quickly driven below ground and caught by the bottom switch body diode. The bottom-switch ON phase begins with the internal low side power switch turning on with nearly zero drain-source voltage. Energy is delivered to the output as the inductor current decreases from its peak down to zero. Once the current through the internal sense resistor reaches zero, the bottom switch turns off and the switch node discontinuous ring phase begins. The inductor resonates with the stray capacitance on the switch node and causes a discontinuous ring. If the VC voltage is still above the switching threshold, the top power switch is turned on again at the peak of the discontinuous ring and another cycle commences. The switching frequency during boundary mode operation is determined by the inductor value, input voltage, output voltage, and output current.

The regulator's maximum output current occurs when the internal VC node is driven to its maximum clamp value by the error amplifier. The value of the typical maximum

OPERATION

switch current is 1.8A. If the current demanded by the output exceeds the maximum current dictated by the internal VC clamp, the TR/SS pin will be discharged, lowering the regulation point until the output voltage can be supported by the maximum current. Once the overload condition is removed, the regulator will soft-start from the overload regulation point.

EN/UV pin control or thermal shutdown will set the soft-start latch, resulting in a complete soft-start sequence.

In light load situations (low VC voltage) , the LT8630 operates in Burst Mode to optimize efficiency. Between bursts, all circuitry associated with controlling the output switch is shut down reducing the input supply current to 16µA. In a typical application, 16µA will be consumed from the input supply when regulating with no load.

To improve efficiency across all loads, supply current to internal circuitry is sourced from the V_{OUT} pin when it's biased at 3.5V or above. If the V_{OUT} pin is below 3.5V the internal supply current is sourced from V_{IN}.

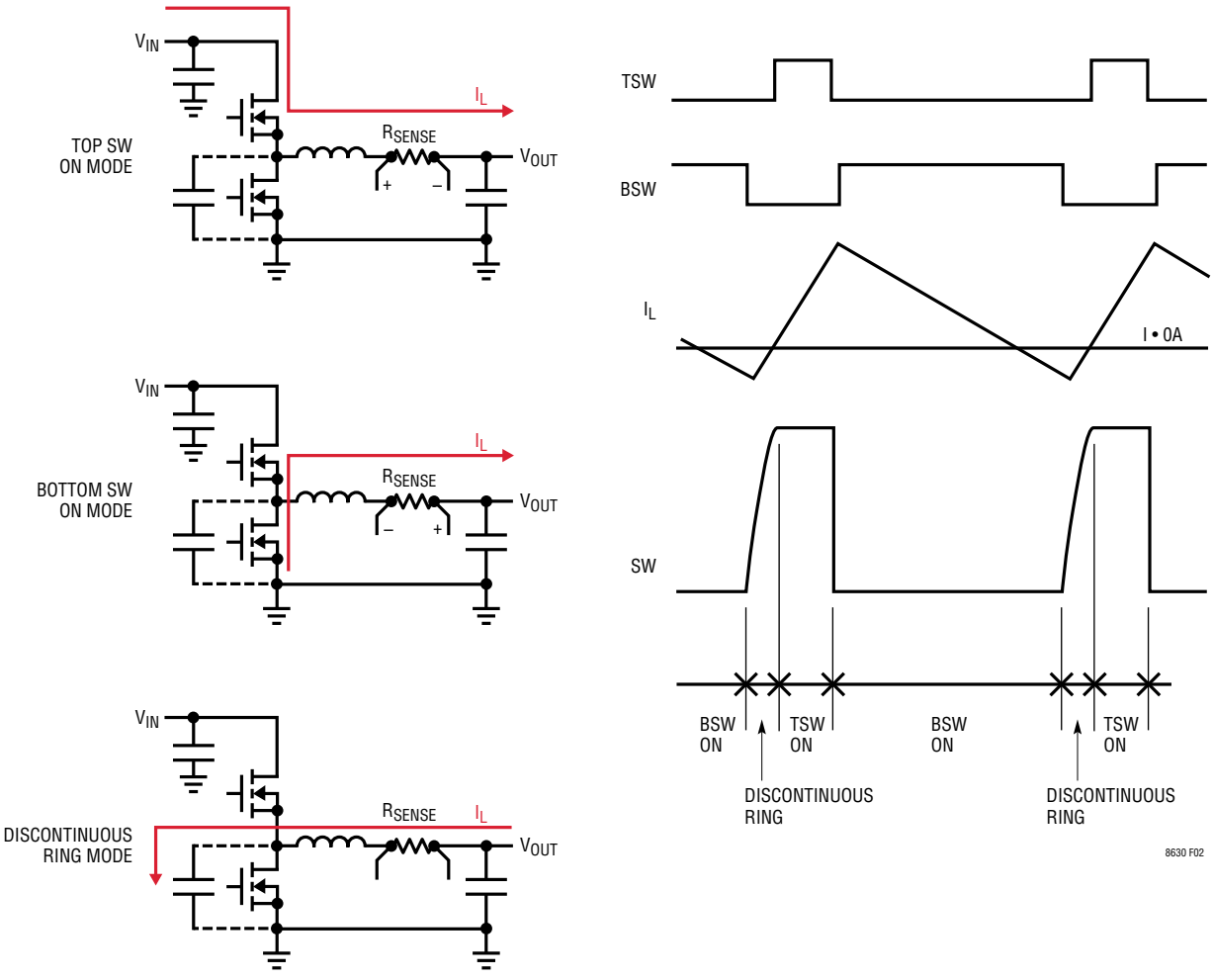


Figure 2

APPLICATIONS INFORMATION

Achieving Low Quiescent Current

To enhance efficiency at light loads, the LT8630 operates in low ripple Burst Mode operation, which keeps the output capacitor charged to the desired output voltage while minimizing the input quiescent current and output voltage ripple. In Burst Mode operation the LT8630 delivers single small pulses of current to the output capacitor followed by sleep periods where the output power is supplied by the output capacitor. While in sleep mode the LT8630 consumes 16µA.

As the output load decreases, the frequency of single current pulses decreases (see Figure 3) and the percentage of time the LT8630 is in sleep mode increases, resulting in much higher light load efficiency than for typical converters. By maximizing the time between pulses, the converter quiescent current approaches 16µA for a typical application when there is no output load. Therefore, to optimize the quiescent current performance at light loads, the current in the feedback resistor divider must be minimized as it appears to the output as a load current.

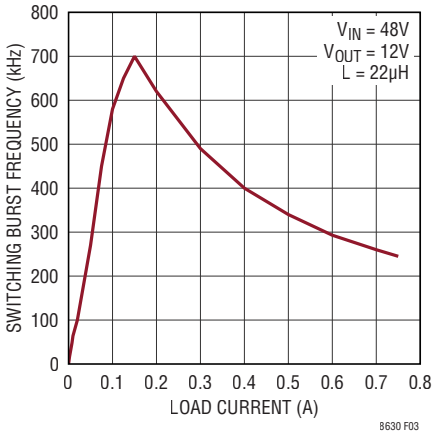


Figure 3. Frequency vs Load Current

While in Burst Mode operation the peak inductor current is approximately 280mA resulting in output voltage ripple shown in Figure 4. Increasing the output capacitance will decrease the output ripple proportionately. As load ramps upward from zero the switching frequency will increase until the LT8630 automatically enters boundary mode operation. The output load at which the LT8630 transitions into boundary mode varies based on input voltage, output voltage, and inductor choice.

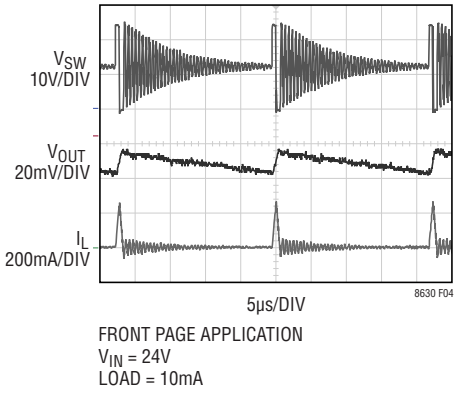


Figure 4. Burst Mode Operation

Choosing the Output Voltage

The output voltage is programmed with a resistor divider between the output and the FB pin. Choose the 1% resistors according to:

$$R1 = R2\left(\frac{V_{OUT}}{0.808} - 1\right)$$

Reference designators refer to the Block Diagram in Figure 1.

If low input quiescent current and good light-load efficiency are desired, use large resistor values for the FB resistor divider. The current flowing in the divider acts as a load

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current, and will increase the no-load input current to the converter, which is approximately:

$$I_Q = I_{QVIN} + \left(I_{QVOUT} + \left(\frac{V_{OUT}}{R1+R2} \right) \right) \bullet \left(\frac{V_{OUT}}{V_{IN}} \right) \bullet \left(\frac{1}{n} \right)$$

where I_{QVIN} is the quiescent current of the LT8630 and the second term is the quiescent current drawn from the output (Iqvout) plus current in the feedback divider reflected to the input of the buck operating at its light load efficiency n. For a 5V application with R1 = 1MΩ and R2 = 191kΩ, the feedback divider draws 4.2µA. With V_{IN} = 12V I_{QVIN} = 3.6µA, I_{QVOUT} = 10µA and n = 50%, the no-load quiescent current is approximately 16µA. For applications with output voltages less than 3.5V, I_{QVOUT} = 0µA and I_{QVIN} is typically 16µA. Graphs of I_{QVIN} and I_{QVOUT} vs V_{OUT} are in the Typical Performance Characteristics section.

When using FB resistors greater than 200k, a 4.7pF to 22pF phase lead capacitor should be connected from V_{OUT} to FB.

Dropout Operation

If the input voltage falls below $V_{IN(MIN)}$ (dropout mode), the LT8630 will automatically reduce the switching frequency to obtain the highest possible output voltage. The lower limit on the switching frequency in dropout mode is determined by the boost threshold. When the voltage between the BST and SW pins is less than the boost threshold, a minimum off-time pulse is generated to recharge the boost capacitor.

Inductor Selection and Maximum Output Current

The inductor, along with the input voltage, output voltage, and load current, determines the LT8630's switching frequency. Higher efficiency is generally achieved with a larger inductor value, which produces a lower frequency. For a given inductor type, however, as inductance is increased, DC resistance (DCR) also increases. Higher DCR translates into higher copper losses and lower current rating, both of which place an upper limit on the inductance.

A good first choice for the inductor value is 22µH. This value represents a good trade-off between a high switching frequency and high efficiency.

For applications with reduced load current or maximum input voltage requirements, a smaller inductance value may be used. However, an additional constraint on the inductor value is the LT8630's minimum discontinuous ring time interval. Use a minimum inductor value of 15µH for proper boundary mode operation.

Once the value for L is known, the type of inductor must be selected. High efficiency converters generally cannot afford the core loss found in low cost powdered iron cores, forcing the use of ferrite cores. Ferrite designs have very low core loss and are preferred at high switching frequencies, so design goals can concentrate on copper loss and preventing saturation. Ferrite core material saturates hard, which means that inductance collapses abruptly when the peak design current is exceeded. The LT8630 safely tolerates operation with a saturated inductor through the use of a high speed current mode architecture. However, inductor saturation results in an abrupt increase in inductor ripple current, power dissipation, and output voltage ripple. In order to avoid inductor overheating and poor efficiency, an inductor should be chosen with a saturation current rating greater than the 2.7A maximum peak current limit of the LT8630.

Maximum Output Current

The maximum output current depends on V_{IN}, V_{OUT}, the effective switch node capacitance, and the inductor value. Provided that the inductor value is at least 15µH, the LT8630 will deliver at least 600mA of output current.

A more accurate guaranteed output current can be found from:

$$\text{OUTPUT CURRENT(A)} = \frac{1}{2} \bullet \left(1.8\text{A} - \frac{V_{IN} - V_{OUT}}{\sqrt{(L / C)}} \right)$$

Where L is the output inductor value and C is the effective switch node capacitance (nominally 140pF).

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Input Capacitor Selection

Bypass the LT8630 input with a 2.2µF or higher ceramic capacitor of X7R or X5R type placed as close as possible to the V_{IN} pin and ground. Y5V types have poor performance over temperature and applied voltage, and should not be used. Note that larger input capacitance is required when a lower switching frequency is used. If the input power source has high impedance, or there is significant inductance due to long wires or cables, additional bulk capacitance may be necessary. This can be provided with a low performance electrolytic capacitor.

A word of caution regarding the use of ceramic capacitors at the input. A ceramic input capacitor can combine with stray inductance to form a resonant tank circuit. If power is applied quickly (for example, by plugging the circuit into a live power source) this tank can ring, doubling the input voltage and damaging the LT8630. The solution is to either clamp the input voltage or dampen the tank circuit by adding a lossy capacitor in parallel with the ceramic capacitor. For details, see Application Note 88.

Output Capacitor Selection

The output capacitor has two essential functions. Along with the inductor, it filters the square wave generated by the LT8630 to produce the DC output. In this role it determines the output ripple, thus low impedance at the switching frequency is important. The second function is to store energy in order to satisfy transient loads and stabilize the LT8630's control loop. Since the LT8630 uses current mode control, it does not require the presence of output capacitor series resistance (ESR) for stability. Low ESR or ceramic capacitors should be used to achieve very low output ripple and small circuit size.

A 47µF, X5R or X7R ceramic capacitor with a voltage rating greater than the desired output voltage is an excellent first choice for most applications. The 47µF output capacitor will provide low output ripple with good transient response. Increasing the value will reduce the output voltage ripple and improve transient response, but may increase application cost and require more board space. Decreasing the value may save cost and board space but will increase output voltage ripple, degrade transient performance, and may cause loop instability. Increasing or decreasing the output capacitor may require increasing or decreasing the 4.7pF feedforward capacitor placed between the V_{OUT} and FB pins to optimize transient response. See the Typical Applications section in the data sheet for suggested output and feedforward capacitor values.

Note that even X5R and X7R type ceramic capacitors have a DC bias effect which reduces their capacitance when a DC voltage is applied. It is not uncommon for capacitors offered in the smallest case sizes to lose more than 50% of their capacitance when operated near their rated voltage. As a result it is sometimes necessary to use a larger capacitance value, larger case size, or use a higher voltage rating in order to realize the intended capacitance value. Consult the manufacturer's data for the capacitor you select to be assured of having the necessary capacitance for the application.

Ceramic Capacitors

Ceramic capacitors are small, robust, and have very low ESR. However, ceramic capacitors can cause problems when used with the LT8630 due to their piezoelectric nature. When in Burst Mode operation, the LT8630's switching frequency depends on the load current, and at very light loads the LT8630 can excite the ceramic capacitor at audio frequencies, generating audible noise. Since the LT8630 operates at a lower current limit during Burst Mode operation, the noise is typically very quiet to the casual ear. If this noise in unacceptable, use a high performance tantalum or electrolytic capacitor at the output. Low noise ceramic capacitors are also available.

Enable Pin

The LT8630 is in shutdown when the EN/UV pin is low and active when the pin is high. The rising threshold of the EN/UV comparator is 1.19V, with 17mV of hysteresis. The EN/UV pin can be tied to V_{IN} if the shutdown feature is not used, or tied to a logic level if shutdown control is required.

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Adding a resistor divider from V_{IN} to EN/UV programs the LT8630 to regulate the output only when V_{IN} is above a desired voltage (see the Block Diagram). Typically, the EN/UV threshold is used in situations where the supply is current limited, or has a relatively high source resistance. A switching regulator draws constant power from the source, so source current increases as source voltage drops. This looks like a negative resistance load to the source and can cause the source to current limit or latch low under low source voltage conditions. The EN/UV threshold prevents the regulator from operating at source voltages where the problems might occur. This threshold can be adjusted by setting the values R3 and R4 such that they satisfy the following equation:

$$V_{EN\ THRESHOLD} = \left(\frac{R3}{R4} + 1\right) \bullet 1.19V$$

where the LT8630 will remain off until V_{IN} is above the EN/UV threshold. Due to the comparator's hysteresis, switching will not stop until the input falls slightly below the threshold voltage.

When operating in Burst Mode operation for light load currents, the current through the EN/UV resistor network can easily be greater than the supply current consumed by the LT8630. Therefore, the EN/UV resistors should be large to minimize their effect on efficiency at low loads.

$INTV_{CC}$ Regulator

An internal low dropout (LDO) regulator produces the 3V supply from V_{IN} that powers the drivers and the internal bias circuitry. The $INTV_{CC}$ can supply enough current for the LT8630's circuitry and must be bypassed to ground with a minimum of 2.2µF ceramic capacitor. Good bypassing is necessary to supply the high transient currents required by the power MOSFET gate drivers. To improve efficiency, the internal regulator draws power from the V_{OUT} pin when the output voltage is 3.5V or higher. If the V_{OUT} pin is below 3.5V, the internal regulator will consume current from V_{IN}. Applications with high input voltage and high switching frequency where the internal regulator pulls current from V_{IN} will increase die temperature because of the higher power dissipation across the regulator. Do not connect an external load to the $INTV_{CC}$ pin.

Soft-Start and Output Voltage Tracking

The LT8630 regulates its output to the lowest voltage present at either the TR/SS pin or an internal 0.808V reference. A capacitor from the TR/SS pin to ground is charged by an internal 4.5µA current source resulting in a linear output ramp from 0V to the regulated output whose duration is given by:

$$T_{RAMP} = \frac{C_{TR/SS} \bullet 0.808V}{4.5\mu A}$$

At power-up, a reset signal (POR) sets the soft-start latch and discharges the TR/SS pin to approximately 0V to ensure proper start-up. The TR/SS pin has a maximum current sink capability of 230µA. If the TR/SS pin is used as a track function for an external voltage, the maximum sink current must not be exceeded during startup. Exceeding the maximum TR/SS sink current will inhibit operation.

When the TR/SS pin is fully discharged, the latch is reset and the internal 4.5µA current source starts to charge the TR/SS pin. When the TR/SS pin voltage is below ~50mV, the V_C pin is pulled low which disables switching.

As the TR/SS pin voltage rises above 50mV, the V_C pin is released and the output voltage is regulated to the TR/SS voltage. When the TR/SS pin voltage exceeds the internal 808mV reference, the output is regulated to the reference. The TR/SS pin voltage will continue to rise to ~3V.

The soft-start latch is set during several fault conditions: EN/UV pin is below 1.19V, $INTV_{CC}$ has fallen too low, V_{IN} is too low, or thermal shutdown. Once the latch is set, the TR/SS pin will discharge to ~0V and a new startup sequence will begin.

If the load exceeds the maximum output switch current, the output will start to drop causing the internal V_C clamp to be activated. As long as the V_C node is clamped, the TR/SS pin will be discharged. As a result, the output will be

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regulated to the highest voltage that the maximum output current can support. For example, if the output on the front page application is loaded by 4Ω the TR/SS pin will drop to 0.48V, regulating the output at 3V. Once the overload condition is removed, the output will soft-start from the temporary voltage level to the normal regulation point.

Since the TR/SS pin is pulled up to the 3V rail and has to discharge to 0.808V before taking control of regulation, momentary overload conditions will be tolerated without a sort-start recovery. The typical time before the TR/SS pin takes control is:

$$T_{TR/SS(CONTROL)} = \frac{C_{TR/SS} \bullet 2.2V}{30\mu A}$$

Output Power Good

When the LT8630's output voltage is within the ±7.5% window of the regulation point (V_{FBREF}) , typically 0.74V to 0.86V, the output voltage is considered good and the open-drain PG pin is a high impedance node, and is typically pulled high with an external resistor. Otherwise, the internal pull-down device will pull the PG pin low. To prevent glitching both the upper and lower thresholds include 1.9% of hysteresis.

The PG pin is also actively pulled low during several fault conditions: EN/UV pin is below 1.19V, V_{IN} undervoltage, or thermal shutdown.

Shorted and Reverse Input Protection

If the inductor is chosen so that it won't saturate excessively, the LT8630 will tolerate a shorted output.

There is another situation to consider in systems where the output will be held high when the input to the LT8630 is absent. This may occur in battery charging applications or in battery back-up systems where a battery or some other supply is diode ORed with the LT8630's output. If the V_{IN} pin is allowed to float and the EN/UV pin is held high (either by a logic signal or because it is tied to V_{IN}), then the LT8630's internal circuitry will pull its quiescent current through its SW pin. This is acceptable if the system can tolerate ~6mA in this state. If the EN pin is grounded the SW pin current will drop to near 5µA. However, if the V_{IN} pin is grounded while the output is held high, regardless of EN, parasitic body diodes inside the LT8630 can pull current from the output through the SW pin and the V_{IN} pin. Figure 5 shows a connection of the V_{IN} and EN/UV pins that will allow the LT8630 to run only when the input voltage is present and that protects against a shorted or reversed input.

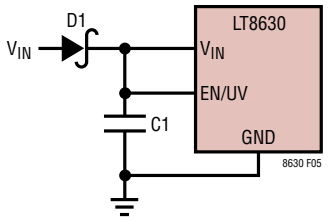


Figure 5. Reverse Input Voltage Protection

PCB Layout

For proper operation and minimum EMI, care must be taken during printed circuit board layout. Figure 6 shows the recommended component placement with trace, ground plane, and via locations. Note that large, switched currents flow in the LT8630's V_{IN} pin and the input capacitor (C1). The loop formed by the input capacitor should be as small as possible by placing the capacitor adjacent to the V_{IN} pin and ground plane. When using a physically large input capacitor the resulting loop may become too large in which case using a small case/value capacitor placed close to the V_{IN} pin and ground plane plus a larger capacitor further away is preferred. These components, along with the inductor and output capacitor, should be placed on the same side of the circuit board, and their connections should be made on that layer. Place a local, unbroken ground plane under the application circuit on the layer closest to the surface layer. The SW and BST nodes should be as small as possible. Finally, keep the FB and RT nodes

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small so that the ground traces will shield them from the SW and BST nodes. The exposed pan on the bottom of the package must be soldered to ground so that the pad is connected to ground electrically and also acts as a heat sink thermally. To keep thermal resistance low, extend the ground plane as much as possible, and add thermal vias under and near the LT8630 to additional ground planes within the circuit board and on the bottom side.

High Temperature Considerations

For higher ambient temperatures, care should be taken in the layout of the PCB to ensure good heat sinking of the LT8630. The exposed pad on the bottom of the package must be soldered to a ground plane. This ground should be tied to large copper layers below with thermal vias; these layers will spread heat dissipated by the LT8630.

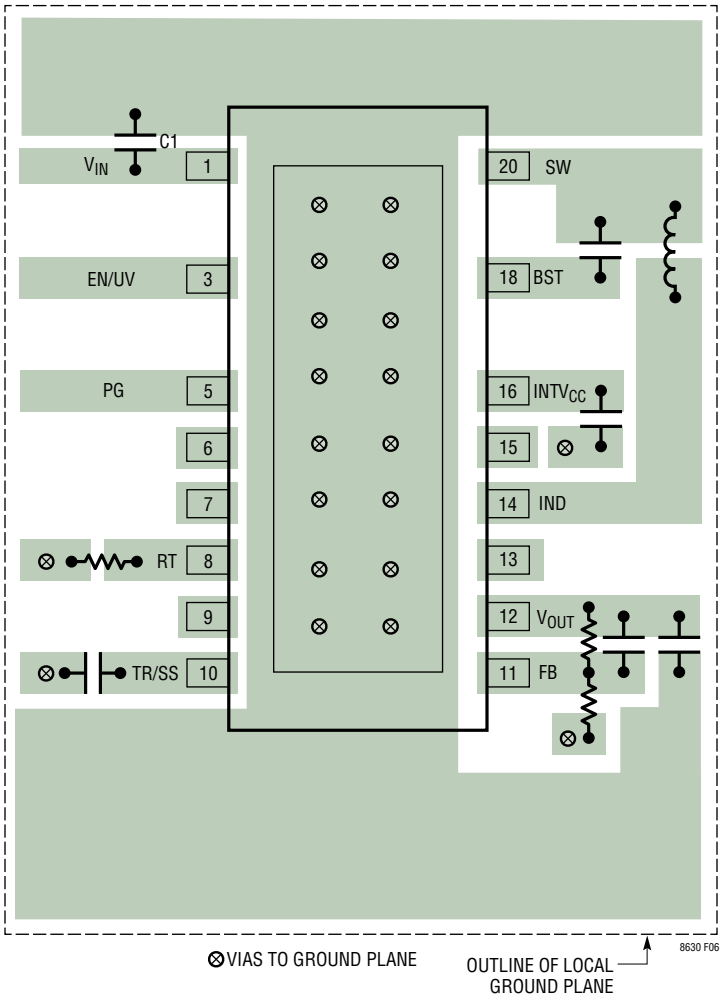


Figure 6. Recommended PCB Layout for the LT8630

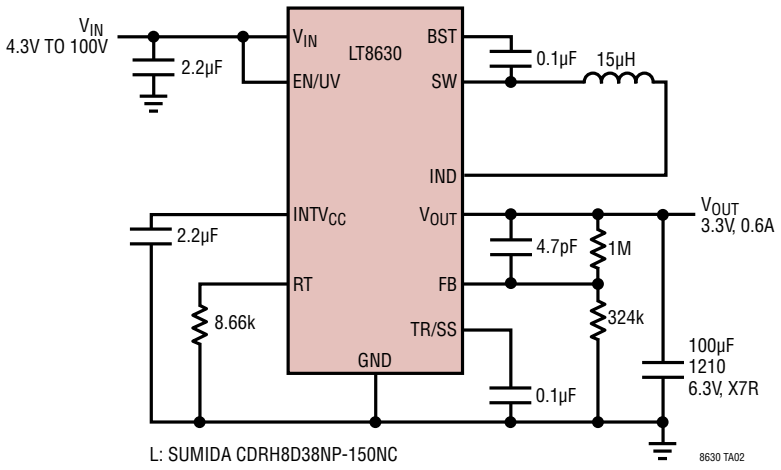
APPLICATIONS INFORMATION

Placing additional vias can reduce thermal resistance further. The maximum load current should be derated as the ambient temperature approaches the maximum junction rating. Power dissipation within the LT8630 can be estimated by calculating the total power loss from an efficiency measurement and subtracting the inductor loss. The die temperature is calculated by multiplying the LT8630 power dissipation by the thermal resistance from junction to ambient.

If safe junction temperature is exceeded, the LT8630 will shutdown and restart with a POR sequence.

APPLICATIONS INFORMATION

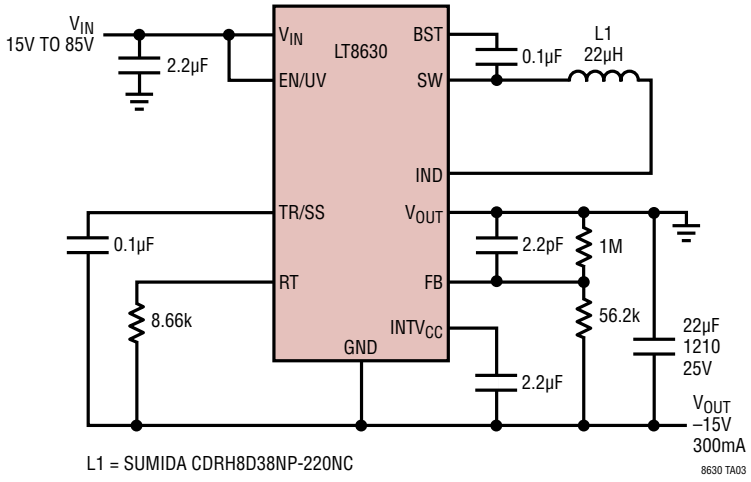
3.3V, 0.6A Step-Down Converter



L: SUMIDA CDRH8D38NP-150NC

PIN NOT USED IN THIS CIRCUIT: PG

–15V, 300mA Step-Down Converter

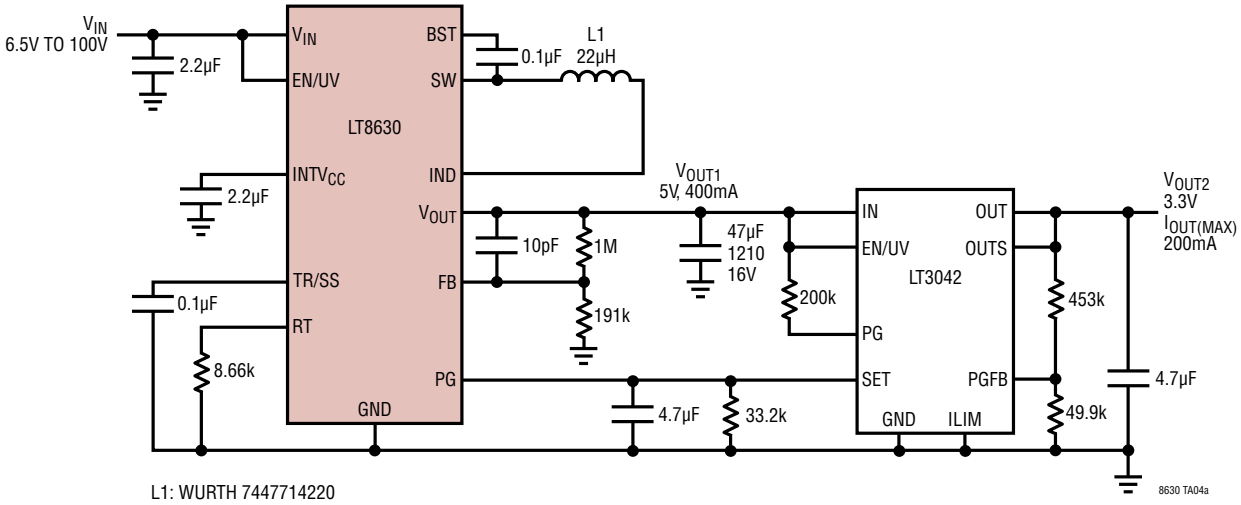


L1 = SUMIDA CDRH8D38NP-220NC

PIN NOT USED IN THIS CIRCUIT: PG

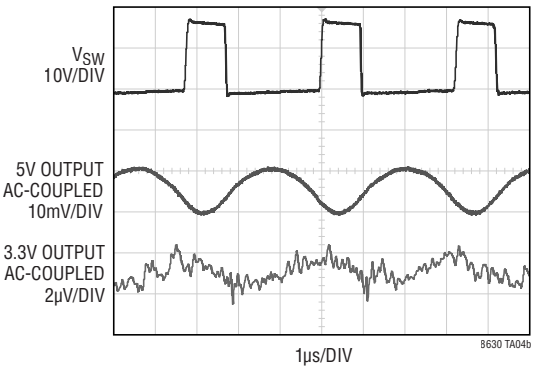
TYPICAL APPLICATIONS

Wide Input 5V and Ultralow Noise 3V Step-Down Converter



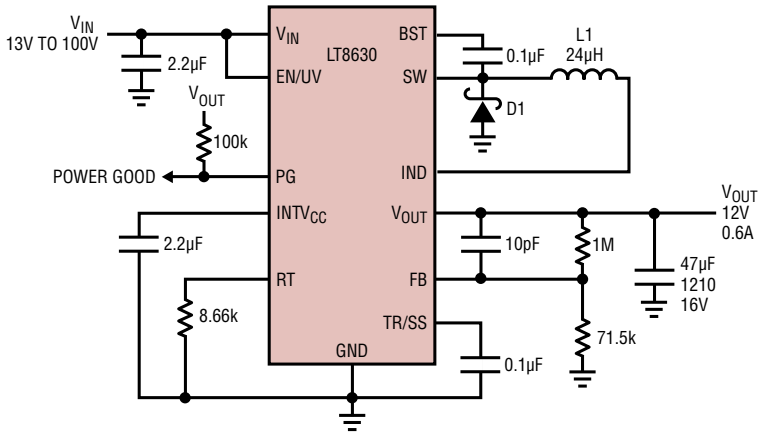
L1: WURTH 7447714220

Wide Input 5V and Ultralow Noise 3.3V Application



TYPICAL APPLICATIONS

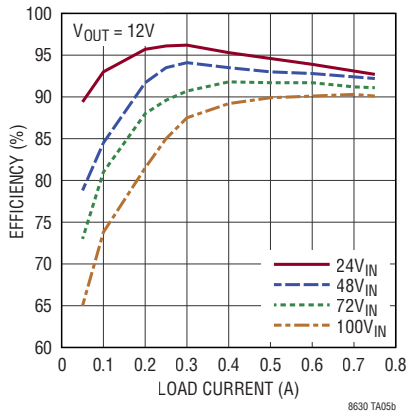
High Efficiency 12V Step-Down Converter



D1: VISHAY SS2PH10
L1: B65807JR49 EPCOS RM6 CORE WITH 0.2mm CENTERPOLE GAP
NINE TURNS 60/38G LITZ WIRE

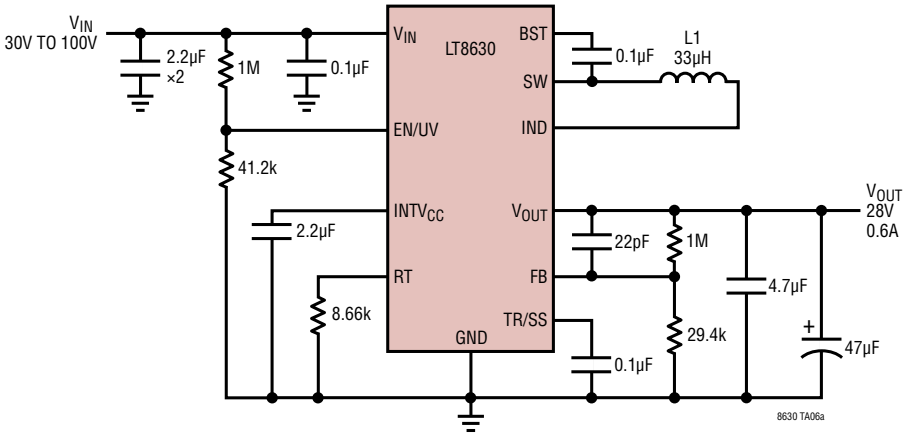
8630 TA05a

Efficiency vs Load Current



8630 TA05b

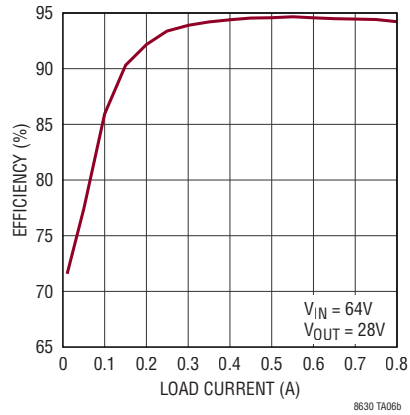
28V Step-Down Converter



L: WURTH 7447714330

8630 TA06a

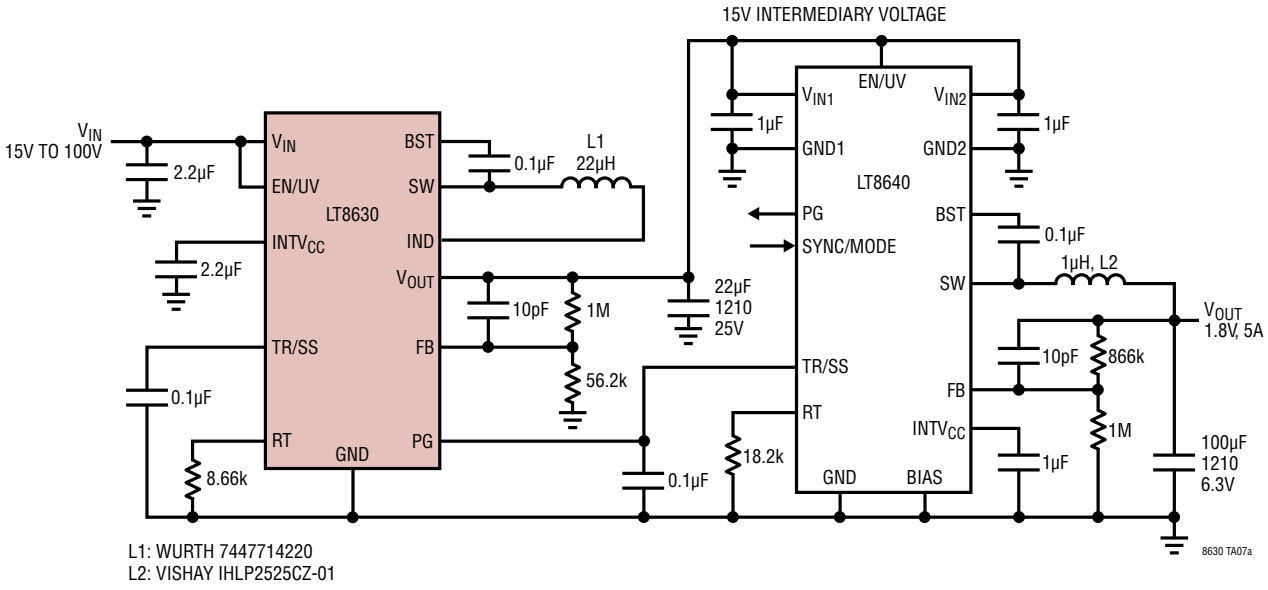
LT8630 Efficiency



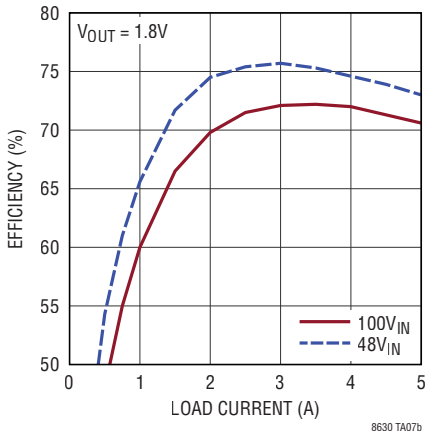
8630 TA06b

TYPICAL APPLICATIONS

Low EMI High Step-Down Ratio 1.8V/5A Converter



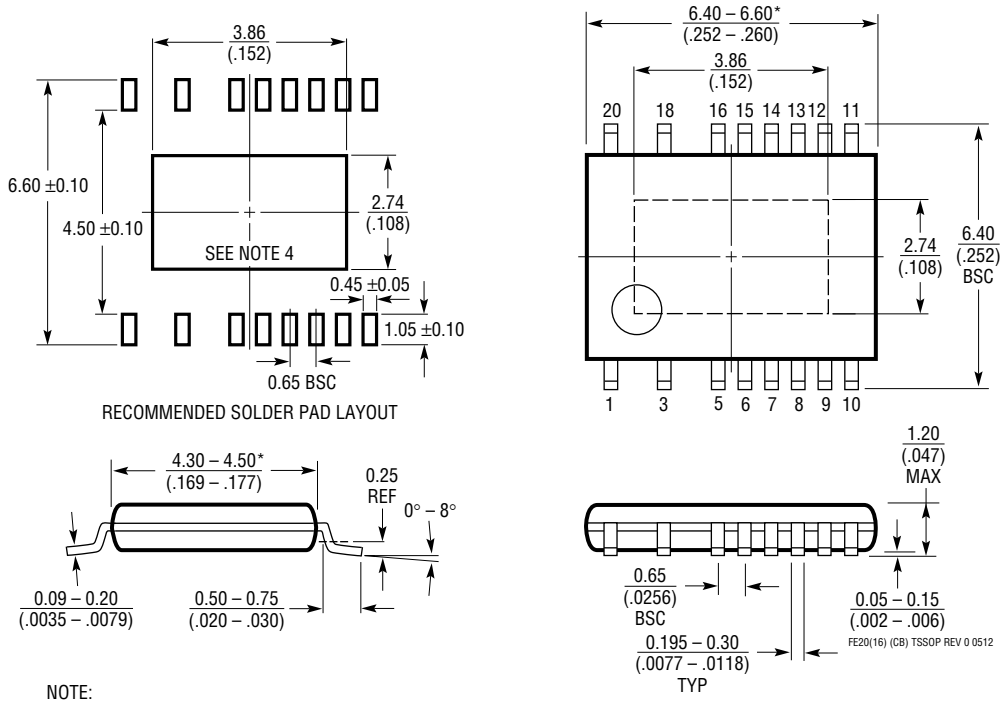
Efficiency for Cascaded LT8630/LT8640 Converter



PACKAGE DESCRIPTION

Please refer to http://www.linear.com/product/LTC8630#packaging for the most recent package drawings.

FE Package
Variation: FE20(16)
20-Lead Plastic TSSOP (4.4mm)
(Reference LTC DWG # 05-08-1924 Rev Ø)
Exposed Pad Variation CB

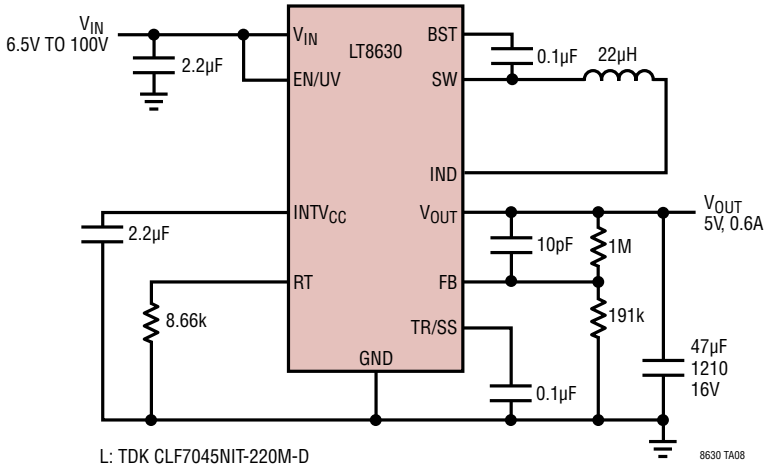


NOTE:
1. CONTROLLING DIMENSION: MILLIMETERS
2. DIMENSIONS ARE IN $\frac{\text{MILLIMETERS}}{(\text{INCHES})}$
3. DRAWING NOT TO SCALE
4. RECOMMENDED MINIMUM PCB METAL SIZE FOR EXPOSED PAD ATTACHMENT
*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.150mm (.006") PER SIDE

Information furnished by Linear Technology Corporation is believed to be accurate and reliable. However, no responsibility is assumed for its use. Linear Technology Corporation makes no representation that the interconnection of its circuits as described herein will not infringe on existing patent rights.

TYPICAL APPLICATION

5V/0.6A Step-Down Converter



L: TDK CLF7045NIT-220M-D

PIN NOT USED IN THIS CIRCUIT: PG

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT8631	100V/1A Micropower Step-Down DC/DC Converter with I_Q = 15µA	V_{IN}: 3V to 100V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 7µA, I_{SD} < 5µA, HV, TSSOP-20E
LT8620	65V, 2A, Synchronous Step-Down DC/DC, Converter	V_{IN}: 3.4V to 65V, $V_{OUT(MIN)}$ = 0.97V, I_Q = 2.5µA, I_{SD} < 1mA, MSOP-16E and 3mm × 5mm QFN Packages
LT3991	55V, 1.2A, Synchronous Micropower Step-Down DC/DC, Converter with I_Q = 2.8µA	V_{IN}: 4.2V to 55V, $V_{OUT(MIN)}$ = 1.20V, I_Q = 2.8µA, I_{SD} < 1µA, 3mm × 3mm DFN-10 and MSOP-10E Packages
LT8610	42V, 2.5A, High Efficiency Micropower Step-Down DC/DC, Converter with I_Q = 2.5µA	V_{IN}: 3.4V to 42V, $V_{OUT(MIN)}$ = 0.97V, I_Q: 2.5µA, I_{SD}: <1µA, TSSOP16E
LT8614	42V, 4A, High Efficiency Micropower Step-Down DC/DC, Converter with I_Q = 1.7µA	V_{IN}: 3.4V to 42V, $V_{OUT(MIN)}$ = 0.97V, I_Q: 1.7µA, I_{SD}: <1µA, QFN-18
LTC®3630A	76V, 500mA Synchronous Step-Down DC/DC Converter	V_{IN}: 4V to 76V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 12µA, I_{SD} = 3µA, 3mm × 5mm DFN-16, MSOP-16(12)E
LTC3637	76V, 1A Nonsynchronous Step-Down DC/DC Converter	V_{IN}: 4V to 76V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 12µA, I_{SD} = 3µA, 3mm × 5mm DFN-16, MSOP-16(12)E
LTC3638	140V, 250mA Synchronous Step-Down DC/DC Converter	V_{IN}: 4V to 140V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 12µA, I_{SD} < 1mA, MSOP-16E Package
LTC3639	150V, 100mA Synchronous Step-Down Regulator	V_{IN}: 4V to 150V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 12µA, I_{SD} = 1.4µA, MSOP-16(12)E

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