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FSDM1265RB

Green Mode Fairchild Power Switch (FPS™)

Features

- Internal Avalanche Rugged Sense FET
- Advanced Burst-Mode operation that consumes less than 1 W at 240VAC and 0.5W load
- Precision Fixed Operating Frequency (66kHz)
- Internal Start-up Circuit
- Improved Pulse by Pulse Current Limiting
- Over-Voltage Protection (OVP)
- Over-Load Protection (OLP)
- Internal Thermal Shutdown Function (TSD)
- Auto-Restart Mode
- Under Voltage Lock Out (UVLO) with Hysteresis
- Low Operating Current (2.5mA)
- Built-in Soft Start

Application

- SMPS (Switch Mode Power Supplies) for LCD monitor and STB
- Adapter

Description

The FSDM1265RB is an integrated Pulse-Width Modulator (PWM) and a SenseFET which is specifically designed for high performance offline SMPS with minimal external components. This device is an integrated high-voltage power switching regulator which combines a rugged avalanche Sense FET with a current mode PWM control block. The PWM controller includes integrated fixed frequency oscillator, under-voltage lockout, leading edge blanking (LEB), optimized gate driver, internal soft-start, and precise current sources that are temperature compensated for loop compensation and self protection circuitry. Compared with discrete MOSFET and PWM controller solution, it can reduce total cost, component count, size, and weight, while simultaneously increasing efficiency, productivity, and system reliability. This device is a basic platform which is well suited for cost effective designs of flyback converters.

OUTPUT POWER TABLE(4)				
PRODUCT	230VAC ±15%(3)		85-265VAC	
	Adapter(1)	Open Frame(2)	Adapter(1)	Open Frame(2)
FSDM0565RB	60W	70W	50W	60W
FSDM0565RBI	60W	70W	50W	60W
FSDM07652RB	70W	80W	60W	70W
FSDM1265RB	90W	110W	80W	90W

Table 1. Maximum Output Power

Notes:

1. Typical continuous power in a non-ventilated enclosed adapter measured at 50°C ambient.
2. Maximum practical continuous power in an open- frame design at 50°C ambient.
3. 230 VAC or 100/115 VAC with doubler.
4. The junction Temperature can limit the Maximum output power.

Typical Circuit

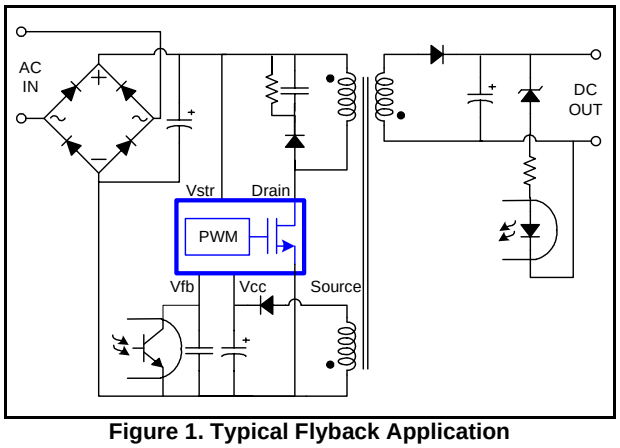


Figure 1. Typical Flyback Application

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Internal Block Diagram

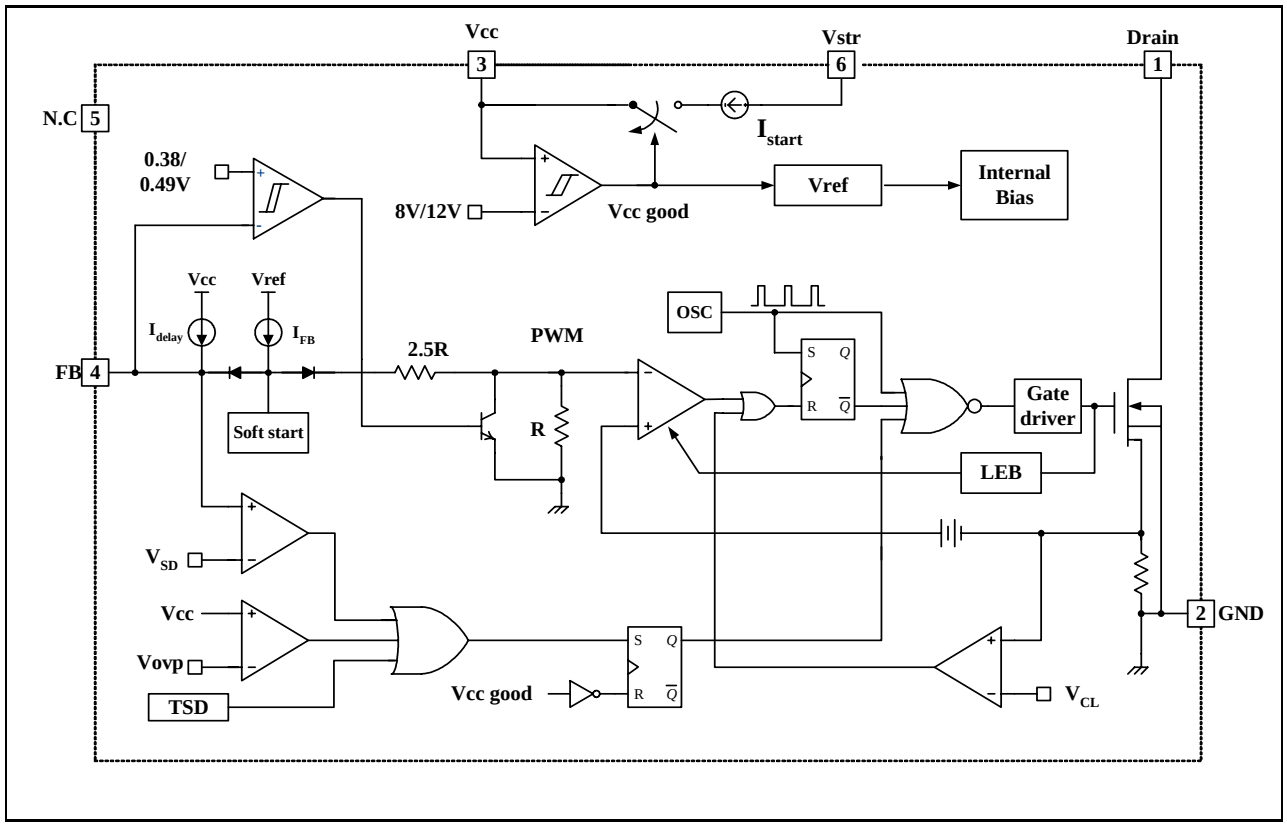


Figure 2. Functional Block Diagram of FSDM1265RB

Pin Definitions

Pin Number	Pin Name	Pin Function Description
1	Drain	This pin is the high voltage power Sense FET drain. It is designed to drive the transformer directly.
2	GND	This pin is the control ground and the Sense FET source.
3	Vcc	This pin is the positive supply voltage input. During startup, the power is supplied by an internal high voltage current source that is connected to the Vstr pin. When Vcc reaches 12V, the internal high voltage current source is disabled and the power is supplied from the auxiliary transformer winding.
4	Vfb	This pin is internally connected to the inverting input of the PWM comparator. The collector of an opto-coupler is typically tied to this pin. For stable operation, a capacitor should be placed between this pin and GND. Once the pin reaches 6.0V, the overload protection is activated resulting in the shutdown of the FPS^{TM}.
5	N.C	
6	Vstr	This pin is connected directly to the high voltage DC link. At startup, the internal high voltage current source supplies internal bias and charges the external capacitor that is connected to the Vcc pin. Once Vcc reaches 12V, the internal current source is disabled.

Pin Configuration

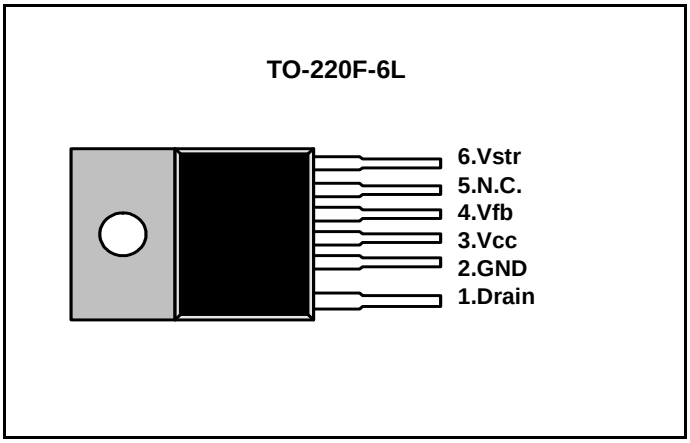


Figure 3. Pin Configuration (Top View)

Absolute Maximum Ratings

(Ta=25°C, unless otherwise specified)

Parameter	Symbol	Value	Unit
Drain-source Voltage	V_{DSS}	650	V
Vstr Max. Voltage	V_{STR}	650	V
Pulsed Drain Current (Tc=25°C)(1)	I_{DM}	15.9	A_{DC}
Continuous Drain Current(Tc=25°C)	I_D	5.3	A
Continuous Drain Current(Tc=100°C)		3.4	A
Supply Voltage	V_{CC}	20	V
Input Voltage Range	V_{FB}	-0.3 to V_{CC}	V
Total Power Dissipation (Tc=25°C with Infinite Heat Sink)	P_D	50	W
Operating Junction Temperature	T_j	Internally limited	°C
Operating Ambient Temperature	T_A	-25 to +85	°C
Storage Temperature Range	T_{STG}	-55 to +150	°C
ESD Capability, HBM Model (All Pins except for Vstr and Vfb)	-	2.0 (GND-Vstr/Vfb=1.5kV)	kV
ESD Capability, Machine Model (All Pins except for Vstr and Vfb)	-	300 (GND-Vstr/Vfb=225V)	V

Notes:

1. Repetitive rating: Pulse width limited by maximum junction temperature

Thermal Impedance

Parameter	Symbol	Package	Value	Unit
Junction-to-Case Thermal	θ_{JC}(1)	TO-220F-6L	2.5	°C/W

Notes:

1. Infinite cooling condition - Refer to the SEMI G30-88.

Electrical Characteristics

(Ta = 25°C unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Sense FET SECTION						
Drain-source breakdown voltage	BV_{DSS}	V_{GS} = 0V, I_D = 250μA	650	-	-	V
Zero gate voltage drain current	I_{DSS}	V_{DS} = 650V, V_{GS} = 0V	-	-	500	μA
		V_{DS}= 520V V_{GS} = 0V, T_C = 125°C	-	-	500	μA
Static drain source on resistance	$R_{DS(ON)}$	V_{GS} = 10V, I_D = 2.5A	-	0.75	0.9	Ω
Output capacitance	C_{OSS}	V_{GS} = 0V, V_{DS} = 25V, f = 1MHz	-	78	-	pF
Turn-on delay time	$T_{D(ON)}$	V_{DD}= 325V, I_D= 5A	-	42	-	ns
Rise time	T_R		-	106	-	
Turn-off delay time	$T_{D(OFF)}$		-	330	-	
Fall time	T_F		-	110	-	
CONTROL SECTION						
Initial frequency	F_{OSC}	V_{FB} = 3V	60	66	72	kHz
Voltage stability	F_{STABLE}	13V ≤ Vcc ≤ 18V	0	1	3	%
Temperature stability (1)	ΔF_{OSC}	-25°C ≤ Ta ≤ 85°C	0	±5	±10	%
Maximum duty cycle	D_{MAX}	-	77	82	87	%
Minimum duty cycle	D_{MIN}	-	-	-	0	%
Start threshold voltage	V_{START}	V_{FB}=GND	11	12	13	V
Stop threshold voltage	V_{STOP}	V_{FB}=GND	7	8	9	V
Feedback source current	I_{FB}	V_{FB}=GND	0.7	0.9	1.1	mA
Soft-start time	T_S	Vfb=3	-	10	15	ms
Leading edge blanking time	T_{LEB}	-	-	250	-	ns
BURST MODE SECTION						
Burst mode voltages(1)	V_{BURH}	Vcc=14V	0.3	0.38	0.46	V
	V_{BURL}	Vcc=14V	0.39	0.49	0.59	V

Electrical Characteristics (Continued)

(Ta = 25°C unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
PROTECTION SECTION						
Peak current limit (2)	I_{OVER}	V_{FB}=5V, V_{CC}=14V	3.0	3.4	3.8	A
Over voltage protection (OVP)	V_{OVP}	-	18	19	20	V
Thermal shutdown temperature (1)	T_{SD}		130	145	160	°C
Shutdown feedback voltage	V_{SD}	$V_{FB} \geq 5.5V$	5.5	6.0	6.5	V
Shutdown delay current	I_{DELAY}	V_{FB}=5V	2.8	3.5	4.2	µA
TOTAL DEVICE SECTION						
Operating supply current (3)	I_{OP}	V_{FB}=GND, V_{CC}=14V	-	2.5	5	mA
	$I_{OP(MIN)}$	V_{FB}=GND, V_{CC}=10V				
	$I_{OP(MAX)}$	V_{FB}=GND, V_{CC}=18V				

Notes:

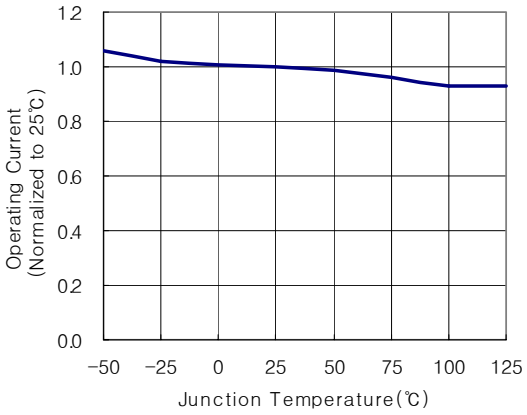
1. These parameters, although guaranteed at the design level, are not tested in mass production.
2. These parameters indicate the inductor current.
3. This parameter is the current flowing into the control IC.

Comparison of FS6M12653RTC and FSDM1265RB

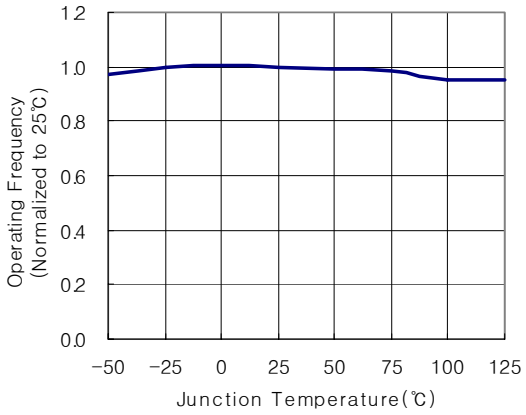
Function	FS6M12653RTC	FSDM1265RB	FSDM1265RB Advantages
Soft-Start	Adjustable soft-start time using an external capacitor	Typical Internal soft-start of 10ms (fixed)	• Gradually increasing current limit during soft-start reduces peak current and voltage component stresses • Eliminates external components used for soft-start in most applications • Reduces or eliminates output overshoot
Burst Mode Operation	• Built into controller • Output voltage drops to about half	• Built into controller • Output voltage fixed	• Improves ight-load efficiency • Reduces no-load consumption

Typical Performance Characteristics

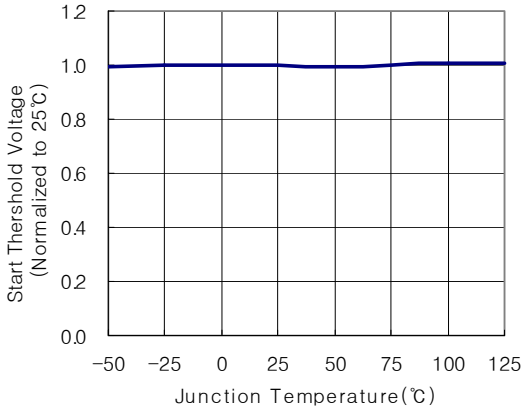
(These Characteristic Graphs are Normalized at Ta= 25°C)



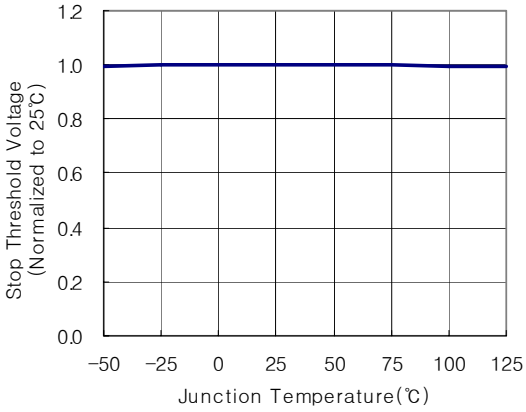
Operating Current vs. Temperature



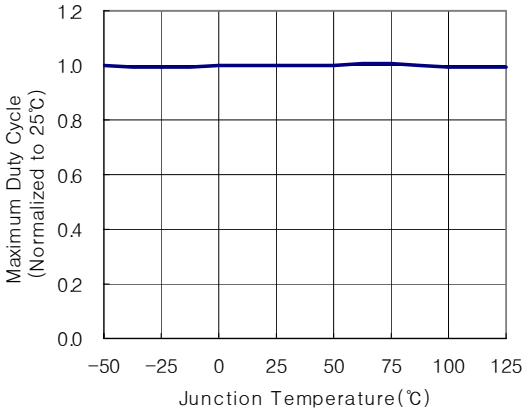
Operating Freqency vs. Temperature



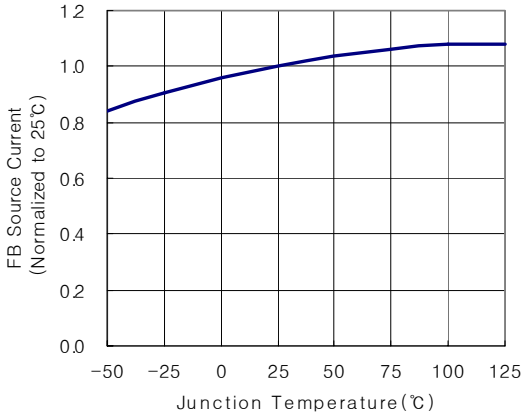
Start Threshold Voltage vs. Temperature



Stop Threshold Voltage vs. Temperature



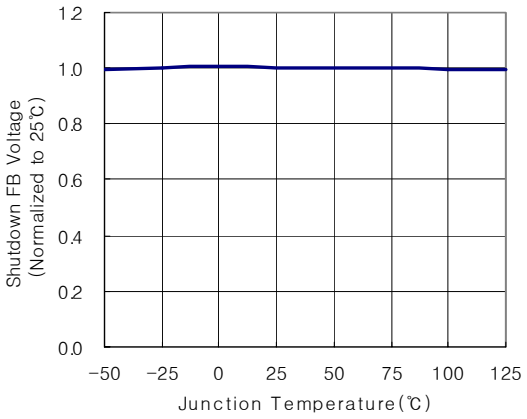
Maximum Duty vs. Temperature



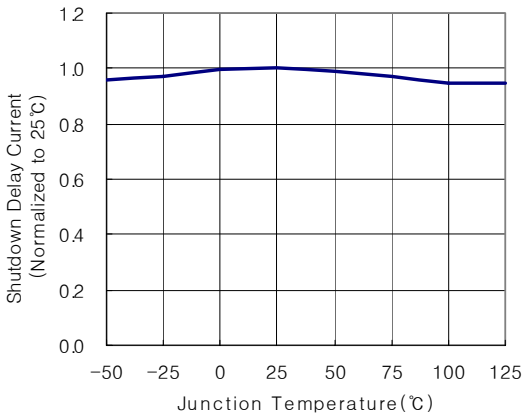
Feedback Source Current vs. Temperature

Typical Performance Characteristics (Continued)

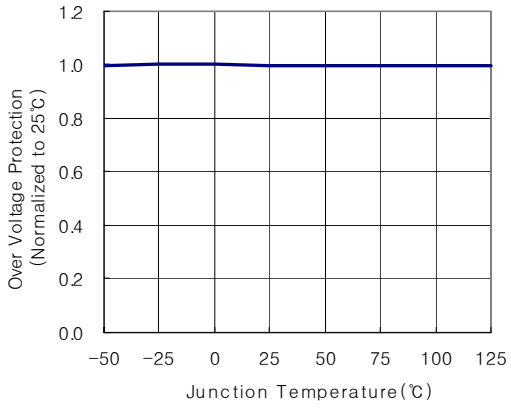
(These Characteristic Graphs are Normalized at Ta= 25°C)



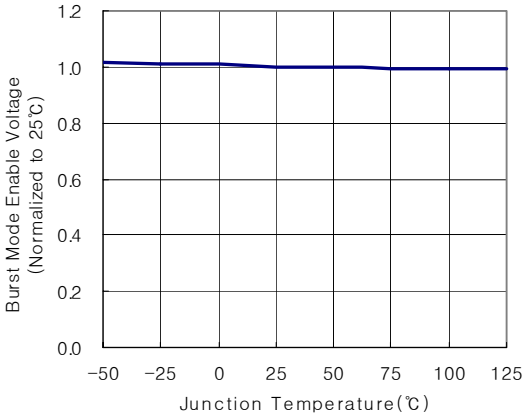
ShutDown Feedback Voltage vs. Temperature



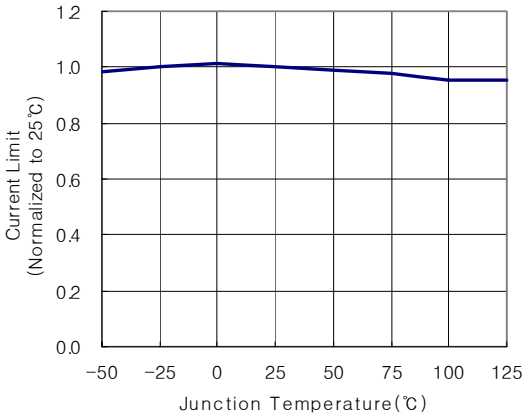
ShutDown Delay Current vs. Temperature



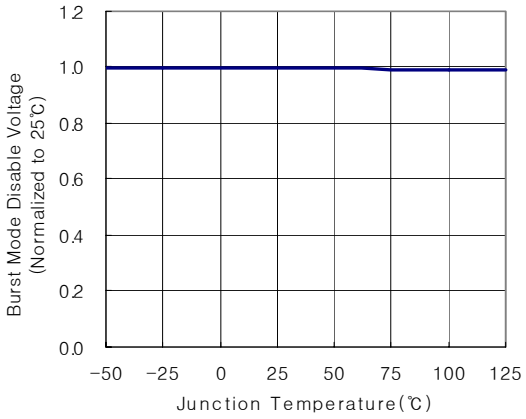
Over Voltage Protection vs. Temperature



Current Limit VS. Temperature



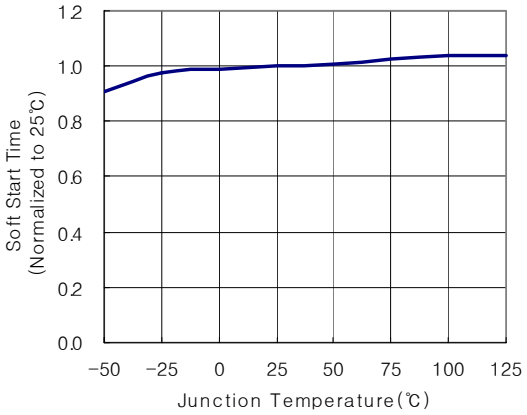
Burst Mode Enable Voltage vs. Temperature



Burst Mode Disable Voltage vs. Temperature

Typical Performance Characteristics (Continued)

(These Characteristic Graphs are Normalized at Ta= 25°C)



Soft-start Time vs. Temperature

Functional Description

1. Star-tup: In previous generations of Fairchild Power Switches (FPS^{TM}), the Vcc pin had an external start-up to the DC input voltage line. In the newer switches, the startup resistor is replaced by an internal high voltage current source. At startup, an internal high voltage current source supplies the internal bias and charges the external capacitor (C_{VCC}) that is connected to the Vcc pin as illustrated in Figure 4. When the Vcc pin reaches 12V, the FSDM1265RB begins switching and the internal high voltage current source is disabled. Then, the FSDM1265RB continues its normal switching operation and the power is supplied from the auxiliary transformer winding unless Vcc goes below the stop voltage of 8V.

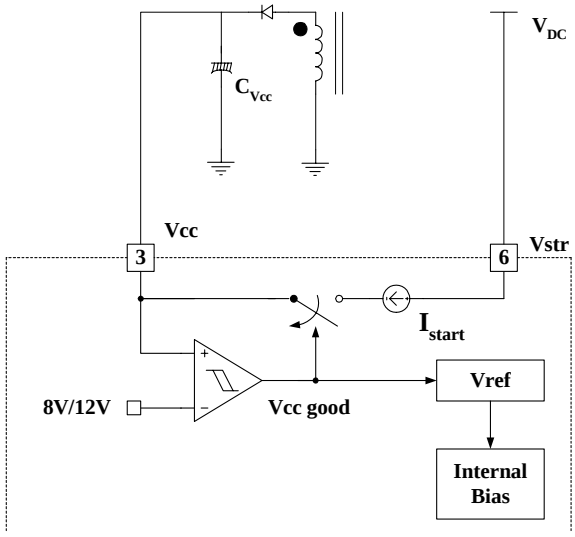


Figure 4. Internal startup circuit

2. Feedback Control: FSDM1265RB employs current mode control, as shown in Figure 5. An opto-coupler (such as the H11A817A) and shunt regulator (such as the KA431) are typically used to implement the feedback network. Comparing the feedback voltage with the voltage across the Rsense resistor in addition to the offset voltage makes it possible to control the switching duty cycle. When the reference pin voltage of the KA431 exceeds the internal reference voltage of 2.5V, the H11A817A LED current increases, thereby pulling down the feedback voltage and reducing the duty cycle. Typically this happens when the input voltage is increased or the output load is decreased.

2.1 Pulse-by-pulse current limit: Because current mode control is employed, the peak current through the Sense-FET is limited by the inverting input of PWM comparator (Vfb*) as shown in Figure 5. Assuming that the 0.9mA current source flows only through the internal resistor (2.5R +R= 2.8 kΩ), the cathode voltage of diode D2 is about 2.5V. Since D1 is blocked when the feedback voltage (Vfb) exceeds 2.5V, the maximum voltage of the cathode of D2 is clamped at this voltage, thus clamping Vfb*. Therefore, the peak value of the current through the Sense FET is limited.

2.2 Leading edge blanking (LEB): When the internal Sense FET is turned on, usually the reverse recovery of the primary-side capacitance and the secondary-side rectifier causes a high current spike through the SenseFET. causes Excessive voltage across the Rsense resistor can lead to incorrect feedback operation in the current mode PWM control. To counter this effect, the FSDM1265RB employs a leading edge blanking (LEB) circuit. This circuit inhibits the PWM comparator for a short time (T_{LEB}) after the SenseFET is turned on.

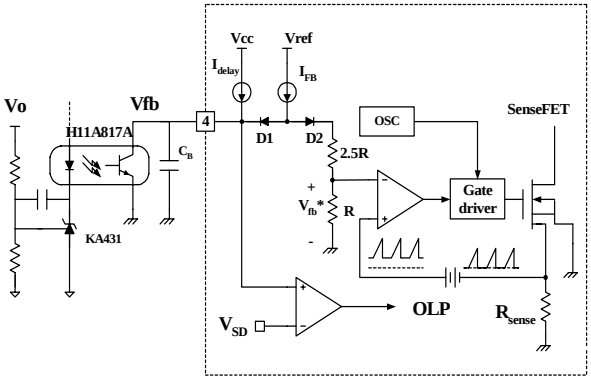


Figure 5. Pulse width modulation (PWM) circuit

3. Protection Circuit: The FSDM1265RB has several self protective functions such as overload protection (OLP), over voltage protection (OVP) and thermal shutdown (TSD). Because these protection circuits are fully integrated into the IC without external components, the reliability can be improved without increasing cost. Once the fault condition occurs, switching is terminated and the SenseFET remains off. This causes Vcc to fall. When Vcc reaches the UVLO stop voltage (8V), the protection is reset and the internal high voltage current source charges the Vcc capacitor via the Vstr pin. When the Vcc reaches the UVLO start voltage (12 V), the FSDM1265RB resumes its normal operation. Thus, the auto-restart alternately enables and disables the switching of the power SenseFET until the fault condition is eliminated (see Figure 6).

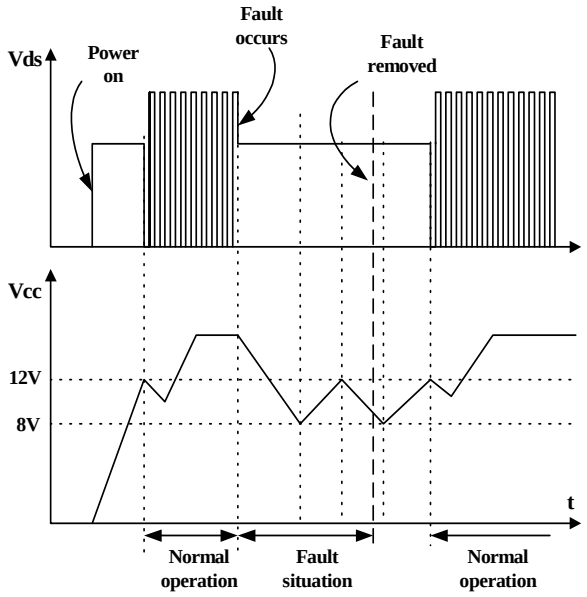


Figure 6. Auto Restart Operation

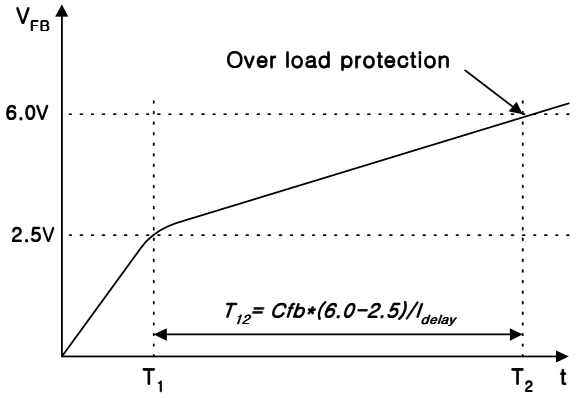


Figure 7. Over Load Protection

3.1 Over Load Protection (OLP): Overload occurs when the load current exceeds a pre-set level due to an unexpected event. The protection circuit (OLP) is activated to protect the SMPS. However, even when the SMPS is operating normally, the OLP circuit can become activate during the load transition. To avoid this undesired operation, the OLP circuit is designed to become activate after a specified time to determine whether it is in a transient or an overload mode. Because of the pulse-by-pulse current limit capability, the maximum peak current through the SenseFET is limited, and therefore the maximum input power is restricted with a given input voltage. If the output consumes beyond this maximum power, the output voltage (Vo) decreases below the set voltage. This reduces the current through the opto-coupler LED, which also reduces the opto-coupler transistor current, thus increasing the feedback voltage

(Vfb). If Vfb exceeds 2.5V, D1 is blocked and the 3.5uA current source slowly starts to charge C_B up to Vcc. In this condition, Vfb continues increasing until it reaches 6V. Then the switching operation terminates as shown in Figure 7. The delay time for shutdown is the time required to charge C_B from 2.5V to 6.0V with 3.5uA. In general, a 10 ~ 50 ms delay is typical for most applications.

3.2 Over voltage Protection (OVP): If the secondary side feedback circuit malfunctions or a solder defect causes an open in the feedback path, the current through the opto-coupler transistor becomes almost zero. Then, Vfb climbs up in a similar manner to the over load situation forcing the pre-set maximum current to be supplied to the SMPS until the OLP is activated. Because more energy than required is provided to the output, the output voltage may exceed the rated voltage before the OLP is activated, resulting in the breakdown of the devices in the secondary side. In order to prevent this situation, an OVP circuit is used. Generally, Vcc is proportional to the output voltage and the FSDM1265RB uses Vcc instead of directly monitoring the output voltage. If V_{CC} exceeds 19V, an OVP circuit is activated resulting in the termination of the switching operation. In order to avoid undesired activation of OVP during normal operation, Vcc should be designed to be below 19V.

3.3 Thermal Shutdown (TSD): The SenseFET and the control IC are built in one package making it easy for the control IC to detect the heat generated by the SenseFET. When the temperature exceeds approximately 150°C, the thermal shutdown is activated.

4. Soft Start: The FSDM1265RB has an internal soft-start circuit, which increases the PWM comparator and slowly inverts the input voltage together with the SenseFET current, after it starts up. The typical soft-start time is 10ms, The pulse width to the power switching device is progressively increased to establish the correct working conditions for transformers, inductors, and capacitors. The voltage on the output capacitors is progressively increased to smoothly establish the required output voltage. This also helps prevent transformer saturation and reduce the stress on the secondary diode during startup.

5. Burst operation: To minimize power dissipation in the standby mode, the FSDM1265RB enters burst mode operation. As the load decreases, the feedback voltage decreases. As shown

in Figure 8, the device automatically enters burst mode when the feedback voltage drops below V_{BURL}(380mV). At this point switching stops and the output voltages start to drop at a rate dependent on the standby current load. This causes the feedback voltage to rise. Once it passes V_{BURH}(490mV), switching resumes. The feedback voltage then falls and the process repeats. Burst mode operation alternately enables and disables switching of the power SenseFET, thereby reducing switching loss in the Standby mode.

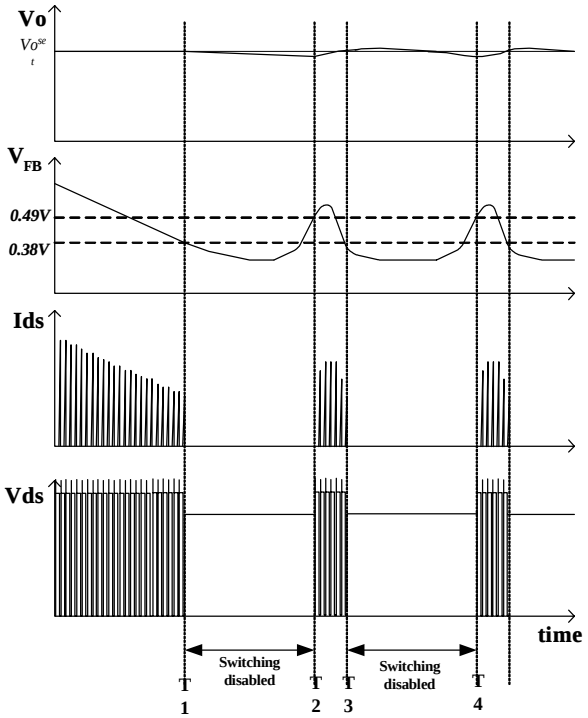


Figure 8. Waveforms of BurstOperation

Typical Application Circuit

Application	Output Power	Input Voltage	Output Voltage (Max. Current)
LCD Monitor	62W	Universal input (85-265Vac)	5V (4.0A) 12V (3.5A)

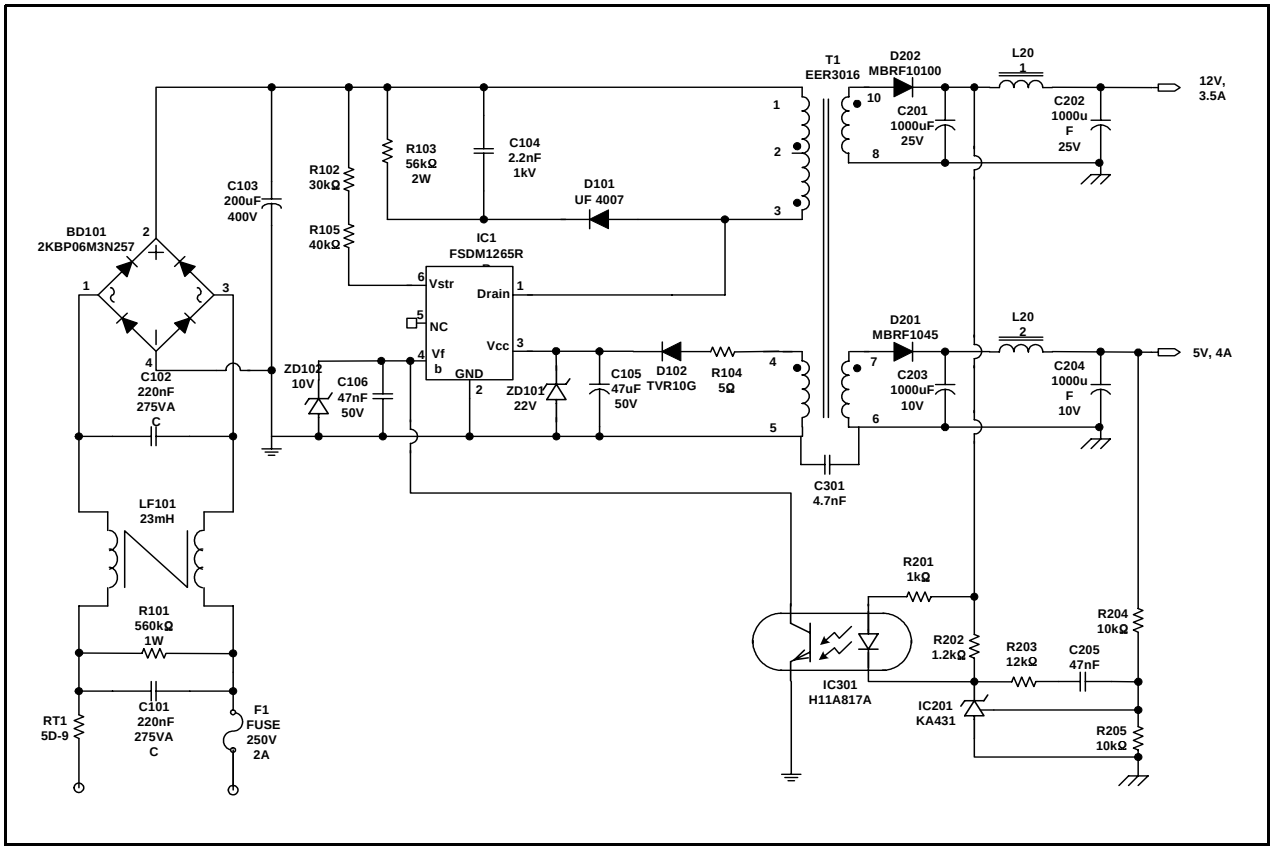
Features

- High efficiency (>81% at 85Vac input)
- Low zero-load power consumption (<300mW at 240Vac input)
- Low standby-mode power consumption (<800mW at 240Vac input and 0.3W load)
- Low component count
- Enhanced system reliability through several protection functions
- Internal soft-start (10ms)

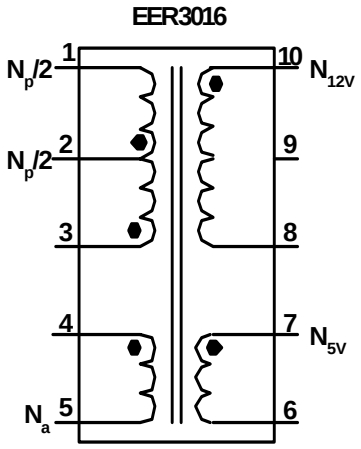
Key Design Notes

- Resistors R102 and R105 are employed to prevent start-up at low input voltage. After start-up, there is no power loss in these resistors since the start-up pin is internally disconnected after start-up.
- The delay time for OLP is designed to be about 50ms with C106 of 47nF. If you require a faster triggering of OLP , reduce the C106 to 10nF.
- Zener diode ZD102 is used for a safety test such as UL. When the drain pin and feedback pin are shorted, the zener diode fails and remains short, which causes the fuse (F1) to blow and prevents explosion of the opto-coupler (IC301). The zener diode also increases immunity against a line surge.

1. Schematic



2. Transformer Schematic Diagram



3.Winding Specification

No	Pin (s→f)	Wire	Turns	Winding Method
Na	4 → 5	$0.2^{\phi} \times 1$	8	Center Winding
Insulation: Polyester Tape t = 0.050mm, 2Layers				
Np/2	2 → 1	$0.4^{\phi} \times 1$	18	Solenoid Winding
Insulation: Polyester Tape t = 0.050mm, 2Layers				
N_{12V}	10 → 8	$0.3^{\phi} \times 3$	7	Center Winding
Insulation: Polyester Tape t = 0.050mm, 2Layers				
N5V	7 → 6	$0.3^{\phi} \times 3$	3	Center Winding
Insulation: Polyester Tape t = 0.050mm, 2Layers				
Np/2	3 → 2	$0.4^{\phi} \times 1$	18	Solenoid Winding
Outer Insulation: Polyester Tape t = 0.050mm, 2Layers				

4.Electrical Characteristics

	Pin	Specifications	Remarks
Inductance	1 - 3	420uH ± 10%	100kHz, 1V
Leakage Inductance	1 - 3	10uH Max.	2^{nd} all short

5. Core & Bobbin

Core: EER 3016
Bobbin: EER3016
Ae(mm2): 96

6.Demo Circuit Part List

Part	Value	Note	Part	Value	Note
Fuse			C301	4.7nF	Polyester Film Cap.
F101	2A/250V				
NTC			**Inductor**		
RT101	5D-9		L201	5uH	Wire 1.2mm
Resistor			L202	5uH	Wire 1.2mm
R101	560K	1W			
R102	30K	1/4W			
R103	56K	2W			
R104	5	1/4W	**Diode**		
R105	40K	1/4W	D101	UF4007	
R201	1K	1/4W	D102	TVR10G	
R202	1.2K	1/4W	D201	MBRF1045	
R203	12K	1/4W	D202	MBRF10100	
R204	10K	1/4W	ZD101	Zener Diode	22V
R205	10K	1/4W	ZD102	Zener Diode	10V
			Bridge Diode		
			BD101	2KBP06M 3N257	Bridge Diode
Capacitor					
C101	220nF/275VAC	Box Capacitor	**Line Filter**		
C102	220nF/275VAC	Box Capacitor	LF101	23mH	Wire 0.4mm
C103	200uF/400V	Electrolytic Capacitor	**IC**		
C104	2.2nF/1kV	Ceramic Capacitor	IC101	FSDM1265RB	FPS^{TM}(12A,650V)
C105	47uF/50V	Electrolytic Capacitor	IC201	KA431(TL431)	Voltage reference
C106	47nF/50V	Ceramic Capacitor	IC301	H11A817A	Opto-coupler
C201	1000uF/25V	Electrolytic Capacitor			
C202	1000uF/25V	Electrolytic Capacitor			
C203	1000uF/10V	Electrolytic Capacitor			
C204	1000uF/10V	Electrolytic Capacitor			
C205	47nF/50V	Ceramic Capacitor			

7. Layout

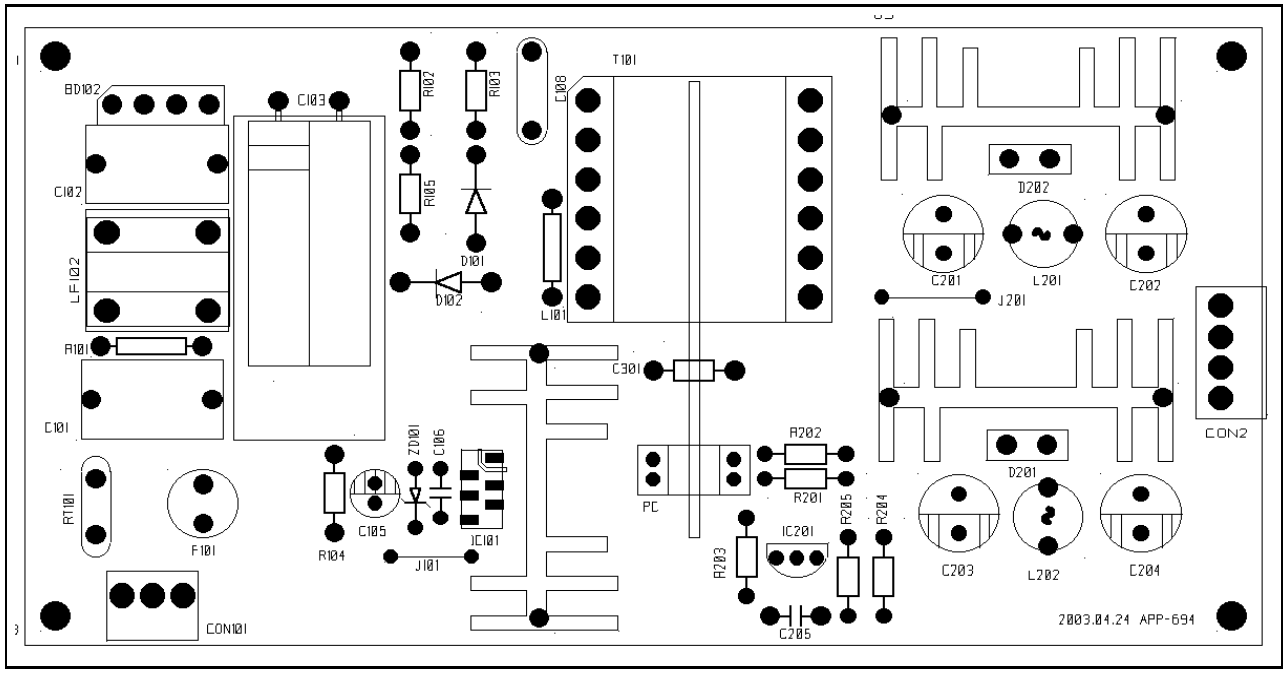


Figure 9. Layout Considerations for FSDM1265RB

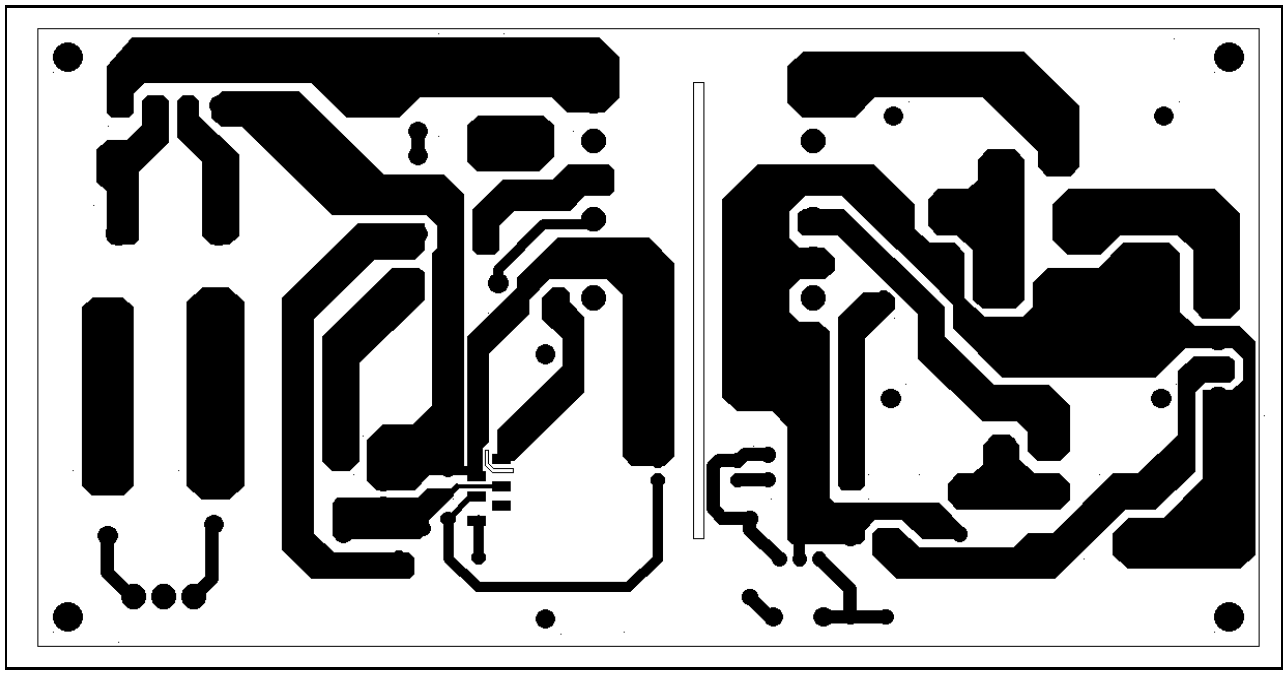
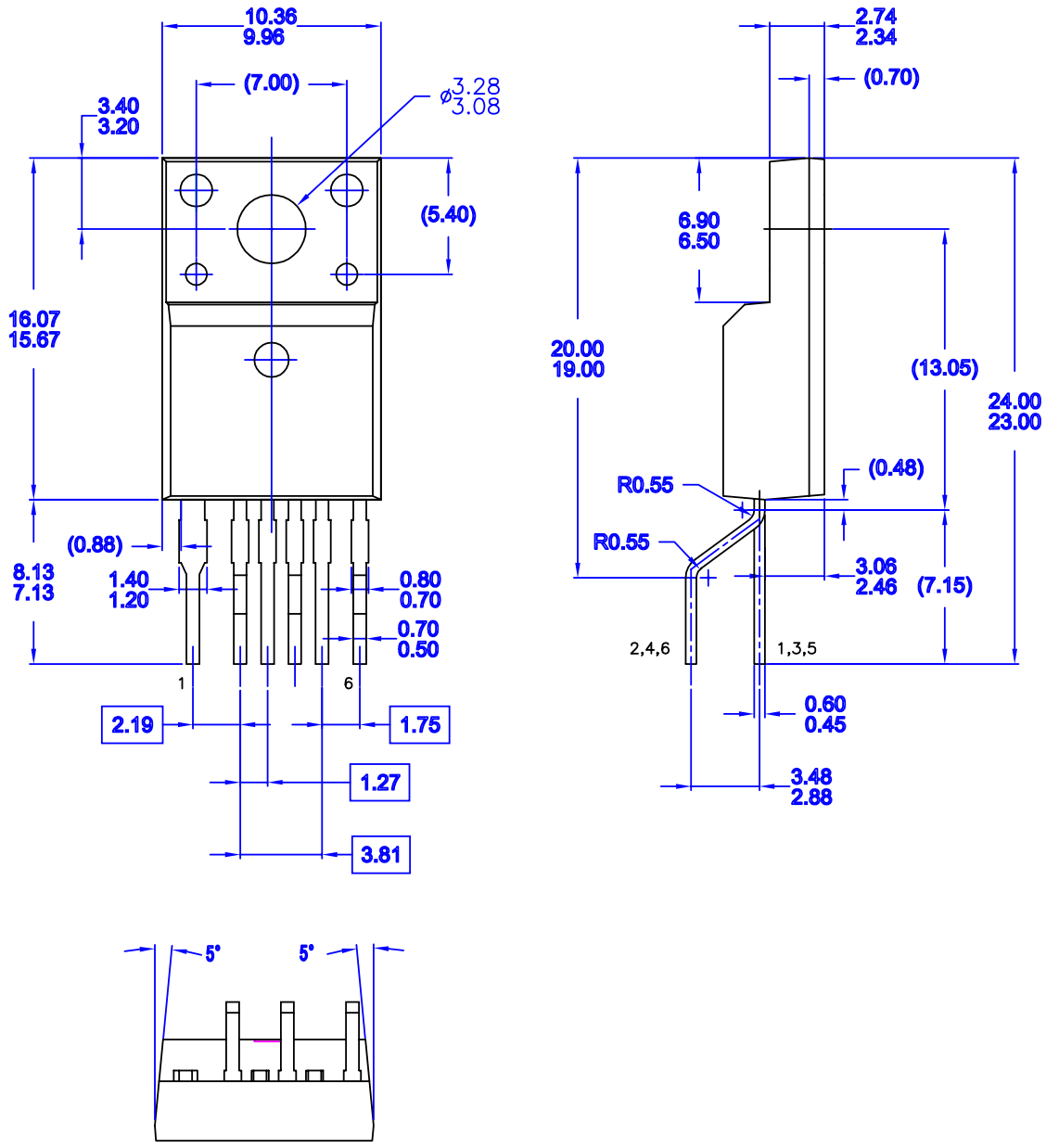


Figure 10. Layout Considerations for FSDM1265RB

Package Dimensions

TO-220F-6L(Forming)



MKT-TO220A06revB

NOTES: UNLESS OTHERWISE SPECIFIED
A) THIS PACKAGE DOES NOT COMPLY TO ANY CURRENT PACKAGING STANDARD.
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
D) LEADFORM OPTION A

Ordering Information

Product Number	Package	Marking Code	BVdss	Rds(on)Max
FSDM1265RBWDTU	TO-220F-6L(Forming)	DM1265RB	650V	0.9 Ω

WDTu: Forming Type

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